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化学生命工学専攻、マテリアル工学専攻

“化学を基盤とするヒューマンマテリアル創成”

平成18年度後期リサーチ・アシスタント報告書

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学年	博士課程 2 年	
研究題目	有機トランジスタにおける閾電圧変化の研究 ～安定な素子動作の実現を目指して～	
指導教員の所属・氏名	東京大学大学院工学系研究科 教授・鳥海明	

I 研究の成果 (1000字程度)

(図表も含めて分かりやすく記入のこと)

One of the important goals of organic field effect transistors (OFETs) is to achieve real applications such as drivers for flexible displays, identification tags. For these applications, a decisive aspect of the organic FET is the stability as well as electrical performances of device. However, the crucial instability is observed as a threshold voltage shift (ΔV_T) and hysteresis in OFETs during bias stress. It has been bottlenecked for the organic device application compared with that of inorganic devices. Also, the origin of threshold voltage shift hasn't been clearly understood although there are some possible causes. Thus, this research is focused on the study of organic device stability related to V_T shift and hysteresis of OFETs.

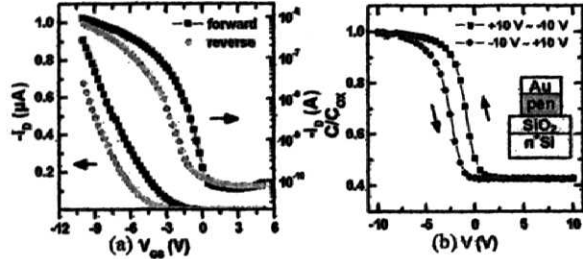


Fig. 1 (a) Threshold voltage shift under bi-directional gate sweep: forward (+5 V \rightarrow -10 V) and reverse (-10 V \rightarrow +5 V) (b) hysteresis of loop direction for bi-directional voltage sweep

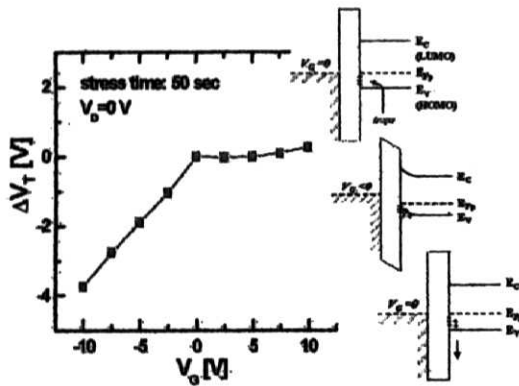


Fig. 2 (a) Gate voltage dependence of threshold voltage shift under a fixed stressing time of 50 sec (b) Charge trapping mechanism based on Energy band diagram generating V_T shift

Fig. 1 shows V_T shift and hysteresis of loop direction for the devices based on SiO_2 dielectric under bi-directional gate bias sweeping. The device instability shown as a difference of threshold voltage under forward and reverse gate bias sweep could be generated by charge trapping, mobile ions and polarization in the defect of insulator, interface or active layer itself. In order to clarify the origin of bias-induced threshold voltage shift, the gate voltage dependence of V_T was inspected depend on different bias stressing given in Fig. 2 (left). The increased magnitude of ΔV_T further into negative direction responds to bias stress indicates that ΔV_T is dominantly attributed to hole trapping in pentacene film. After each gate bias stressing, an equal amount of charges per unit area is being accumulated up to ΔV_T in localized trapping sites.

Thus, if the trapping state is located uniformly in the interface between insulator and active layer, an increment of bias gives rise to larger threshold voltage shift resulting from the effect of deeper level trapping. V_T shift mechanism in accordance with applied bias stress is presented based on energy level diagram in Fig. 2 (right).

The structural order of molecule in organic film is deeply related to the electrical properties of organic devices which directly determines the carrier trapping and transport in active region. It is also widely recognized that the transport properties of crystalline organic films depend strongly on the intermolecular overlap of electronic

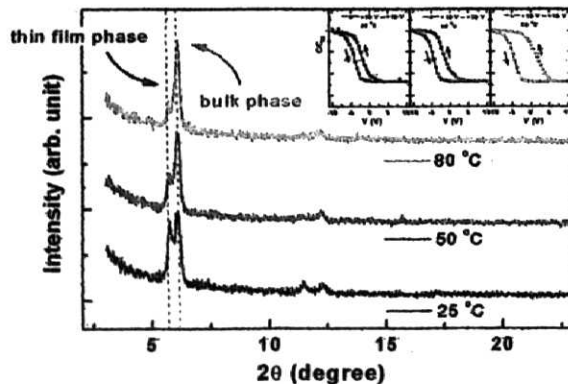


Fig. 3 hysteresis variation depending on substrate temperature during pentacene layer deposition

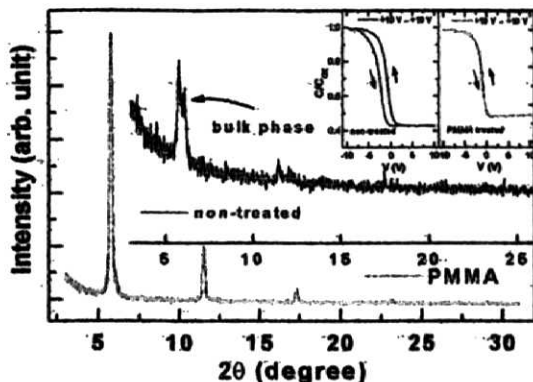


Fig. 4 Improved hysteresis characteristics after the surface modification with PMMA and comparison of XRD spectra before- and after surface modification

wave functions within the semiconductor layer, which is very sensitive to the molecular packing in the crystal. The correlation of molecule structural order and device stability is also studied given in Fig. 3. The intensity of the set of peaks corresponding to the thin film phase is reduced with increasing substrate temperature. This result identify one phase, a substrate induced thin film phase, forms directly onto the SiO₂ substrate and constitutes a layer consisting of strongly faceted grains. In organic semiconductor, carrier transport in the channel is thought to occur in the first few layers of the semiconductor, or perhaps the first layer, in

proximity with the dielectric layer adjacent to the gate electrode. Therefore, the intensity reduction of the fraction of thin film phase peaks and the variation of device stability generated by this effect suggests that surface reaction is changed between SiO₂ and evaporated molecule on surface due to the variation of activation energy of molecule respond to substrate temperature which can lead to changed structural order and trapping site in near the channel regime.

TFT characteristics largely depend on the surface properties of gate dielectric such as insulating qualities, wettability and the chemical reactivity of the surface. The hydrophobic terminal state was provided by the surface modification with polymethyl methacrylate (PMMA) solution on SiO₂ dielectric to reduce the mismatched interface terminal state between SiO₂ dielectric (O-H: hydrophilic) and pentacene active layer (C-H: hydrophobic). Changed hysteresis behavior after the each surface modification is illustrated on inserted C-V

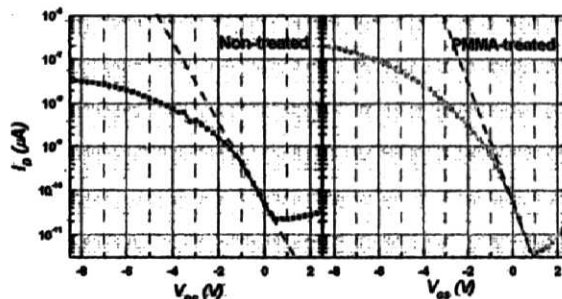


Fig. 5 subthreshold slope (SS) variation before- and after surface modification

characteristics in Fig. 4. The remarkably reduced flatband voltage shift is observed about 0.01 V after PMMA surface modification. Otherwise, non-treated device has V_T shift of about -2 V. X-ray diffraction (XRD) spectroscopy was performed on 50 nm-thick pentacene films deposited on the split surface condition in order to obtain insight into the differences of crystal structure of films respond to the changed surface. As illustrated in Fig. 4, XRD pattern shows the low crystalline characteristics for the film grown on non-treated insulator. Whereas drastically well ordered thin film phase is achieved in the film grown on the modified surface with PMMA solution. As we already proved in Fig. 3, this result also supports that the correlation of molecular peaking and device stability, again. That is, the reduction of ΔV_T is strongly affected by the efficient formation of the thin film phase and it may lead to the decrease of molecular trapping state in active layer.

It is also noteworthy that the presence of surface treatment layer cause significant changes in the subthreshold slope (SS) of the TFTs since it is strongly correlated to interface trap density of the TFTs. The interface trap density (D_{it}) was estimated for non-treated and PMMA treated devices as 6.50×10^{12} , $3.48 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ with SS value of 1.04 and 0.60 V/decade from I_D versus V_{GS} plot given in Fig. 5 using the subthreshold current method, respectively. Therefore, this result evidently presents that the interface contribution for the reduction of trapping state resulting from the surface modification. Namely, a highly functionalized surface plays a role to reduce interface defect between interface and active layer by providing hydrophobic terminal state. Conclusively, the threshold voltage shift caused by hole trapping is deeply correlated to interface state as well as molecular ordering and also it can be reduced by reducing the mismatched interface terminal state and highly ordered film formation.

II 学術雑誌等に発表した論文（掲載を決定されたものを含む。）

共著の場合、申請者の役割を記載すること。

（著者，題名，掲載誌名，年月，巻号，頁を記入）

学術雑誌と学会等のプロシーディングなどを以下のように区別して記入すること。

- (1) 学術論文（査読あり）
- (2) 学会等のプロシーディング
- (3) その他（総説・本）

学術論文

• Chang Bum Park, Keum-Dong Jung, Sung Hun Jin, Byung-Gook Park, and Jong Duk Lee,
“Pentacene-Based Thin Film Transistors with Improved Mobility Characteristics using
Hybrid Gate Insulator,” Journal of Information Display, Vol. 6, No. 2, 2005.

その他（修士論文）

“A Study on High Mobility Pentacene Thin Film Transistors with Hybrid Gate Dielectric
Layer,” Seoul National University, directed by Prof. Jong Duk Lee, Aug. 2005.

III 学会において申請者が口頭発表もしくはポスター発表した論文
(共同研究者(全員の氏名), 題名, 発表した学会名, 場所, 年月を記載)
国内学会および国際学会を区別して記入のこと

◆ Conference

- Chang Bum Park, Takamichi Yokoyama, Tomonori Nishimura, Koji Kita and Akira Toriumi, "Study of Bias-Induced Threshold Voltage Shift in Pentacene Field Effect Transistors for Stable Device Operation," COE-BK21 Joint Seminar 2006, Seoul, Korea, December 11-12, 2006.
- Chang Bum Park, Tomonori Nishimura, Takamichi Yokoyama, Koji Kita and Akira Toriumi, "Reduction of Bias-Induced Threshold Voltage Shift in Pentacene Field Effect Transistors by Interface Modification and Molecular Ordering," Int'l Conf. on Solid State Devices and Materials 2006, Yokohama, Japan, September 12-15 2006. [INTL]
- Chang Bum Park, Sung Hun Jin, Byung-Gook Park, and Jong Duk Lee, "Hybrid Insulator Organic Thin Film Transistors with Improved Mobility Characteristics," Int'l Conf. on International Meeting on Information Display 2005, Seoul, Korea, July 19-23, 2005. [INTL]
- Keum Dong Jung, Sung Hun Jin, Chang Bum Park, Hyungcheol Shin, Byung Gook Park and Jong Duk Lee, "Effects of Peripheral Pentacene Region on C-V Characteristics of Metal-Oxide-Pentacene Capacitor Structure," Int'l Conf. on International Meeting on Information Display 2005, Seoul, Korea, July 19-23, 2005. [INTL]
- Sung Hun Jin, Sang Min Yi, Keum Dong Jung, Chang Bum Park, Chong Nam Chu, Hyung Chul Shin, Byung-Gook Park, and Jong Duk Lee, "Pentacene TFTs Fabricated by High-aspect Ratio Metal Shadow Mask," Int'l Conf. on Solid State Devices and Materials 2004, Tokyo, Japan, September 15-17 2004. [INTL]
- Ki Hyun Ryoo, Cheon An Lee, Sung Hun Jin, Keum Dong Jung, Chang Bum Park, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park, "Triple Layer Passivation for Organic Thin-Film Transistors," Int'l Conf. on International Meeting on Information Display 2005, Seoul, Korea, July 19-23, 2005. [INTL]