Hyper Suprime-Cam: back-end electronics for CCD readout

Tomohisa Uchida*[a], Hironao Miyatake[a], Hidehiko Nakaya [b], Hiroaki Aihara[a], Satoshi Miyazaki[c]
[a]Dept. of Physics, University of Tokyo,
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-0033, Japan;
[b]Subaru Telescope, National Astronomical Observatory of Japan,
650 North Aohoku Place, Hilo, HI, 96720, USA;
[c]National Astronomical Observatory of Japan,
2-21-1, Osawa, Mitaka, Tokyo, 181-8588, JAPAN

ABSTRACT

The development status of a prototype readout module for Hyper Suprime-Cam, a next-generation prime-focus camera for the 8.2 m Subaru Telescope, is presented. The camera has a field of view 1.5° in diameter, and produces 2.1 Gbyte of data per exposure. The module transfers the data to computers of a data acquisition system using TCP/IP and Gigabit Ethernet. We have measured the performance of data processing and data transfer of the developed module. The results indicated sufficient performance to read data from all CCDs within the required readout time.

Keywords: Readout Electronics, CCD mosaic camera

1. INTRODUCTION

The Hyper Suprime-Cam (HSC) [1] is a next-generation prime-focus camera for the 8.2 m Subaru Telescope at the summit of Mauna Kea, Hawaii. The camera covers a field of view 1.5° in diameter and provides an approximately 10-fold increase in the survey speed as compared with the current prime-focus camera (Suprime-Cam) [2]. The camera uses a fully depleted Charge Coupled Device (CCD) [3] [4]. The CCD is fabricated on high resistive n-type silicon, and was developed in collaboration between the National Astronomical Observatory of Japan (NAOJ) and Hamamatsu Photonics K.K. To cover the field, 110 CCDs of size 2 kpixels × 4 kpixels are employed. The total number of pixels is 1 Gpixels. The output signal of the CCDs is analog, and is converted to 16-bit digital data with analog-to-digital converters (ADCs). Thus, the camera produces 2.1 Gbyte of image data per exposure, overhead data included. A readout system [5] [6] processes the image data, which are then transferred to a data acquisition (DAQ) system within the required readout time.

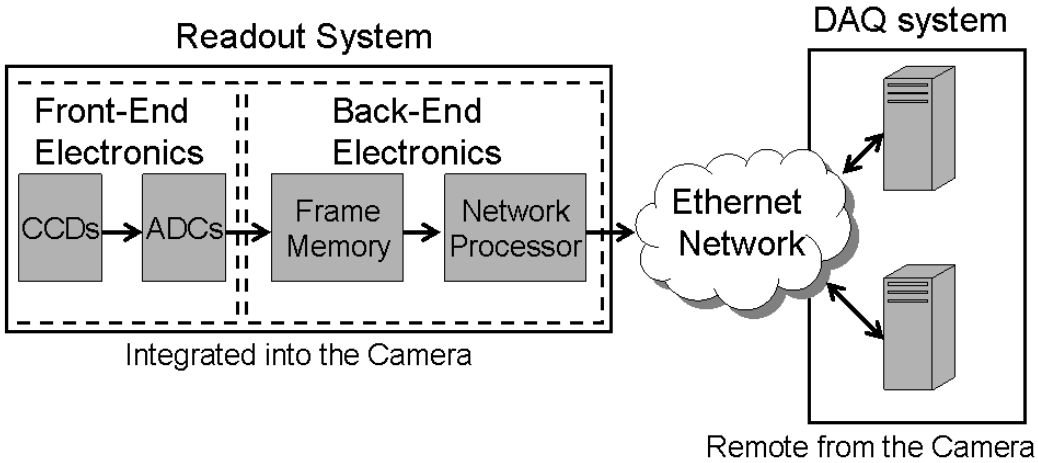

Fig. 1. Schematic diagram of the readout system, which consists of front-end electronics (FEE) and back-end electronics (BEE). The FEE reads data from the CCDs and digitizes these data. The BEE stores the digitized data and transfers these data to a DAQ system. The DAQ system analyzes these data as images.

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Figure 1 shows a schematic diagram of the readout system integrated into the camera, which controls the camera and processes data produced by the CCDs. The DAQ system is located remotely from the camera, in an observing room, and analyzes the data as images. These two systems are connected *via* Gigabit Ethernet [7]. The system consists of front-end electronics (FEE), an analog part, and back-end electronics (BEE), a digital part. The FEE reads the analog signals from the CCDs and converts these signals to digital data using 16-bit ADCs. The BEE temporarily stores those digitized data in a frame memory, and the stored data are transferred to the DAQ system *via* Gigabit Ethernet. The required readout time is less than 10 s. Thus, the required transfer speed between BEE and the DAQ system is greater than 1.6 Gbit/s. Reductions in weight, size, and power consumption are also important issues because BEE is mounted on the prime-focus plane. To satisfy these requirements, we have developed a prototype readout module for this system.

2. BACK-END ELECTRONICS

The back-end electronics (BEE) provide the interface between the front-end electronics (FEE) and the DAQ system. The BEE must be capable of processing one 2.1-Gbyte frame of data and transferring it within 10 s. The required processing rate is 1.6 Gbit/s.

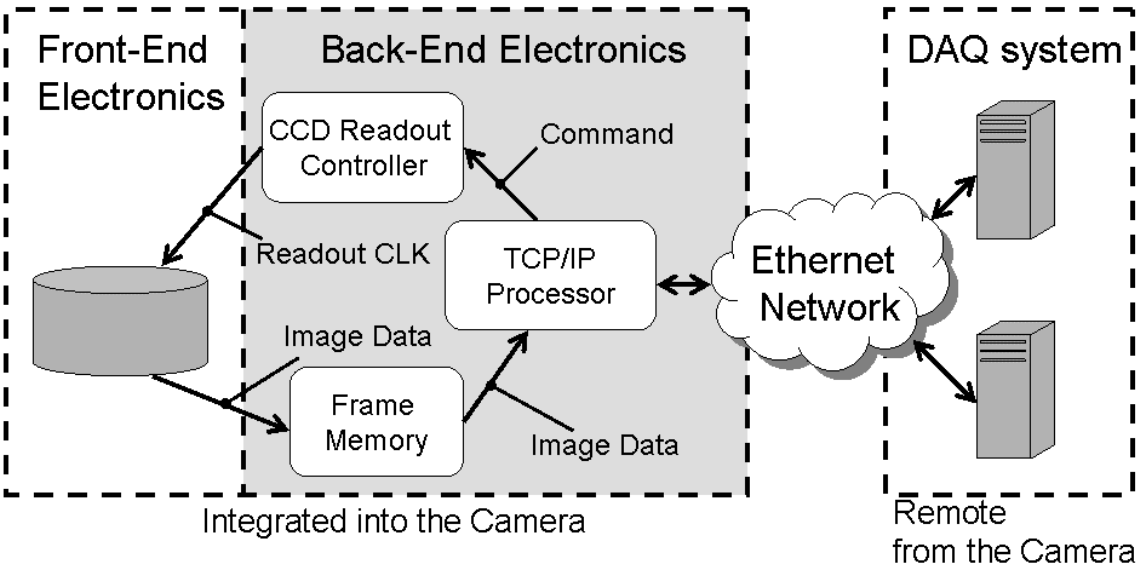

Fig. 2. Schematic of the readout system.

Figure 2 shows a schematic of the readout system for the HSC. The FEE and BEE are integrated into the camera, while the DAQ system is located remotely from the camera. The BEE and DAQ communicate over Gigabit Ethernet using Transmission Control Protocol (TCP) [8] [9] and User Datagram Protocol (UDP) [10] as parts of the TCP/IP protocol suite [8]. Ethernet and TCP have been widely used and have been implemented in a variety of commodity products, and TCP/IP is the de facto standard network protocol and is implemented in many operating systems (OS). The DAQ system also employs TCP/IP and Ethernet as a common interface. Thus, adopting TCP/IP and Ethernet provides high connectivity between the BEE and the DAQ system. The main tasks of BEE are CCD control, storage of image data, and transfer of image data to the DAQ system within the required readout time. The DAQ system controls the FEE by sending commands to the BEE for image data readout. The commands are processed by a TCP/IP processor. A CCD readout controller generates readout clocks for the CCDs. The output image data of the CCDs are converted to digital signals by ADCs in the FEE. The converted image data are transferred to the BEE and stored in a frame memory. The stored image data are read from the memory and transferred to the TCP/IP processor by a command from the DAQ system, and the image data are finally transferred to the DAQ system.

Issues with the development of this BEE are reduction of weight, size, and power consumption while maintaining high-speed data transfer capability. Generally, TCP/IP is processed by software making use of standard OS. A powerful

hardware and CPU are required to process these protocols at gigabit rates, and thus power consumption is of the order of several tens of watts and the size and weight are both large, e.g., a single/double height 6U-Euro-card. To overcome these difficulties, we have adopted a hardware-based TCP/IP processor called SiTCP [11]. As the logic size of the processor is small enough for implementation on a single Field Programmable Gate Array (FPGA), we can implement circuits for all the main tasks BEE on a single FPGA. This allowed us to design a small and lightweight system that has high-speed data transfer capability.

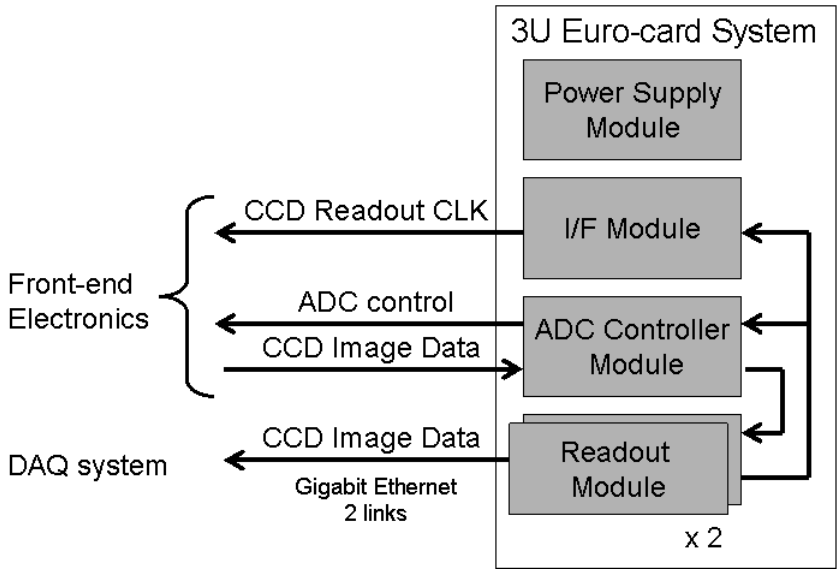

Fig. 3. Schematic diagram of a planned back-end electronics system

Figure 3 shows a block diagram of the planned BEE system using the 3U Euro-card system. The system consists of five modules: two Readout Modules, an I/F module, an ADC controller module, and a Power Supply Module. The Readout Module is the main module in this system, and has the following functionalities: this module generates a readout clock for the CCDs, stores image data into the Frame Memory, and transfers these data to the DAQ system *via* Gigabit Ethernet. To satisfy the requirement for the transfer speed to be greater than 1.6 Gbit/s, two Readout Modules are used. The I/F Module converts signaling standards of digital signals: from/to LVDS to/from CMOS 3.3V. The ADC Controller module controls the ADCs in the FEE with a Serial Peripheral Interface (SPI), and then transfers converted image data to the Readout Modules through LVDS signal lines. We have developed a prototype of the Readout Module, and discuss details of the module in the following sections.

3. THE PROTOTYPE READOUT MODULE

Figure 4 shows a photograph of the prototype readout module seen from the front. This module has the following features: small size, light weight, low power consumption, gigabit data transfer rate, and a large memory capacity. The module measures 149 mm × 79 mm × 12 mm and weighs 100 g, compatible with the Common Mezzanine Card (CMC) size specified as IEEE P1386 [12]. Generally, CMC are designed to be plugged into a slot on the host's motherboard. BEE employs a host board of 3U Euro-card size. The Readout Module is independent of the system of host modules. Hence, various systems can be used in different phases of development. For example, to evaluate the function of CCD readout, the current Suprime-Cam system [8] can be used. This is advantageous for development. The power consumption of the module is less than 8 W. One Gigabit Ethernet port of 1000BASE-T, with Unshielded Twisted Pair cabling (UTP), is used for image data transfer to the DAQ system. The final version of the module is expected to use 1000BASE-SX. However, at present, we have adopted 1000BASE-T for ease of debugging the module and the system. One DDR2-SDRAM Small Outline Dual In-line Memory Module (SO-DIMM) with capacity of up to 2 Gbyte is employed as the frame memory.

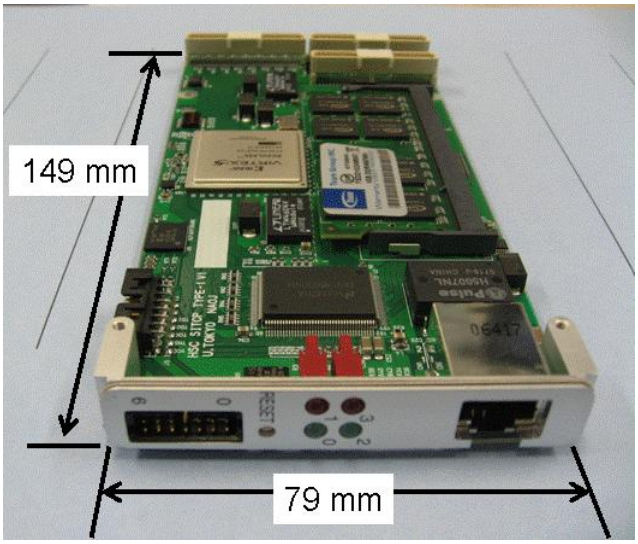

Fig. 4 Photograph of the prototype readout module (Front view)

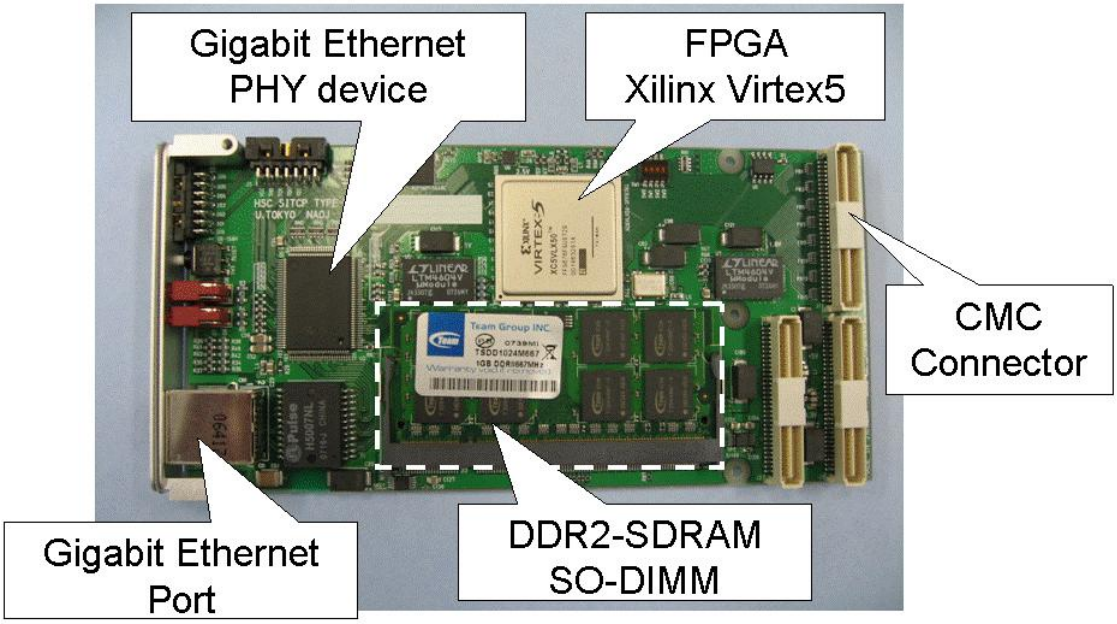

Fig. 5. Photograph of the prototype readout module (Top view)

Figure 5 shows a photograph of the prototype readout module seen from the top. The module consists of three main devices: a Gigabit Ethernet Physical Layer Device (PHY) (DP83865DVH; National Semiconductor Corp.), an FPGA (XC5VLX50-FFG676-2I; Xilinx Inc.), and an SO-DIMM. This design includes no CPU. 1000BASE-T Gigabit Ethernet is used for communication between the BEE and a computer in the DAQ, transferring the image data and exchanging commands and status. The FPGA processes network protocols, generates CCD clocks, and controls the SO-DIMM as the frame memory. Signal lines between the BEE and FEE are connected *via* the Pn4 in CMC connectors [12]. All pins of the connector are connected directly to the FPGA.

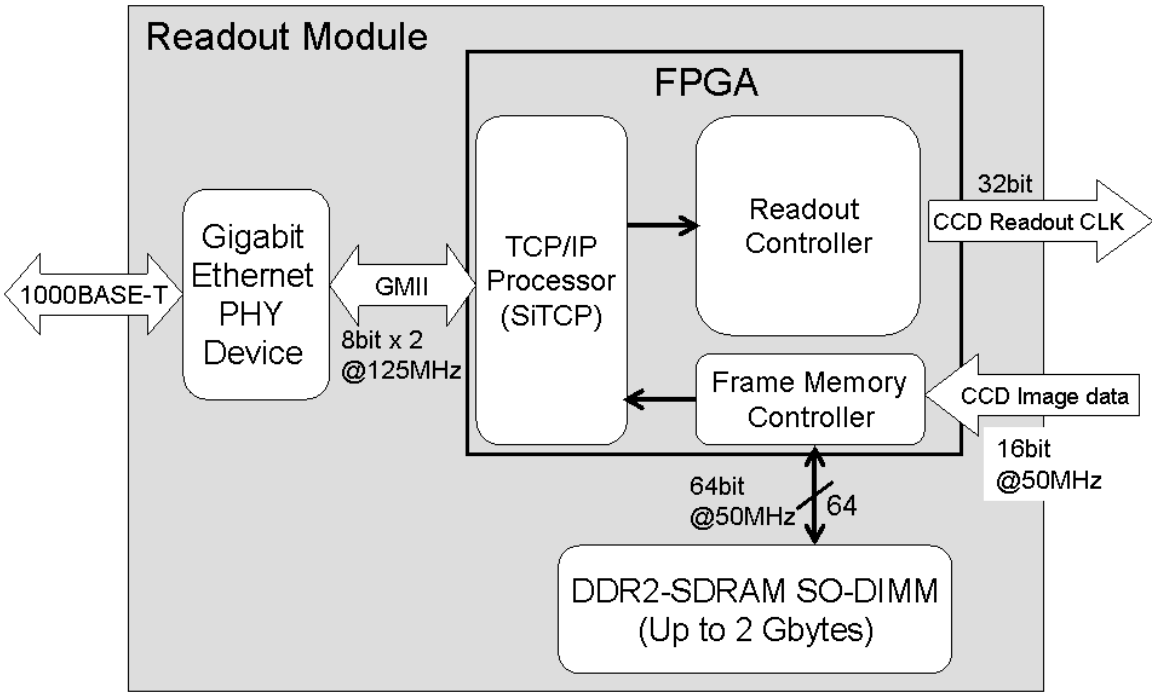

Fig. 6. Block diagram of the readout module

Figure 6 shows a block diagram of the readout module. The PHY device processes an Ethernet layer protocol, with clock recovery, data encoding, and decoding. The PHY and the SiTCP are connected with the standard interface, Media Independent Interface (MII) specified by IEEE802.3 [7]. The SiTCP processes TCP packets for image data transfer and UDP packets for slow control [11]. Internet Control Message Protocol (ICMP) [8] and Address Resolution Protocol (ARP) [8] packets for network management are also processed by the SiTCP. The Readout Controller generates CCD readout clocks with a programmable sequencer and clock patterns stored in a clock pattern memory. A program for the sequencer and clock pattern data are set by a PC of the DAQ system with the slow control mechanism of the SiTCP. After the Readout Controller is started, image data are acquired from ADCs. The image data are stored in the frame memory by the Frame Memory Controller. Generally, DDR2-SDRAM devices run at a clock frequency of 125 MHz or higher. We use the frame memory at a clock frequency of 50 MHz to reduce power consumption. Thus, the maximum bandwidth between the frame memory and the FPGA is 6.4 Gbps. The Frame Memory Controller reads back image data from the memory and transfers these data to SiTCP when a TCP link is established. The image data received by the SiTCP are transferred as TCP packets to the DAQ system.

4. TESTS AND RESULTS

The prototype module is currently under development. We tested the critical issue of gigabit-rate data transfer at the beginning of the system development. The performance of the BEE may be limited by transfer speed of the two interfaces for CCDs and the network. The former interface is similar to that of the current system, Suprime-Cam [4]. We expect that it will provide sufficient performance to read from all CCDs. On the other hand, the network interface, Gigabit Ethernet and TCP/IP, is a new interface since the development of Suprime-Cam. Confirmation of TCP throughput is also required.

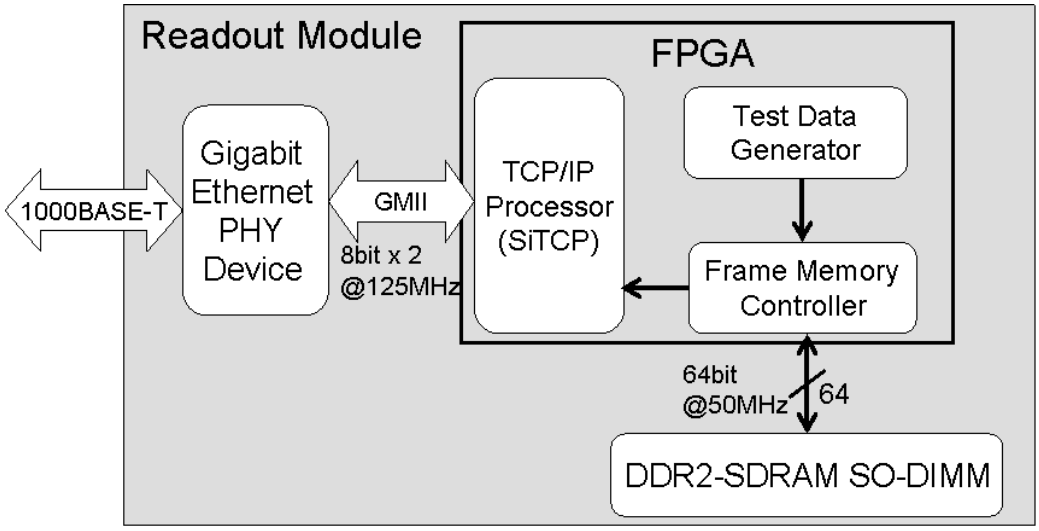

Fig. 7. Block diagram of the test circuit

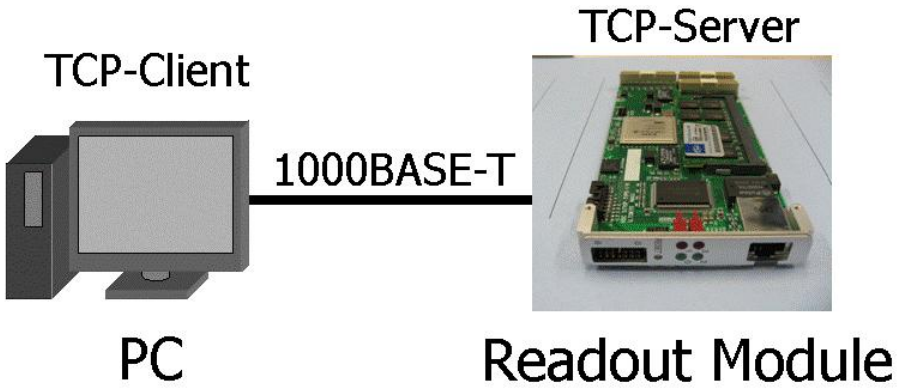

Fig. 8. Measurement setup. The Readout Module and PC, which were connected directly with a crossover cable, acted as the TCP server and client, respectively.

We measured TCP data throughput of the prototype module by implementing a test circuit in the FPGA. Figure 7 shows a block diagram of the test circuit. The Test Data Generator generates data of sequence numbers with a width of 32 bits. These data are temporarily stored in the frame memory by the Frame Memory Controller. When a TCP connection is established, the Frame Memory Controller reads back and transfers these data to the SiTCP. The data are transferred to a PC through an Ethernet link as TCP packets by the SiTCP.

Figure 8 shows the measurement setup. The Readout Module and PC, which were connected directly with a crossover cable, acted as the TCP server and client, respectively. Forwarding devices were not used to avoid any influence on performance. The PC used was a Dell PowerEdge SC1430 Dual Core Xeon 5120 (4 MB L2 Cache, 1.86 GHz, 1066 MHz FSB) running Scientific Linux CERN SLC release 4.5. A simple program to read the socket and to check the receiving data was used with no parameter tuning. The throughput was calculated from the received data size and transfer time. The measured throughput was about 949 Mbps, corresponding to the upper limit of Gigabit Ethernet (Tmax) of 949 Mbps. The Tmax is calculated by:

$$Tmax = 1Gbps \times \frac{MSS}{IPG + H_{MAC} + H_{IP} + H_{TCP} + MSS}$$
$$= 949Mbps$$

Here, *MSS* is the maximum segment size of TCP, 1460 bytes; *IPG* is the inter-packet gap defined by the specification IEEE802.3, 12 bytes; H_{MAC} is the overhead length of Ethernet, 26 bytes; H_{IP} is the length of the IP header, 20 bytes; and H_{TCP} is the length of the TCP header, 20 bytes. Power consumption of the prototype module was less than 8W in this measurement.

5. CONCLUSION

We have developed a prototype readout module for Hyper Suprime-Cam. To measure performance, we have implemented a test circuit consisting of a test data generator, network processor, and frame memory controller. We measured transfer performance by generating test data and transferring these data to a PC. The module can transfer data through a Gigabit Ethernet link at close to the theoretical upper limit of 949 Mbps. As the required minimum throughput is 800 Mbps and the power consumption of this system is less than 8W, we concluded that the readout module has sufficient performance for image data transfer.

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