論 文 の 内 容 の 要 旨

論文題目　Growth Technology of High-Density Carbon Nanotube Arrays for Enhanced Electric and Thermal Conduction
（電気・熱伝導促進を目指したカーボンナノチューブ高密度配列の成長技術の開発）

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1. Introduction

Carbon nanotubes have gathered great interests because of their various potential applications including nanoscale electronic devices due to the attractive properties of individual CNTs such as high electric and thermal conductivity, high tensile strength with flexibility, and thermal and chemical stabilities. Especially, vertically-aligned CNT (VA-CNT) arrays, grown by chemical vapor deposition (CVD) on catalyst-supported substrates, are attractive for electric and thermal transport due to their anisotropic, uni-directional structure, however they usually contain CNTs at a few vol% with air at >90 vol%. To pull out the potential of CNTs, dense CNT arrays must be grown on device substrates, which changes with target applications. This research aims at development of growth technology of high-density CNT arrays on device substrates for possible applications to via interconnects in large-scale integrated circuits (LSIs) and thermal interface materials (TIMs).

2. Sub-micrometer-tall, high-density CNT arrays on conductive underlayer at 400 ºC for LSIs

CNTs are attractive as a wiring material in LSIs because they can carry electric current at a density three-orders of magnitude higher than Cu. VA-CNT arrays can be grown by CVD under various conditions, however mostly on insulating substrates at low densities of 0.03−0.07 g cm^{-3} at high temperatures of 600−800 °C. To be applied to LSIs, CNTs must be grown on conductive underlayer at high density of ~1 g cm^{-3} at low temperature of ≤400 °C. Recently, two groups realized dense multi-wall CNT (MWCNT) arrays on conductive underlayer at ~450 °C. However, the direct counting of the number of CNTs and their walls has not been realized yet. It is highly demanded to establish both growth and analytical methods of VA-CNT arrays.

There are two main approaches for catalyst preparation. One is to pre-form the catalyst particles and then deposit the particles on the substrate. When we attempt to deposit the catalyst densely, catalyst particles inherently deposit on the catalyst particles and/or aggregate (Fig. 1a).

The other approach is to pre-form the catalyst layer on substrates and then transform the layer into particles. However, spaces inherently form between the catalyst particles (Fig. 1b). Here we propose the third approach, direct nucleation and growth of catalyst particles on substrates (Fig. 1c). When catalyst is sputter-deposited on heated substrates, catalyst adatoms diffuse over the surface, attach to each other, and nucleate particles (islands). As deposition proceeds, nucleated particles grow larger and get percolated. If deposition is stopped prior to percolation, catalyst particles can be acquired that are densely packed with minimal space between them. Even at ambient temperature, metal particles nucleate and grow during sputtering on substrates, but their density is too high to retain the high density upon heating. Preparing catalyst particles at high, but not too high, density should be key.

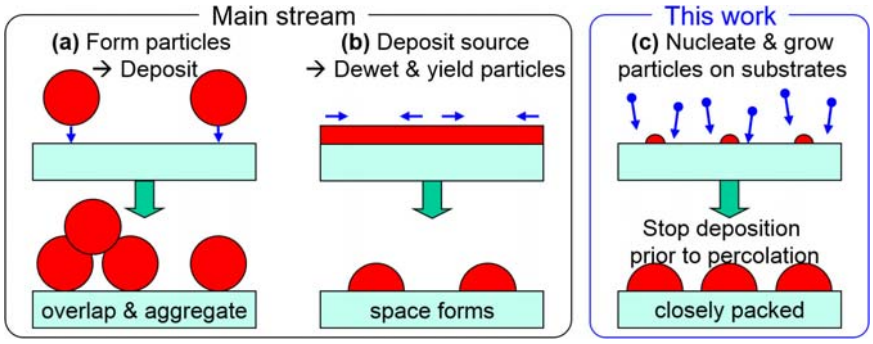

Fig. 1 Existing approaches and our strategy for preparation of catalyst particle arrays.

Based on this concept, we prepared catalyst and CNT arrays and characterized their structures in detail. Ni islands were prepared at a moderate density as deposited by enhancing the surface diffusion of Ni over TiN during sputtering at low deposition rate (8.1 pm s^{-1}), with substrate heating (400 °C) and bias voltage (−20 V), resulting in a dense Ni particle array (2.8×10^{12} cm^{-2}) after annealing at 400 °C (Fig. 2f). By lowering C_2H_2 pressure to 0.13–1.3 Pa so as not to kill the catalyst, dense VA-CNT arrays (~1 g cm^{-3}) were grown at a low temperature of 400 °C on the conductive TiN underlayer (Fig. 2a). Such arrays were transferred to transmission electron microscope (TEM) microgrids or Si substrates with their roots up. Bottom-view SEM images show the densely packed CNT bundles (Fig. 2b). AFM images enabled direct counting of the roots of individual CNTs (Fig. 2c−e). HRTEM images realized direct counting of the walls within individual CNTs to be ~8. These analyses evidence that Ni catalyst particles at 2.8×10^{12} cm^{-2} grew CNTs at 1.5×10^{12} CNTs cm^{-2} and 1.2×10^{13} walls cm^{-2}. Such CNTs, formed on a conductive TiN layer at process temperatures ≤ 400 °C using conventional sputtering and CVD apparatuses meet many of requirements for application to via interconnects in LSIs.

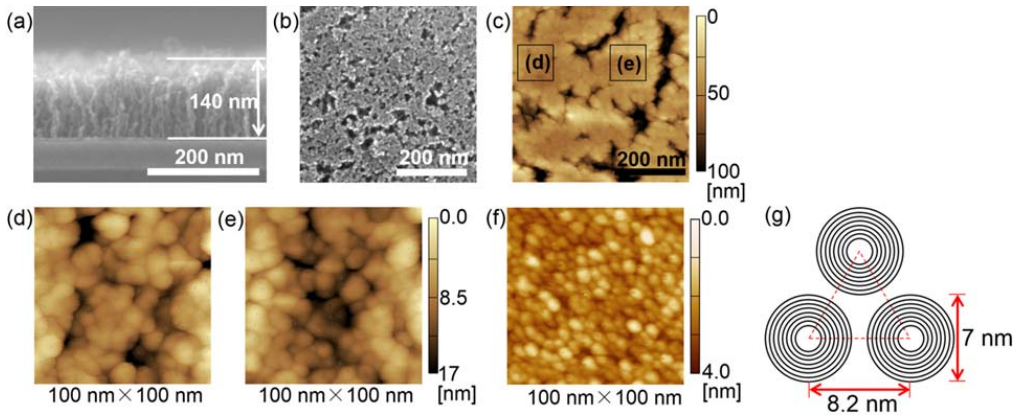

Fig. 2 Structural analyses of the dense VA-CNT arrays (~1 g cm^{-3}, 1.5×10^{12} CNTs cm^{-2}, 1.2×10^{13} walls cm^{-2}) grown at low temperature (400 °C) on conductive TiN underlayer.

3. Tens-micrometer-tall, high-density CNT arrays on both sides of Cu foils for TIMs

CNTs have high thermal conductivity and mechanical flexibility and thus their arrays on both faces of metal foils (typically Cu) are attractive as TIMs, which fill the micrometer-scale gaps between the heat sources (devices) and heat sinks. CNT arrays can be either grown directly on the foils or transferred to the foils. Such structure has been demonstrated, however further improvement is needed to achieve higher thermal conductivities both in the interior of the arrays and at the interface between the arrays and substrates. Fabrication of such CNT/Cu/CNT TIMs were examined by the direct CNT growth in this chapter.

To prevent the alloying of catalyst metals (Ni, Co, Fe) with Cu foils, Ta layer (being used as diffusion barrier for Cu in LSIs) and TiN layer (known effective as catalyst underlayer for CNTs) are applied. The surface elemental composition of catalyst-supported Cu foils before and after annealing was examined by X-ray photoelectron spectroscopy. Without Ta layer, a strong Cu peak was observed with a weakened Fe peak after annealing, showing the essential role of Ta preventing intermixing of Fe and Cu. Without TiN layer, Ta peaks get evident after annealing, showing the essential role of TiN in preventing the surface segregation of Ta. This TiN/Ta bilayer with proper thicknesses (15 nm/10 nm) is essential to keep Fe catalyst particles active during CVD at 700 °C.

By optimizing the catalyst metals and thickness (Fe and 0.8−2.5 nm), and CVD temperature and C_2H_2 pressure (700 °C and 27 Pa), several-tens-micrometer-tall VA-CNT arrays were directly grown on both faces of Cu foils. Fig. 3a shows side-view SEM images of a typical TIM. The tradeoff between the height and the density of the CNT arrays are evident (Fig. 3b). As the CNT grew tall from a few to 140 μm, the mass density decreased from 0.30 to 0.11 g cm^{-3}. Relatively high density CNT arrays (0.21 g cm^{-3} at 61 μm) were realized with 2-nm-thick Fe catalyst. Then, the same approach as the previous chapter, i.e. careful control of surface diffusion of catalyst during sputtering, was applied and the high number density of Fe particles

(8.0×10^{11} cm^{-2}) and mass density of CNT arrays (0.30 g cm^{-3} at 45 μm) were realized. The thermal resistance of these CNT/Cu/CNT TIMs was evaluated (Fig. 3c). The thermal resistance decreased drastically from 86 to 24 mm^2 K W^{-1} with increasing CNT density from 0.05 to ~0.2 g cm^{-3}. The best CNT/Cu/CNT TIMs showed a thermal resistance comparable with that of a typical indium sheet TIM.

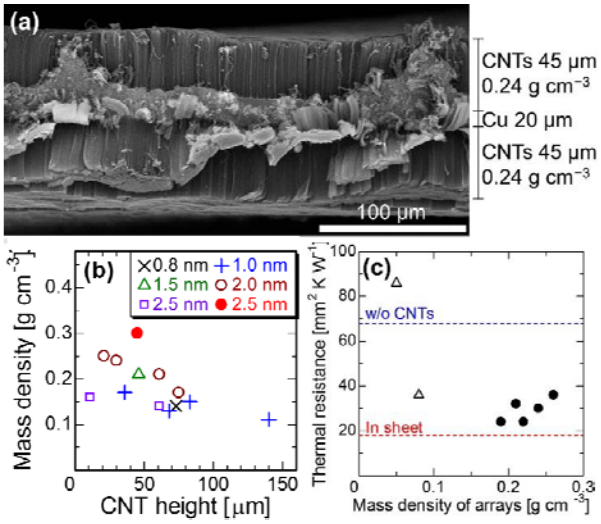

Fig. 3 CNT/Cu/CNT TIMs by direct CNT growth on Cu foils. (a) Side-view SEM image of a typical TIM. (b) mass density vs. CNT height of the CNT arrays. (c) thermal resistance vs. mass density of the CNT arrays.

4. Conclusions

Toward practical use of VA-CNT arrays in devices, VA-CNT arrays must be formed at fairly high densities on device substrates under acceptable process temperatures. In this work, direct nucleation and growth of catalyst particles are proposed and developed, in which catalyst deposition was stopped prior to percolation, and dense catalyst particle arrays were realized even after thermal annealing. Low temperature growth (down to 400 °C) of VA-CNT arrays was achieved by moderating the C_2H_2 feed so as not to kill the catalysts. The VA-CNT arrays of high densities (1 g cm^{-3}, 1.5 CNTs cm^{-2}, 1.2×10^{13} walls cm^{-2}) directly grown on conductive TiN layer with a maximum process temperature of 400 °C meet the requirements for use as via interconnects in LSIs. The 40−60-μm-tall VA-CNT arrays of moderate densities (0.19−0.26 g cm^{-3}) directly grown on both faces of Cu foils show enhanced thermal conductivity, which are attractive for TIM applications. Such VA-CNT arrays were realized by using conventional sputtering and CVD apparatuses. Logical design and engineering of processes meeting application requirements will put CNTs toward their practical use in society.