博士論文（要約）

Study on Device Design Guideline for Ultra-Low Power MOSFETs in Sub-0.3 V Operation

（サブ 0.3V 動作超低消費電力 MOSFET のデバイス設計指針に関する研究）

by

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Submitted to the Department of
Electrical Engineering and Information Systems
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHYLOSOPHY

at the Graduate School of the UNIVERSITY OF TOKYO

June 1, 2015

Thesis Supervisor

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Abstract

The mobile applications with the internet of things (IoT) features are become more widespread in our lives due to people's pursuit of convenience. Such portable electronic devices require ultra low power consumption even batteryless system. The low power technology can play an important role in addressing the issue of power and energy consumption. The most simplest and effective way to reduce power consumption is supply voltage (V_{dd}) scaling. Meanwhile, the characteristics in scaled V_{dd} are very sensitive to device variation. Therefore, it is highly required to design the device carefully which operate in scaled V_{dd}.

In this study, the device design guideline for ultra-low power metal-oxide semiconductor field-effect-transistors (MOSFETs) in sub-0.3 V operation is proposed. The two main purpose of this study is to realize complementary MOS (CMOS) logic circuits and static random access memory (SRAM) cells for sub-0.3 V operation. Two major parts of this thesis are verified and considered from all viewpoints such as measurement, simulation, calculation and fabrication.

The first half of the thesis deals with drain-induced barrier lowering (DIBL) effects on subthreshold devices. Even if there are lots of previous researched have been studied to improve subthreshold characteristics for low power consumption, so far, very little attention has been paid to the effects of DIBL to CMOS logic circuits, especially in subthreshold region. 1k nMOSFETs by the 65 nm technology are measured and analyzed in terms of DIBL effects on actual devices. From results, large DIBL device shows severe performance degradation particularly in subthreshold region compared with small DIBL device. Furthermore, in order to investigate DIBL effects on CMOS logic circuits, CMOS ring oscillators with various DIBL are assumed by simulation. The large DIBL devices show much more current and delay degradation because effective current (I_{eff}) or peak trajectory current is degraded by DIBL despite of same on current (I_{on}). Additionally, the

degradation becomes even more serious in subthreshold region. As a result, the energy consumption becomes increasingly larger with DIBL increase in subthreshold region in spite of reduction in power consumption by V_{dd} scaling. In order to improve energy efficiency, steep s-factor transistors are an excellent candidate because of its superior subthreshold characteristics. In spite of that, steep s-factor transistors show increase of energy consumption by 'threshold voltage (V_{th}) shift by drain voltage (V_{ds}) or η factor' which is similar to DIBL in conventional MOSFETs.

The rest of half of this study suggest new operation mechanism whose name is V_{th} self-adjustment for sub-0.3 V operation even enhancing stability of SRAM cells. V_{th} self-adjusting MOSFETs with FD-SOI show two kinds of V_{th} state (dynamic characteristics) and improved on/off current ratio and s-factor (static characteristics) by time-lag of tunneling phenomenon. The V_{th} shift in dynamic characteristics can be used for enhancing stability of SRAM cells. Moreover, improved on/off current ratio and s-factor is suitable for low voltage operation. However, V_{th} self-adjusting MOSFETs with planar structure show crucial weakness in short channel effects due to limitation of vertical scaling down. Thus, the tri-gate nanowire structure is introduced to V_{th} self-adjusting MOSFETs. This approach shows not only operation in ultra-low voltage operation with V_{th} self-adjustment but also strong immunity to short channel effects.

This paper has argued that device design for ultra-low voltage operation. The results of this investigation show that it is important to suppress DIBL for CMOS logic circuits and V_{th} self-adjusting MOSFETs are very promising for low power operation, furthermore enhancing stability of SRAM cells.

Contents

Chapter 1

Introduction

1.1 Background

Our lives become digitalized architecture from analogue one by rapid industrialization. For more advanced our digitalized life, the internet of things (IoT) which is the concept of sharing information among integrated electronic devices by network system has come into our lives [1]. This can be applied to smart home, healthcare or social networking using wireless sensors, mobile phones or radio frequency identification (RFID) system [2-5]. Basically, these kinds of technologies are required ultra-low power consumption than high performance because they are required portability and simplicity with self-powered by batteryless energy harvest system. In the semiconductor devices era, the most effective way to reduce power consumption is reducing supply voltage (V_{dd}) [6-9]. According to the international technology roadmap for semiconductors (ITRS) annual reports, the V_{th} is scaling down into sub-0.7 V after 10 years for low power technology [10]. However, one major drawback of this approach is that severe degradation in operation speed in complementary metal-oxide semiconductor (CMOS) devices due to reduced gate over drive. In order to overcome the obstacle, mostly, the threshold voltage (V_{th}) is getting scaled to obtain acceptable on-current (I_{on}). Nevertheless, this strategy has not escaped from exponential increase of leakage current despite of linear V_{th} scaling. Several recent studies to mitigate the contradiction between high performance and suppressing leakage current have been carried out using advanced channel materials for high I_{on} [11-14] and new operation mechanism, for example, tunnel field effect transistors (TFET) [15, 16] or ferroelectric field-effect transistors (Fe-FET) [17, 18] with steep subthreshold swing slope (SS). Besides, analyzing the random dopant fluctuation (RDF) [19]

or bias temperature instability [20] have been adopted to evaluate the effectiveness of suppressing instability for low power consumption. Meanwhile, energy efficiency; a product of power consumption and delay time improves with V_{dd} scaling and reaches minimum point when the V_{dd} is around 0.3 V as subthreshold region [21, 22]. Moreover, the electric and logic characteristics in subthreshold region become very sensitive to various factors compared with above-threshold region. Consequently, a profound consideration of what kind of structure or operation mechanism is required, and what factors affect energy efficiency of the subthreshold CMOS devices is now necessary. Therefore, this dissertation seeks to explain the guideline of device design for ultra-low power metal-oxide semiconductor FETs (MOSFETs) in sub-0.3 V operation.

1.2 Objectives

This study offers two important insights for sub-0.3 V operation.

(1) Low Power CMOS Logic Circuits in Sub-0.3 V Operation

As mentioned previously, to date, a number of studies have reported about low power operation. Despite extensive researches, what is not yet clear is the impact of drain-induced barrier lowering (DIBL) to energy efficiency of CMOS logic circuits. DIBL is a kind of short channel effects, which causes V_{th} decrease by drain voltage (V_{ds}) increase in scaled devices. DIBL affect not only single transistors but also CMOS array such as static random access memory (SRAM) or non volatile memory [23-26]. Furthermore, the effects of DIBL become worse in subthreshold region because the drain current (I_{ds}) is affected exponentially. Hence, understanding the correlation between DIBL and energy efficiency of subthreshold CMOS logic circuits should be required.

(2) Low Power SRAM Cells in Sub-0.3 V Operation

As the V_{dd} is scaling down for low power consumption, contribution of the leakage power increase especially in memory part, and the V_{dd} of the memory part is larger than that of the logic

part remarkably in subthreshold region [27]. Besides, the V_{th} variability by random dopant fluctuation (RDF) become even worse in recent aggressively miniaturization so that stability of the SRAM is serious concerns for designing minimum operation voltage (V_{min}) [28]. In order to break the current limitation of V_{dd} scaling in SRAM cells, it is highly required to be suggested new operation mechanism. V_{th} self-adjustment is one of the suitable candidates for low voltage operation because of its enhanced on/off current ratio [29, 30]. Additionally, the V_{th} shift by sweep speed and direction difference facilitate improvement of stability in SRAM cells. In this study, V_{th} self-adjusting MOSFETs are analyzed in detail and combined with nanowire to realize SRAM cells for sub-0.3 V operation, also suppressing short channel effects.

1.3 Chapter Organizations

The overall structure of this study takes the form of two primary aims. The first half of the thesis (Chapter 2 and 3) introduce the CMOS logic circuits in subthreshold region from viewpoint of the DIBL. In chapter 2, in order to investigate about correlation between the DIBL and the energy efficiency, the subthreshold devices are analyzed by measurement, circuit simulation and calculation. Also, most of the advanced devices have overlooked the DIBL effects so that chapter 3 sheds light on a blind point about DIBL effects in steep subthreshold swing transistors. The second half of the thesis (Chapter 4 and 5) presents the new operation mechanisms for low power SRAM cells. In chapter 4, fundamentals of new operation mechanism which is called by V_{th} self-adjustment are ascertained by device simulation. Next, in chapter 5, fabrication of the V_{th} self-adjusting MOSFETs with nanowire and their electric characteristics is given. Also, simulation of SRAM cells with V_{th} self-adjustment on the basis of MOS parameters from fabricated devices is described. Lastly, conclusion and consideration of this study is summarized in chapter 6.

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Chapter 2

DIBL Effect on Subthreshold Devices

2.1 Introduction

For accomplishing low voltage operation regime, reducing leakage current is primarily requirement rather than fast operating frequency. The subthreshold device which is operated at near threshold region or further scaling subthreshold region is suitable for applying to ultra-low power consumption with moderate performance such as pacemakers, smart watch or tablet PC [1-4]. Hence, V_{dd} become less than V_{th} and subthreshold current use as operation current, in which is from channel with depletion or weak inversion. Meanwhile, in subthreshold region, the I_{ds} is heavily affected by abnormal factors, for example, short channel effects by aggressively scaled transistor sizes. DIBL is a sort of short channel effects as mentioned in chapter 1 and its impacts are already reported on single transistors, memory devices, even in the logic circuits [5, 6]. However, the effects of DIBL in subthreshold region have not been researched. Therefore, in this chapter, the DIBL effects on performance of the subthreshold devices and logic circuits are investigated. First, two transistors which have quite different DIBL are measured and compared to find out DIBL effects on actual devices. Next, CMOS ring oscillators with assuming various DIBL and V_{dd} are simulated for investigating circuit performance. Finally, the energy efficiency is calculated using simple analytic model to set up the correlation between DIBL and energy efficiency in subthreshold region.

2.2 DIBL Effect on Single Transistor in Subthreshold Region

1k bulk nMOSFETs by the 65 nm technology are measured and their DIBL are extracted. The DIBL distribution of 1k nMOSFETs is shown in Fig. 2.1. Among them, two nMOSFETs which

have large difference of DIBL are selected. This large distribution of DIBL is referred to originate from RDF [7, 8]. It is well known that V_{th} has random variability caused by RDF. It has been reported that DIBL has also variability due to RDF. In ref. [7], it is clearly shown by simulation that a device which happens to have more channel impurities near drain has larger DIBL, while a device which happens to have more channel impurities near source has smaller DIBL. Figure 2.2 (a) and (b) shows measured transfer curves of these two nFETs. DIBLs are 58.1 mV/V (Fig. 2.2 (a)) and 163.3 mV/V (Fig. 2.2 (b)). In order to examine the effects of DIBL with V_{dd}, normalized I_{ds} (I_{on}/I_{ds}) is shown in Fig. 2.3 as a function of normalized drain voltage (V_{ds}/V_{dd}), in which I_{on} is I_{ds} when $V_{gs} = V_{ds} = V_{dd}$. In Fig. 2.3 (a), the I_{ds} is degraded with large DIBL, but the decrement is not remarkable. In case of the V_{dd} = 0.3 V as subthreshold region (Fig. 2.3 (b)), the I_{ds} of the small DIBL shows similar characteristic with V_{dd} = 0.9 V. On the other hand, there is a huge current degradation with large DIBL and it is notable phenomenon compared with above threshold region (V_{dd} = 0.9 V). Figure 2.4 shows this phenomenon by different points of view. Figure 2.4 (b) shows broad variation of normalized I_{ds} with V_{dd} in contrast with Fig. 2.4 (a). This variation with V_{dd} is re-plotted in Fig. 2.5. The normalized I_{ds} (at V_{ds}/V_{dd} = 0.5) is shown as a function of V_{dd} with small and large DIBL devices. In small DIBL device, the I_{ds}/I_{on} show small variation and keep about 0.85 with V_{dd} scaling. On the contrary, there is substantial current degradation in large DIBL device and the I_{ds}/I_{on} eventually drop to minimum value at V_{dd} = 0.3 V as subthreshold region. Thus, the performance of the subthreshold device is strongly influenced by DIBL compared with above threshold region because the characteristics become very sensitive in subthreshold region. Interestingly, the I_{ds}/I_{on} increase again with more scaling less than 0.3 V in large DIBL device. It is considered that the V_{ds} is too small to affect performance despite of subthreshold region.

2.3 DIBL Effect on CMOS Logic Circuit

The effects of DIBL on the characteristics of actual devices were confirmed in the subthreshold region, and the results said that DIBL heavily affects device performance in the subthreshold region. In order to estimate DIBL effects on circuit performance, CMOS logic circuits were simulated using SPICE. Five sets of nMOSFETs and pMOSFETs (A–E) with different DIBL values are adopted and summarized in Table I. Among them, the transfer characteristics of the smallest DIBL device (~20 mV/V) (Fig. 2.6 (a)) and the largest DIBL device (~ 180 mV/V) (Fig. 2.6 (b)) are plotted in Fig.3. I_{off} and I_{on} are fixed at V_{ds} = 1.2 V so that DIBL affect I_{ds} at V_{ds} = 0.05 V. The V_{th} change with V_{ds} of each nMOSFETs and pMOSFETs are shown in Fig. 2.7. Figures 2.8 (a) and 2.8 (b) show the output characteristics of simulated five sets of nMOSFETs and pMOSFETs at V_{dd} = 1.2 V and 0.3 V, respectively. I_{on} is fixed at $V_{gs} = V_{ds} = V_{dd}$ among the devices. Both of Fig. 2.8 (a) and (b) shows current degradation with DIBL increase at V_{ds}/V_{dd} = 0.5, but the decrement is much more severe as the V_{dd} is scaled down into 0.3 V at subthreshold region. Moreover, the saturation characteristics almost disappears with DIBL increase at V_{dd} = 0.3 V. It means that DIBL affect device performance and it become even critical in subthreshold region same as actual devices in chapter 2.2 and Fig. 2.9. There is a comparison between simulation and measurement which have similar DIBL in Fig. 2.9, the normalized I_{ds} as a function of V_{ds}. Both of them show similar current degradation and non-saturation characteristics. Also, it is confirmed that the simulation is well-matched with measuring actual devices.

In order to examine the effects of DIBL on circuit characteristics, the CMOS ring oscillators are simulated with the five sets of nMOSFETs and pMOSFETs (A–E). Figure 2.10 (a) shows the delay times of the simulated CMOS ring oscillators. Even though all the devices have same I_{on} as shown in Fig. 2.8, the largest DIBL device ‘E’ shows the slowest delay at whole V_{dd}. Figure 2.10 (b) shows delay increment ratio with various DIBL and V_{dd}, which are normalized by the smallest DIBL device ‘A’. In spite of the large DIBL device ‘E’, the delay increment ratio is less than 30 % in

above threshold region (V_{dd} = 0.6 ~ 1.2 V). On the contrary with above threshold region, in subthreshold region at 0.3 V, the delay increment ratio dramatically rises up to approximately 80 % in the largest DIBL device 'E'.

This phenomenon is well explained by introducing the effective current (I_{eff}) [5, 6]. Conventionally, I_{on} is a good parameter to estimate CMOS delay time. However, when the CMOS logic switches actually, the charging and discharging current from load capacitor does not reach to I_{on} [9-12]. Figures 2.11 (a) and (b) shows simulated output curves of nMOSFETs and trajectory curves with various DIBL at V_{dd} = 1.2 and 0.3 V, respectively. As shown in Fig. 2.11, the current values of trajectory curves do not reach to I_{on}. Once I_{eff} is adopted instead of I_{on}, the actual switching current in CMOS logic operation is well covered so that I_{eff} is a more proper metric delay (CV/I_{eff}) to estimate CMOS rather than I_{on} (CV/I_{on}). The correlation between I_{eff} and CMOS delay time with various DIBL and V_{dd} is shown in Fig. 2.12. The delay time and I_{eff} are exponentially degraded with V_{dd} scaling and this phenomenon is getting worse in subthreshold region. Furthermore, this degradation becomes more severe with DIBL increase (from the smallest DIBL device 'A' to the largest DIBL device 'E"). In addition, trajectory curves in Fig. 2.11 (b) shows more degradation by DIBL compared with Fig. 2.11 (a) and these results also support the correlation. This is the reason why the delay degradation by DIBL increase in subthreshold region is more critical compared with above threshold region despite of the same I_{on} [5].

2.4 Energy Efficiency in Subthreshold Region with DIBL

From chapter 2.3 and 2.4, the negative effects of DIBL to actual devices and simulated CMOS logic in subthreshold region was proven. Consequently, current and delay degradation by DIBL may affect energy efficiency because it is product of power consumption and delay time. Hence, in this chapter, the energy consumption with various DIBL in subthreshold region is calculated using

simple analytic equation.

First, the subthreshold current is expressed as,

$$I_{sub.} = I_0 \exp\left(\frac{q\left(V_{gs} - (V_{th} - \eta V_{ds})\right)}{nkT}\right) \qquad (1)$$

where I_0 is reference current at $V_{gs} = V_{th}$ and in this case, 100 nA. q/kT and n are reversed thermal voltage and body factor, respectively. DIBL is adjusted by η factor which is defined by $|\Delta V_{th}/\Delta V_{ds}|$. Figure 2.13 shows calculated subthreshold current with various DIBL. In Fig. 2.13 (a), the I_{on} and I_{off} is fixed at $V_{gs} = V_{ds} = V_{dd}$ same as in Fig. 2.6. Figure 2.13 (b) shows output characteristics of calculated subthreshold current with DIBL value of 180 mV/V. The current degradation at $|V_{ds}/2|$ and non-saturation characteristics is very similar with measured actual devices and simulation. Even if energy efficiency has various previous models [13-17], in this study, the model become more simplified and the equation is defined as,

$$\mathrm{E} \propto \mathrm{P} \times \mathrm{D} = \left(\xi I_{eff} + I_{off}\right)V \times \frac{CV}{I_{eff}} = CV^2\left(\xi + \frac{I_{off}}{I_{eff}}\right) \qquad (2)$$

$$I_{eff} = \frac{\left(I_{ds}\ @\ V_{gs} = \frac{V_{dd}}{2}, V_{ds} = V_{dd}\right) + \left(I_{ds}\ @\ V_{gs} = V_{dd}, V_{ds} = \frac{V_{dd}}{2}\right)}{2} \qquad (3)$$

where I_{eff} and C are effective drive current [6] and load capacitance, respectively. ξ is active time ratio which is the average number of transistor switches per cycle and set to be 0.01 in this chapter. In the previous research [14], the DIBL effects on energy efficiency have already been reported. The main differences between this study and ref. [14] are twofold: (1) V_{th} is fixed at linear region in Ref. [14], whereas V_{th} is fixed at saturation region in this study as shown in Fig. 2.6 and 2.13 (a); (2) CV/I_{on} metric is used for delay calculation in Ref. [14], whereas in this study, CV/I_{eff} is introduced for more proper estimation.

Figure 2.14 shows calculated energy consumption with various DIBL as a function of V_{dd}. Energy consumption decreases with V_{dd} decrease into the subthreshold region and reaches optimal

point below 0.3 V due to reduction of power consumption by V_{dd} scaling [15, 16]. However, the optimal points of V_{dd} and energy consumption are getting worse with DIBL increase because delay time degradation become dominant with V_{dd} scaling into subthreshold region. Therefore, these results suggest that suppressing DIBL is highly required to realize for high energy efficiency subthreshold circuits.

2.5 Summary

The DIBL effects on actual devices and CMOS circuits operating in the subthreshold region are examined by measurement and simulation. It is confirmed from measuring actual device that a transistor with a large DIBL shows severe current degradation compared with a small DIBL, especially in the subthreshold region. This is because the DIBL make V_{th} change and the subthreshold characteristic is very sensitive to V_{th} variation. Additionally, CMOS ring oscillators composed by large DIBL transistors show degraded delay, especially in subthreshold region because I_{eff} degraded by DIBL and it become worse in subthreshold region despite of same I_{on}. As a result, severe delay degradation by DIBL in subthreshold region leads to energy consumption increase although the power consumption is reduced by V_{dd} scaling. Therefore, DIBL should be suppressed for designing of high energy efficiency CMOS circuits in the subthreshold region.

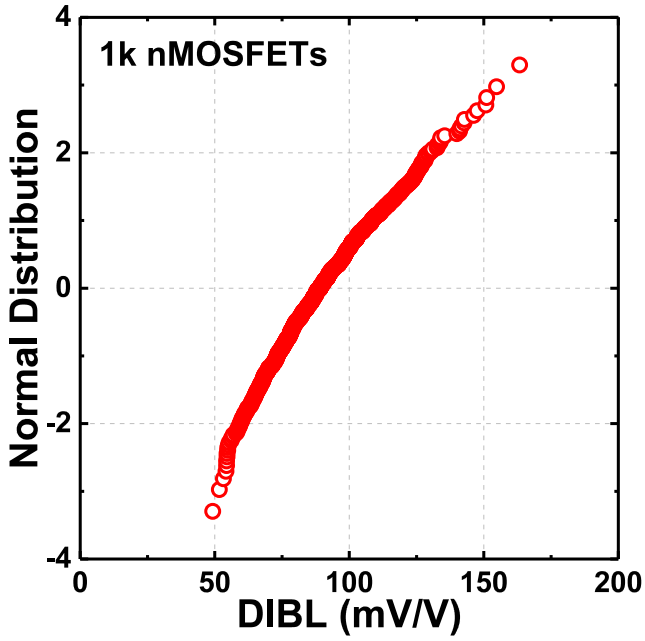

Figure 2.1 Normal distribution of DIBL from 1k bulk nMOSFETs fabricated by the 65 nm technology. The DIBL distribution is caused by unbalanced impurities location in the channel.

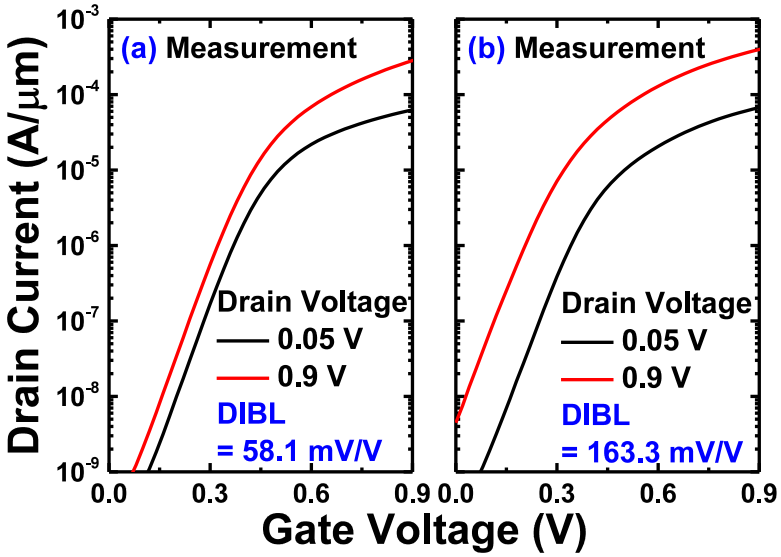

Figure 2.2 Transfer curves of measured bulk nMOSFETs with (a) small (58.1 mV/V) and (b) large DIBL (163.3 mV/V).

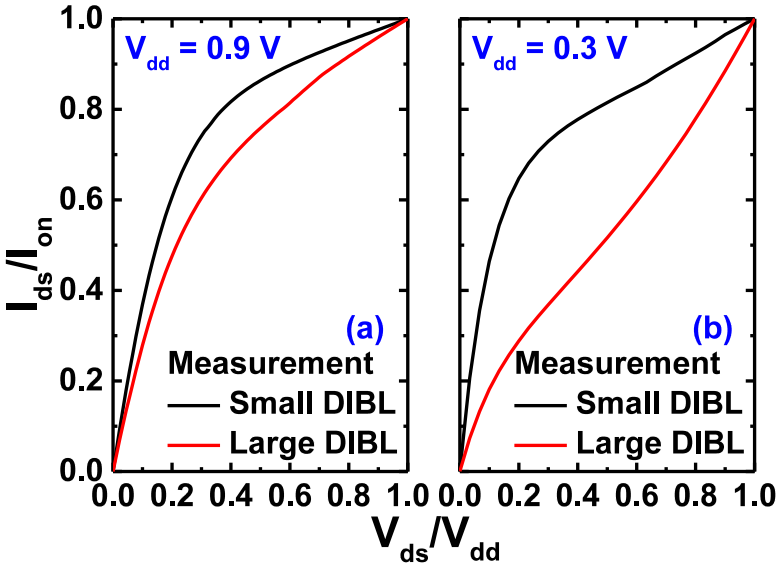

Figure 2.3 Normalized output curves of measured bulk nMOSFETs with DIBL in (a) above threshold region (V_{dd} = 0.9 V) and (b) subthreshold region (V_{dd} = 0.3 V). There is severe current degradation between small and large DIBL in subthreshold region.

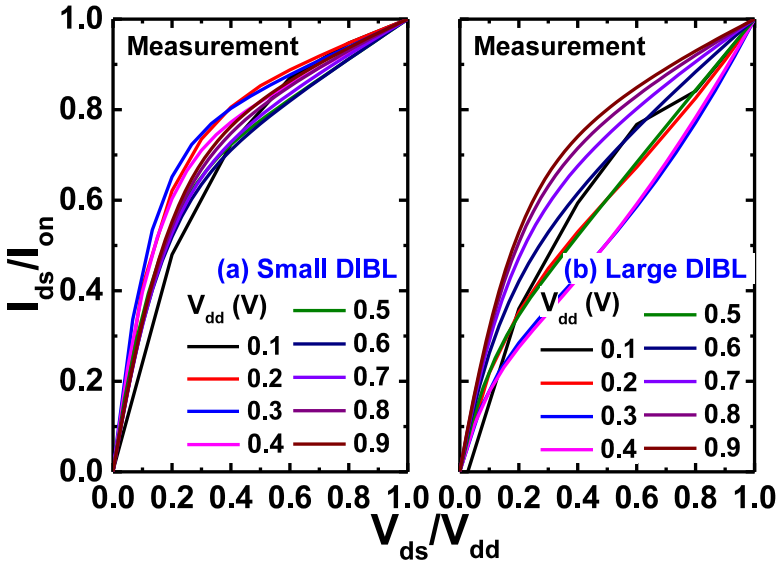

Figure 2.4 Normalized output curves of measured bulk nMOSFETs with various V_{dd}. (a) shows small DIBL and (b) shows large DIBL. Large DIBL device shows more variation in performance.

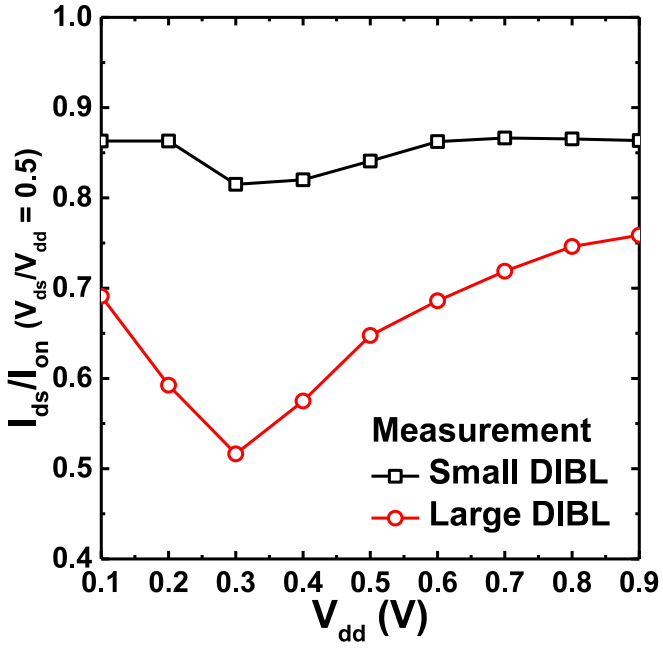

Figure 2.5 Normalized I_{ds} (at V_{ds}/V_{dd} = 0.5) as a function of V_{dd} with small and large DIBL. Large DIBL device shows huge current degradation until at V_{dd} = 0.3 V, subthreshold region.

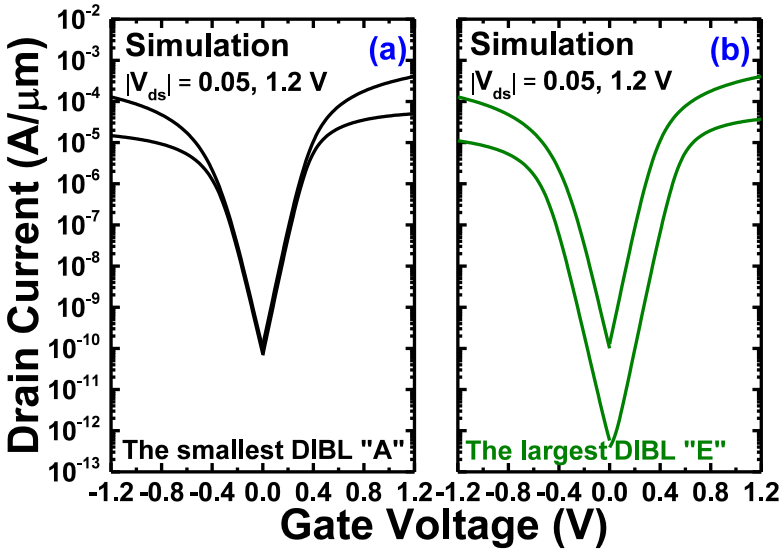

Figure 2.6 Simulated transfer curves of (a) the smallest DIBL device 'A' and (b) the largest DIBL device 'E'. I_{on} and I_{off} is fixed at $V_{gs} = V_{ds} = V_{dd}$ so that DIBL is reflected at V_{ds} = 0.05 V

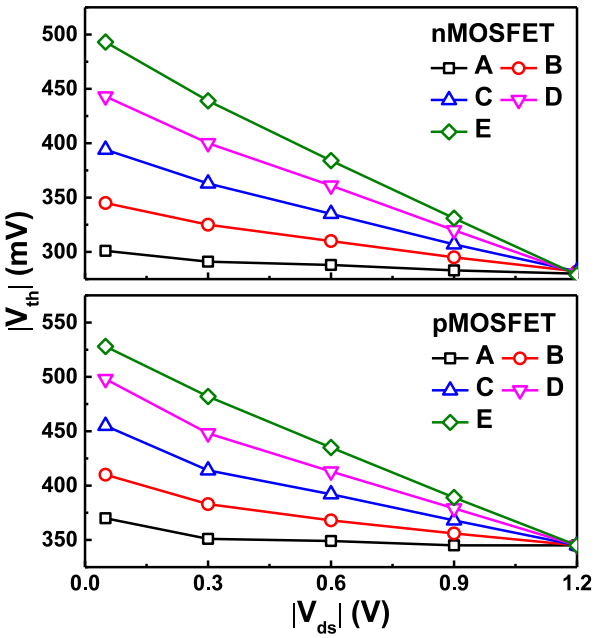

Figure 2.7 V_{th} shift by various V_{ds} with simulated nMOSFETs and pMOSFETs.

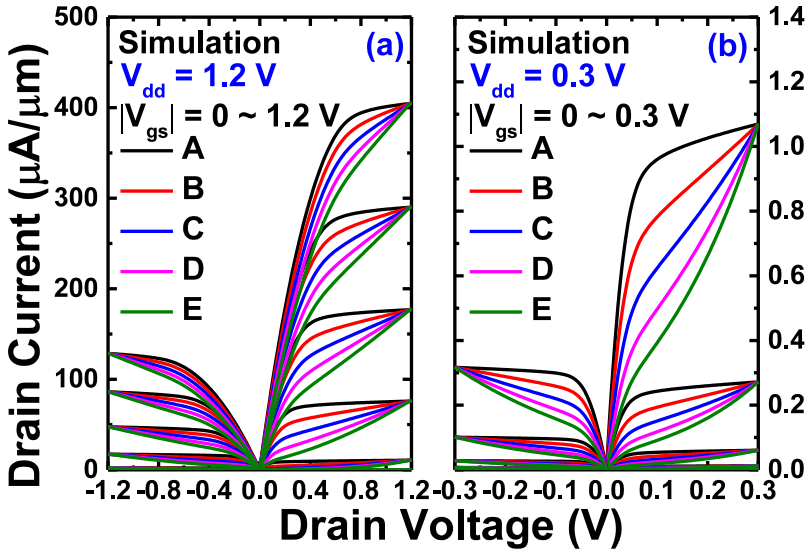

Figure 2.8 Simulated output curves with various DIBL of (a) above threshold region (V_{dd} = 1.2 V) and (b) subthreshold region (V_{dd} = 0.3 V). Current at $|V_{ds}/2|$ is degraded by DIBL increase, particularly at V_{dd} = 0.3 V.

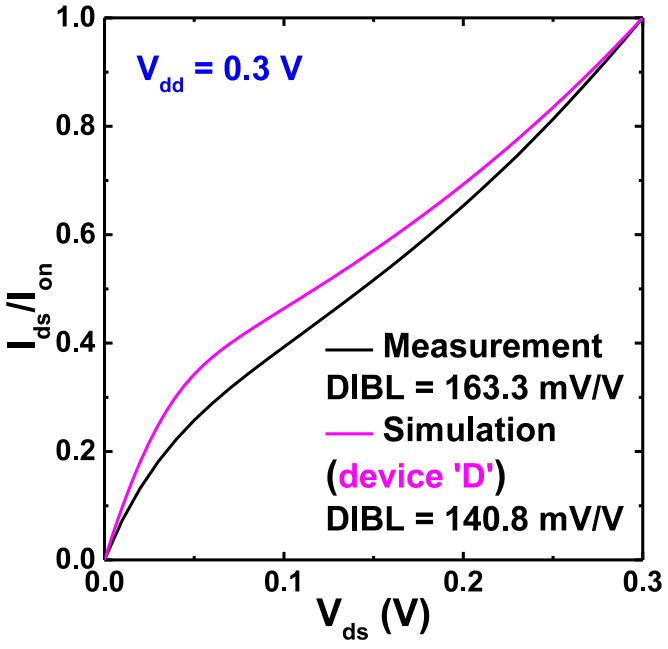

Figure 2.9 Comparison between normalized I_{ds} of measurement and simulation which have similar DIBL in subthreshold region. The simulation is well-matched with actual device.

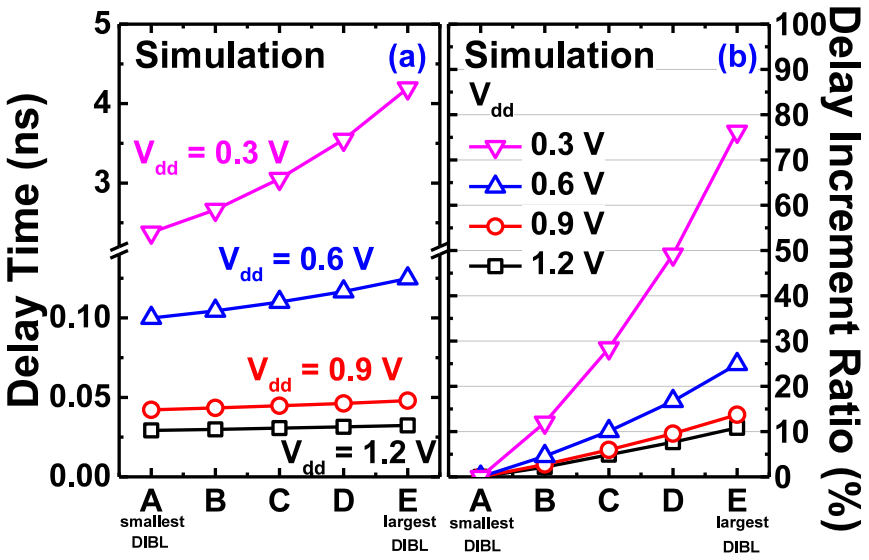

Figure 2.10 Delay time of CMOS ring oscillators with various V_{dd} and DIBL The largest DIBL device 'E' in subthreshold region shows the slowest delay time.

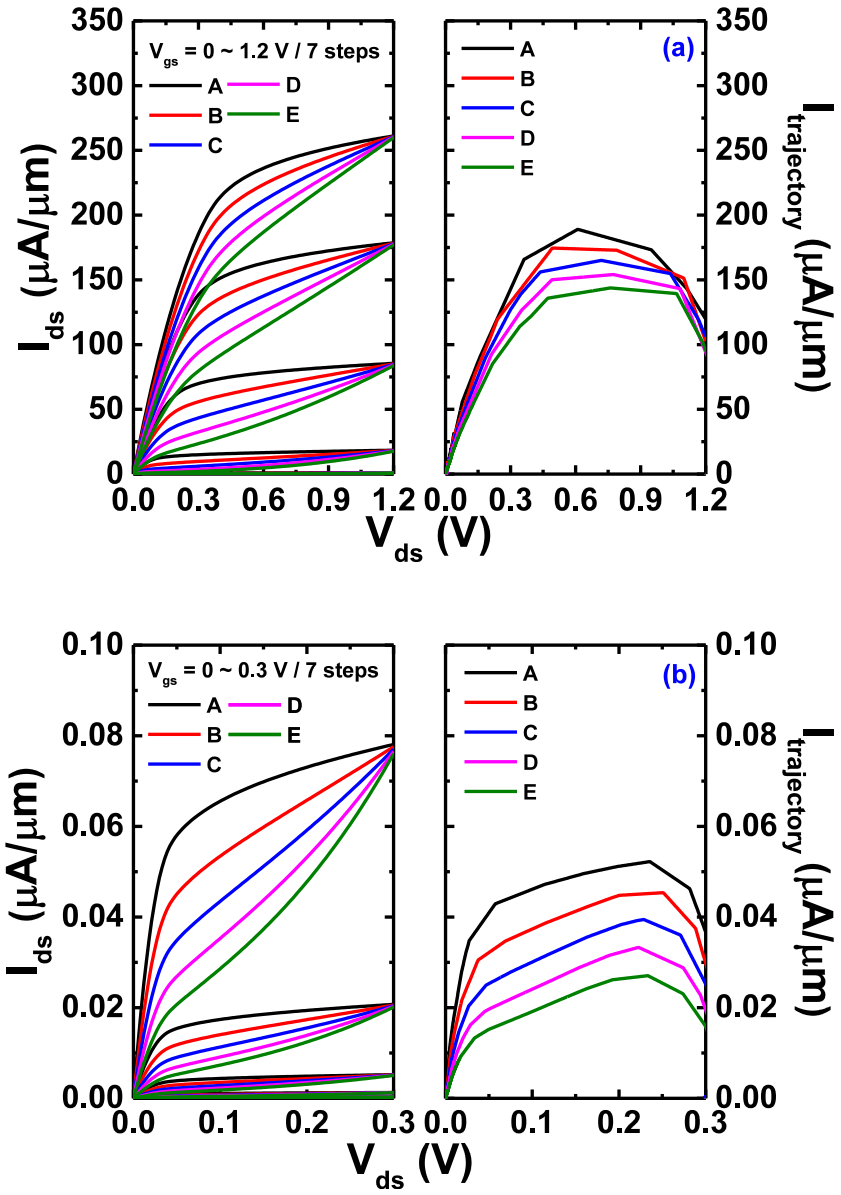

Figure 2.11. Simulated output curves and trajectory current with various DIBL at (a) V_{dd} = 1.2 V and (b) 0.3 V. The degradation of trajectory current by DIBL at V_{dd} = 0.3 is much more severe than V_{dd} = 1.2 V.

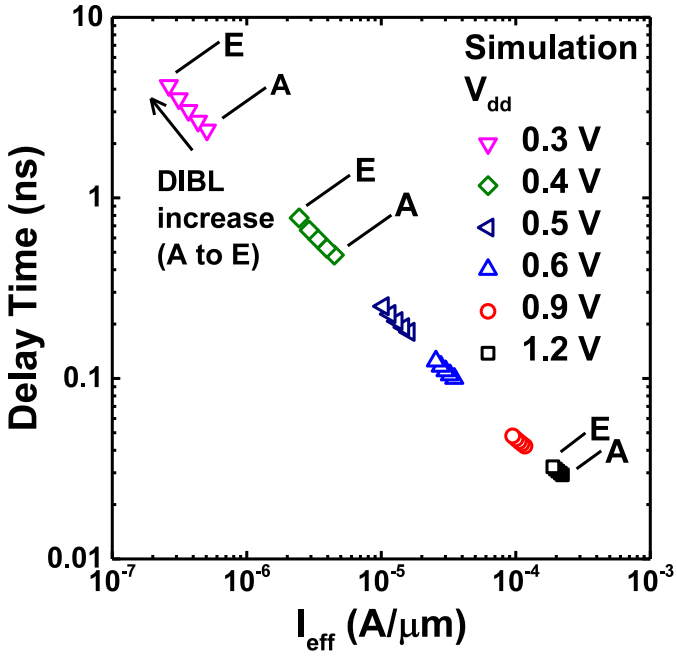

Figure 2.12 Correlation between delay time and I_{eff} with various V_{dd} and DIBL. Delay time and I_{eff} is degraded exponentially with V_{dd} scaling and becomes worse with DIBL increase.

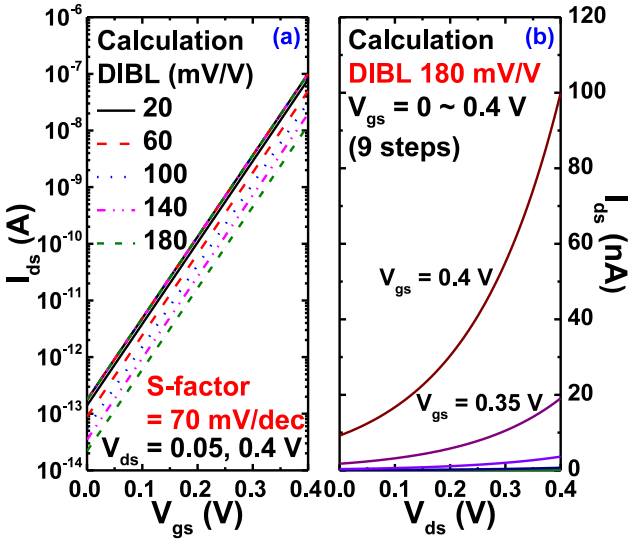

Figure 2.13 Calculated subthreshold current in (a) transfer curves with various DIBL and (b) output curves with DIBL value of 180 mV/V.

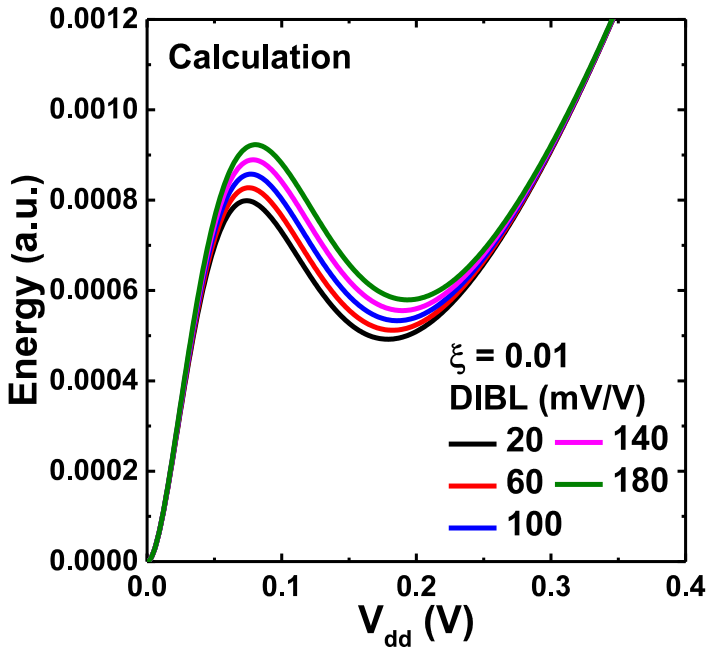

Figure 2.14 Calculated energy efficiency with various DIBL as a function of V_{dd}. The minimum points of energy consumption and V_{dd} become worse with DIBL increase.

	DIBL (mV/V) at V_{dd} = 1.2 V	
	nFET	pFET
A	18.2	21.7
B	55.6	53.5
C	98.2	95.6
D	140.8	133.0
E	184.3	171.3

Table I DIBL values of the simulated five sets of nMOSFETs and pMOSFETs.

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Chapter 3

DIBL Effect on Steep Subthreshold Swing Transistors

3.1 Introduction

Trade-off between low power consumption and high performance is one of the most frequently stated problems in advanced semiconductor industry. The simplest way to overcome the obstacle is improving subthreshold characteristics. The parameter which reflect how sharply current rise and current drop in subthreshold characteristics is subthreshold swing slope (s-factor) and following as,

$$\mathrm{s-factor} = (\ln 10)\frac{dV_{gs}}{d(\ln I_{ds})} = (\ln 10)\frac{kT}{q}\frac{dV_{gs}}{d\Psi_s} = (\ln 10)\left(1+\frac{C_d}{C_{ox}}\right) \qquad (1)$$

where ψ_s is surface potential of channel and kT/q is thermal voltage. C_{ox} and C_d is capacitance of gate oxide and channel, also C_d/C_{ox} means body factor, γ. If there is no potential drop from gate to channel or body factor is zero, the s-factor becomes 60 mV/dec which is theoretical limit. To break the limit for obtaining further low power consumption and high performance simultaneously, the advanced researches whose name are steep s-factor transistors have been studied [1-6]. Therefore, the steep s-factor transistors are strong contender for energy efficient CMOS device.

Meanwhile, the researches of the steep s-factor transistors to date have tended to focus on realizing s-factor less than 60 mV/dec with obtaining high I_{on}. However, some TFETs which are the most prospect technology among steep s-factor transistors have been shown 'V_{th} shift by V_{ds}', *e.g.* vertical structure of InGaAs TFET showed 0.92 between V_{ds} = 0.05 and 0.75 V [7] and in case of InAs nanowire TFET, it showed as large as 0.74 below V_{ds} = 0.3 V [8]. This variation in TFETs is similar to DIBL in conventional MOSFETs but the mechanism is different [9]. Up to now, far too little attention has been paid to 'V_{th} shift by drain V_{ds}' in TFETs and it may have an effect on energy efficiency of steep s-factor transistors. Therefore, the correlation between DIBL and s-factor in

terms of energy efficiency is investigated in this chapter using calculation with simple analytic model.

3.2 Energy Efficiency with Subthreshold Swing

Figure 3.1 shows transfer curves of conventional MOSFET and steeper s-factor transistor. Once s-factor become steeper, higher I_{on} can be obtained. Hence, it is not required to reduce V_{th} for high I_{on} current with V_{dd} scaling so that low leakage current can be attained. Consequently, high energy efficiency can be expected to achieve. In order to estimate energy efficiency with s-factor, first, the subthreshold current is calculated using equation (1) in chapter 2.4. Figure 3.2 shows calculated subthreshold current with various s-factor from 30 to 70 mV/dec with $\eta = 0$. η was DIBL factor in chapter 2.4, but in this chapter, η defines 'V_{th} shift by V_{ds}' factor. I_{off} is fixed among various s-factors to reflect appropriate steep s-factor effect. From Fig. 3.2, the subthreshold characteristics improve exponentially with steeper s-factor. The energy efficiency with various s-factor is calculated using equation (2) in chapter 2.4 and shown in Fig. 3.3. The optimal points of energy consumption and V_{dd} are getting smaller with steeper s-factor. Especially, V_{dd} is scaled down into even around 0.1 V with extremely low energy consumption when the S is 30 mV/dec. As a result, the steep s-factor transistors are very suitable for high energy efficiency by improving subthreshold characteristics.

3.3 Energy Efficiency of Steep Subthreshold Swing Transistors with DIBL

Even though the steep s-factor transistors showed high energy efficiency, what will be the result if device is influenced by 'V_{th} shift by V_{ds}'. Figure 3.4 shows calculated subthreshold current of steep s-factor transistor with 30 mV/dec. Figure 3.4 (a) shows transfer curves with various η factors and I_{on} and I_{off} is fixed at $V_{gs} = V_{ds} = V_{dd}$ so that DIBL affect device performance at $V_{ds} = 0.05$ V.

Figures 3.4 (b) and (c) shows linear and semi-log plot of output curves with η = 0.2, respectively. Note that, as the s-factor is getting steeper, subthreshold characteristics become extremely sensitive. Thus, current degradation by η factor is much more severe and I_{ds} shows exponential property with V_{ds} compared with conventional MOSFETs in Fig. 2.8. Figure 3.5 shows calculated V_{dd} dependence of energy consumption at steep S as 30 mV/dec with various η factors. It is found that the minimum point of energy consumption and V_{dd} is increasingly larger with η factor increase. In case of η as 0.7, the minimum point of energy consumption and V_{dd} almost doubled compared with η = 0 despite of s-factor = 30 mV/dec. Once the η factor is getting worse, I_{eff} is degraded. Therefore, the I_{off}/I_{eff} ratio become increasing so that the energy efficiency is worsening.

3.4 Summary

The steep s-factor transistors are one of the promising technologies for high energy efficiency because V_{dd} can be scaled down with keeping allowable I_{on}. However, even though the transistor has steep s-factor, the energy efficiency is degraded if the η factor is getting worse. Consequently, the η factor should be suppressed to take advantage of steep s-factor effect in energy efficient CMOS logic using steep s-factor transistors.

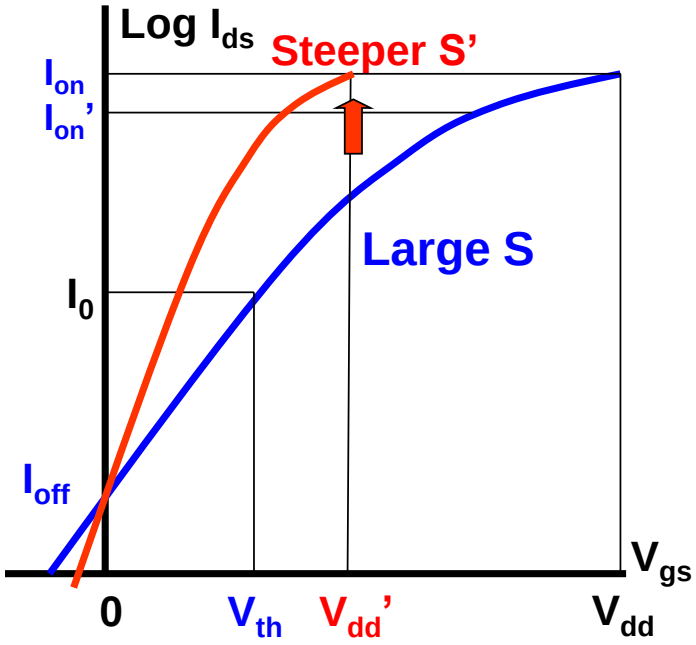

Figure 3.1 Transfer curves with large and steeper s-factor. Steeper s-factor leads to high performance with V_{dd} scaling.

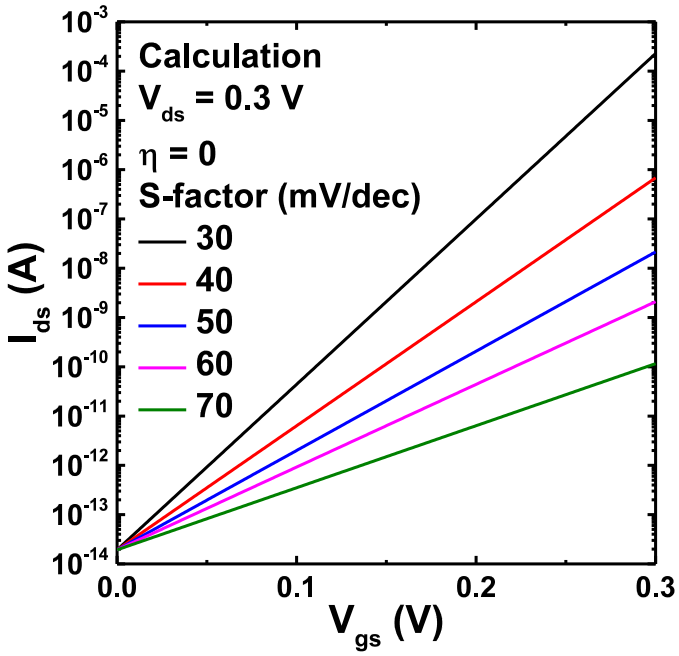

Figure 3.2 Calculated transfer curves with various s-factors.

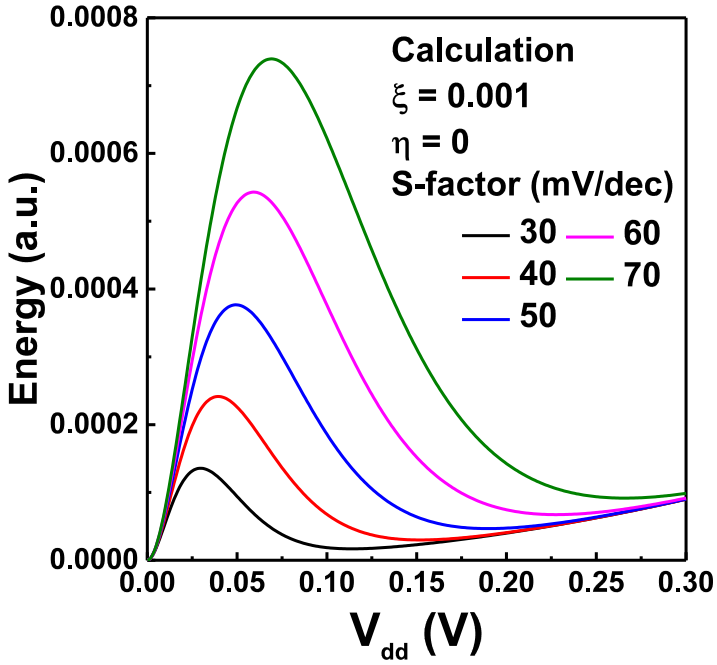

Figure 3.3 Calculated V_{dd} dependence of energy consumption with various s-factors when η factor is zero. The minima of V_{dd} and energy consumption decrease with steeper s-factor.

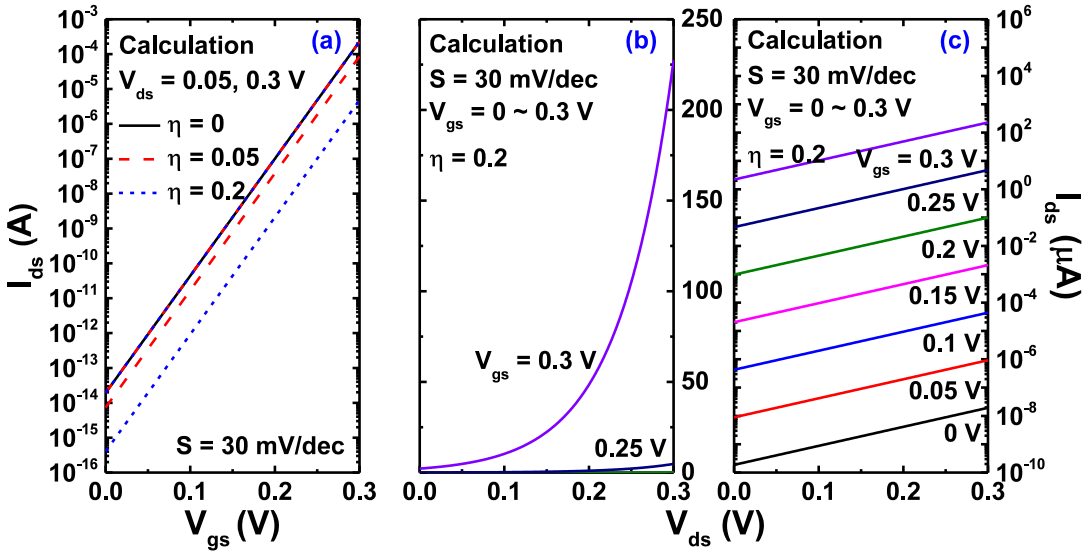

Figure 3.4 Calculated subthreshold current of steep s-factor as 30 mV/dec. (a) transfer curves with various η factors. (b), (c) linear and semi-log plot of output curves with η factor = 0.2, respectively.

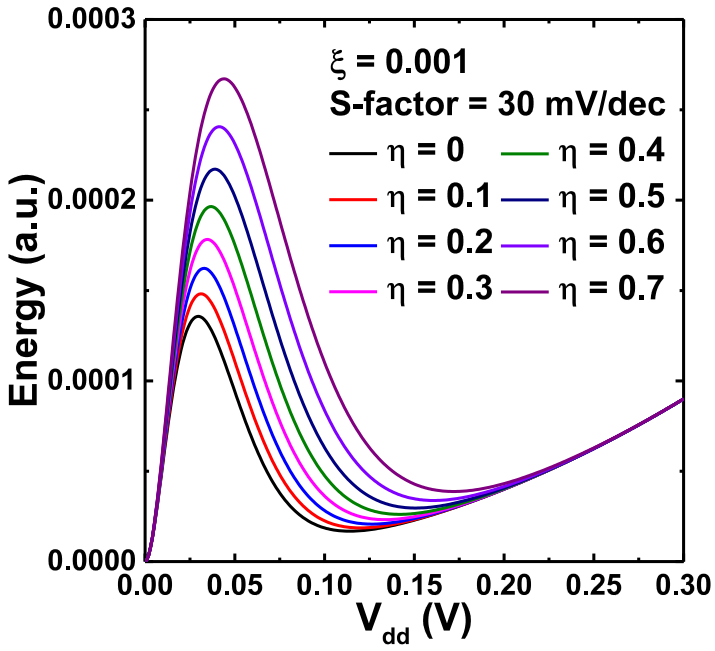

Figure 3.5 Calculated V_{dd} dependence of energy at s-factor =30 mV/dec with various η factors. The optimal points of V_{dd} and energy consumption become larger with η factor increase.

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Chapter 4

New Mechanism for Low Power Operation

4.1 Introduction

To date, half of this study suggested the way to achieve high energy efficiency CMOS logic circuits operating in sub-0.3 V. For aggressively scaled integration of semiconductor chips, it is required to achieve not only miniaturization of logic circuits but also integration with the other components, for example memory chips, image signal processors (ISP) or audio signal processors (ASP). Such an embedded approach which is called by system-on-chip (SoC) is very important concept in future semiconductor industry. Moreover, mobile application processors (AP) for portable devices such as cell phone, tablet PC or hand-held electronic devices also demand SoC technology for more integration as well as low power operation. Meanwhile, as the V_{dd} is scaled down into subthreshold region, memory parts in embedded chips become increasingly large part of power consumption [1]. The SRAM cells are dominant on power consumption among memory blocks due to consisting of their relatively a large number of transistors. Consequently, SRAM cells with low operation voltage are necessary to develop for advanced embedded multi chip package.

A major concern about SRAM operation with low voltage is stability as expressed by static noise margin (SNM). In scaled V_{dd}, the random variability of transistors becomes severe so that it is required to develop careful and complex design for suppressing operation failure. To enhance the properties of SRAM cells in scaled V_{dd}, dynamic V_{th} MOSFET (DTMOS) SRAM have been suggested [2, 3]. In DTMOS, body potential follows gate potential because the gate electrode and body are tied. Thus, V_{th} can be shifted by body effect; high V_{th} for low leakage current (standby mode), low V_{th} for high I_{on} (active mode) [4-6]. The controllable V_{th} in DTMOS facilitate flipping

range of the cross-coupled inverters in SRAM cell. Therefore, the stability of SRAM cells can be improved even in the operation in subthreshold region. In future VLSIs, fully depleted silicon-on-insulator (FD-SOI) is essential to enable further improvement of MOSFETs. However, the FD-SOI is hard to apply to DTMOS because of trade-off between body factor and s-factor. Somewhat body factor is needed for DTMOS, but thick buried oxide (BOX) layer in FD-SOI make body factor small and hinder V_{th} shift. Once thickness of BOX layer becomes thin for obtaining large body factor, s-factor is degraded and even parasitic capacitance between substrate and drain increase. Although variable body factor FD-SOI has been studied, the additional electrode leads to complex device design [7, 8]. Hence, new operation mechanism to complement the DTMOS emerged, whose name is V_{th} self-adjusting MOSFETs [9, 10]. V_{th} self-adjusting MOSFETs have similar structure with conventional floating gate memory but the tunneling site is different. The time-lag approach enable control the carrier tunneling so that two states of V_{th} (standby and active mode for dynamic characteristic) are feasible and on/off current ratio can be improved (thermal-equilibrium mode for static characteristic).

Therefore, in this chapter, the operation mechanism of V_{th} self-adjusting MOSFETs is investigated. Even if V_{th} self-adjusting MOSFETs have been studied, they showed high operation voltage [9, 10], non-silicon based transistor as ferroelectric material [9] and furthermore, weak device structure to short channel effects [11]. Thus, tri-gate nanowire MOSFETs with V_{th} self-adjustment is proposed to apply SRAM cells with strong immunity to short channel effects and sub-0.3 V operation.

4.2 Operation Mechanisms of V_{th} self-adjusting MOSFETs

Figure 4.1 shows schematic structure and transfer curves of conventional floating gate memory (Fig. 4.1 (a)) and V_{th} self-adjusting MOSFET (Fig. 4.1 (b)). In conventional floating gate memory,

the tunneling site is located between channel and floating gate because of thin tunnel oxide layer. Once the electrons come into floating gate (program), V_{th} become increase and *vice versa* (erase). ΔV_{th} is determined by capacitance of control oxide (C_c) and charges in floating gate (Q). The most different thing between conventional floating gate memory and V_{th} self-adjusting MOSFETs is position of tunneling site. The control oxide between control gate and floating gate become thinner and gate oxide become thicker so that carrier tunnel through upper oxide layer. Therefore, control gate governs not only electric field to channel but also tunneling between control gate and floating gate. There are two operation characteristics in V_{th} self-adjusting MOSFETs. The sequence of sweep voltage versus sweep time is plotted on Fig. 4.2. Dynamic characteristics (forward and backward sweep) show fast (or finite) sweep time after slow (or infinite) hold time. On the other hand, there is slow (or infinite) sweep time per each applied voltage in static characteristic. As a result, there is time-lag between dynamic and static characteristics so that tunneling of carriers is under the control by sweep time. Figures 4.3 (a) and (b) show electric potential of dynamic and static characteristics in case of nMOSFET (Fig. 4.3 (a) shows forward and static, Fig. 4.3 (b) shows backward and static characteristic). In Fig. 4.3 (a), forward and static show same electric potential because of infinite hold time at initial point. During infinite hold time, electrons tunnel into control gate from floating gate. The infinite hold time is enough to make same potential between control gate and floating gate (thermal-equilibrium state). On the contrary, if the gate voltage increases, there is time-lag between dynamic and static characteristics. Electrons can tunnel into control gate in case of static characteristic same as initial point. However, there is no enough time to tunnel in dynamic characteristic (transient state). Thus, electrons remain in floating gate and make potential lower. The potential difference between dynamic (Ψ_{Si} (forward)) and static (Ψ_{Si} (static)) characteristics bring about s-factor difference referring to equation (1) in chapter 3. The improved s-factor in static characteristic leads to enhanced on/off current ratio. The backward and static

characteristics in Fig. 4.3 (b) also can be explained by same way. In other words, tunnel oxide can be ignored because control and floating gate have same electric potential in static characteristic. So, the gate oxide is considered as entire oxide layer in MOSFET. On the other hand, in dynamic characteristic, the potential of floating gate have no enough time to catch up with that of control gate, hence, the combination of tunnel oxide, floating gate and gate oxide become entire oxide layer in MOSFET. Namely, the difference between dynamic and static characteristics is gate capacitance of MOSFET. This structural difference is simplified in Fig. 4.4. When the tunnel oxide layer is 1 nm and gate oxide layer is 1 nm, the dynamic and static structure become like Fig. 4.4 (a). Besides, Fig. 4.4 (b) and (c) show in case of thicker tunnel oxide and thinner gate oxide, respectively. Figure 4.4 shows schematic structure, transfer curves, electric potential and s-factor with V_{dd} = 1 V of each case in order of the vertical. When the thickness of tunnel oxide becomes thicker in Fig. 4.4 (b), the ΔV_{th} become larger because of small C_c and large electric potential drop difference between forward and backward. As a result, improvement of s-factor between dynamic and static become enhanced. In case of thinner gate oxide in Fig. 4.4 (c), even if ΔV_{th} become smaller, the entire s-factor is improved. To sum up, in order to obtain large ΔV_{th} and small s-factor, the tunnel oxide should be as thick as possible to occur tunneling and the gate oxide should be as thin as possible to prevent tunneling between channel and floating gate. Figure 4.5 shows schematic structure, transfer curves, electric potential and s-factor at V_{dd} = 0.3 V, subthreshold region with same assumption in Fig. 4.4 and the results correspond to above threshold region.

4.3 Scalability of V_{th} Self-adjusting MOSFETs

In order to investigate the V_{th} self-adjusting MOSFETs for suppressing short channel effects and sub-0.3 V operation, two-dimensional device simulation is carried out using HyENEXSS. Figure 4.6 shows schematic structure of simulated V_{th} self-adjusting MOSFET with FD-SOI. Note that

thickness difference between tunnel oxide and gate oxide. Performances of V_{th} self-adjusting MOSFETs are heavily depend on tunneling phenomenon and it is correlated to thickness of tunnel oxide and sweep speed. Figure 4.7 shows simulated ΔV_{th} with tunnel oxide thickness as a function of sweep time. In case of thin tunnel oxide, ΔV_{th} become small with same sweep speed because of large C_c as mentioned above. Also, as the sweep speed is getting faster, ΔV_{th} become larger because electrons are restrained tunneling between control and floating gate by further time-lag. Figure 4.8 shows simulated transfer curves of V_{th} self-adjusting MOSFET at V_{dd} = 1 V with 2 nm of tunnel oxide. The sweep speed is 1 V/ms. The ΔV_{th} and improvement of on/off current ratio is successfully demonstrated. The ΔV_{th} is 75.9 mV and it is enough to apply to SRAM cells for enhancing its stability [10]. Figure 4.9 shows simulated transfer curves of V_{th} self-adjusting MOSFET at V_{dd} = 0.3 V. The V_{th} self-adjusting characteristics is confirmed even in the subthreshold region and it means that V_{th} self-adjusting MOSFETs are suitable for sub-0.3 V operation. Figure 4.10 shows ΔV_{th} as a function of V_{dd}. Even though ΔV_{th} become smaller with V_{dd} scaling, V_{th} self-adjusting characteristic is clearly shown in ultra-low V_{dd} such as 0.1 V.

Meanwhile, in the nanometer regime of CMOS devices, it is required to be scaled down not only transverse direction but also perpendicular direction for by scaling factor to suppress short channel effects. However, V_{th} self-adjusting MOSFETs with planar structure have to keep perpendicularly floating gate to hold carriers and somewhat thickness of gate oxide to prevent tunneling. Hence, it is constrained from suppressing short channel effects. Figure 4.11 shows simulated transfer curves with channel length (L_{ch}) of 5 and 0.15 μm. As expected, there are severe short channel effects when L_{ch} is scaled down to even 0.15 μm. The DIBL and s-factor with channel length form 5 to 0.08 μm is shown in Fig. 4.12. The DIBL and s-factor are drastically degraded from sub-0.3 μm and these results clearly show weakness of V_{th} self-adjusting MOSFETs with planar structure to short channel effects. Therefore, it is necessary to introduce advanced structure to V_{th} self-adjusting

MOSFETs for effective channel control.

4.4 Tri-gate Nanowire MOSFETs with V_{th} Self-adjustment

The most effective way to reduce short channel effects is enhancing channel controllability using multiple gate [12, 13]. Actually, the combination of gate-all-around (GAA) structure and nanowire channel is the most certain structure to control the channel. Nevertheless, it is unavailable to be applied to V_{th} self-adjusting MOSFETs because GAA structure has zero body factor. Thus, tri-gate structure with nanowire channel is introduced to V_{th} self-adjusting MOSFETs in this study due to its strong channel controllability as well as somewhat body factor. Figure 4.13 shows schematic structure of tri-gate nanowire MOSFET with V_{th} self-adjustment for three-dimensional simulation. The height and width of nanowire is 20 nm and it is entirely covered all around by floating gate. However, the control gate has tri-gate structure so that it is exploited for V_{th} self-adjustment. Figure 4.14 shows simulated transfer curves of tri-gate nanowire MOSFET with V_{th} self-adjustment. The V_{th} self-adjusting characteristics is successfully demonstrated in tri-gate nanowire structure. Figure 4.15 shows comparison between planar and tri-gate structure of V_{th} self-adjusting MOSFET in terms of short channel effects. The tri-gate structure shows superior immunity of short channel effects to planar structure thanks to excellent channel controllability. To conclude, tri-gate nanowire MOSFETs with floating gate are appropriate to ultra-low voltage operation as sub-0.3 V taking advantage of remarkable controllability to channel.

4.5 Summary

In this chapter, the operation mechanism of V_{th} self-adjustment is verified. The V_{th} self-adjusting characteristics are derived from gate capacitance difference by time-lag between dynamic and static characteristics. To obtain large ΔV_{th} and small s-factor, tunnel and gate oxide layer should be thick

and thin, respectively as possible as keeping proper tunneling. The V_{th} self-adjusting MOSFET with planar structure shows possible to operate in ultra-low voltage, but it exposes weakness to short channel effects. Therefore, the tri-gate nanowire structure is introduced to V_{th} self-adjusting MOSFET to take advantage of its excellent channel controllability. As a result, the tri-gate nanowire MOSFET with floating gate shows great suppression of short channel effects as well as V_{th} self-adjusting characteristics. Therefore, the tri-gate nanowire MOSFET with V_{th} self-adjustment outstanding possibility to operate in sub-0.3 V with aggressively shrunk channel size, further application to SRAM cells.

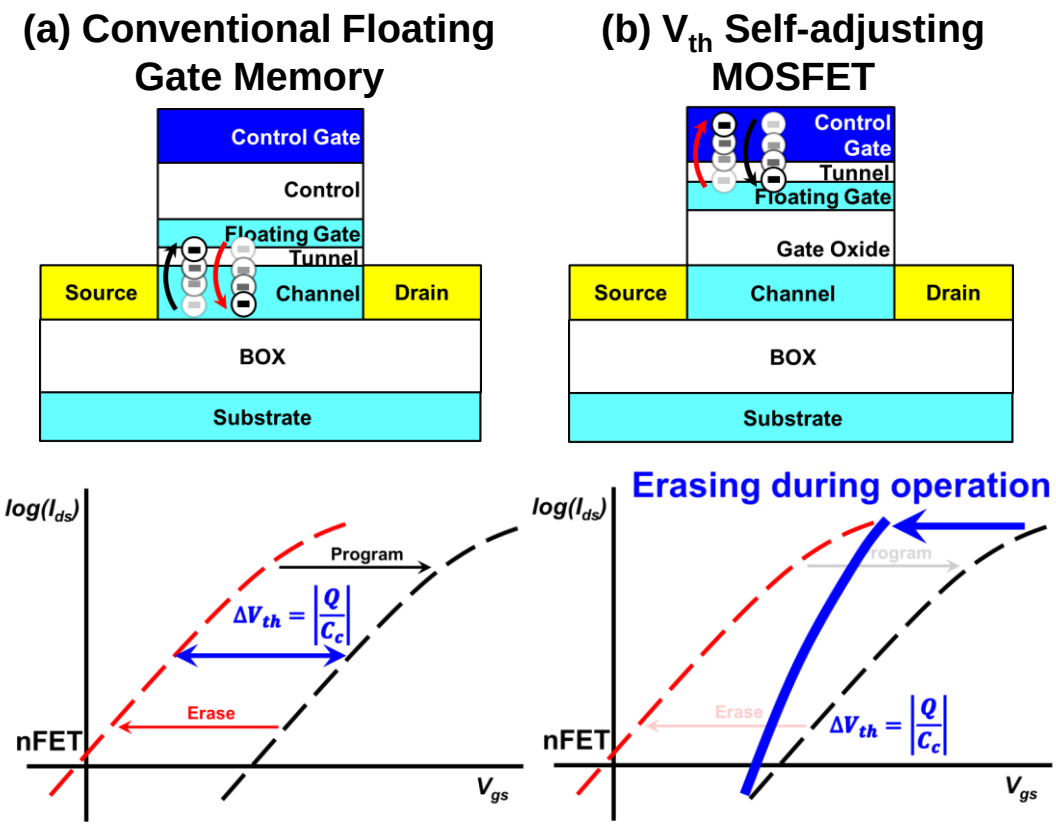


Figure 4.1 Schematic structure and transfer curves of (a) conventional floating gate memory and (b) V_{th} self-adjusting MOSFET. Note that thickness and location of tunnel oxide difference.

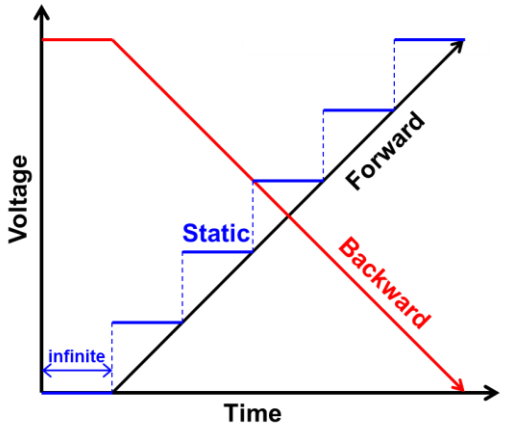
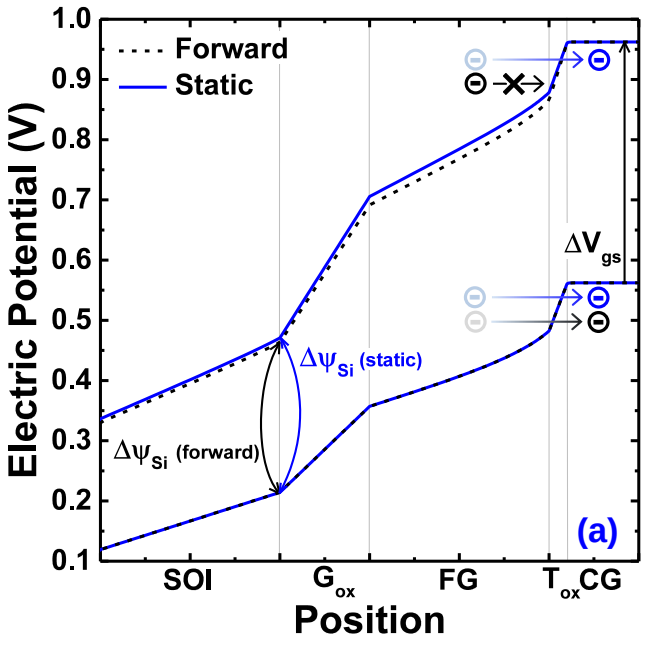


Figure 4.2 Sweep time and voltage sequence of dynamic (forward, backward) and static characteristics. There is time-lag between dynamic and static characteristics except initial point.



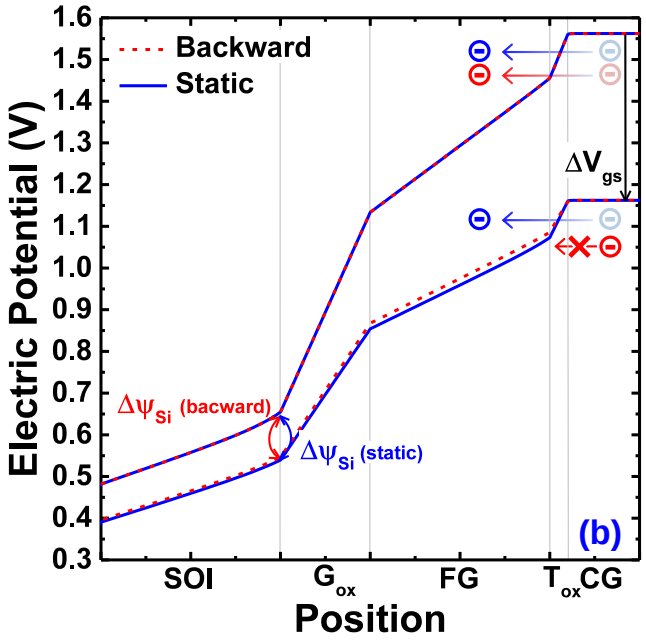


Figure 4.3 Electric potential between dynamic ((a) forward, (b) backward) and static characteristics in case of nMOSFET. The tunneling of electrons is under the control by time-lag.

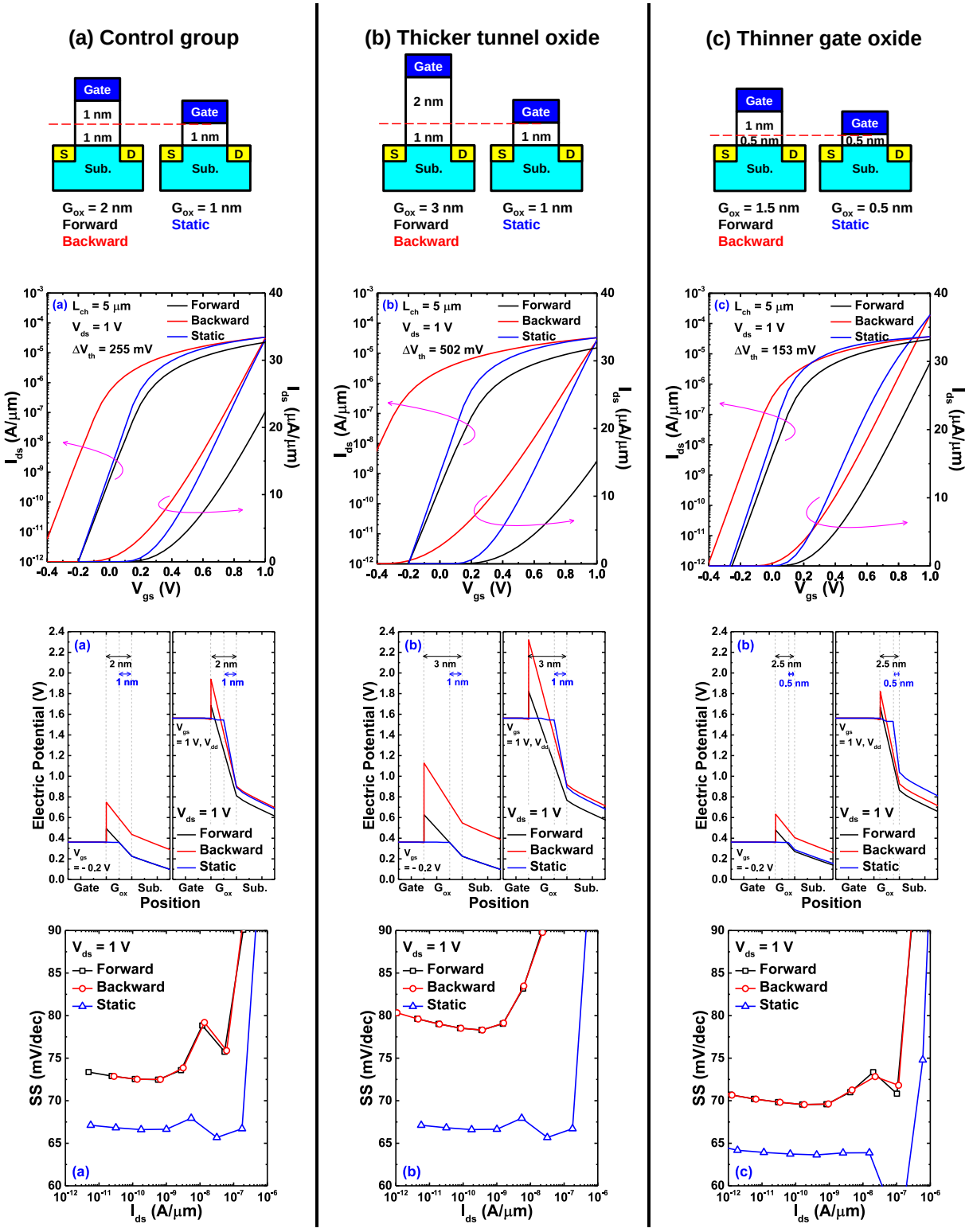


Figure 4.4 Simplified modeling structure and its transfer curves, electric potential and s-factor of V_{th} self-adjusting MOSFET at V_{dd} = 1 V with (a) control group, (b) thicker tunnel oxide and (c) thinner gate oxide.

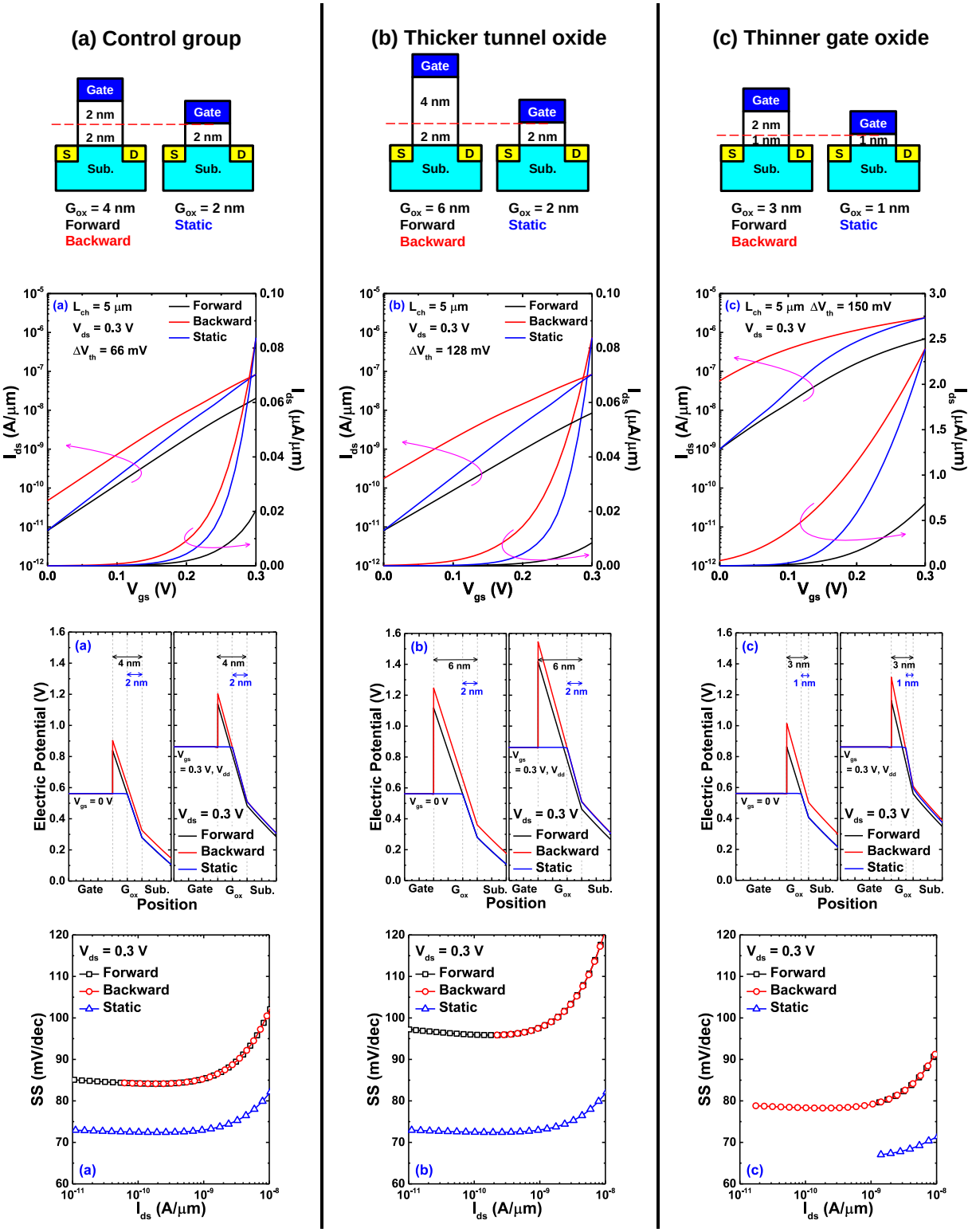


Figure 4.5 Simplified modeling structure and its transfer curves, electric potential and s-factor of V_{th} self-adjusting MOSFET at V_{dd} = 0.3 V with (a) control group, (b) thicker tunnel oxide and (c) thinner gate oxide.

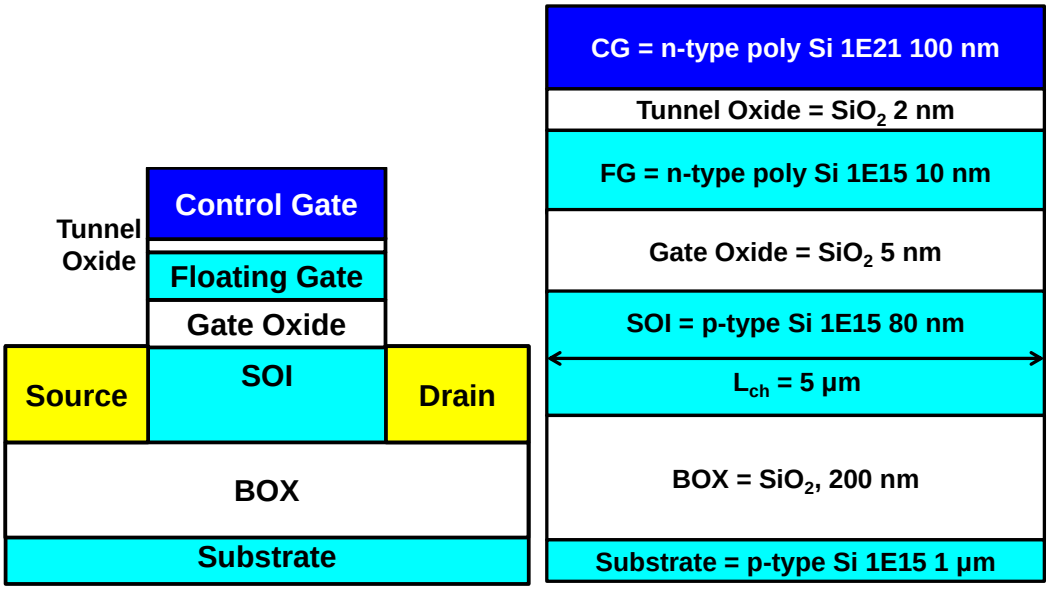


Figure 4.6 Schematic structure of simulated two-dimensional V_{th} self-adjusting MOSFET with FD-SOI.

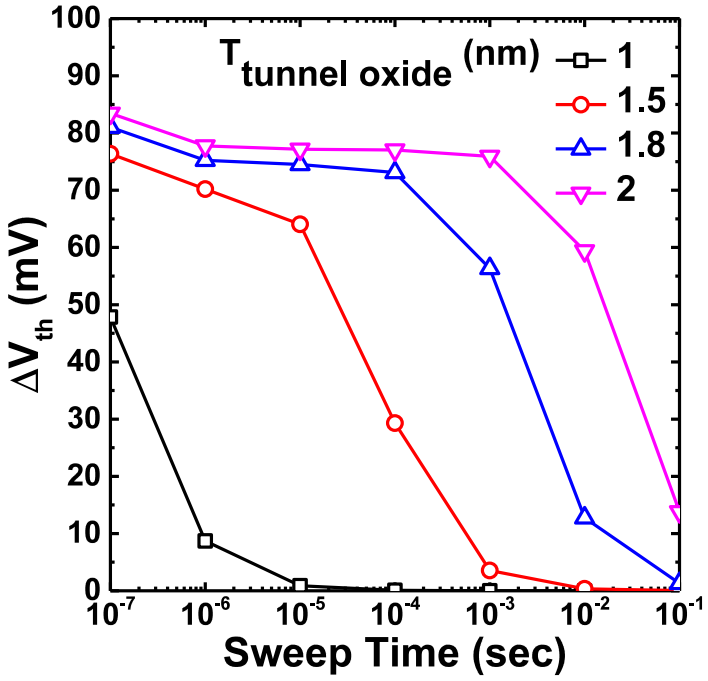


Figure 4.7 ΔV_{th} as a function of sweep time and tunnel oxide thickness. As the sweep time and tunnel oxide thickness is getting faster and thicker, ΔV_{th} become larger.

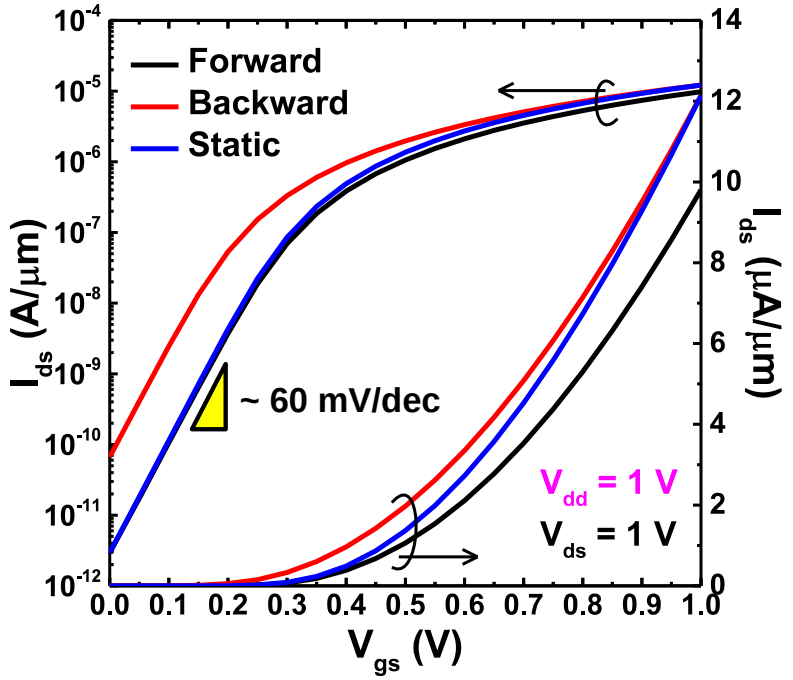


Figure 4.8 Simulated transfer curves of V_{th} self-adjusting MOSFET at V_{dd} = 1 V.

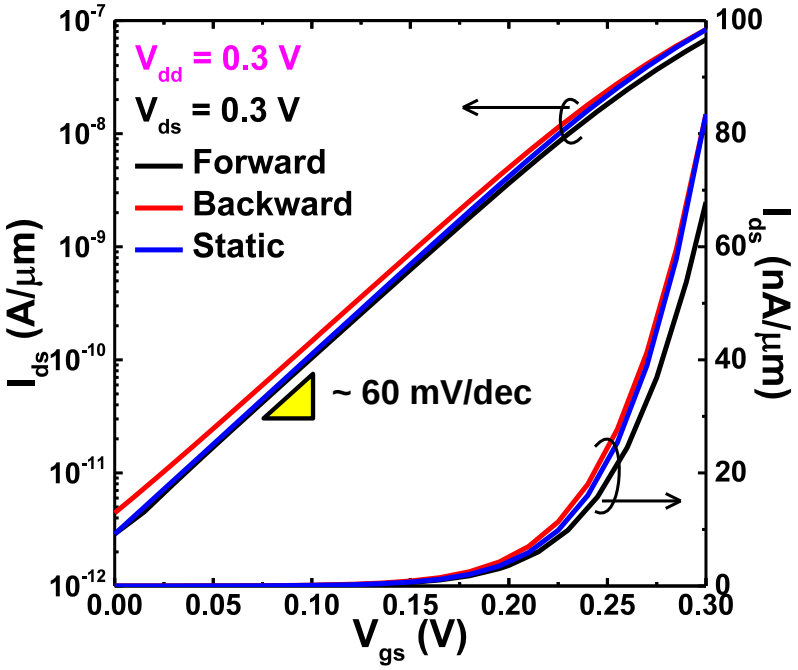


Figure 4.9 Simulated transfer curves of V_{th} self-adjusting MOSFET at V_{dd} = 0.3 V.

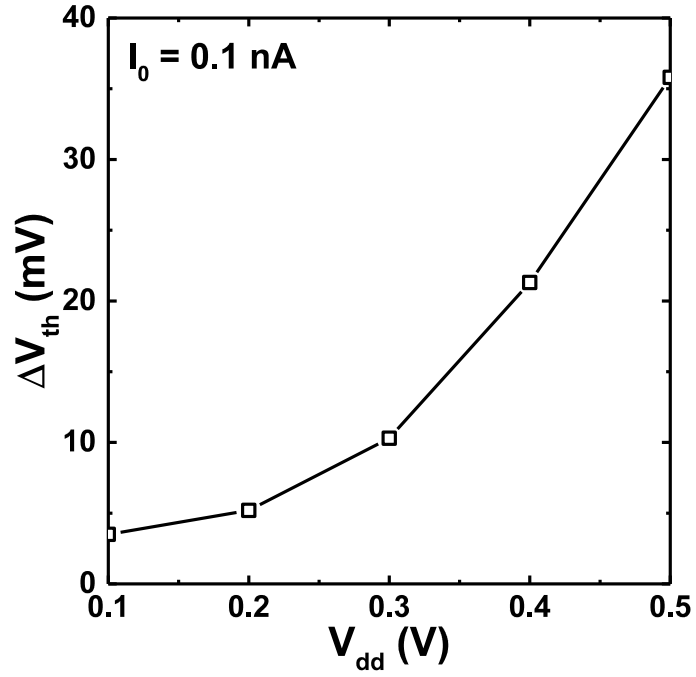


Figure 4.10 Extracted ΔV_{th} with V_{dd} scaling. V_{th} self-adjusting characteristic is clearly shown even if ΔV_{th} become smaller.

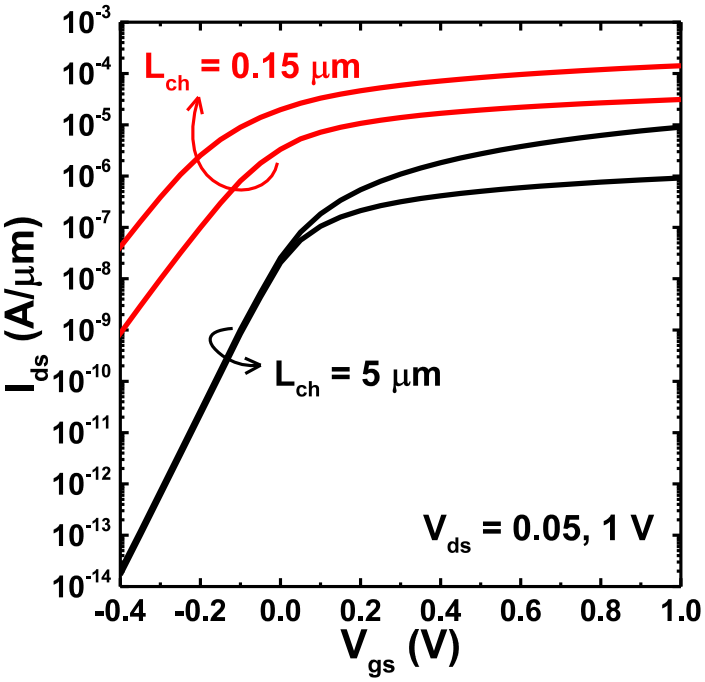


Figure 4.11 Simulated transfer curves of V_{th} self-adjusting MOSFETs with L_{ch} = 5 and 0.15 μm. The severe short channel effects are appeared in shorter L_{ch}.

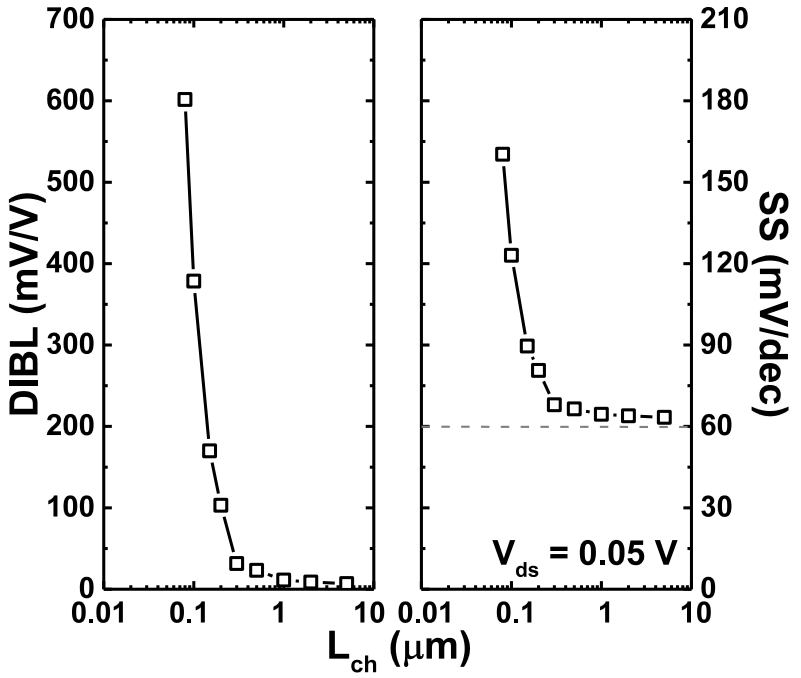
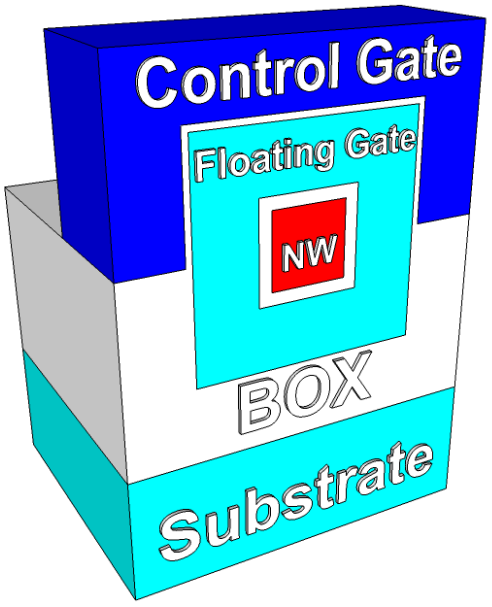


Figure 4.12 DIBL and s-factor with L_{ch} of V_{th} self-adjusting MOSFETs.



- Control gate = n-type poly Si (10^{21} cm^{-3}) 100 nm
- Tunnel oxide = SiO_2 2 nm
- FG = n-type poly Si (10^{15} cm^{-3}) 50 nm
- NW = p-type Si (10^{15} cm^{-3}) 20/20 nm
- Gate oxide = SiO_2 10 nm
- BOX = SiO_2 200 nm
- Substrate = p-type Si (10^{15} cm^{-3}) 300 nm

Figure 4.13 Three-dimensional schematic structure of proposed tri-gate nanowire MOSFET with floating gate to suppress short channel in V_{th} self-adjusting MOSFETs.

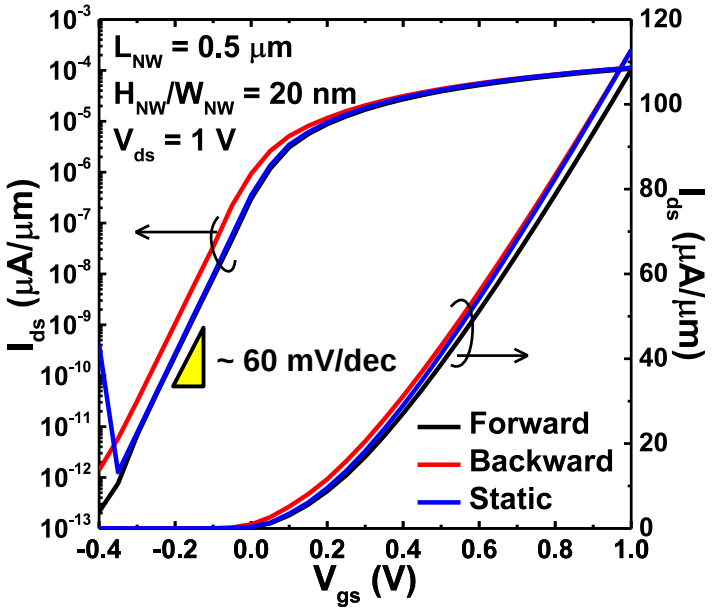


Figure 4.14 Simulated transfer curves of tri-gate nanowire MOSFET with V_{th} self-adjustment.

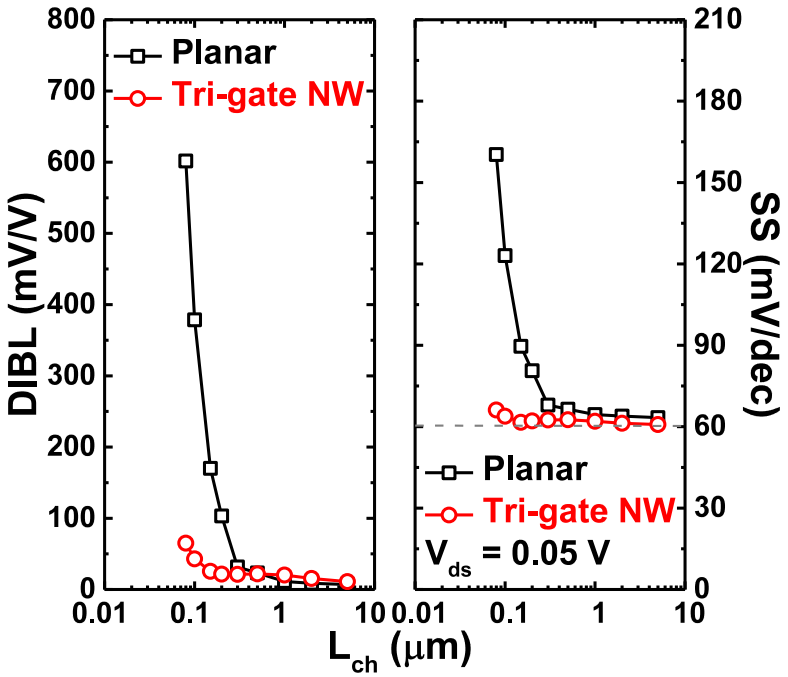


Figure 4.15 DIBL and s-factor with L_{ch} of planar and tri-gate nanowire structure. Tri-gate nanowire structure shows excellent immunity to short channel effects.

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Chapter 6
Conclusions

In this thesis, the device design guideline for ultra-low power MOSFETs in sub-0.3 V operation was proposed in terms of low power CMOS logic and SRAM cells. In order to achieve high energy efficiency CMOS logic in subthreshold region, DIBL is should be suppressed even in steep s-factor transistors. Moreover, tri-gate nanowire MOSFET with floating gate showed great potential for low power SRAM cells, which is demonstrated by simulation and fabrication. The primary results in this study are summarized as following.

In Chapter 2, the effects of DIBL on devices and circuits operating in the subthreshold region are investigated by measurement and simulation. The measurement results deliver that large DIBL device shows severe performance degradation particularly in subthreshold region compared with small DIBL device. It is caused by the subthreshold characteristics become very sensitive to change of V_{th} by DIBL. Furthermore, CMOS ring oscillators consisting of large DIBL devices show much more current and delay degradation because I_{eff} or peak trajectory current are degraded by DIBL despite of same I_{on}. This phenomenon is also getting worse with V_{dd} scaling. As a result, the energy consumption becomes increasingly larger with DIBL increase in subthreshold region in spite of reduction in power consumption by V_{dd} scaling.

In Chapter 3, the correlation between η factor and energy efficiency in steep s-factor transistor is examined by simple analytic calculation. The steep s-factor transistor shows high energy efficiency with zero η factor because of its excellent subthreshold characteristics. Nevertheless, the energy consumption is getting worse when η factor give influence to steep s-factor transistors.

From Chapter 2 and 3, DIBL (or η factor) should be repressed to realize energy efficient CMOS

logic circuits for sub-0.3 V operation.

In Chapter 4, V_{th} self-adjusting MOSFETs for low power SRAM cells are proposed. From verifying operation mechanisms, in order to obtain large ΔV_{th} and small s-factor, tunnel oxide and gate oxide layer should be thick and thin, respectively as possible as keeping proper tunneling phenomenon. The V_{th} self-adjusting MOSFET with planar structure is successfully demonstrated using two-dimensional simulation even in the ultra-low voltage operation (V_{dd} = 0.1 V). However, planar structure shows crucial weakness in short channel effects due to limitation of vertical scaling down. Thus, the tri-gate nanowire structure is introduced to V_{th} self-adjusting MOSFETs. This approach shows not only operation in ultra-low voltage operation with V_{th} self-adjustment but also strong immunity to short channel effects.

The main goal of this study is proposal of device design for ultra-low voltage operation. The most significant finding to emerge from this study is suppressing DIBL for CMOS logic circuits and V_{th} self-adjustment for SRAM cells. Continued efforts are needed to achieve sub-0.3 V operation CMOS devices, but this research extends our knowledge about how to device design for sub-0.3 V operation.