博士論文

High-frequency organic thin-film transistors for conformable large-area electronics

(コンフォーマブル大面積エレクトロニクスのための高周波有機薄膜トランジスタ)

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Abstract

Background

Organic thin-film transistors (OTFTs) are one of the most important building elements to realize large-area flexible electronics. Recent material advancements allow organic transistors to be environmentally and thermally stable and provide good electrical performance. This progress enabled the fabrication of electronic circuits for practical applications, such as displays and processing units. High frequency operation of single devices and oscillators could also be demonstrated on thick plastic foils. In addition to their improved electrical properties, the mechanical flexibility and conformability of such devices can be improved by reducing the thickness of the base films. Organic elements manufactured on ultrathin substrates can provide smaller bending radii and better conformability to complex objects including human skins.

Despite the impressive development of organic electronics, no demonstration for large area electronics that provides both excellent conformability, large bandwidth (cutoff frequency > 100 kHz) and good uniformity (~10% device variation) has been made yet. Organic transistors on thin films suffer from narrow bandwidth due to limited scaling methods and inherently low carrier mobility. So far, only low frequency OTFTs and circuits were demonstrated on ultrathin and conformable substrates. Thermally stable organic devices could be achieved only by the use of specific transistor structure on rather thick plastic foils. Uniformity of organic transistors over large area is another main issue towards reliable implementation of practical applications.

Objective

In this study we develop a novel method for fabrication of high frequency organic transistors and circuits on large area and ultrathin foils, which shows high degree of uniformity, mechanical and environmental stability. The technology is based on the fabrication of high performance, short channel OTFTs in the bottom contact architecture to enhance devices bandwidth in low operation voltages. We aim to demonstrate large area compatibility on ultrathin substrates to enable the realization of future conformable sensor sheets for wearable or implantable devices.

Method

Our method for devices improvement towards reliable and conformable OTFTs is based on three main principles, demonstrated simultaneously for the first time in this study:

- **Substrate thickness**
  Reduction of the base film down to ~1 µm thick substrates, allows devices to conform to any three-dimensional object. Small device thickness also facilitates the stress applied on the transistors and enhances their mechanical flexibility.
- **Bottom contact structure**
  The bottom contact structure allows reliable high resolution patterning using photolithography to increase transistor's cutoff frequency.
- **Vapor deposited polymeric gate dielectric**
  The choice of flexible vapor deposited polymeric gate dielectric allows uniform device performance and ultrathin, pinhole free interface with the organic semiconductor for reduction of operation voltage.

We utilized those principles in our device fabrication and discuss their effect on device performance.

First, we adapt photolithography to be used on ultrathin parylene diX-SR foils and fabricate OTFTs for the first time using this technology on 1 µm substrates. By utilizing the bottom contact architecture we pattern channel lengths down to 2 µm to realize air stable, dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT) based OTFTs. We improve device performance by applying contact modification techniques using pentafluorobenzenethiol (PFBT) self-assembled-monolayer (SAM) and optimize mobility with different deposition conditions. We compare this method to other available contact modification techniques and discuss the challenges when applying to ultrathin films.

Second, we perform thorough electrical device characterization and analyze important OTFT parameters. Thanks to the effective contact modification we could realize saturation mobility of ~0.2 $cm^2/V{\cdot}s$ for short channel transistors (~2 µm channel length) in bottom contact architecture with transfer length of only 1 µm. The obtained contact resistance in our devices was found to be 5.5 kΩ·cm which is comparable to top contact devices with the same materials. The fine patterning method allowed us to reduce the overlap capacitance of less than 0.5 pF per channel were achieved. High ratio between ON and OFF currents of 10^7 was demonstrated which is important for practical sensing applications. We could reduce operation voltage down to 8V by reduction of dielectric thickness to less than 100 nm and still keeping leakage current lower than 100 pA during transistor operation. Theoretical and measured transistor cutoff frequency exceeded 100

kHz on ultrathin foils. We discuss the successful results in light of the top gate architecture implementation and fabrication technique.

Further stress characterization were conducted on the ultrathin devices. Transistors were tested under severe mechanical bending and crumpling and showed good durability against the mechanical stress. While only 2 μm thick, devices could be rolled down to 600 μm bending radius and be crumpled several times with showing practically no degradation in performance (< 10% in mobility). We discuss the theoretical considerations in applying stress on the bottom contact structure in the ultrathin form.
Additionally, we evaluated devices environmental stability by performing thermal annealing tests. We showed that ultrathin OTFTs in the bottom contact structure could endure heating up to 170°C in N_2 and 150°C when annealed in air. We provide evidence to cyclic stability of those devices after repeated annealing steps. We calculated that thanks to the short channel implementation, cutoff frequency of devices could be kept above 100 kHz even after annealing at 170°C. We analyze the changes in channel and contact resistances and by electrical and topological means,

Finally, we demonstrate the reliability of our OTFTs by the realization of electrical circuits and large area active matrix. We designed and successfully fabricated pseudo-CMOS inverters with gain of as high as 30 dB. We also showed that inverter gain can be improved by at least 150% after simple post annealing step at 150°C. Organic amplifier with improved frequency response of up to 25 kHz (f_{3dB}) and 45 kHz unity gain could be achieved in the AC coupled architecture. For the closed loop design we added parylene capacitors in total active area of 45 mm^2, which achieved constant frequency response of from 3Hz to 3kHz. By integrating our devices with aluminum-oxide capacitors (~500 nF/cm^2) we reduce effective amplifier area to only 15 mm^2 which is suitable to implementation for high resolution sensing devices. Integrated amplifiers showed a closed loop gain of ~6 dB and stable operation between 5Hz-700Hz. The large area uniformity of our devices was successfully demonstrated by the fabrication of 6x6 cm^2 transistor array which showed excellent yield (98.6% out of 144 transistors) and only 0.019 $cm^2/V{\cdot}s$ standard deviation from the average value of 0.12 $cm^2/V{\cdot}s$. The transistors were used as a large area pressure sensor to demonstrate their applicability.

Summary

We have successfully demonstrated the highest frequency OTFTs reported on ultrathin films (~1 μm) in the bottom contact architecture. Channel patterns down to 2 μm length with cutoff frequencies greater than 1 MHz were realized. Using ultrathin parylene diX-SR gate dielectric, we could maintain low voltage operation for our devices. OTFTs showed excellent durability to mechanical and thermal stress thanks to our design and material selection. Transistors reliability was demonstrated by the fabrication of ultrathin inverters

and amplifier circuits, showing record high bandwidth (25 kHz) for a single organic amplifier. The smallest organic closed-loop amplifier (15 mm^2 of active area) was realized by integrating the transistors with AlOx capacitors, presenting uniform gain up to 700Hz. Excellent uniformity (~15% of mobility standard variation) and device yield (98.6%) was realized on 36 cm^2 active matrix with 144 transistors, utilized as an ultrathin pressure sensor.

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1 Introduction

Organic field effect transistors have made a tremendous progress since they were first reported in 1987 [1]. By important process and material improvements, organic transistors have made their way outside from research labs into the commercial, practical world of applications. Organic solar cells [2,3], organic light emitting diodes (OLEDs)[4,5] and organic logic units [6,7] were successfully demonstrated and are now available for the benefit of users around the world. According to recent forecast, the market of organic electronics has a compound annual growth of (CAGR) of 29.5% until 2020 with an expected value of 79.6 billion USD [8]. Within this market, OLED is estimated to have the largest share (about 2/3 of the market) where system components (such as logic and memory) will compose the second largest portion, reaching 20% of the total revenue.

Organic electronics are attractive due to several important factors. First, organic devices are very flexible. The flexibility of devices is originated from the molecular structure of the active semiconducting material. The organic semiconductor is constructed from conjugated molecular chains that are connected to each other by weak van der Waals bonds. Conduction mechanisms occur by an interplay between charge carrier hopping and band transport [9]. The relatively weak bonding between molecules allow the material to be more flexible and less brittle when mechanical stress is applied. Second important advantage of organic devices is their processability. Organic materials can be deposited by low cost per area procedures and at relatively low temperatures [10]. These properties allow fabrication of organic devices over large areas and on wide variety of surfaces. Substrates such as papers, bank note and large area plastic foils [11–15] could be successfully used as the base film for organic device fabrication.

Recently, based on the unique properties of those device, a new branch of organic electronics was proposed – the imperceptible electronics [16]. Imperceptible electronics describe functional electronic devices that are deposited on ultrathin substrates (roughly 1/30 thinner than a human hair) and can be used for many purpose in an unnoticeable manner. The substrates in use are usually plastic foils (such as polyethylene naphthalate, polyethylene terephthalate and poly(p-xylylene)) in thicknesses that do not exceed a few micrometers. In a very short period of time, great development was made in this field and devices such as active matrices [16,17], organic photovoltaic cells [18], organic electrochemical sensors [19] and circuits [20] could be realized on those ultrathin films. Inorganic and oxide electronics devices can also be transferred onto such films [21,22] however the organic counterparts carry the advantage of direct fabrication at low temperatures and in lower cost per area.

Naturally, the application of organic imperceptible electronics to large-area sensor sheets have attracted much attention, presenting promising features as the next-generation wearable and implantable devices. The basic principle behind those devices is

to allow signal detection - such as thermal, electrical or mechanical - by certain proximity to the monitored object [23]. The detected signal is often translated into electrical signal and transmitted for further processing. In order to provide reliable signal detection the

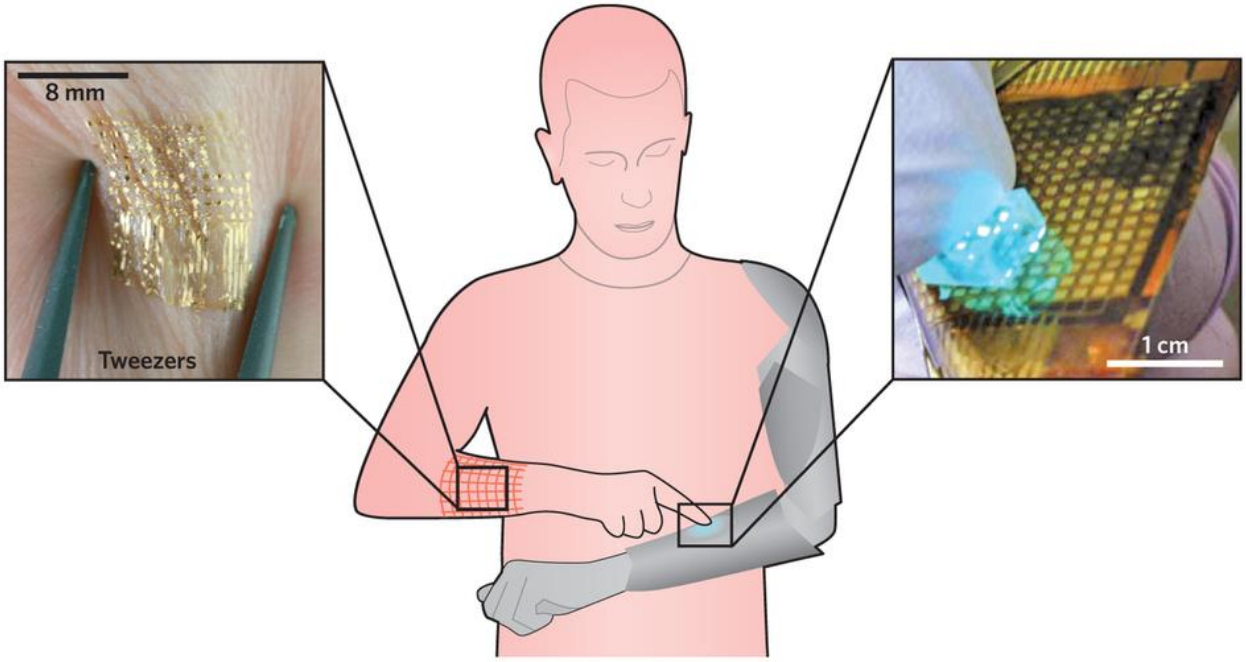


Figure 1: A conceptual image of intimate electronic devices, presenting ultrathin conformable sensor and an interactive light-emitting touch panel on human skin [23].

sensor arrays should satisfy several conditions. First, the arrays should be large enough and conformable to the monitored object to provide intimate proximity. Good signal-to-noise ratio is of utmost importance for this purpose and can be improved by 'on-site' active amplification. Additionally, devices should be mechanically and environmentally stable to prevent degradation over time and operate in low voltages for efficient energy consumption. Lastly, sensors' amount and their resolution should also be considered, depending on the application. Fast multiplexing large number of signals form sensors is important to provide real-time monitoring of objects.

One the challenges in making large area sensors from organic materials is their limited bandwidth. Transistors' frequency response is closely related to the frequency of signals from sensors (e.g. neural signal at ~1 kHz) and to multiplexing large number of signals from a composed device. Although organic devices have improved their field effect mobility by few orders of magnitudes in the last 28 years and surpass values of amorphous silicon [9], they still present relatively low speed of charge carrier transport, caused by their polycrystalline structure. One of the methods to overcome this problem and improve transistors bandwidth is to reduce their dimensions, i.e. channel length and parasitic overlap ($f_T \propto {}^{1}/_{L^2}$). Many groups have tried to improve those properties by various methods [24–28], however there is still a trade-off between the scaling methods,

fabrication complexity and device performance, which is caused by the sensitive organic semiconductor and the application of aggressive scaling methods on plastic foils. So far, there was no demonstration of high frequency (>100 kHz) organic transistors on ultrathin films.

In this research we will challenge the scaling methods of organic transistors on

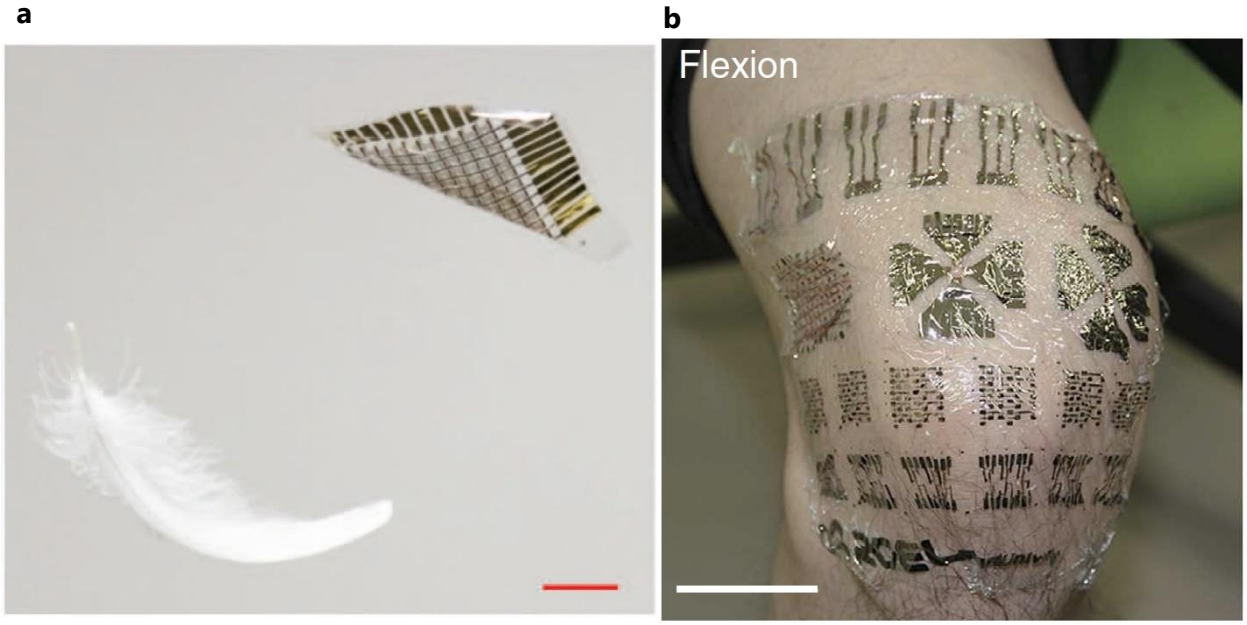


Figure 2: (a) Demonstration of the lightweight of an ultrathin active matrix. Scale bar is 1 cm [16]. (b) Illustration of the potential of large area, imperceptible sensor arrays for health monitoring. Scale bar is 4 cm [17].

ultrathin films in order to improve their frequency response. The materials and methods in this study will be chosen to allow the fabrication of reliable imperceptible electronic devices to be used as large area sensor sheets. Operation voltage, device stability and uniformity will be considered as well for the practical implementation of our method.

The thesis is constructed as follows: in Chapter 2 and Chapter 3 , we start with describing the background of the organic transistor structure and analysis, following by the materials and methods required for fabrication. We elaborate on our selection for device exploration. In Chapter 4 we give details on single transistor fabrication in the bottom contact architecture. The transistor structure is optimized on ultrathin films, emphasizing the contact resistance issue in our device structure. Several methods are considered and experimented. The optimized design is thoroughly analyzed for its electrical properties. Device mobility, contact resistance, ON/OFF ratio, device uniformity and other important transistors properties are studied. The fabrication results are discussed in light of the specific methods and the application on ultrathin films. Chapter 5 describes the transistors behavior upon mechanical bending stress. We bend the ultrathin devices down to small bending radii (600 μm) and crumple the transistors several times

to verify their durability. We test OTFTs with several channel lengths and compare their performance. Different bending orientations are also evaluated. The successful results are theoretically analyzed by calculating the stress on the device in its ultrathin form. In Chapter 6 we report on the high thermal stability of our devices, when annealed up to 170°C. Comparative study of devices annealed in air and N_2 environment is conducted as well as detailed inspection of behavior of different channel lengths. We show that the theoretical cutoff frequency of devices can be maintained above 100 kHz even when annealed at high temperatures. In addition, transistors can show good cyclic stability after several thermal cycles. Surface topology and transistor resistance values during heating are investigated to clarify the change in devices. Chapter 7 illustrates the reliability and uniformity of our technology by the demonstration of several organic electronics circuits. Pseudo-CMOS inverters are designed and fabricated with high gain on ultrathin films. We also optimize the design and manufacturing of an AC coupled organic amplifier. Amplifier gain can range between 5-15 dB and f_{3dB} can reach 25 kHz. The total device area can be minimized to only 30 mm^2 by the integration of AlOx capacitors. In Chapter 8 we demonstrate a large area application of our fabrication method by fabricating 36 cm^2 active matrix. The active matrix exhibits high device yield with uniform mobility and threshold voltage, which verifies the successful achievement of a reliable technique for large area, bottom contact transistors on ultrathin foils.

2 Organic Thin Film Transistors (OTFTs)

Organic thin film transistors (OTFTs) are one of the most important building blocks of organic electronics. With a relatively simple operation model and structure they provide useful mechanism for implementing wide range of applications with organic materials, such as flexible displays, pressure sensors, amplifiers and more [29–31]. In this chapter we will review some of the essential design principles, operation modes and characterization methods of this influential unit.

2.1 Architecture

The organic thin film transistor has four main design architectures, namely the bottom gate – top contact, bottom gate – bottom contact, top gate – top contact and top gate – bottom contact (*Figure 3*). The names bottom and top contacts are derived from the position of the contacts in relation to the semiconductor. The architectures can also be distinguished by their channel location in relation to the source and drain: coplanar (such as the bottom gate - bottom contact and top gate - top contact) and staggered (such as the bottom gate – top contact and top gate – bottom contact). All design layout are based on a three terminal transistor structure with gate, source and drain electrodes. In addition organic semiconductor and gate dielectric are deposited as thin films.

Although the OTFT carries some similarities to the conventional metal-oxide-semiconductor field-effect-transistor (MOSFET), the OTFT operates in a different manner. The organic thin film transistor works only in the accumulation mode, where the current is produced by the majority carriers. By applying electrical field from the gate electrode, the organic semiconductor (which will be discussed in detail in section 3.2) changes its holes or electrons concentration in the channel. For example, a negative bias on p-type organic semiconductor (holes are majority carriers), holes are accumulated in the channel area. The change in carrier concentration modifies the channel conductivity between the source and drain electrodes. If conductivity becomes high enough (transistor is 'ON'), additional voltage on the two other terminals (the source and the drain) can modulate the current flowing through the device.

The transistor architecture has an immense effect on the manufacturing process and device operation of the OTFT. The thin film transistor is built by stacking metals, organic and inorganic layers on top of each other and each layer patterning method and characteristics are influenced by its predecessor. Properties such semiconductor quality, patterning resolution, energy level barriers and others are affected by the order of layer deposition and the interaction between them. In the following paragraphs we will discuss several considerations and issues related to the OTFT architecture.

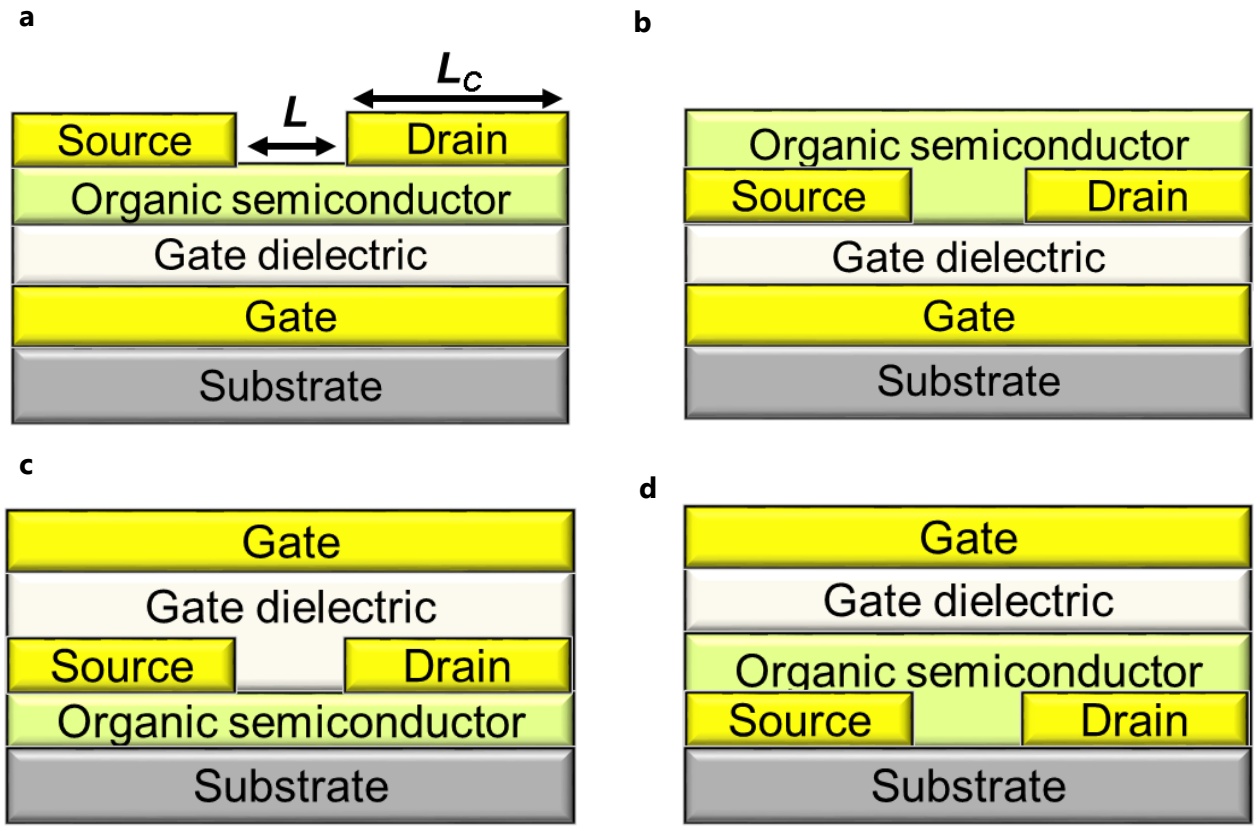


Figure 3: (a) bottom gate – top contact, (b) bottom gate – bottom contact, (c) top gate – top contact and (d) top gate – bottom contact. OTFT design. Channel length (L) and contact length (L_C) are denoted. Modified from [10].

One of the most important layers interplay is the contacts-semiconductor interface. For example, in bottom contact structures where the semiconductor is deposited after the source and drain pattern, larger process window for metal patterning. Processes such as photolithography or e-beam lithography can be implemented and smaller channel dimensions can be achieved [32,33]. Such methods are more difficult to implement on top contact devices due to the organic semiconductor's sensitivity to solvents and high energy procedures [34]. Additional consideration for semiconductor deposition is the surface energy of the underneath layer. Deposition on high surface energies is often disadvantageous for small molecules semiconductor growth and results in worse device performance [35]. In this case, metal electrodes with high surface energy can degrade charge carrier transportation on contact area in the bottom contact structure. Another interesting aspect related to the OTFT layout is that staggered structures are less sensitive to energy barriers between metal and semiconductor than the coplanar structure [36–38]. In addition surface modification of top gate – bottom contact (*Figure 3*d) shows better modification by self-assembled-monolayer than the bottom gate – bottom contact (*Figure 3*b) due to better surface orientation [39]. This gives an important advantage to utilize this

structure for high performance thin film devices. Mechanical durability of devices can also be affected by device structure on flexible films where the metal contacts can be delaminated from the semiconductor during bending [40].

Similarly, the gate dielectric deposition should also be compatible with the semiconductor and previous TFT layers. The thickness of the dielectric plays an important role in determining the operation voltage and leakage current of the device. The gate dielectric – semiconductor interface is very important for parameters such as threshold voltage, device hysteresis and charge carrier mobility. In top gate structures, the use of specific solvents for solution processed gate dielectrics can also degrade the semiconductor. In case of bottom gate structures, surface roughness and energy of the dielectric (and previous layers) should be considered for semiconductor nucleation and quality [38]. Deposition of gate dielectrics by high energy processes (such as chemical vapor deposition of silicon oxide) should be avoided on top of flexible substrate or organic semiconductors [10]. By adopting the bottom gate structure, thin oxides can be deposited on top of metals to provide very thin dielectrics with good insulating properties [41]. During device operation, effect of gate dielectric layer was found to be very important for device durability against mechanical strain in the top contact structure [42].

In summary, the OTFT design is significant for device operation and the selection of materials and methods for fabrication. Interfaces between the layers and growth mechanisms affect charge transport and transistor's performance. Device layout influences the effective charge injection area and surface modification quality to enhance device performance. Device design is also an important consideration for durability against external mechanical stresses. Finally, patterning methods should be selected carefully in the specific design to prevent damage to the already patterned layers.

2.2 Operation modes

Similarly to MOSFET, the organic thin film transistors has three main operation regimes: cutoff, linear and saturation. For sake of simplicity we will analyze those regions in the case where the semiconductor is p-type, meaning that holes are the majority carriers. As mentioned earlier, the OTFT is based on the accumulation of charge carriers in the channel as a result of gate bias.

2.2.1 OFF state

The first transistor state we analyze is the transistor's OFF state. This state is based on the low conductivity of the semiconductor under positive (or no) gate bias. When no (or small positive) voltage is applied, the organic material shows high resistivity. In this case, if small drain voltage (V_{DS}) exists, the conductivity of the film (σ) and channel dimensions

determine the current between the source and the drain (I_{DS}), according to the simple film resistivity model [43]:

(1) $$I_{DS} \cong \sigma V_{DS} \frac{L}{W \cdot t}$$

where L, W is the channel length and width respectively and t is the semiconductor thickness. We define this condition as the transistor OFF state where the channel shows very high resistivity and low currents.

2.2.2 Linear regime

The conductivity of the channel can be enhanced by applying negative gate voltage on the metal-insulator-semiconductor (MIS) structure. When applying a negative bias to the gate, accumulation of majority carriers (holes in the p-type semiconductor) occur in proximity to the semiconductor-insulator region in order to compensate the total charge in the metal-insulator interface. The conductivity of the channel becomes significant when the gate voltage is larger (more negative) than a threshold voltage (V_{TH}) which represents the energy level difference between the metal and semiconductor and the charge carrier density in the semiconductor [44]:

(2) $$V_{TH} = 2\varphi_B + \frac{Q_{sc}}{C_i}$$

Here φ_B is the gap between the gate work function and the semiconductor Fermi's level (the value $2\varphi_B$ is also defined as the flat-band voltage V_{FB}), Q_{SC} is the charge carrier density in the semiconductor and C_i the gate-dielectric capacitance per area. The accumulation creates an area in the semiconductor with charge density approximated as $C_i(V_{GS}-V_{TH})$. When V_{DS} is small enough ($|V_{DS}| << |V_{GS}-V_{TH}|$), the drain-source current can be represented as [45]:

(3) $$I_{DS} = \frac{W}{L}\mu C_i (V_{GS} - V_{TH}) V_{DS}$$

Here we introduce an important transistor parameter, the mobility (μ), which represents the relation between the drift velocity and the electric field in the semiconductor. This figure of merit is essential for the evaluation of charge carrier transportation in the channel:

(4) $$\mu = \frac{v_{drift}}{E}$$

The drain current is directly proportional to the drain voltage and this regime is defined as the linear state of transistor operation.

2.2.3 Saturation regime

This state may be changed by further increasing the drain-source voltage. The drain-source voltage creates a potential gradient in the channel. The channel potential in channel location x is defined as V(x) and equals to the drain voltage near the drain and similarly, to the source voltage in the vicinity of source port. The charge density in the channel would be proportional to the value $|V_{GS}-V(x)|$. Thus, an increase of the drain voltage to the value $V_{DS}=V_{GS}-V_{TH}$ yields the threshold potential (VTH) near the drain and to the creation of low charge density in this region. This state is called channel 'pinch-off', due to the low conductivity channel area near the drain. In this case, further increase of drain voltage would not (ideally) increase the drain-source current and the current through the ports is denoted by [45]:

(5) $$I_{DS} = \frac{W}{2L}\mu C_i (V_{GS} - V_{TH})^2$$

In this state, the drain-current is saturated in regard to the drain-source voltage and this regime is defined as the saturation regime of transistor. The saturation current will be referred in this thesis as the ON current of transistor.
Ideally, the mobility in the linear and saturation regimes should be equal but in practice, especially in the case of organic semiconductor, this value may be different between the two operation regions. Phenomena such as gate-dependent mobility, short channel effects and contact resistance differ the values between the linear and saturation states [46–48].

2.2.4 Subthreshold regime

In the linear and saturation operation, we analyzed the transistor when $V_{SG}>V_{TH}$ and the drain voltage is increased. Here we analyze the operation in a different manner. In case we fix the drain voltage to its saturation value ($V_{DS}=V_{GS}-V_{TH}$) and sweep the gate voltage from $V_{SG}<V_{TH}$ to $V_{SG}>V_{TH}$ we encounter a different conduction mechanism in the channel. In this scenario, the current depends exponentially in the gate-source voltage [49]:

(6) $$I_{DS} \propto e^{V_{GS}/kT}$$

Where k is the Boltzmann constant and T the temperature. When plotted on a logarithmic scale, with increasing the gate voltage to the threshold value, we can define the area where the drain current increases from its OFF value as the subthreshold swing [49]:

(7) $$S_S = \ln(10)\frac{kT}{q}(1 + {}^{C_d}/_{C_i})$$

Where C_d is the depletion capacitance of the semiconductor and is closely related with the trap concentration in the semiconductor [10]. The subthreshold swing is given in units of V/decade (decade – a 10 times increase in drain current) and the minimum value in room temperature is 60 mV/decade, when $C_i \to \infty$. Low value of S_S indicates high switching speed of the transistor in a narrow voltage range. The subthreshold slope, which is the reciprocal of the subthreshold swing is sometimes referred.

2.3 Characterization

For characterizing OTFT, many single device characteristics can be extracted from two simple voltage sweeps: the output curve and the transfer curve. For both cases, all three of transistor's voltage port should be well defined. Follows is the description of those important characterization methods and a summary of the parameters extracted from them.

2.3.1 Transfer characteristics

The transfer curve describes the relation between the gate-source voltage (V_{GS}) and drain-source current (I_{DS}). The transfer curve is measured by holding the drain voltage constant, and sweeping the gate voltage from the non-conductive region to the conductive region and in reverse. The source port is always connected to the common ground of the circuit. The values of V_{DS} and V_{GS} sweep are determined so that $V_{DS}=V_{GS,\,MAX}-V_{TH}$ to achieve the maximum saturation current. $V_{GS,\,MAX}$ is defined as the maximum negative (positive) voltage in case of p-type (n-type) semiconductor. The initial V_{GS} ($V_{GS,\,0}$) is slightly more positive (negative) than the threshold voltage in case of p-type (n-type) transistors. During the sweep of the V_{GS}, the drain current (I_{DS}) and the leakage current (I_{GS}) are recorded using a parameter analyzer. From the transfer curve we can extract several parameters related to transistor operation.

Two of the parameters which can be directly extracted from the transfer curve are the ON/OFF ratio and the maximum leakage current. We can directly recognize the current when transistor is OFF (at $V_{GS,\,0}$) and the maximum currents, I_{DS} and I_{GS}, when the transistor is ON (at $V_{GS,\,MAX}$). The OFF current (ideally minimum value of $|I_{DS}|$) and maximum leakage (maximum value of $|I_{GS}|$) can imply on the energy consumption of the transistor when it is OFF and are important for circuit design. The leakage current is also important for the evaluation of the gate dielectric insulating properties. The maximum ON current points on transistor's current drive capabilities. An important interpretation of those value is the

transistor's ON/OFF ratio which is essential for switching applications of organic transistors [50].

By derivation of the transfer curve - $g_m = {\partial I_{DS}}/{\partial V_{GS}}$ - an important transistor parameter is calculated. g_m is the transistor's transconductance (or the transfer conductance) which describes the response of the output current (I_{DS}) to the input voltage (V_{GS}). From equations (3) and (5) we can quantitavely derive the values of g_m in the linear and saturation regimes

(8) Linear regime: $g_m = \frac{W}{L}\mu C_i V_{DS}$; Saturation regime: $g_m = \frac{W}{L}\mu C_i (V_{GS} - V_{TH})$

The transconductance is closely related to the transistor ability to drive current but also to other key parameters of transistor performance (such as the cutoff frequency) and for circuit design.

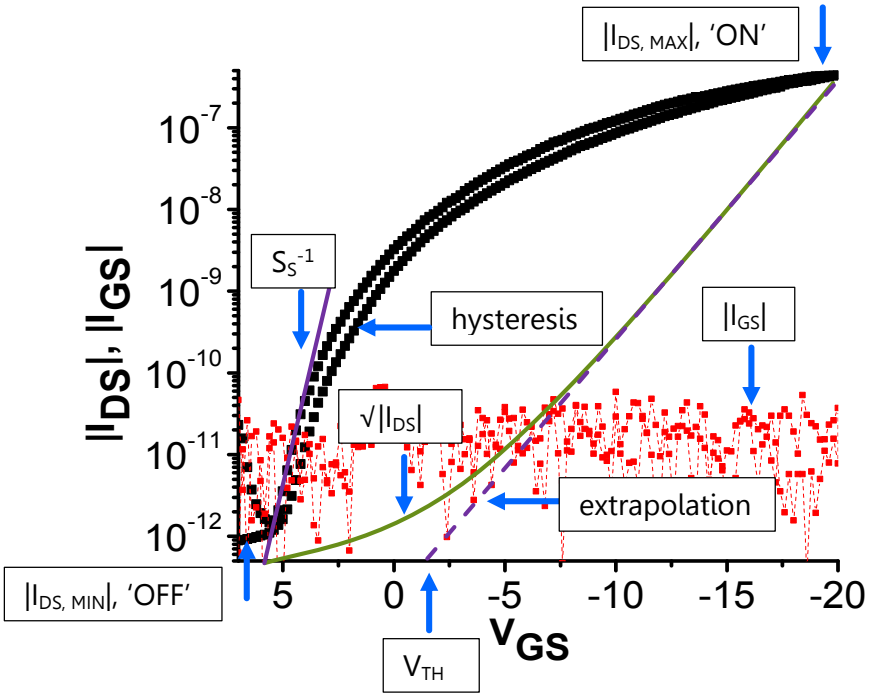


Figure 4: Illustration of transfer curve and some of the important parameters which are extracted from it. The black scattered line represents the $|I_{DS}|$ record where the red line exhibits the $|I_{GS}|$ values during scan.

A key parameter extracted from the transfer curve is the transistor's field effect mobility. The mobility is one of the most material-related parameters and gives important information about the transport mechanism of charge carrier in the semiconductor. This value is sensitive to the presence of traps, impurities or molecular disorders [35,51] and implies on the quality of the semiconductor and transistor's conductivity. The mobility

can be easily calculated from equations (3) and (5) for the different operation regimes of the transistor:

(9) Linear regime: $\mu = \left(\frac{W}{L}C_i\right)^{-1} {V_{DS}}^{-1}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)$; Saturation regime: $\mu = 2\left(\frac{W}{L}C_i\right)^{-1}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2$

As mentioned earlier, in the ideal case the linear and saturation field-effect mobility should be identical as they represent a physical property of the transistor during conduction, however they values may differ as a result of imperfections. In this thesis we mostly refer to field effect mobility in saturation as it is relevant to transistor operation in its ON state. In addition, many studies use this value as a benchmark parameter for comparison.

Information regarding the threshold voltage and subthreshold swing can also be derived from the transfer curve. According to equation (5), the threshold voltage can be found by extrapolation of the square root of I_{DS} and identifying its intersection with the x-axis. This method is similar to the widely used ELR method [52]. Although this method has some limitations [52] we will apply it through the thesis for consistency. Additionally, the subthreshold swing can be simply obtained from finding the slope of the curve in its exponential region, just before V_{GS} reaches the threshold voltage. As mentioned earlier this value contain information about the trap density of the semiconductor.

Finally, information regarding trap states in the semiconductor can also be identified by the presence/absence of hysteresis in the transfer curve. Hysteresis referred as the difference between the forward and reverse scan of V_{GS}, which creates a quantified shift in threshold voltage, according to the sweep direction. The dependence on the scan direction is caused by the history of trapping and releasing of charge carriers from energy states when as a result of voltage application.

Some of the parameters that can be directly extracted from the transfer curve are depicted in *Figure 4*.

2.3.2 Output characteristics

The output curve describes the relation between the drain-source voltage (V_{DS}) and drain-source current (I_{DS}). In the output curve we can readily detect the transistor's operation in the linear and saturation regimes. The output curve is measured by holding the gate voltage constant, and sweeping the drain voltage from 0 to a pre-defined maximum value. The source port is always connected to the common ground of the circuit. The scan is usually done for several gate voltages to evaluate the transistor performance in different operating voltages. During the scan of V_{DS}, the drain current (I_{DS}) is recorded using a parameter analyzer. The output curve is important for characterizing the device in its linear and saturation region and is essential for circuit design (for example when transistors are used as current sources).

By a qualitative observation of the output curve we can estimate the ideality of the linear and saturation regions. The output curve should present a linear behavior at small V_{DS} values and saturated, constant current in the saturation regime. Deviation from this forms implies on inconsistencies with the transistor model. For example, in case that the drain current exhibits non-linear current increase with small values of V_{DS}, a non-ohmic interface exists between the contact and channel. A Schottky barrier caused by energy gap between the semiconductor and the contact or the presence of space charge limited region (SCLC) in case of short channel devices, hinders charge injection and create a deviation from the model [53]. Non-saturated current at high values of V_{DS} implies on additional conduction mechanisms when the channel is not 'pinched-off' properly [47].

The output curve is also useful for calculating two important resistance values of the transistor – the contact resistance and the output resistance (in saturation). The contact resistance is commonly derived by calculating the linear region resistance ($^{\partial V_{DS}}/_{\partial I_{DS}}$) for transistors with different channel lengths and implementing the transmission line method (TLM) [54]. The contact resistance becomes very important when decreasing channel length. In short channel lengths the contact resistance accounts for larger portion of the total resistance and decreases the effective mobility of the device. We will implement this method in our work to evaluate the performance of our transistors in short channel lengths. From TLM, we can also extract the transfer length (L_T) which is an essential parameter for determining the dimensions of the source and drain contacts [54–56]. The output resistance is also calculated from the derivation of the drain voltage in relation to the drain current for a single device in the saturation regime. Ideally, this resistance should go to infinity because the drain current does not depend on the drain voltage. In practice high values of this resistance are preferred, especially for application as current source or load resistance of inverters.

2.3.3 Cutoff frequency

The cutoff frequency of a transistor is the frequency where its current gain (i.e. i_{DS}/i_{GS}, here i represents small signal) equals to unity. In this frequency, the transistor cannot function anymore as a useful device as the current through the dielectric becomes substantial. It can be shown that the gate-source current ahs a linear dependence in frequency where the drain-source current does not depend in the input signal frequency. This leads to the following relation, describing the ratio between the small signals of the gate and the drain [10]:

(10)
$$\left|\frac{i_{DS}}{i_{GS}}\right| = \frac{g_m v_{GS}}{2\pi f C_G v_{GS}} = \frac{g_m}{2\pi f C_G}$$

where C_G denote the total gate capacitance and is composed of parasitic capacitance and channel capacitance. The parasitic capacitances are originated from the overlap between the gate and source and drain and are independent in the operation mode of the transistor. The channel capacitance, on the other hand, depends on the operation regime. The total gate capacitance is can be presented as [57]:

(11) Linear regime: $C_G = C_i W(L + 2L_C)$; Saturation regime: $C_G = C_i W\left(\frac{2}{3}L + 2L_C\right)$

For long channel lengths, the two terms can be approximated to be equal. We will adopt this approximation in our case. By depicting the condition of $\left|\frac{i_{DS}}{i_{GS}}\right| = 1$ at the cutoff frequency with equations (10) and (11) we derive the following relation for cutoff frequency f_T [10,33]:

(12) $$f_T = \frac{g_m}{2\pi f C_G} \cong \frac{g_m}{2\pi W C_i (L + 2L_C)} = \frac{\mu(V_{GS} - V_{TH})}{2\pi L(L + 2L_C)}$$

This relation clearly shows the importance of the channel dimension to the improvement of transistor's cutoff frequency, as the dependence in the channel length is quadratic. Increasing the device mobility and transconductance can also contribute to high frequency operation.

3 Material and Methods

3.1 Ultrathin plastic foils

Recently, great development is being made in the field of ultrathin, imperceptible electronics. Large area OTFT fabrication, stretchable photonics devices, epidermal functional tattoos and others [16,18,21,22,58] have shown the feasibility to make electronic circuits more intimate and light that they have ever been before. Besides being imperceptible and conformable to surfaces, ultrathin electronic devices has additional attractive features. Ultrathin devices can achieve higher signal to noise ratio than their thicker counterparts, even when only passive electrodes are implemented on it [59]. Furthermore, reducing substrate thickness significantly reduces the mechanical stress on the device in case of bending. This property allows ultrathin devices to be rolled and crumpled down to very small bending radii [16].

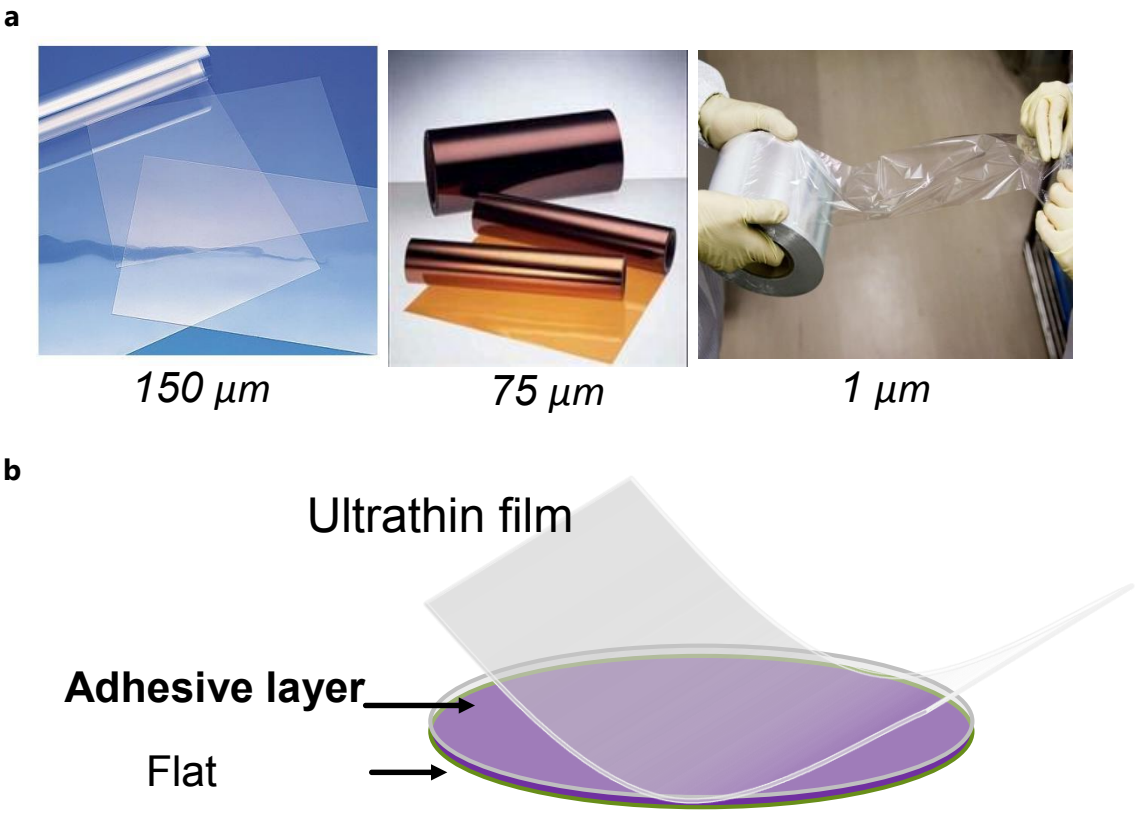


Figure 5: (a) Flexible films, common in use in the plastic electronics research and industry. From left to right: 150 µm polyethylene-naphthalate (PEN) film, 75 µm polyimide (PI) film and 1 µm polyethylene-terephthalate (PET) film. (b) Common lamination method of ultrathin films on flat surfaces using adhesive layer.

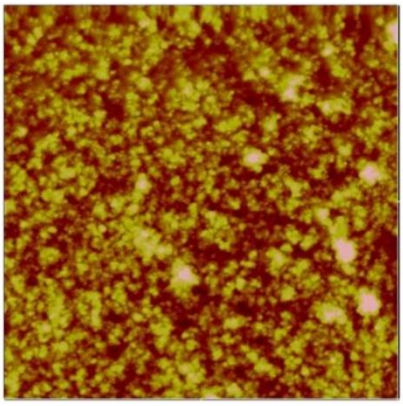
For device fabrication on ultrathin films, there are several important considerations. First are the film mechanical properties and surface characteristics. The film should be mechanically durable to reasonable (depends on the application) lateral stress to allow device handling without failure. In addition, surface roughness is of utmost importance when one tries to fabricate organic electronic devices. Semiconductor quality is very sensitive to surface roughness during deposition and shows negative correlation to an increased surface roughness. Surface energy is also important in case that the semiconductor is deposited directly on the thin film [35]. Another requirement is that the film will be flat and stable during device fabrication. This is an important perquisite for reliable patterning and semiconductor deposition. The ultrathin film is easy to wrinkle and change its form during device fabrication. In *Figure 5*a, we give examples of common flexible substrates used for electronic device fabrication. It can be easily seen that the ultrathin foil has different mechanical properties than the thicker plastic foils.

In order to maintain a flat form of an ultrathin film during device fabrication, there are two main approaches: lamination of existing film on flat surface (*Figure 5*b) or direct film formation. In the first method, an adhesive layer (usually spin-coated polymer) is used to provide strong adhesion of the foil to the substrate during processing, yet it should enable stress-free delamination when device fabrication is completed. In this approach, the film can be prepared/purchased separately and be used as a substrate for device fabrication. The lamination procedure should be done in a contamination-free environment and avoid air gaps between the ultrathin film and the adhesive layer in a precise process. In addition, the utilization of this layer limits the process window on the film and device fabrication should also consider the properties of this layer. On the other hand, direct formation of films, using vapor deposition or spin coating, is a simple method that allows good adhesion to surface and compatibility to wide range of processes. Thickness of the film is determined during the formation process. This kind of deposition assures full contact of the film to the substrate once it is done in a clean environment or under vacuum.

Material selection and adhesion technique was critical for successful fabrication of short channel devices on ultrathin films. Previously reported adhesion layers (based on Polydimethylsiloxane) were not applicable to our process. The ultrathin film was easily delaminated when we applied the photolithography process due to use of organic solvents. In order to overcome this issue and improve our device performance we chose parylene diX-SR as a base substrate for device fabrication. Parylene diX-SR shows very small surface roughness of 4 nm RMS (when deposited using SCS LABCOTER, *Figure 6*a [60]), which is considerably lower than ultrathin polyethylene-naphthalate (PEN) [16] and only slightly higher than thick polyimide film [60]. In addition, the material has good yield strength (52.7 MPa) and high melting point of 303.2°C [61]. For practical applications with organic electronics, moisture vapor transition rate (MVTR) and oxygen transmission rate (OTR) are important parameters to keep device stability and prevent degradation.

Parylene derivatives (most commonly parylene-C) are known as good encapsulations in the biomedical field for implantable devices [62,63] due to their relatively low transmission rates. Parylene diX-SR presents MVTR of 0.09 g·mm/m^2·24h and OTR of 2 cm^3·mm/m^2·24h·atm which are comparable to parylene C and provide relatively low rate for device encapsulation [64]. In order to deposit parylene diX-SR in an ultrathin form, we used chemical vapor deposition (CVD) by SCS LABCOTER to form ~1 µm thick layers directly on Si/SiO_2 wafers. The ultrathin film showed strong adhesion to the rigid substrate and we could apply all lithography process steps to the substrate. After the completion of device fabrication, the ultrathin substrate could be carefully delaminated from the rigid Si/SiO2 support to obtain free-standing ultrathin films. In *Figure 6*b surface properties and main typical film characteristics of parylene diX-SR as substrate are summarized.

a



b

Material Property	Parylene diX-SR
Density [g/cm^3]	1.28
Yield Strength [MPa]	52.7
Tensile Strength [MPa]	58.5
Tensile Modulus [GPa]	4
Melting point [°C]	303.2
MVTR [g·mm/m^2·24h]*	0.09
OTR [cm^3·mm/m^2·24h·atm]**	2
Water absorption [%]***	<0.1

**at 37°C; **at 23°C; ***over 24 hours*

Figure 6: (a) Atomic force microscope scan of parylene diX-SR substrate, deposited using SCS LABCOTER [60]. (b) Typical values of parylene diX-SR 25 µm thick film [136].

3.2 Organic semiconductor

The organic semiconductors are the most essential element that defines the field of organic transistors. The Organic semiconductors are hydrocarbon based materials that can change their conductivity according to external stimulation such as voltage application. Organic semiconductors can be found in two forms: conjugated polymers and conjugated small-molecules [10]. Small molecule semiconductors based OFETs are often preferable due to their advantages of a defined molecular structure, a definite molecular weight, high purity and good reproducibility compared with their polymeric counterparts. Though, processing of conjugated polymers can carry advantages in terms of ease of fabrication and cost. The basic principles of these materials can be described by the valence bond theory and the Born–Oppenheimer approximation [65]. The conduction mechanism is based on the molecular level bonding between the organic

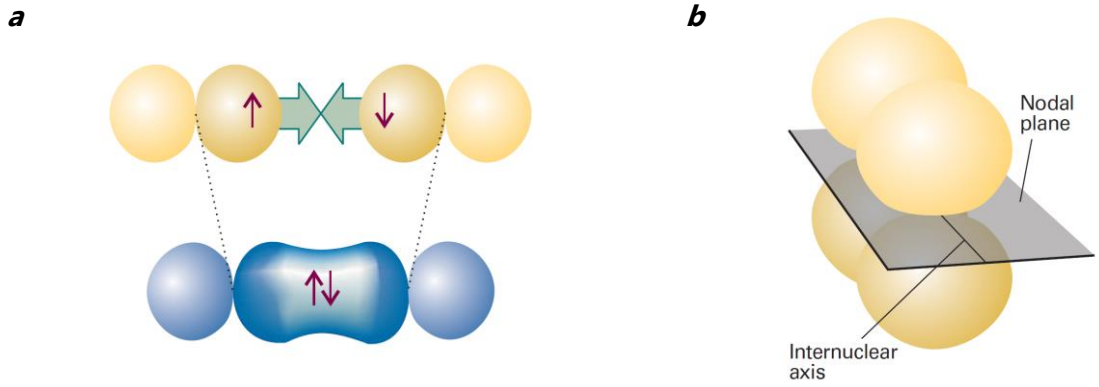


Figure 7: Illustration of simple (a) σ bond orbitals with cylindrical symmetry around the internuclear axis and (b) π bonds perpendicular to the internuclear axis [65].

molecules and their energy gap. In this section, we will review some of the important principles related to the molecular structure and energy levels.

Atoms in the organic material are connected by σ and π chemical bonding which are described by the spatial distribution of electron orbitals. The σ bonds are connections between atoms that their electrons orbitals have cylindrical symmetry around the internuclear axis. On the other hand, π bonds do not have cylindrical symmetry and arise from spin pairing of electrons in orbitals that approach side by side, perpendicular to the axis between nuclei (*Figure 7*). In the case of polyatomic structure, the bonds can be created by hybridization between s and p orbitals to forms hybrid orbitals which consist of σ and π bonds [65]. As an example, we will analyze the hybrid sp^2 orbital which is found in the elementary ethene molecule (or ethylene). In ethane, two carbon atoms are connected via a double bond and to additional 4 hydrogen atoms (*Figure 8*a). The ground state of carbon is $2s^1p_x^1p_y^1p_z^1$ which allows 4 free electrons for each carbon to bond with

its neighbor atoms. In this configuration three bonds in the sp^2 hybridization are localized σ bonds and found in the same internuclear plane. The remaining p_z electron is free to form a perpendicular and delocalized π bond, above and below the σ bonding plane (*Figure 8*b). The energy levels of the π-bonds are concentrated in two bands separated by an energy gap - the band gap (*Figure 8*c). Charge transport occurs either in the Highest Occupied Molecular Orbital (HOMO) or in the Lowest Unoccupied Molecular Orbital (LUMO).

Conduction in organic semiconductor, based on the HOMO and LUMO levels of the material, is made via the overlapping π orbitals between molecules which are found in physical proximity to each other (π-π stacking). A preferable orientation between molecules is the parallel one, when charge transport is made perpendicular to the

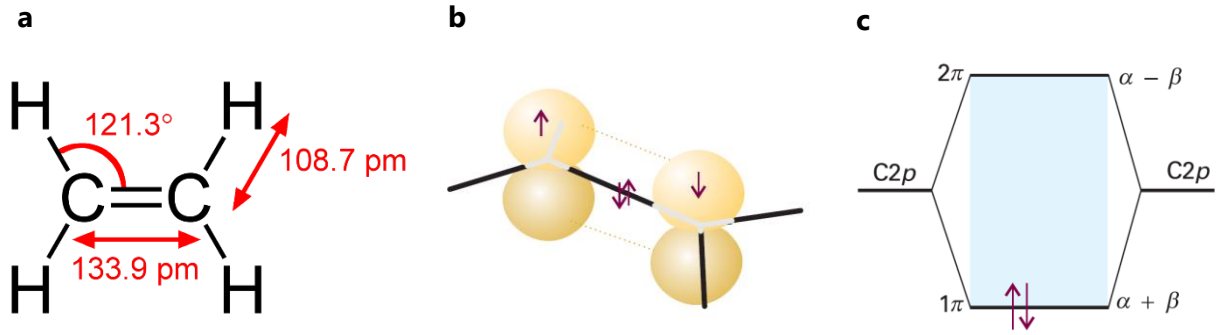


Figure 8: (a) Ethene molecular structure and spatial angles between atom bonds (from 'Ethylene', Wikipedia). (b) Illustration of ethene π bonds (yellow spheres) in the sp^2 hybridization. (c) Highest occupied molecular level (HOMO) denoted with 1π bond and the lowest unoccupied molecular level (LUMO, 2π) of the sp2 hybridization in ethane (illustration). Images were adopted from [65].

molecular plane [10,66]. It is important to note that the electronic structure of an organic solid largely preserves that of a molecule or a single chain, as the molecules are attached to each other by weak Van der Waals interaction [67]. Hence the ionization energy and electron affinity of a material correspond to the HOMO and LUMO levels (in relation to the vacuum level) in the molecular case (*Figure 9*a).

The HOMO and LUMO levels are critical in determining the charge injection from contacts to the semiconductor and affects the material air stability. The HOMO and LUMO can be considered as the valence and conduction bands as in the case of inorganic semiconductors. Conduction of holes is made through the HOMO level and electrons are transferred in the LUMO level. Please note that the conduction in organic semiconductors does not strictly follow the band-like mechanism [9,67], but this simplification is useful for device modeling. P-type and n-type organic semiconductor are characterized by the majority of charge carriers in the materials, holes and electrons respectively. In order to inject carriers from metal to the semiconductor, the energy barriers for injection should be overcome (*Figure 9*a). For example, charge transfer from a contact to a p-type

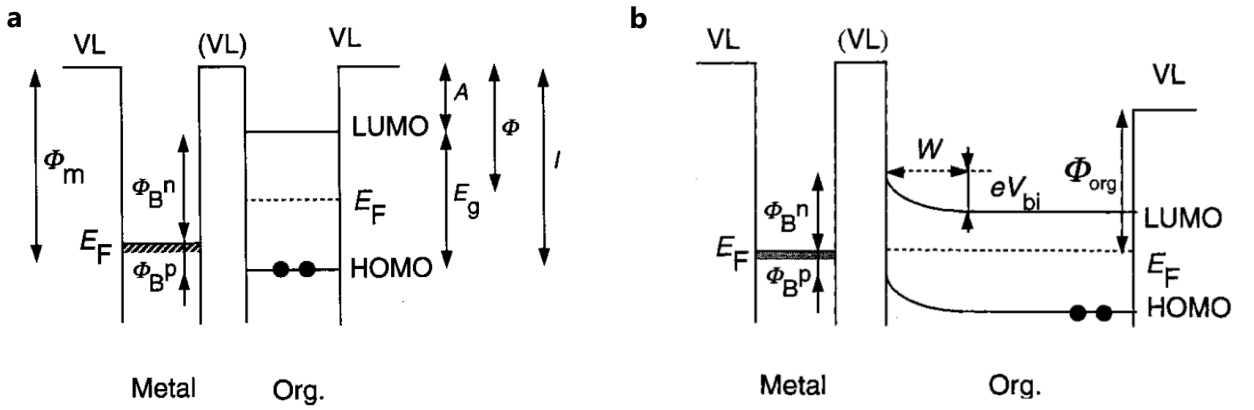


Figure 9: (a) Energy band diagram of metal and organic semiconductor. HOMO and LUMO levels correspond to the ionization (I) and electron affinity (A) of the material. Eg is the energy gap between the HOMO and LUMO level. $\phi_B n$ and $\phi_B p$ are the injection barriers from the metal for electrons (to LUMO) and holes (to HOMO) respectively. (b) Band bending and build in potential (eV_{bi}) of metal and semiconductor with the same vacuum level. Diagrams adopted from [67].

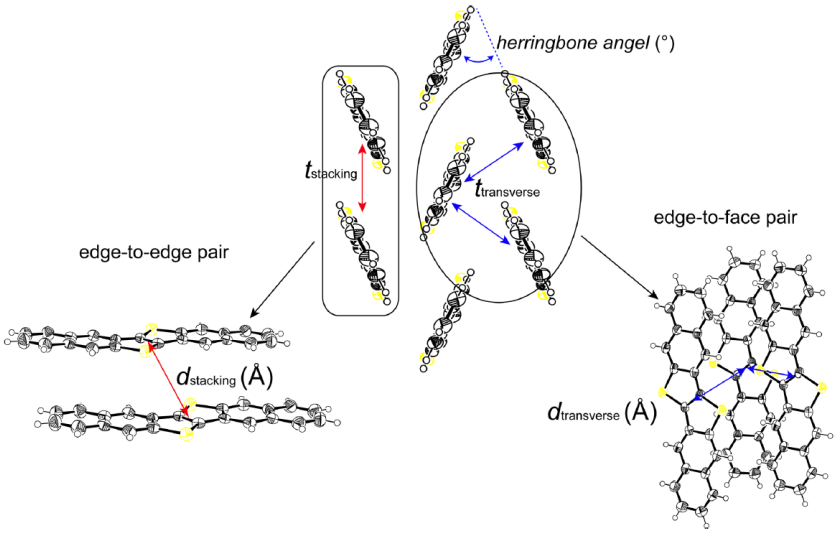
semiconductor is facilitated when the contact's Fermi level is deeper than the HOMO level of the p-type semiconductor. Analogous consideration can be done for n-type materials and their LUMO levels. The energy barrier changes when the metal and semiconductor are interfaced according to the build-in potential which represents the difference in vacuum levels between the solids (*Figure 9*b).

For an organic semiconductor, the key features are high majority carrier mobility, good processability and excellent air and environmental stability. For several years, n-type organic semiconductors fell short in performance and air stability from their p-type counterparts. The reason was mainly the air instability of these materials to reaction with O_2 and H_2O species [68,69]. An onset LUMO energy of approximately −4.0 eV is essential to stabilize electrons during charge transport. Deeper LUMO level may be better for stabilizing the organic semiconductor however too deep levels (<−4.5 eV) can cause low ON/OFF ratio at device level due to unintentional doping [69]. Recently great improvement is made in this field and n-type semiconductors start showing good air stability and device performance towards complementary organic electronics [69,70]. On the other hand, p-type semiconductors have shown good device mobility (> 1 $cm^2/V{\cdot}s$) and air stability. Acene and thiophene based p-type organic semiconductors have advantageous π-bond topology and were among the leading functional molecular groups for achieving good electrical and environmental properties [71–73]. Among these groups, pentacene is one of the most studied p-type semiconductor for device and morphological investigations [51,74–78].

In this work, we will utilize the air stable, thiophene based, dinaphtho[2,3-b:2′3′-f]thieno[3,2-b]thiophene (DNTT) as a small molecule organic semiconductor. DNTT was first reported by Takimiya and Yamamoto [79] and since then was proven as a high

mobility organic semiconductor with excellent environmental and thermal stability. In its single crystalline form mobility of over 8 $cm^2/V{\cdot}s$ could be achieved [80] where in the thin film, polycrystalline layout high hole mobility of 3 $cm^2/V{\cdot}s$ was obtained [79]. Air stability tests have demonstrated several months of un-encapsulated operation with negligible degradation [81]. The thermal stability of the semiconductor was also tested in long channel OFET devices that were successfully implemented for biomedical application [82]. Different derivatives of DNTT, such as DPh-DNTT or C_{10}-DNTT, can exhibit enhanced performance in terms of device mobility and stability [83–85]. The main properties of the semiconductor are summarized in *Figure 10*.

dinaphtho[2,3-b:2′3′-f]thieno[3,2-b]thiophene (DNTT) – p-type organic semiconductor



HOMO level	–5.4 eV
Band gap (thin film)	2.6 eV
$d_{stacking}$ (A)	6.19
$t_{stacking}$ (meV)	71
$d_{transverse}$ (A)	4.93
$t_{transverse}$ (meV)	91
Herringbone angle (deg)	52.6

Figure 10: Molecular structure (left) and key parameters (right) of dinaphtho[2,3-b:2′3′-f]thieno[3,2-b]thiophene (DNTT) organic semiconductor. Images and data were adopted from [72].

3.3 Gate dielectric

The organic semiconductor is not the only critical component in structuring the organic transistor. An appropriate gate insulator is very important for device characteristics and has immense effect on transistor's mobility, operation voltage and more. The dielectric can affect the morphology of the organic semiconductor and the orientation of molecular segments, via their interaction with the dielectric (especially in bottom gate devices). Furthermore, the interface roughness and sharpness may be influenced by the dielectric itself, the deposition conditions, and the solvents used [35,86]. Large surface roughness creates irregularities in the channel area that can act like charge traps or prevent proper nucleation during the semiconductor growth. Interface traps between semiconductor and gate dielectric can also cause undesired phenomena such as device hysteresis or gate voltage dependent mobility. Polarity of the dielectric interface can lead to morphological inhomogeneity or affect the distribution of the electronic states (*Figure 11*) [41,87,88].

Many of the first OFET deices utilized Si/SiO_2 as gate and gate dielectric due to the availability of this structure and the optimized defect free interface between the gate and dielectric. However, using SiO_2 as dielectric to interface the semiconductor has many disadvantages. The SiO_2 tend to absorb hydroxide or water molecules which negatively affect the interface with the organic semiconductor. Interface states on the inorganic layer also lead to increased hysteresis and charge trapping. In addition, applying oxides as dielectric layers in the bottom gate architectures affects nucleation and semiconductor morphology due to polarity in the interface, which reduces device mobility [89]. Lastly, Si/SiO_2 devices require large operation voltage which leads to high energy consumption.

The gate dielectric layer should satisfy several conditions. One of the crucial parameters is the maximum possible electric displacement D_{max} that the gate dielectric can endure [90]:

(12) $$D_{max} = \varepsilon_0 k E_{Breakdown}$$

where ε_0 is the vacuum permittivity, k is the dielectric constant of the material and $E_{Breakdown}$ is the breakdown electric field. The capacitance per area is then defined by:

(13) $$C_i = \varepsilon_0 k / d$$

where d is dielectric layer thickness. High capacitance per area can be achieved in two approaches: reducing dielectric thickness or using materials with high dielectric constants. Increasing the capacitance per area of the dielectric leads to a reduced operation voltage, according to the following relation:

(14) $$n = {}^{1}/_{e}\, C_i (V_{GS} - V_{TH})$$

where e is the elementary charge and V_{GS}, V_{TH} are the gate-source and threshold voltage respectively, and n is a specific charge carrier density in the channel. Lower operation voltage provides safer and more energy efficient devices. Additionally, dielectric layer should provide 'traps free' (ideally) interface with the semiconductor and allow proper nucleation and semiconductor growth. For example in the case of thermally evaporated small molecules organic semiconductors, low surface energy with small surface roughness substrates are generally preferred [35]. Finally, the gate dielectric should be ideally compatible with flexible substrate, allow mechanical durability and preferably low cost

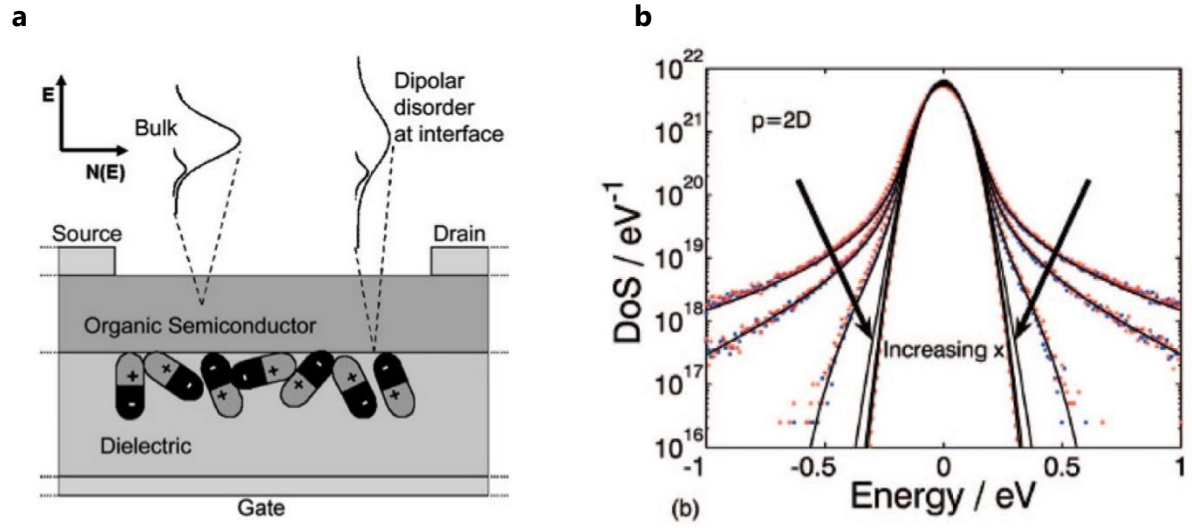


Figure 11: (a) The density of states (DOS) in the bulk of the semiconductor and at the interface with the dielectric as a result of local polarization [88]. (b) Calculated DOS broadening due to static dipolar disorder in the dielectric with increasing distance into the semiconductor [87].

processes. In principle, insulators for OFET application can be classified into 3 main categories: high-k inorganics, polymers and self-assembled small molecules to satisfy the above requirements [41,90].

As mentioned earlier, the use of high-k inorganic materials as insulators can benefit in low operation voltage and high capacitance per area. High permittivity dielectrics have been extensively used in inorganic FETs however only in 1999, Dimitrakopoulos and coworkers were the first to use high-k oxides as dielectrics in OFETs [91]. As a result, the group could reduce operation voltage down to 5V and achieve higher mobility due to an increased charge carrier density in channel at low voltages. Since then, many groups have utilized metal oxide dielectrics for organic electronics. Al_2O_3 (k~8 and Ta_2O_5 (k~23) are amongst the most experimented species however other metal oxides such as HfO_2 (k~22-25), TiO_2 (k~41) and ZrO_2 (k~25) are also useful materials for application in OFETs [41]. One of the problems in inorganic oxide layers is their high roughness and surface polarity that degrade the efficiency of charge transport in the channel. This might be solved by surface modifications such as hexamethyldisilazane (HMDS), Octadecyltrichlorosilane (OTS) or others. Additional concerns are the often use of high energy processes, such as

plasma enhanced CVD (PECVD), sputtering or atomic layer deposition (ALD), that may damage the plastic substrate during deposition. In this sense, anodization can provide a good compatible process for thin films application. Another issue with the high-k approach the poor mechanical durability of those layers, as they are based on oxides or ceramics.

Polymeric dielectrics have a great potential for utilization as OFETs gate insulators. Their characteristics can be tailored to allow different solubility, processability and dielectric coefficients. Polymers can be often deposited by simply spin coating, casting or printing under ambient conditions [10]. In *Figure 12* some of the common polymers used for gate dielectric are presented. The first detailed study on polymeric gate dielectrics was made in 1990 by Peng et al. [92]. The group could show better mobility values and I/V characteristics than the ones achieved on SiO_2 and reported on a positive correlation between the dielectric constant and device mobility. Operation voltage was in the range of 30V. The interface between the gate dielectric and the semiconductor affects not only the semiconductor morphology but also the density of states in the channel. By

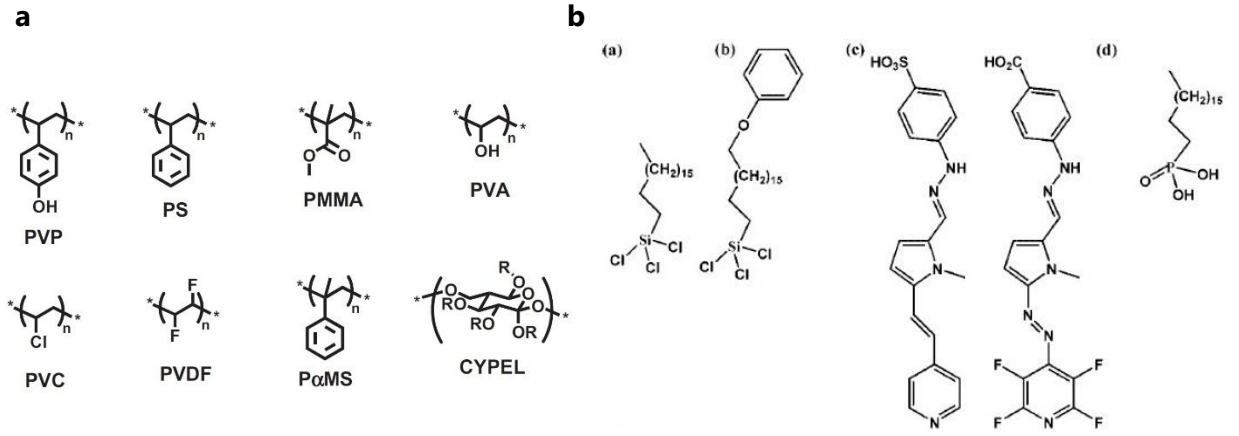


Figure 12: Chemical structure of common (a) polymers and (b) self-assembled-monolayers used as gate dielectrics for OFETs. Images adopted from [90] and [41] respectively.

introducing high-k material, random dipole fields at the interface can cause carrier localization and change the density of states in the channel. In 2004, casting of a high breakdown strength (>3 MV/cm) polymeric dielectric layer was demonstrated for the first time in thickness below 300 nm [93]. The devices based on PEDOT:PSSR semiconductor exhibited mobility of 10^{-4} $cm^2/V{\cdot}s$ with only 50 nm of gate insulator. Further efforts with polymers (poly-4-vinylphenol and polystyrene) and cross-linking reagents could reduce dielectric thickness down to phenomenal values of 10-20 nm for a pinhole free layer [94]. Different approach, utilizing the top gate structure, vapor deposited parylene-C as the dielectric on top of the semiconductor [95]. Dielectric thickness reached 540 nm and devices ON/OFF ratio exceeded 10^4. In summary, polymer dielectric layers can readily achieve high breakdown voltage with very small thicknesses in simple fabrication

techniques. Nevertheless, the ultimate polymer dielectric, presenting low voltage operation, device uniformity, low surface roughness and good device characteristics, was not demonstrated yet.

The use of self-assembled-monolayer (SAM) as dielectrics is another promising strategy to provide high capacitance per area for reliable low voltage operation. The basic principle is to deposit a few nanometer thick SAM that has good leakage properties to improve or create a dielectric layer. SAM dielectrics can reach capacitance per area in the order of ~100 nF/cm^2 and leakage currents in the order of 10^{-8} A/cm^2. The use of a SAM as a gate dielectric was pioneered in 1996 by the deposition of octadecyltrichlorosilane (OTS) onto SiO_2, to realize reasonable OFET devices with low leakage [96]. Self assembled monolayers can be grown directly on various oxides, to improve leakage current, semiconductor formation and device mobility [41]. H. Klauk and his group has made significant contribution in the field by depositing n-octadecylphophonic acid (ODPA) on aluminum gates and obtaining operation voltage of only 2V with low leakage and high device mobility, for n-type and p-type case. The group has demonstrated the reliability of this method by applying it to organic circuits and applications [7,13,24,82]. The versatility of the SAM approach was demonstrated by the development of self-assembled nanodielectric (SAND) by alternating constituent layers and modify the dielectric characteristics [97]. The group has shown that depending on the selected elements, they could change capacitance per area and other dielectric properties, as well as to apply the dielectric to wide variety of semiconductors (including inorganic).

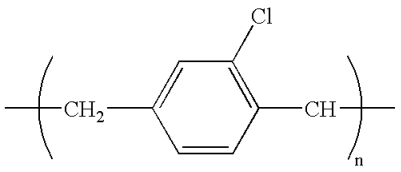
All the above approaches could show promising results towards low voltage, easy processable, mechanically stable and low leakage dielectrics. Intensive study for achieving the optimal gate dielectric for good OFET performance is still ongoing. New approaches for material improvements, deposition techniques and hybrid solutions are being proposed and implemented for this purpose [41]. Currently, the ultimate gate dielectric, achieving all requirements, is still beyond reach and dielectrics for OFETs are often chosen by the specific application.

In order to choose the appropriate dielectric layer for our device fabrication we considered several application issues. First, as we aim for ultrathin and ultraflexible devices, mechanical flexibility and stability have high importance in our consideration. Polymer based dielectric is a natural selection in this case allowing compatibility for ultrathin film fabrication and high flexibility. Second, for the use as 'ambient electronics' and large area sensor sheets, low operation voltage and is also critical. We aim for operation voltage < 10V to realize such application reliably and effectively. The requirement for large area constraints us to choose a method for uniform deposition on large scales. Finally, the dielectric should provide interface for the organic semiconductor to enable good device performance for high frequency operation. A brief summary of the requirements is given in *Figure 13*a.

In our contribution, we utilized low-k polymeric gate dielectric for our OTFTs implementation. The chosen material is a derivative of poly(p-xylylene) - parylene diX-SR, provided by KISCO Ltd. The material has dielectric constant of k=3.06 at 1 kHz. Parylene diX-SR can be deposited reliably on large areas (400 cm^2) in a high vacuum CVD process [98], presents thicknesses below 100 nm and provides capacitance per area in the range 10-100 nF/cm^2. The utilization of CVD allows facile and conformable coating of many kinds of surfaces. The layer is pinhole free and shows leakage current density lower than 10^{-8} A/cm^2 at 1 MV/cm [60]. The dielectric has very small surface roughness (~2 nm RMS) and is compatible with good performance of organic semiconductor and mobilities of ~0.5 $cm^2/V{\cdot}s$ were obtained in the top contact architecture. Lastly, parylene diX-SR is thermally and environmentally stable for practical applications. The main characteristics of the dielectric and CVD system description are given in *Figure 13*. The choice of this

a

Requirements
Flexible
Low leakage
Low voltage
Device performance
Large area



Properties	
k	3.06
Leakage	10^{-8} A/cm^2 (1MV/cm)
Thickness	< 100 nm
Surface RMS	~2 nm
Area	400 cm^2

b

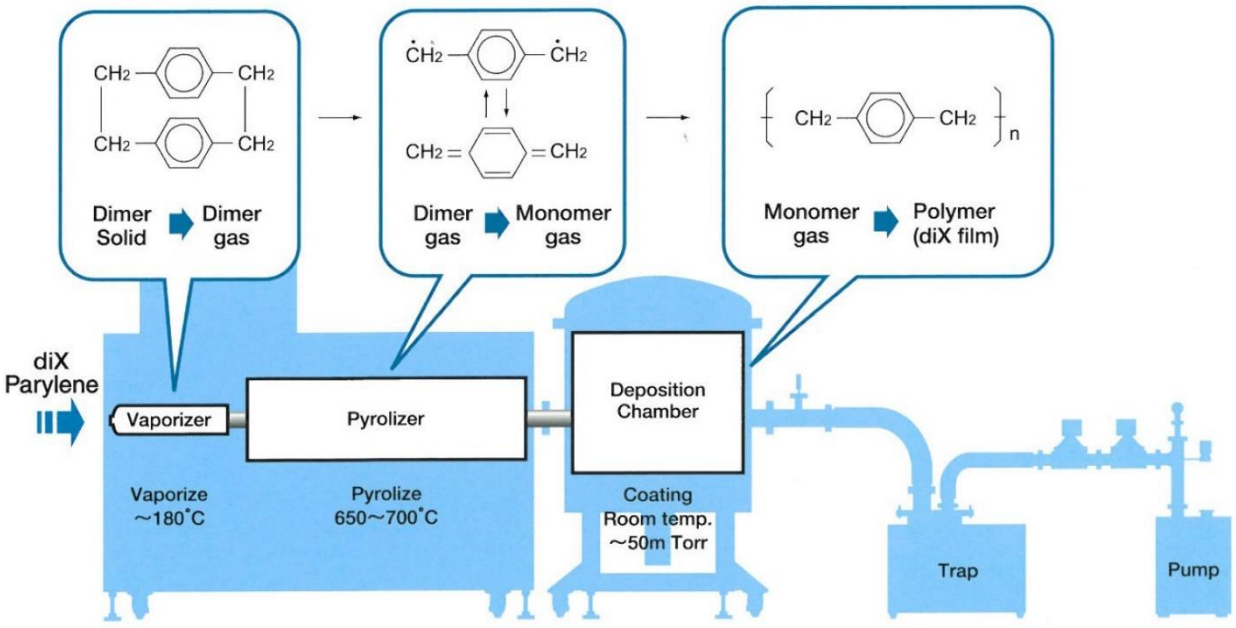


Figure 13: (a) Summary of requirements and main features of parylene diX-SR at high vacuum chemical vapor deposition. The chemical structure of parylene C is given as illustration. (b) CVD process and system description as it appears in [98].

material as gate dielectric is a key parameter for a successful fabrication of high frequency devices on ultrathin foils.

3.4 Photolithography

3.4.1 Process principles

Photolithography is an optical patterning process made on light-sensitive polymer (photoresist). The process is one of the most important building blocks in the semiconductor industry creating structures and components for billions of transistors every year. Ideally, the process designed to transfer the mask pattern to the photoresist, defined by the thickness of the polymer walls. Photolithography patterns are commonly used for selective etching and ion implantation as well as metal deposition using 'lift off' techniques. The process itself is complicated and involves many steps and theoretical background however here we summarize the characteristics of the typical process steps, based on professional resources [99–101]:

Substrate preparation
Proper substrate preparation is required to provide clean surface for the process and improve the photoresist adhesion to it. Surface contamination can take the form of organic or in-organic particles attached to the substrate. These contamination can be removed chemical, mechanical or plasma tripping followed by an additional dehydration step to remove adsorbed water. Dehydration takes place in elevated temperatures for several minutes. The substrate is then allowed to cool down, preferably in a dry environment and coated with photoresist as soon as possible. Adhesion promoters, such as hexamethyldisilizane (HMDS), are often to enhance the surface hydrophobicity for better photoresist coverage.

Photoresist coverage
Spin coating is the most common way to apply photoresist on a substrate. Layer uniformity and thickness controllability are of the most important properties of the photoresist coat. Resist properties (viscosity, composition), substrate topography and spin-coat speed and acceleration mainly affect layer thickness and uniformity but also humidity control, resist temperature and spinner cleanliness have some importance on the final result. As a rule of thumb the photoresist thickness is given by: $d \propto \frac{\upsilon^{0.4}}{\omega^{0.5}}$ [99]where υ is the photoresist viscosity and ω represents the spin-coat speed. Artifacts such as photoresist waviness, streaks (due to particles larger than the photoresist thickness) or edge beads can occur and reduce the coverage uniformity.

Post apply bake (PAB)

The post apply bake stage is implemented to remove excess solvent (~20%-40%) from the spin-coated photoresist in order to stabilize it before exposure [99]. Hot plate baking is usually preferable on convection oven baking due to the shorter heating periods and its uniformity. The main outcomes from this process step are the reduction of film thickness, adhesion improvement and tackiness reduction. PAB also changes the film reaction to later stages such as post exposure bake (PEB) and development. Care should be taken for applying the right conditions because elevated temperatures and long annealing time may decompose the photoactive component in the photoresist or crosslink the photoresist resin. It is also important to notice that baking continues even after the wafer is removed from the heating apparatus. As a result, for a well-controlled process, a subsequent cooling step should be performed after baking.

Exposure

Exposure is one of the most important steps in the photolithography procedure. During this step the pattern is transferred to the photoresist by light exposure which initiate a change in the resist solubility in the developer. There are two types of photoresists: negative and positive type. When the positive type is exposed to light, it becomes soluble to the photoresist developer where the contrary occurs to the negative type. The negative photoresist is initially soluble in the developer and exposure to light in the appropriate wavelength make it insoluble. As an example, diazonaphthoquinone, a common photoactive component (PAC) in positive photoresists is converted to the soluble (in aqueous base developer) carboxylic acid after exposure to UV light between 350 nm – 450 nm. By exposing the pattern to the photoresist, only the parts that become soluble will be removed by the subsequent developing stage. Positive photoresists considered to be more expensive and achieve better resolution and step coverage than the negative type ones.

For the exposure stage, a mask is prepared by the desired pattern. Before exposing the photoresist, the mask should be strictly aligned to the previous pattern on the wafer. Uniform and accurate focus is also evaluated along the surface. Light is then projected through the mask towards the photoresist. The most common method for exposure is by projecting printing which is preferable on contact or proximity printing due to improved resolution and minimal contamination. Projection lithography involves a set of lenses for transmitting parallel light to the mask and restoring a miniature focused pattern on the substrate surface. The patterning resolution is mainly limited by the smallest image that arrives to the surface and by the photoresist restoring capabilities.

Post exposure bake (PEB)

Post exposure bake strongly depends on the photoresist characteristics and might be considered in the following cases [99]:

- Chemically amplified resists: In this kind of photoresists, the photo-activation of the resist is only initiated during the exposure and have to be followed by a PEB for the completion of the reaction and obtaining optimal results.
- Negative resists crosslinking: In many negative photoresists the PEB is an essential step for crosslinking the polymer after exposure. This step makes the photoresist layer more stable towards the development stage.
- Highly refractive substrates: In the case of highly refractive substrates, some of the monochromatic light is reflected to the photoresist during exposure. This effect is called the 'standing wave' effect and it creates a standing wave pattern on the photoresist's walls. PEB in this case promotes diffusion of the active component and smoothen the surface of the resist's profile, preventing the transfer of the standing wave to final pattern.
- Mechanical relaxation: In the case of thick photoresist layers, PEB is taken to reduce the stress formed during PAB and exposure and improve adhesion to the substrate.

When none of the above applies, PEB may be skipped.

Development

Followed by exposure and PEB, resist development is a critical step for photolithography patterning. The resist-developer interaction determines the final pattern characteristics and resolution. There are a few common ways for resist developing: batch development, spin development, spray development and puddle development. Batch development was widely used in the past where large number of wafers were brought into a slightly agitated developer bath and then taken out and rinsed. With the move toward in-line processing other methods were adopted. In spin development the developer is poured on the wafer during spinning where in spray development only a spray of fine mist of developer is introduced to the wafer. During puddle development the developer is poured on slowly rotated wafer and then stopped and remains motionless until for the development time. After the development period ends, the developer is spin-rinsed and dried. Puddle development minimizes the developer in use however it may suffer from developer depletion and slow down the development in areas where large amount of photoresist was removed.

Hard bake

A hard bake (also known as post bake) is usually needed to harden the final resist pattern before exposing it to the harsh conditions of ion implantation or etching. The elevated temperatures crosslink the resin polymer in the photoresist, improving its adhesiveness and making it more thermally stable. Hard bake can also remove residues such as water or solvents from the resist pattern. Higher temperatures or baking periods may damage the pattern quality and make the resist more durable to stripping.

Pattern transfer

Pattern transfer to the substrate can be made in several ways. The most common way is by etching where the photoresist 'protects' the areas to be remained on the substrate. Etching can be made by a wet chemical process or by dry plasma etching. Another method utilizes selective deposition to the substrate (also known as 'lift off' process). This process is usually used where etching processes are not available (as in the case of copper stripping). Lithography pattern is made according to the desired pattern on the substrate and deposition is made on the substrate and photoresist. After stripping the photoresist, only the deposited pattern remains on the surface. Selective ion implantation can also be transferred using photolithographic pattern. When exposed to ion stream, the uncovered areas will be bombarded with ions where the regions covered with photoresists remain un-doped. These methods give photolithography a large processing window for implementing this technique to wide range of materials and technologies.

Photoresist stripping

Two methods are available for photoresist stripping: wet and dry stripping. Most commercial organic strippers are phenol based and present better performance than acetone in removing residual scums. For inorganic applications, acid-based strippers are used in elevated temperatures. Nevertheless, in most cases wet stripping cannot completely remove all photoresist remains, especially if the photoresist has gone through hard baking and harsh processing steps. Dry oxygen plasma stripping is more suitable in that case and can remove the organic residues of the photoresist without damaging inorganic surfaces. It is important to notice that for organic electronic application this step should be taken in extreme care due to the sensitivity of the organic substrates and compounds involved.

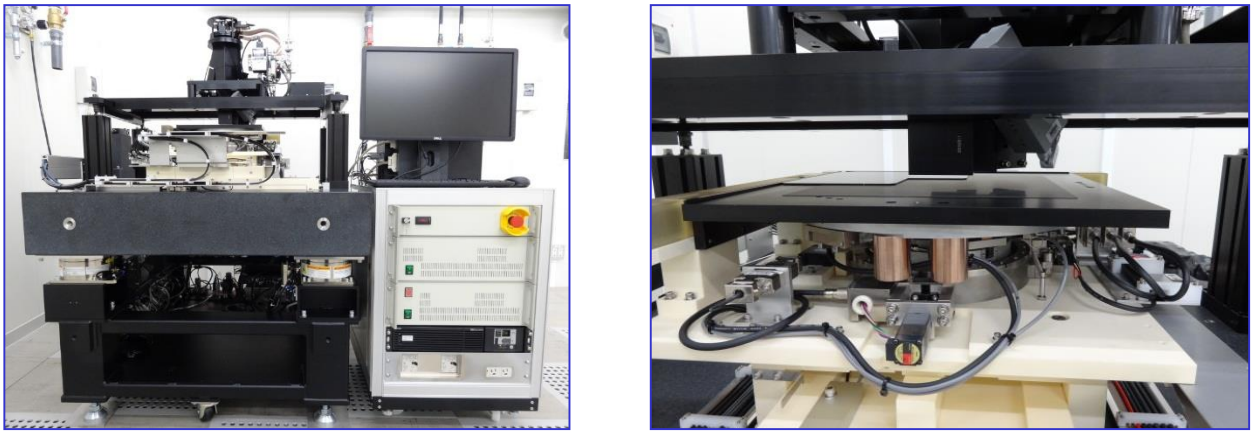
3.4.2 Application to ultrathin films

The application of fine patterning using photolithography on flexible substrates requires process modifications compared with the standard application on rigid substrates. First, flexible substrates can be easily curved and change their form which makes accurate focusing on their surface more difficult. This issue becomes more significant the thinner the substrate is. Second, flexible plastic substrates are more sensitive to some of the standard processes during lithography, such as high temperature annealing, plasma cleaning and solvent cleaning. Plastic substrates can adsorb solvents and change their properties, be easily etched by plasma treatment or deform during excessive heating. Lastly, plastic surfaces can be rougher than the conventional silicon or glass substrate. Surface roughness should be considered as a lower limit for the pattern size available. For

these reasons, specific care should be taken in order to apply photolithography to flexible polymer foils.

When we consider the utilization of photolithography on ultrathin substrates, first we should take care of the correct way to stabilize and planarize the substrate during the process. For thicker films and use of shadow masks, it is possible to hold the film flat by clipping it to a rigid support. However, this is not sufficient in the case of photolithography and the use of easily crumpled ultrathin films. One method is to adhere the ultrathin film by adhesive layers to a rigid, flat substrate [16]. It is important that the adhesive layer would sustain 'wet' processes and the use of developers and photoresist strippers to keep the plastic foil flat at all times. On the other hand, the adhesive layer

a **b**



Manufacturer	PMT corporation, Japan
Maximum patterning area	300x300 mm^2
Resolution	500 nm
Exposure wavelength (LED)	365 nm
Focus depth	1.5 µm
Dynamic focus (during scan)	±50 µm
Scan speed	0.2-2.5 mm/s

Figure 14: LED mask-less photolithography system. (a) Ovreview and (b) photolitography stage close-up of the system. Table describes main characteristics and specifications.

should allow easy delamination of the film in the end of the fabrication process to obtain a free-standing device.

Solvent selection and proper cleaning methods are also a key factor for a successful fabrication on the ultrathin films. It is very important to keep the surface clean during all process steps to avoid patterning faults and un-uniformities. Additionally, solvents that

does not change surface properties negatively (e.g. reduce surface energy), and are not easily absorbed by the plastic are preferable.

For our process, we chose parylene diX-SR as our ultrathin substrate. Parylene dix-SR is a thermally stable material with melting temperature of 300°C [61] and small surface roughness. Parylene diX-SR can also be easily deposited by chemical vapor deposition in various thicknesses. For the use with photolithography patterning technique, we found that direct deposition of the parylene layer on top of a silicon – silicon dioxide substrate obtains reliable and flat stratum that can sustain all lithography steps without failure. In

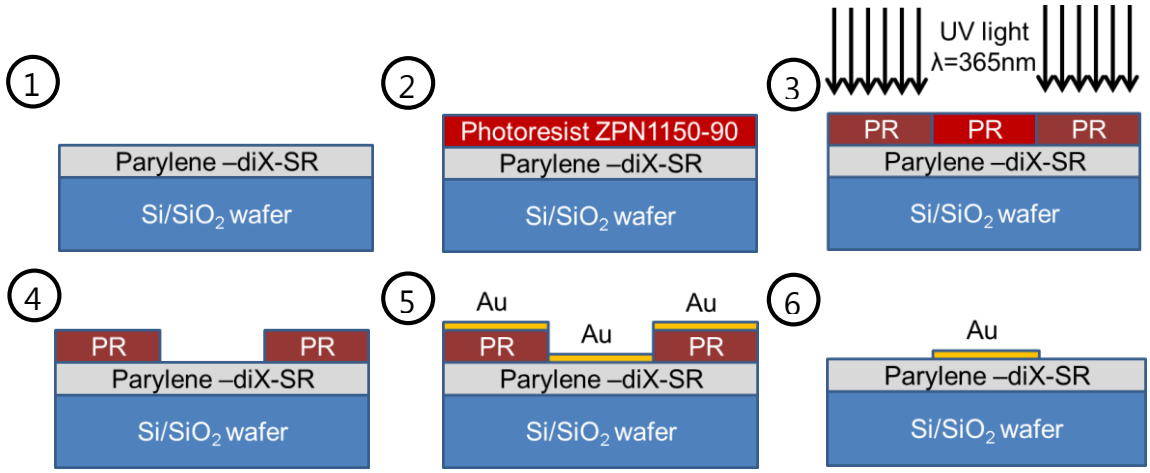


Figure 15: Gold patterning using LED mask-less UV exposure system on ultrathin parylene diX-SR substrate: 1. CVD formation of ultrathin parylene diX-SR (1 µm) on flat Si/SiO_2 4" wafer; 2. Spin coating of negative type photoresist: ZEON ZPN 1190-50, 3000 rpm, 20 seconds. The photoresist is soft baked for 90 seconds at 90°C; 3. UV exposure using LED mas-less scanning at 0.5 mm/s of the negative desired pattern; 4. Post exposure baking (110°C for 1 minute) and development of the unexposed photoresist using Tetramethylammonium hydroxide (TMAH) 2.38% solution; 5. Gold deposition using thremal evaporation vacuum chamber. Thickness may vary between 20 nm – 100 nm according to the application; 6. Photoresist 'lift-off' using acetone leaves the desired pattern on ultrathin substrate.

the end of the process, the ultrathin parylene layer can be easily detached from the wafer thanks to the hydrophobicity of the silicon dioxide. We paid special attention to the solvents in use and used solely organic solvents such as acetone, ethanol and isopropanol for cleaning the substrate and stripping the photoresist.

By applying the above key technical methods, we could pattern fine dimensions using photolithography. We implemented a novel LED mask-less UV exposure system that has a dynamic focus capabilities to compensate small curvature changes in the surface (Figure 14). This ability allows larger processing window for the thin film deposition and patterning. We used the photoresist ZEON ZPN 1150-90 in the thickness of ~3 µm. The key process steps of the photolithography patterning are denoted in Figure 15. We optimized the photoresist thickness and exposure scan speed to obtain the desired

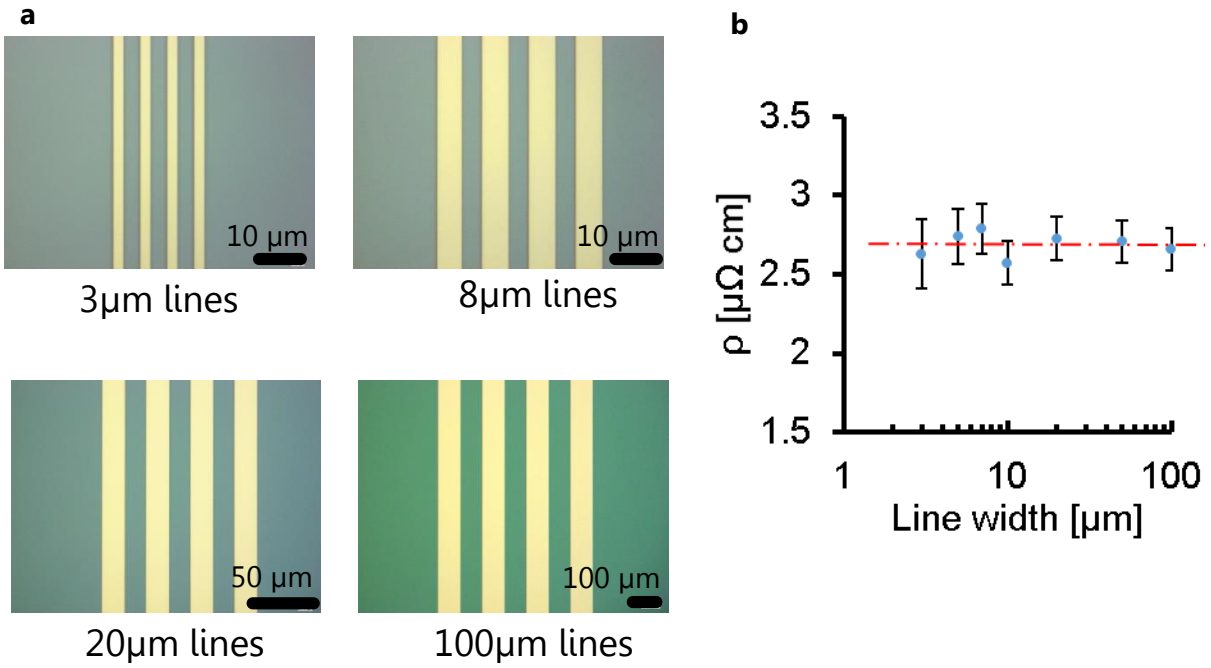


Figure 16: (a) optical microscope images of line patterning using photolithography on 1µm parylene film. (b) Resistivity of gold lines with diffeentiating line width on ultrathin film. Gold sheet resistivity is 2.4 µm·cm.

patters. After the optimization process, we could achieve reliable patterns in different line widths down to 3 µm (Figure 16*a*.).

An interesting aspect of the thin line patterning on plastic substrates is the thin film resistance after patterning. The resistivity of the gold line can be affected by the underlying layer and the metal film thickness. We evaluated the resistivity of lines with different widths from 3 µm to 100 µm and constant thickness of thermally evaporated gold of 100 nm. We can notice from Figure 16b that the resistivity of the thin lines patterned by photolithography on ultrathin parylene diX-SR is slightly higher that the bulk resistivity of gold (2.4 µΩ·cm [102]). This low resistivity of gold, albeit the fact it is deposited on thin plastic foil, enables the utilization of reliable metal layer for device fabrication.

3.5 Vapor deposition

3.5.1 Basic principles

Thin solid films can be deposited on different substrates by various techniques. Electro-deposition, chemical reactions of substances and vacuum evaporation are among the popular methods for that purpose. The specific method may be selected according to several parameters such as the target material to be deposited, substrate's properties and the required film structure and thickness. Each method has its own characteristics and advantages however in this section we will describe the important principles for vacuum deposition techniques. Vacuum deposition is a general name for processes used to deposit thin films (typically less than few mm) atom-by-atom or molecule-by-molecule [103]. The process than can be classified to physical vapor deposition (PVD) and chemical vapor deposition (CVD) depending on the vapor source. PVD processes utilize liquids or solids as the source for deposition where CVD processes implement chemical vapor precursors.
Some materials can be vaporized and deposited on substrates in atmospheric conditions but this kind of coating usually has high surface roughness due to chemical reactions between the evaporated material and air [103]. Air of course may be replaced with as inert gas, such as nitrogen, nevertheless the temperature required for deposition of metals and in-organic materials are high for practical use. The utilization of low pressure chamber for deposition hinders chemical reaction with the environmental gas and reduces the energy needed for deposition. In this section we present an introduction for vacuum deposition using physical or chemical methods, based on professional resources [103–106].

3.5.2 Physical vapor deposition (PVD)

Physical vapor deposition relates to methods for condensation of vaporized materials onto substrates in order to form thin films coating. The vaporized material is usually in the form of liquid and solid and its condensation on the substrate made by a physical manner. The process generally consists of 3 main stages correlated to the molecules of the source material: evaporation, transportation and deposition [103]. Physical vapor deposition allows large variety of materials for deposition and provides reliable and durable film coating. However the high temperatures involved require efficient cooling equipment and special care by users.

Evaporation –

Source materials can be vaporized through several methods:

- Thermal evaporation – Material is heated to elevated temperature until it reaches its vapor phase. For controlled deposition of materials, the target material is generally mounted in a heated support, e.g. a crucible, to control the material's temperature during deposition. In that method many metals, alloys, in-organic and some organic materials can be deposited as thin films.
- Electron beam PVD (EBPVD) – Thermal energy is transferred to the source material by bombardment of an accelerated electron beam. The energy increases material's vapor pressure and initiate its vaporization. This method considered to be energy efficient and provides controlled deposition rate ranging from few nm/min to several μm/min.
- Pulsed laser deposition (PLD) – A high power laser beam is focused on the source material under ultra-high vacuum condition ($<10^{-7}$ Pa). The laser beam penetrates the substance and locally releases electrons from their atoms, leading to the creation of an electromagnetic field which transferred to heat. The detailed physical phenomenon is out of the scope of this book.
- Sputter deposition – Atoms are ejected from the source material by energetic particles bombardment, driven by momentum exchange. Sputter deposition is often done with inert gas to prevent chemical reaction with the source material but some processes may also include reactive gases. For effective deposition, atomic weight of the gas should be similar to the one of the source material. Sputter deposition usually yields thin films with better adhesion to the substrate and is also available for materials with high melting points.
- Cathodic arc deposition (Arc-PVD) – In this method, an electric arc is used to heat the source material and vaporize its molecules. The arc is caused by a short high current and low voltage pulse applied to the source material carrier (cathode). The arc carries large energy density which ionize the material's molecules and release its molecules to the gas phase. In this process, additional macro-particles can be released from the material which can reduce the quality of the formed layer. To minimize this effect, pulse length should be kept short.

Transportation –

In transportation we refer to the transition of the vaporized molecules from the source material to the target surface for deposition. In most of the above methods the transport is made within a straight line of sight. During the transportation, the particles might react with other molecules to create a compound with the source material (e.g. metal oxides). In cases that the material is required to be deposited purely, minimal reaction with the medium molecules is desired.

An important consideration in vacuum deposition is the mean free path of molecules. The path of vaporized molecules travelling to the surface might be impeded by collisions with other molecules in the gas medium. The amount of molecules reaching the surface determines the deposition speed. Chemical reaction with the gas can also affect the quality and structure of the film. In order to evaluate the necessary pressure required for deposition we apply the principle of mean free path. The mean free path of molecules traveling in gas increases as the pressure decreases. For an initial number of vaporized molecules, N_0, the relation: $N = N_0 e^{-l/L}$ denotes the number of particles, N, travelling distance l without collision. The mean free path of molecules in air is about 50 cm at 25°C at 10^{-2} Pa [103]. For lower pressures only limited number of collision would occur which assures high evaporation speeds and low probability for chemical reaction of the vaporized molecules with air components. Please note that even for these lower pressures, contamination on the deposited thin film can arise from gas molecules coming in contact with the surface (and not by interacting with the vaporized molecules in air). Such contamination should be reduced by lower pressures and shorter deposition time.

Deposition –

The deposition is the final stage where the molecules of the vaporized material are condensed on the target surface due to the temperature difference between the vapors and the surface. Depending on the transport rate, the coating can be made molecule by molecule, covering the areas within line of site from the source material. In some cases, a reaction can also be taken on the surface itself simultaneously with the deposition process. One of the concerns regarding deposition on plastic substrates is the fact they usually contain organic components, known as plasticizers, or water molecules. Those components may be released from the substrate at low vapor pressures when brought into vacuum and reduce the pumping down speed causing lower vacuum levels. The release of those molecules cause residual contamination which may affect negatively on the vacuum system operation and maintenance. It is important to notice that degassing of large amount of water and organic materials from the plastic substrate due to long deposition time or high temperatures can affect main properties such as the plastic's flexibility. The phenomenon becomes more important as the plastic substrate dimensions increase. The presence of plasticizers on the surface of the plastic substrate also affects the adhesion of the thin film to the substrate. Those factors should be taken into consideration when applying the vacuum deposition technique to flexible organic materials.

3.5.3 Chemical vapor deposition (CVD)

Chemical vapor deposition is a process that provides coating of high purity materials on surfaces by a chemical reaction near or on the surface. The method allows deposition of various materials ranging from silicon to carbon nanotubes and high-k dielectric materials, in different morphologies. Where PVD which might be simpler to process and involve relatively low temperature, CVD usually provides higher purity coating and better surface coverage and uniformity [106]. Due to the application of chemical reaction, the thin films tend to have less porosity and can be used as good encapsulation layers and dielectric for semiconductor industry.

CVD processes are usually categorized by their pressure: atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD) and ultrahigh vacuum CVD (UHCVD). APCVD is used to chemically vapor coating films without vacuum condition nevertheless their quality are usually lower and the process control (e.g. gas flow and turbulences) is more complex. Most of the implemented systems today utilize vacuum mechanisms in the LPCVD (<10 kPa) and UHCVD (<10-6 Pa) configurations where the lower the gas pressure the more uniform the coating. The process of CVD typically follows the following schemes: Reactants (gas phase) -> film formation (solid) + byproducts (gas phase)

The reactants are the elements which are responsible to the chemical reaction and the film formation. The reactants are usually vaporized to their gas phase by using sublimation or evaporation. Reaction between the elements are taken above the activation energy either in the gas phase or on the solid but should be designed to be favorable on the surface to avoid nucleation and inhomogeneity of the film coverage. For that purpose, surfaces to be covered are often brought to elevated temperatures. The energy can be transferred through pure heating (thermal CVD) or via plasma bombardment which ionizes the materials, making them more reactive (plasma enhanced CVD - PECVD). PECVD takes place in lower temperatures and considered to obtain higher film density easier maintenance and cleaning. The reactants are usually carried by a non-reactive gas to the chamber (reactor) where the chemical reaction should take place.

For CVD processes, there are two kinds of reactors which the film coating can occur in: hot wall and cold wall reactors. In the hot wall reactor the chamber walls and the substrate are at the same temperature. In that configuration, many samples can be covered simultaneously and smaller temperature gradient presents in the chamber (for laminar gas flow). Nevertheless, in this case film formation can occur on the reactor walls and might fall down on the surface to create pinholes and contaminations. In the cold wall reactor, minimal deposition occurs on the walls and higher quality films may be expected. In addition, these systems are dominated by the surface temperature itself for reaction control and are easier for maintenance and cooling.

Deposition rate is one of the important factors for the film formation. The deposition rate is mainly affected by the gas supply and the reaction rate on the surface. Thus, deposition rate in vacuum systems is usually separated into two regions: mass transport limited and surface reaction limited. In the mass transport limited region the reaction speed is fast hence the flow of reactants to the surface limits the deposition rate. This process is typically characterized with high substrate temperature and affected by the gas dynamics near the surface. On the other hand, the surface reaction limited zone demonstrates low reaction rates in low temperatures and is less affected by the rate of reactants reaching to the surface. This region is considered to be better for more uniform films and step coverage.

In order to keep the reactor's low pressure and cleanliness during deposition, an exhaust system is required. The exhaust system utilizes pumps to extract the byproducts and maintain a constant pressure in the chamber. The choice of vacuum pumps depends on the process. Mechanical chemical pumps and water rings pumps are often utilized in higher process pressures (>3 kPa). For lower pressures mechanical boosters may be used. Care should be taken for the polymerization of the vacuum system due to the process byproducts and to the back-diffusion of particles form the vacuum pump back to the reactor.

3.5.4 Application to ultrathin polymer films

The application to thin plastic film should take into consideration the energy involved in the deposition process. High temperatures and high energy ions (such as in plasma enhanced deposition) can damage the polymer structure and change its surface properties. Plastics has generally lower melting and glass transition temperatures than rigid substrates such as glass or silicon substrates and hence are more vulnerable to excess heat. For example, the deposition of silicon-oxide or silicon-nitride (as common gate dielectric materials) using CVD requires high thermal energy that is not suitable to certain thin films [10]. In addition, polymeric films are soft and flexible. High energy ions, directed to the thin plastic film, can change its surface energy and roughness which are important for device fabrication and performance [35]. Ideally, the deposition on the plastic film should be done with low energy particles and at low temperatures (roughly < 100°C).

In our process we implement physical vapor deposition of gold particles and organic semiconductor in vacuum (~10^{-5} Pa) under low temperatures. The target material is heated approximately 25 cm from our substrate and particles are evaporated in direct line of sight. For the parylene diX-SR, a chemical vapor deposition is applied. The diamer (powder) is vaporized (175 °C), separated into monomers (690 °C) at high temperatures and then transported to the deposition chamber which is under room temperature. This method is used both for the substrate and gate dielectric however different systems are

used for each step. The substrate is deposited using SCS LABCOTER (Specialty Coating systems TM.) which is done under 25 Pa and allows deposition thicknesses of up to several micrometers. The gate dielectric is deposited using U-diX coating system (KISCO Ltd.) in lower pressure (~mPa) and much lower thicknesses (< 100 nm) and provides higher film quality and smoothness.

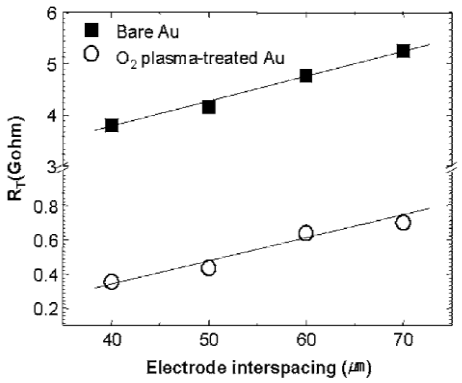
4 Short Channel Organic Transistors on 1 μm Thick Film

4.1 Contact modification

4.1.1 O_2 plasma treatment

Oxygen plasma is a known as a cleaning method in the semiconductor industry. The cleaning of surface is done by collision and chemical reaction of high energy oxygen ions with contaminations on the surface. It was found that oxygen plasma can also be an effective method for gold contact modification [107]. As shown in *Figure 17*, gold contacts can change their surface energy and work function when treated with O_2 plasma. As a result the modified contacts can be used with much lower contact resistance for device fabrication. The devices analyzed in *Figure 17* were fabricated on rigid substrates and demonstrated one order of magnitude reduction in contact resistance compared with the untreated case.

a



b

O_2 plasma treatment time (s)	Contact angle (°)		γ_S^P (mJ/m^2)	γ_S^D (mJ/m^2)	γ_S (mJ/m^2)
	Water	Diiodomethane			
0	81.2	27.8	2.4	42.7	45.1
10	39.0	19.6	26.0	35.7	61.7
30	30.3	21.3	31.9	33.8	65.7
60	26.2	19.4	33.8	33.9	67.7
120	13.6	23.0	39.8	31.7	71.5
240	26.4	20.0	33.8	33.7	67.5
480	31.3	20.0	31.0	34.4	65.4

Figure 17: (a) Change in contact resistance and (b) surface energy of O_2 treated gold electrodes [107].

Contact modification is necessary for our bottom contact transistors as a high contact resistance value is observed in the device characteristics. As a comparison, top contact devices fabricated with the same conductor and gold contacts present contact resistance of only 1.5 kΩ·cm compared with the ~50 kΩ·cm achieved in our fabrication of bottom contact structure. We evaluated modification with O_2 plasma by introducing 50 Watts of plasma treatment for 1 minute on the patterned gold contacts.

The time and power of plasma treatment were carefully chosen in light of the use of flexible plastic substrates. It is well know that exposure to plasma affects the surface of plastic foils, making them rougher and Increases their surface energy [108–110]. Increase of surface energy is disadvantageous for deposition of organic small molecules using

evaporation, which is used in this study. The treatment of plasma is the most effective when introduced just before the semiconductor deposition. In the parylene, top gate-bottom contact case, the channel area consists of thin plastic film. Hence, special care should be considered when treating the channel area with O_2 plasma. Because the surface energy of the polymer changes in relation to the exposure time, we had to choose relatively short time that will change the contacts but not degrade the underlying surface by reducing its surface energy. Treatment of 1 minute by 50 Watts of O2 plasma is relatively short treatment with low energy to prevent significant degradation of the substrate.

In *Figure 18* we present the results of device characteristics after oxygen plasma treatment. The transfer curve shows high OFF current at V_{GS}=4V of approximately 10 nA which results in poor device's ON/OFF ratio. Gate leakage current shows good characteristics with less the 100 pA of maximum leakage. As we utilize the top-gate structure, the gate dielectric is not affected by the oxygen treatment. Transistor shows

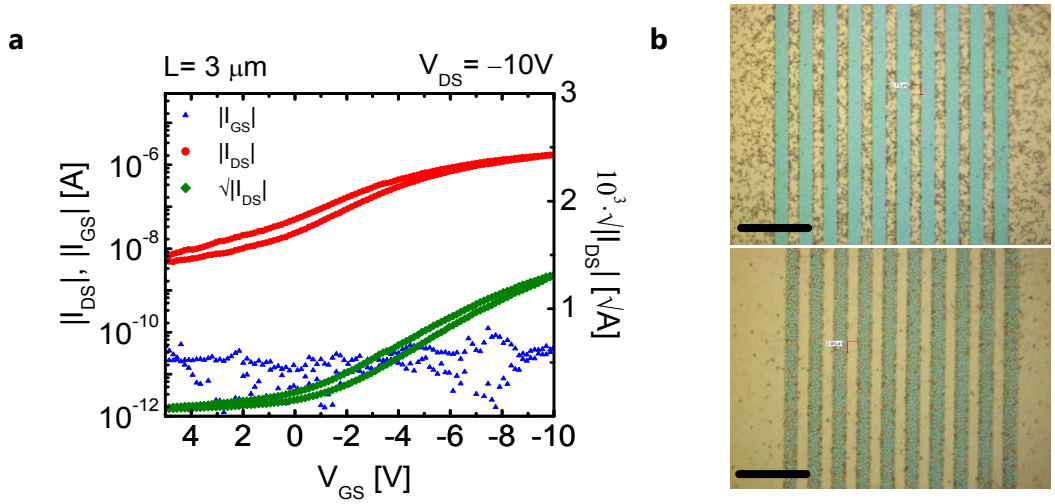


Figure 18: (a) transfer characteristics of O_2 treated transistor. Treatment was done after gold evaporation to modify the contacts work function. Typical mobility was ~10^{-3} $cm^2/V{\cdot}s$. (b) optical microscope images of channel area of control (top) and treated (bottom) transistors. Transistors' width to channel length is 160. Scale bar is 10 μm.

low mobility of ~10^{-3} cm^2/Vs. The low mobility reveals that the oxygen treatment, although short and low energy, still affects the semiconductor growth in channel and degrades its quality during formation. In *Figure 18b*, from the optical microscope image we notice clear change in semiconductor area which implies on its formation difference.

4.1.2 Pentafluorobenzenethiol (PFBT) self-assembled-monolayer (SAM)

Self-assembled monolayers are a well-established and powerful way to change surface properties [111–117]. Using a 'head' chemical group a monomolecular functional films

can be chemically bonded to the surface. With a proper 'tail' group, the self assembled monolayers can create new surface properties such as hydrophobicity, electrical work function, or change device threshold voltage.

Thiol-based SAM is a well known method to modify metal surfaces [118–120]. Aromatic thiols, and especially the benzenethiolate group is one of the simplest form for effective modification of gold [121,122].The benzenethiol group (*Figure 19*a) is dissociatively adsorbed on metal surfaces via the sulfur atom to form a tilted

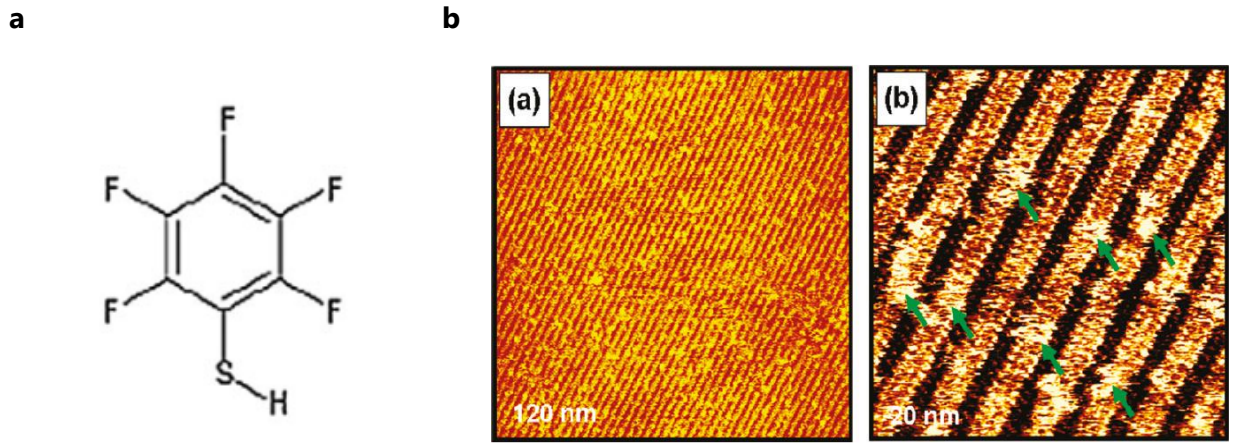


Figure 19: (a) Pentafluorobenzenethiol chemical structure and (b) scanning tunneling microscope (STM) image of the SAM modified gold surface. Long, ordered SAM chains are observed in accordance to the gold atomic structure [123].

benzenethiolate (C_6H_5S) group. It is considered controversial whether benzenethiol forms a well ordered chains on top of Au (111) however recently Kang et al. [123] demonstrated that pentafluorobenzenethiol can obtain long ordered structure on top of gold surfaces, following its lattice dimensions (*Figure 19*b). The presence of PFBT SAM changes the work function of gold from −5 eV to −5.5 eV [124]. When using the DNTT semiconductor with a work function of −5.4 eV, this change can improve the charge injection of holes from the metal to the semiconductor. It was reported that PFBT can also positively change transistor performance with C_{10}-DNTT semiconductor on rigid substrates while reducing their contact resistance [125].

Here, we try for the first time to apply the PFBT on flexible substrate for changing gold properties. One uncertainty is the stability of the plastic foil during deposition. The film might change its properties or be delaminated from the supporting substrate. Another concern is the effectiveness of PFBT in case of not ordered gold films on plastic foils. The thermally evaporated gold on flexible substrate does not form in a perfect (111) orientation and hence the change in work function should be independently evaluated on the flexible substrate.

We applied different recipes of PFBT on gold contacts deposited on ultrathin parylene film, before the semiconductor evaporation. We measured the device mobility as a function of the formation conditions. We expect that upon modification of the gold work

function we will be able to see an improved device mobility. We prepared a 1mM PFBT solution in ethanol and applied it to the surface in various conditions. We differentiate the application time and temperature between 1 to 6 hours and 25°C to 75°C respectively. The mobility optimization procedure is summarized in *Figure 20*a. We observe that the SAM formation process at room temperature is in any case worse than the formation at 75°C. This fact is due to the additional energy needed for the reaction between the benzenthiol and the gold atoms to form the chemical bond. We found that the best mobility of 0.12 $cm^2/V{\cdot}s$ could be achieved after 2 hours at 75°C. Device uniformity was also very good under those conditions. Application for longer time resulted in less uniform and worse mobility devices. This observation is in correlation with previous report on ordered gold surfaces that showed the best ordered structure of the SAM at 2 hours and that longer time obtains less ordered structure [25].

In b we demonstrate the effect of the optimized conditions on transistor performance by its transfer curve. We applied 1mM PFBT SAM for 2 hours at 75°C on transistors with channel length of 6 μm and parylene gate dielectric of 200 nm. The SAM was applied just before DNTT evaporation in the tested sample. Both the control sample (no PFBT) and the test sample went to a similar process except the SAM formation. We can clearly observe how the SAM positively affects device characteristics in terms of saturation current and device's ON/OFF ratio. Average device mobility improved by 1 order of magnitude from 10^{-2} $cm^2/V{\cdot}s$ to 0.1 $cm^2/V{\cdot}s$.

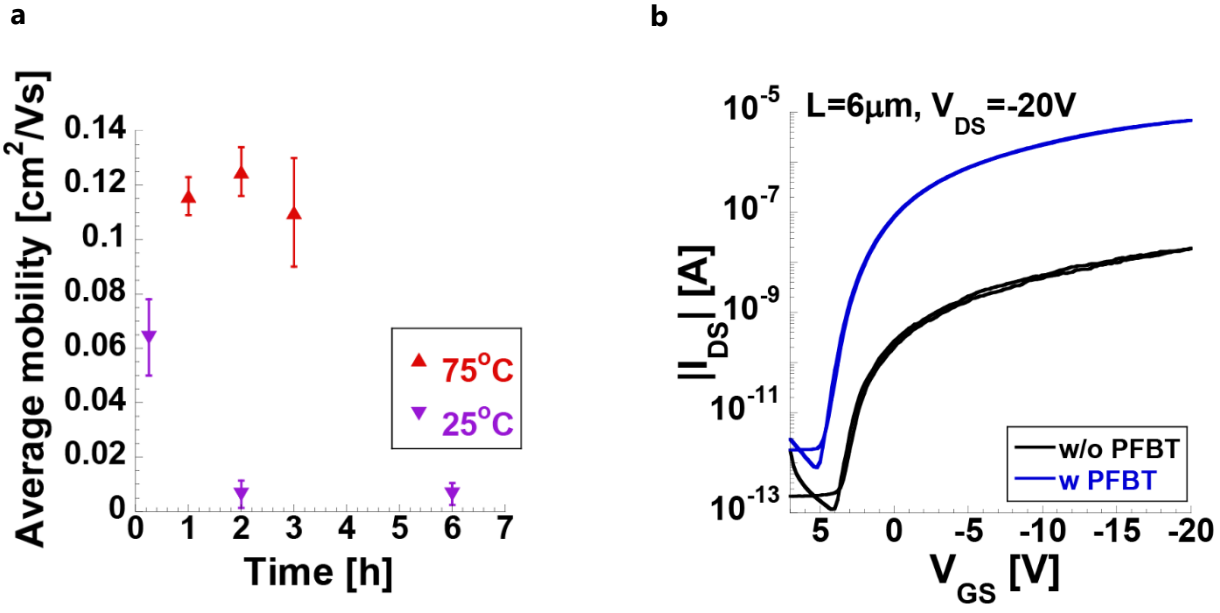


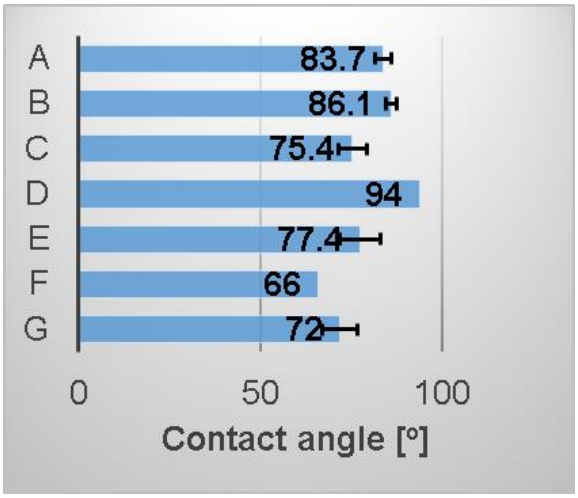
Figure 20: (a) Mobility optimization of PFBT treatment by time and process temperature. Best results are observed after 2 hours in 75°C. (b) Comparison between treated and untreated transistor showing substantial increase in On/Off ratio and saturation current.

Besides the work function modification, previous reports has shown that semiconductor alignment is a crucial property for good device performance [35,51]. The alignment on high surface energy substrates tend to be in 'lying' formation which is perpendicular to the desired holes transport direction. Especially deposition of pentacene on gold shows very low deposition angles, even compared with silver or other metals [51]. This orientation causes larger injection barrier at the interface and another injection barrier when the holes move from the contact area to the channel on the top gate structure. Thus, maintaining constant and relatively low surface energy at all transistor regions is a desired property for good device characteristics.

Here we investigate whether the PFBT can modify the surface energy of gold surfaces for the first time. We evaluate this property by measuring the water contact angle on the

a

A	parylene, no treatment
B	parylene, annealed @ 120C
C	Gold
D	Gold w/ PFBT
E	Gold w/ PFBT after 1 week
F	parylene w/ PFBT no wash
G	parylene w/ polyimide



b

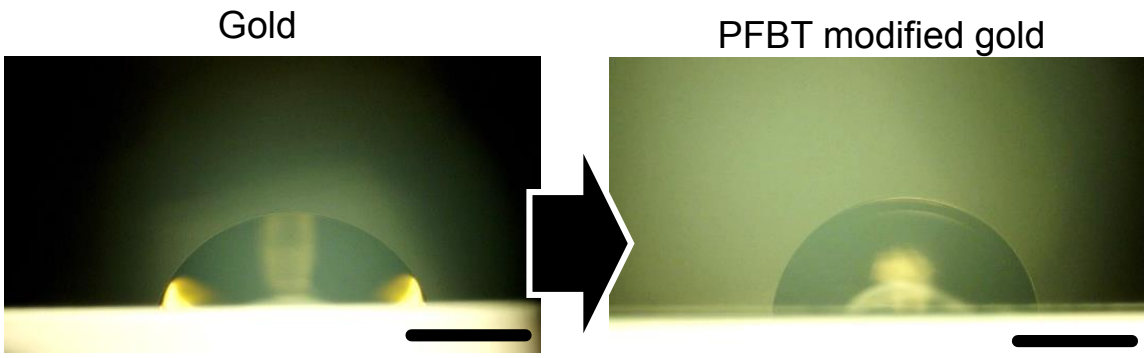


Figure 21: (a) Water contact angles of treated and untreated parylene and gold surfaces. (b) Microscopic image of the PFBT SAM treated gold surface, on ultrathin parylene film, compared with the untreated one.

surface and compare it to different surface modification methods and to the untreated parylene diX-SR layer. We measured the contact angle of seven different surface as

featured in the left inset of *Figure 21*a: (A) as deposited parylene diX-SR; (B) annealed parylene diX-SR for 1 hour at 120°C; (C) as deposited gold film on parylene diX-SR; (D) gold film on parylene diX-SR, modified with the optimal recipe of PFBT; (E) same sample as D, after 1 week; (F) parylene diX-SR treated with the optimal recipe of PFBT, no rinse; (G) parylene diX-SR modified with spin coated polyimide. The contact angle was measured by dropping 1 μl of ultrapure water on top of the tested surface and taking a microscopic image using a perpendicular microscope lens (*Figure 21*b). Later, the contact angle is measured and calculated by image analysis. The results are presented on the right panel of *Figure 21*a in correlation to the sample alphabetic order.

Several conclusions can be drawn from the above contact angle results. First, PFBT modifies gold to become more hydrophobic. The contact angle increased from 75.4° on the untreated gold to 94° on the treated one. This increase in hydrophobicity may contribute to the semiconductor molecular alignment during evaporation. Additionally, parylene diX-SR annealing slightly reduces the surface energy of the substrate. Other treatments of parylene diX-SR we experimented, namely polyimide spin coating and PFBT without rinse, increased surface energy and reduced the water contact angle. We can conclude that PFBT treatment showed excellent results in terms of mobility improvement and surface energy. The treatment reduces contact resistance by modifying the metal work function and by increasing contact hydrophobicity. By finding the optimal recipe for SAM formation, mobility has improved by at least 1 order of magnitude compared with the untreated samples. Additionally, the treated samples show good uniformity.

Pentafluorobenzenethiol treatment showed very promising results in device characteristics, both mobility and uniformity. We considered several other additional treatments to estimate their effect on transistor's performance.

4.1.3 PFBT and substrate heating

Annealing during semiconductor deposition was shown to improve organic field effect transistors performance [70,85]. The thermal energy delivered to the substrate during deposition improves the molecular orientation and has the potential to improve charge transport mechanisms. We experimented devices with PFBT modification with substrate heating during semiconductor deposition. The addition of PFBT for work function modification and the annealing during semiconductor deposition have the potential to improve further the transistor performance.

Previous reports showed that the optimal annealing temperature is between 70°C-80°C for mobility improvement of C_{10}-DNTT based transistors [85]. We have fabricated OTFT with channel length of 2 μm and soaked them in 1mM PFBT solution for 2 hours at 75°C. Immediately after this process step, we rinsed the sample with ethanol and brought into the vacuum chamber for DNTT thermal evaporation using shadow mask. The

substrate was heated inside the chamber up to 75°C before the evaporation has started. During the entire evaporation process, the temperature was fixed to this value. In the end of the evaporation, the annealing was turned off and the substrate left for cooling down in the vacuum chamber for approximately 1 hour. Following this step, parylene diX-SR gate dielectric of 60 nm was vapor deposited in high vacuum and the gate electrodes were deposited.

The results of the substrate annealed sampled are presented in *Figure 22*. The transfer characteristics show reasonable ON/OFF ratio of 10^5, low leakage current (< 100pA) and no hysteresis. Nevertheless, device mobility was not changed compared with the untreated sample and devices obtained mobility of ~10^{-2} $cm^2/V{\cdot}s$. The only PFBT treated devices, could show higher mobility compare to the substrate annealed ones. In *Figure 22*b, optical images of the channel area of a thermally annealed sample and the control are presented. We can observe denser semiconductor aggregation near the channel injection area. We speculate that this aggregation might reduce the effect of the PFBT treatment and reduce the mobility values back to ~10^{-2} $cm^2/V{\cdot}s$. In summary, although the transistor shows good transfer characteristics, the mobility of the device could not be improved by thermal annealing during deposition.

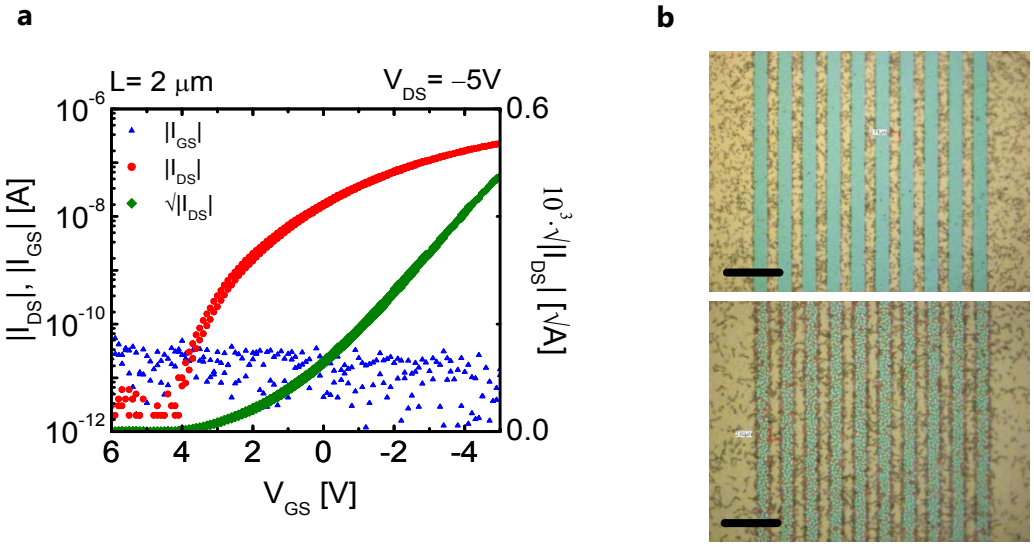


Figure 22: (a) Transfer characteristics of thermally annealed transistor during semiconductor evaporation. Typical mobility was ~10^{-3} $cm^2/V{\cdot}s$. Transistors' width to channel length is 25. (b) Optical microscope images of channel area of control (top) and annealed (bottom) transistors. Scale bar is 10 μm.

4.1.4 PFBT and O_2 plasma treatment

Oxygen plasma is a common process in the semiconductor industry. It can be used for surface cleaning or functional modification by introducing O_2 molecules to the surface. In the previous sections we described that O_2 plasma can also modify gold work function and improve transistor characteristics on rigid substrates. The same process did not work well on the flexible substrate and could not improve significantly device mobility (although it did not degrade device performance). Another option for using O_2 plasma is for surface cleaning. Due to the use of very sensitive ultrathin films, our material selection for cleaning photoresist and other residues is limited. Hence, cleaning with short O_2 plasma could be an interesting approach for surface cleaning.

In this section we test the effect of a combined treatment of plasma and PFBT for device optimization. First we describe an O_2 treatment step before gold evaporation and just after photoresist patterning to clean surface and improve adhesion of the gold films. The treatment was of 50 Watts for 1 minute to prevent hard baking of the photoresist.

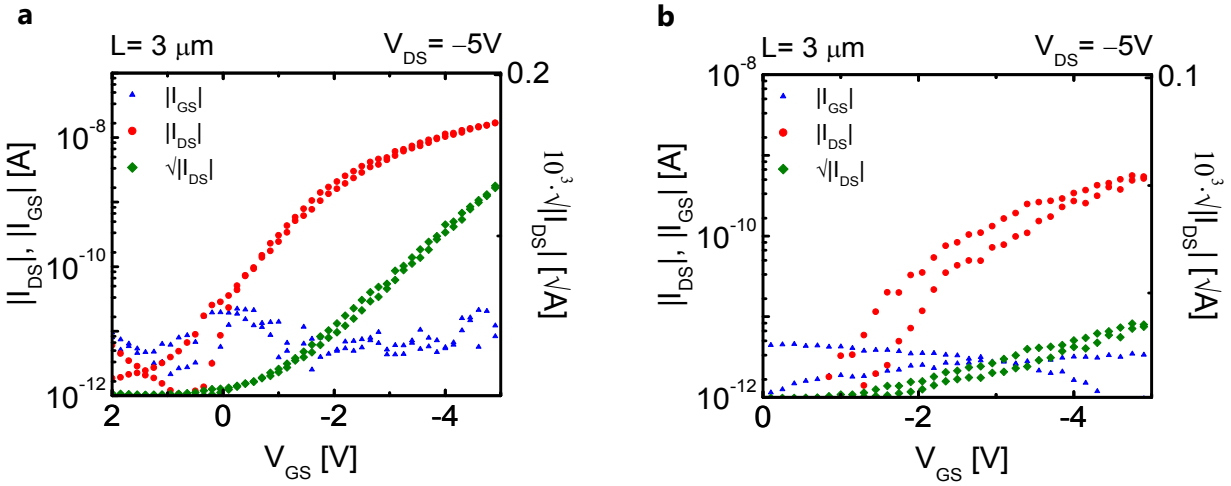


Figure 23: Transfer characteristics of O_2 treated transistors (a) before and (b) after gold deposition. Both samples were treated with PFBT SAM on the gold contacts. Typical mobility was ~10^{-4} $cm^2/V{\cdot}s$ and ~10^{-6} $cm^2/V{\cdot}s$ respectively. Transistors' width to channel length is 160.

Immediately after the O_2 treatment we brought the samples to a vacuum chamber to thermally evaporate 30 nm of gold. The final patterning was completed by lift-off technique. Following the gold patterning we formed a PFBT SAM on the gold contacts by soaking the sample for 2 hours at 75°C in 1mM PFBT solution. Parylene gate dielectric of 60 nm and gate electrode were deposited to complete the structure. The second sample was treated by O2 plasma only after the pattern definition by lift-off. The treatment was similar – 50 Watts for 1 minute – and was followed by PFBT formation with the above recipe. Next fabrication steps were done in tandem with the first sample. Transistor

characteristics of the two samples are plotted in *Figure 23*. In *Figure 23*a, the transfer curve of the sample that was treated with O_2 before gold deposition is presented. We can detect low saturation current but reasonable leakage current for this device. The ON/OFF ratio of this device is 10^4. Calculated saturation mobility from the $\sqrt{I_{DS}}$ linear plot is ~10^{-4} $cm^2/V{\cdot}s$ and is 2 order of magnitude lower than the bottom contact transistors with no treatment. In *Figure 23*b, the transfer curve of transistors treated with O2 plasma after gold deposition is plotted. Here we observe relatively large hysteresis and low saturation current, less than 1 nA. As a result, saturation mobility of only ~10^{-4} $cm^2/V{\cdot}s$ could be achieved. We note that in both cases, a significant negative shift in threshold voltage can be identified. Oxide modified surfaces often show this negative tendency as more negative oxygen ions are accumulated on the surface. In our case, this phenomenon cause a shift in the threshold voltage of the devices.

4.1.5 PFBT and ultraviolet-ozone treatment

Ultraviolet-ozone (UV-O_3) surface treatment is another common cleaning technique in the micromachining industry. Together with UV irradiation, the O_3 molecules that are introduced to the surface causes decomposition of organic contaminations. This treatment can be done in relatively wide range of energies and create less damage on the cleaned surface. This fact is of high importance when in comes to application on thin and flexible substrate. As on can deduct form *Figure 24*a, the UV ozone process can also modify gold contacts on glass substrates. After treatment time of approximately 30 minutes, a change of −0.7 eV in the work function of gold can be detected [126]. Bringing gold work function to these values would be beneficial for holes injection to the semiconductor [127].

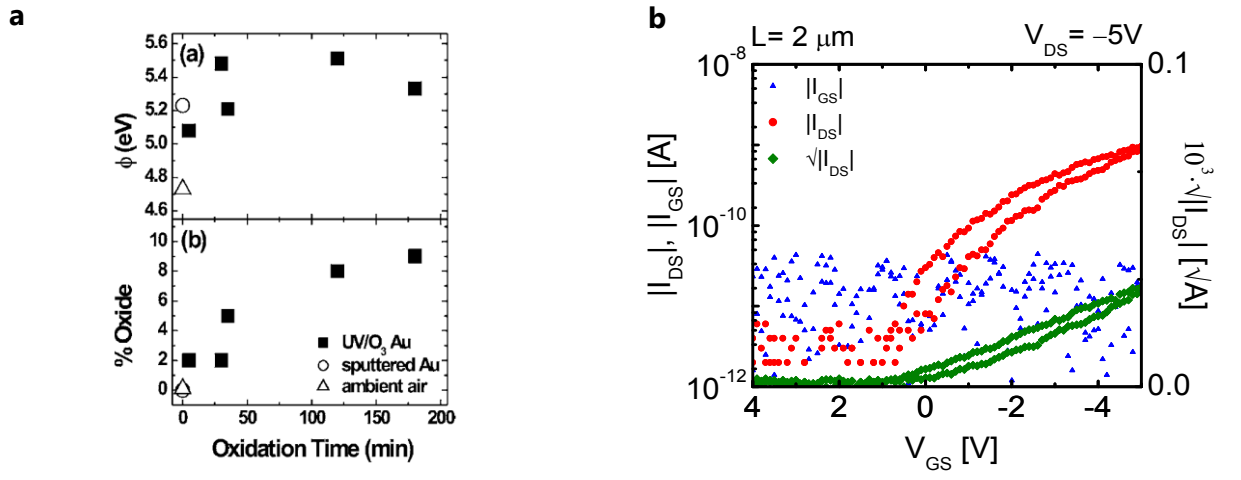


Figure 24: (a) Effect of UV-O_3 treatment on gold work function. Adopted from [126]. (b) Transfer characteristics of UV ozone treated transistors, just before PFBT SAM formation. Typical mobility was ~10^{-5} $cm^2/V{\cdot}s$ and transistors' width to channel length is 250.

In this section we will try to apply the UV-O_3 treatment on gold which is patterned on flexible, ultrathin parylene diX-SR film.

In order to apply the UV ozone process to ultrathin films, we should consider the time and energy of treatment. Too long time of processing would cause a significant change in the properties of the film and undesired device characteristics due to low surface energy. We applied the procedure after the patterning of gold contacts using photolithography and 'lift-off' techniques. Process parameters were chosen to provide low energy to the surface with 5 minutes exposure [128]. Immediately after the UV exposure, a PFBT SAM was formed at 75°C for two hours (1mM). The transistors fabrication was completed by evaporating 35 nm of DNTT, 60 nm of parylene gate dielectric and 30 nm of gold gate.

The transistor's characteristic in *Figure 24*b shows a device with very low saturation current and mobility, large hysteresis and negative threshold voltage. ON/OFF ratio was found to be roughly 10^3. Saturation mobility was in the range of 10^{-5} $cm^2/V{\cdot}s$ and threshold voltage of -1V. The negative threshold voltage is caused by the presence of negative ions on the surface. The UV-O_3 treatment was found to be not effective for improving device characteristics under those conditions. Apparently, even a very short treatment by oxygen obtains a negative effect on the semiconductor formation which results in worse device performance.

4.1.6 Triptycene

Surface energy is a very important factor for vertical alignment of organic semiconductor. Low surface energy leads to better alignment of molecules for charge transport within the semiconductor and increases mobility [35]. Moreover, changes in surface energy of the target surface create border regions where misalignment of the organic molecules hinder charge transport. A constant and low surface energy is thus desirable for deposition of organic semiconductor. In the top contact structure this can be easily achieved as the semiconductor is patterned solely on the gate dielectric or substrate. In case a hydrophobic surface can be obtained, either by inherent properties or by surface modification, high carrier mobilities can be achieved. However, in the bottom contact structure this property is difficult to obtain. The semiconductor, by definition, is deposited on conductive electrode and gate dielectric/ substrate which generally have different surface energies. A barrier in injection between the two different regions can cause lower mobilities and worse device performance.

Recently, triptycene, was demonstrated as a promising method to modify bottom gate-top contact transistors to improve mobility [60]. The modified gate dielectric shows very high hydrophobicity (water contact angle >100°) and triptycene can be deposited uniformly on wide variety of surfaces. This ability of being formed on any surface by thermal evaporation may be an important factor in changing and unifying the surface

energy of both the contacts and the gate dielectric and cerate an identical, hydrophobic surface for semiconductor deposition in the bottom contact structure. In this set of experiment we want to evaluate triptycene as a surface modifier for enhancing transistor performance.

We designed the experimental procedure to check triptycene in the following forms: deposition on top of the contacts and channel area, deposition after PFBT treatment and deposition before PFBT SAM formation. As a control sample, we fabricated PFBT SAM contact modified transistors. All triptycene coating were conducted in the following manner: the sample is brought into a vacuum chamber and 5 nm of triptycene is thermally evaporated on the surface. After evaporation the samples were brought to a nitrogen glove box and annealed at 120°C for 1 hour [60]. PFBT SAM treatment was identical for all samples, with 1mM PFBT solution mixed in ethanol and left for 2 hours at 75°C. Samples were thoroughly rinsed with ethanol after the soaking process. All transistors had similar

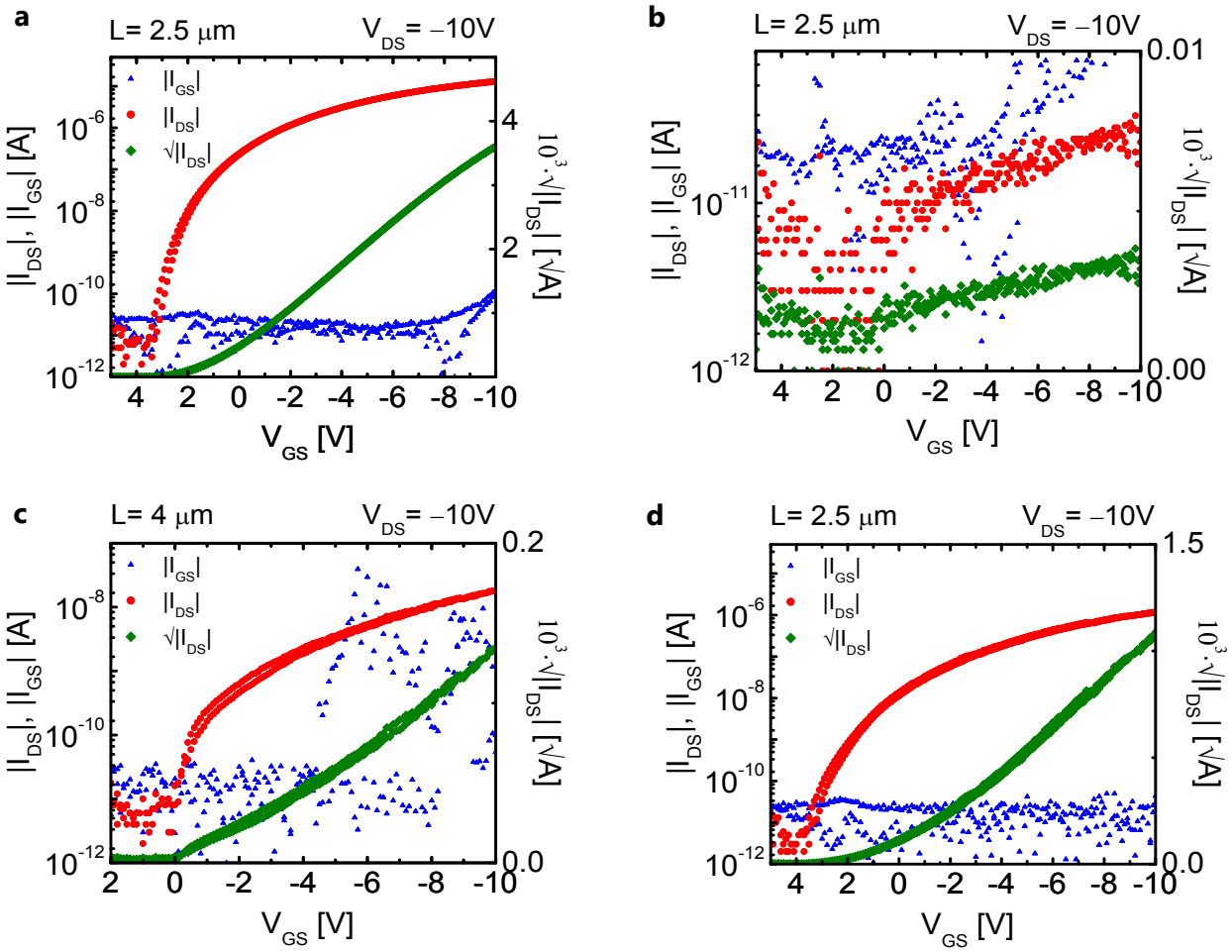


Figure 25: Effect of triptycine treatment on transistors in bottom contact structure. (a) Transfer curve of PFBT treated transistor (control). (b) Transfer characteristics of triptycine treated transistor after gold contact patterning. (c) Effect of triptycine on PFBT treated transistor and (d) effect of PFBT SAM on triptycine treated transistor.

channel dimensions (2.5 μm – 4 μm) and same gate dielectric thickness (80 nm) they were formed during the same process.

In *Figure 25* the transfer characteristics of all tested samples are presented. *Figure 25*a shows the control sample, treated with only PFBT SAM on the gold contact area. Good device characteristics with low hysteresis and high ON/OFF ratio of 10^7 could be achieved. Compared with the control sample, devices that were treated with only triptycene (*Figure 25*b) show very bad device characteristics. Saturation current was lower than the leakage current yielding to almost no difference between ON and OFF current of transistors. This result is related to the large band gap of triptycene which practically creates charge injection barrier even when deposited in very low thicknesses. When applying triptycene on gold contacts which are already modified with PFBT SAM (*Figure 25*c) we can detect a clear improvement from the case of the bare gold contacts treated with triptycene. ON/OFF ratio increased to 10^3 and saturation mobility could be determined by the $\sqrt{I_{DS}}$ curve (green) to be 10^{-4} $cm^2/V{\cdot}s$. The best performance among the triptycene treated transistors could be achieved by applying PFBT SAM after triptycene evaporation. The results are plotted in *Figure 25*d. No hysteresis and high ON/OFF ratio of 10^6 could be achieved in this manner. Saturation mobility was calculated to be 10^{-2} $cm^2/V{\cdot}s$ from the square roof of the absolute value of the drain-source current.

In summary we can conclude that the treatment of triptycene as a modifier for gold contacts does not improve device characteristics compared with PFBT SAM modified contacts. This result can be related to the fact the triptycene has a wide band gap and is used as a hole blocker for charge injection from the metal to the semiconductor. Even though the formed triptycene layer was only 5 nm (2-3 monolayers), which is the thinnest layer to obtain reliable stratum, it could affect negatively the charge injection and degrade transistor performance. The improvement in surface hydrophobicity could not compensate the blocking properties of this layer when deposited on the gold contacts.

4.1.7 Summary

We have successfully improved device's saturation mobility, uniformly and reproducibly, by gold contacts surface modification. In this chapter we experimented several ways to improve charge injection between the gold contacts and the semiconductor in the bottom contact structure. The injection barrier is considered higher in the bottom contact structure because of work function and different surface energies of the metal and the gate dielectric. This modification was found to be more challenging than in the rigid substrate case. We applied several methods: oxygen plasma treatment, self assembled layer formation (PFBT), UV-O_3 treatment and surface modification using triptycene. Oxygen treatments (O_2 plasma and UV-O_3) were successfully reported as work function modifier on glass or silicon substrates. However, when we applied those methods for the ultrathin film case those treatments degraded transistor performance. We relate this

observation to the change those treatments are causing to the channel, such as increasing surface roughness and energy, in contrast to the rigid substrate case. The application of triptycene, which was successfully demonstrated to improve OTFT's mobility in the top contact structure, was also not successful to improve the performance in the bottom contact architecture. Triptycene improves surface hydrophobicity and forms a uniform

Table 1: Summary of mobility optimization with different surface treatments methods. The results are presented in relation to the untreated sample mobility.

Sample	PFBT	O_2[1]	Sub. heating[2]	UV ozone[3]	Triptycine[4]	Relative Mobility*
1						1
2	✓					10
3	✓		✓			1
4		✓				1
5	✓	✓	✓			N/A
6	✓	✓				10^{-4}
7	✓			✓		10^{-2}
8	✓		✓	✓		10^{-2}
9					✓	10^{-4}
10	✓				✓	10^{-1}

[1] 50W 1min [2] 75°C during DNTT evaporation [3] 5 minutes [4] 5 nm by evaporation

layer on top of the contacts and the channel area, however it creates a hole blocking layer even when deposited in only few monolayers. The treatment that showed the best and most significant performance improvement was pentafluorobenzenethiol (PFBT) self assembled monolayer on top of the gold contacts (*Table 1*). The PFBT process was found to be compatible with the ultrathin parylene diX-SR substrate and effectively changed work function of the gold contacts. It was also shown that the PFBT reduces the surface energy of gold and contribute to the vertical alignment of the organic semiconductor on

top of the contacts. After our optimization process, the utilization of PFBT SAM improved the mobility of devices by one order of magnitude compared with the untreated samples and with other treatments. Combination of PFBT treated devices with other treatments did not improve further the results as one can conclude from *Table 1*.

4.2 Electrical device characterization

4.2.1 Optimized structure and process

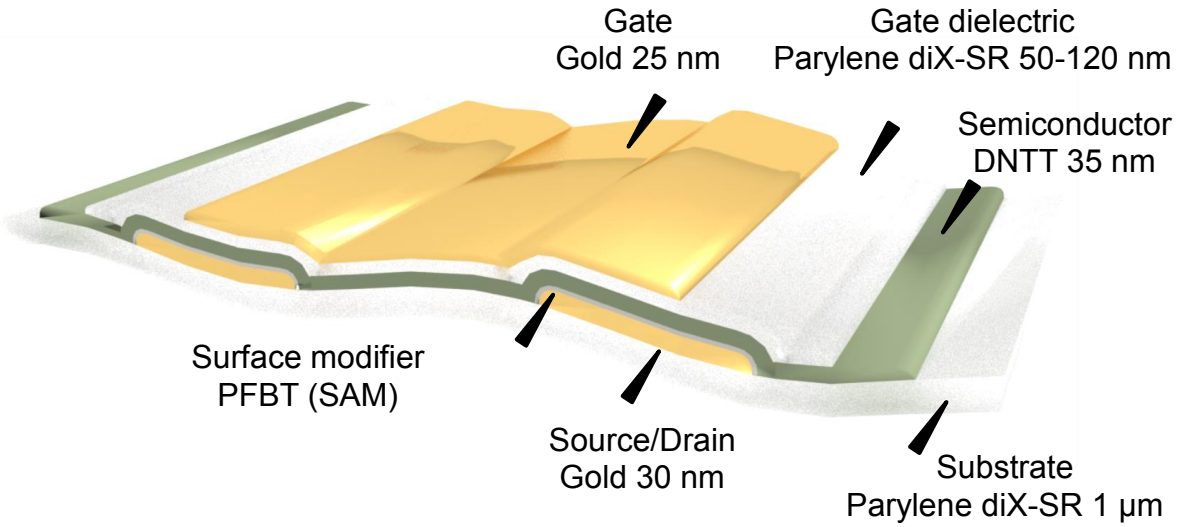


Figure 26: Schematic of transistor structure in top gate-bottom contact architecture. The thicknesses represent the optimal conditions for achieving the highest mobility, given those structure and materials.

Following the above optimization procedures, we have successfully formulated a fabrication process to obtain high performance short channel organic transistors in the bottom contact layout on ultrathin plastic foils. Layer thicknesses were optimized to achieve the highest mobility. The process obtains reliable and reproducible results and is compatible with large area fabrication techniques. Device structure is described in *Figure 26*. Here we bring the optimized design fabrication process:

Optimized fabrication process

1. Formation of 1 µm thick parylene diX-SR on bare Si-SiO_2 wafer using CVD.
2. Device annealing for 1 hour at 120°C.
3. Photolithography patterning of source and drain mask (ZEON ZPN 1150-90).
4. Thermal evaporation of 30 nm gold layer.
5. Lift off using organic solvent (ethanol/ acetone).
6. Soak in 1mM PFBT in ethanol solution for 2 hours at 75°C.
7. Rinse with ethanol.

8. Thermal evaporation of semiconductor (DNTT), 35 nm.
9. CVD formation of parylene diX-SR as gate dielectric.
10. Device annealing for 1 hour at 100°C.
11. Photolithography patterning of gate mask (ZEON ZPN 1150-90).
12. Thermal evaporation of 30 nm gold layer.
13. Lift off using organic solvent (ethanol/ acetone).

After the above fabrication process, transistors are ready to be used and functional with saturation mobility of 0.1-0.2 $cm^2/V{\cdot}s$. As a comparison, top contact devices with parylene diX-SR gate dielectric obtain only slightly higher mobility of average 0.5 $cm^2/V{\cdot}s$ [60] which implies on the structure effectiveness to create short channel transistors with good

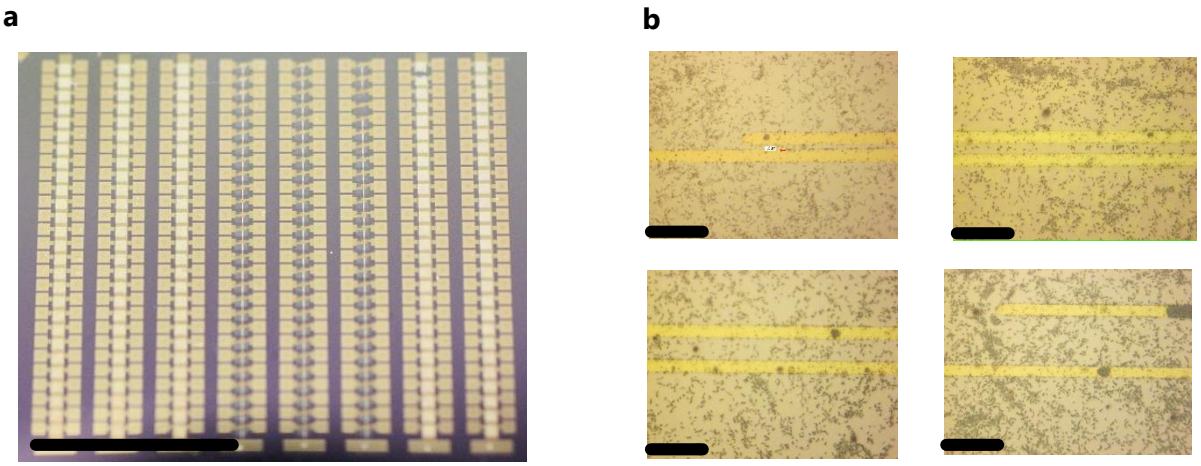


Figure 27: (a) Optical micrographs of the fabricated transistor array. Scale bar is 1 cm. (b) Representative channel dimensions of the bottom contact transistors. Plotted are transistors with channel lengths of 2-20 μm, channel width is fixed to 200 μm. Scale bar is 10 μm.

mobility.

4.2.2 Transfer characteristics

To evaluate further device performance, uniformity and output characteristics we fabricated large number of transistors in the area of 2.5x2.5 cm^2 (*Figure 27*a). Transistors with different channel lengths were fabricated on the same batch. Channel length dimensions are demonstrated in *Figure 27*b, plotting devices with 2-20 μm (largest channel was 48 μm). Channel width was determined in all cases to 200 μm. 'Finger' width, which determines the line width of the source and drain, was set to be 3-4 μm. Small finger size allows us to reduce the gate-source overlap and reduce the parasitic capacitance of the transistor. As mentioned earlier the parasitic capacitance of transistor is an important factor in determining its cutoff frequency. We utilized the above recipe for transistor fabrication where the gate dielectric thickness was determined to be 120 nm. We measured transistors output and transfer curves using parameter analyzer and extracted their main features such as mobility, threshold voltage, ON/OFF ratio, leakage current etc.
In *Figure 28* we plot the transfer characteristics of 5 different transistors with varying channel length from 2 μm – 48 μm. The measurement was done while VDS was kept at −8V and VGS was swept from 5V to −8V and in reverse. We could achieve saturation properties for the transistors at low operation voltage (<10V) thanks to the utilization of only 120 nm parylene diX-SR as gate dielectric. When we examine device properties, first we note that the leakage current in our devices (blue) is smaller than 100 pA in all cases. The low leakage current is a property of the parylene diX-SR which presents good current blocking characteristics even at relatively small thicknesses. The leakage is, as expected, independent with channel length and mainly affected by the small 'finger' dimensions we set for the source and drain. Another important parameter we note is the low OFF current of transistors of approximately 1 pA. The low current implies on the purity of the semiconductor and the good switching properties of the device. The low OFF current leads to ON/OFF ratio larger than 10^5 which are excellent values for transistor switching applications. Our transistors also show no hysteresis which results from the purity of the dielectric and the dielectric-semiconductor interface. All transistors show good match to the conventional transistor model and $\sqrt{|I_{DS}|}$ (green) presents linear dependence on the gate voltage. Considering the different channel lengths, we calculated average saturation mobility of 0.2 $cm^2/V{\cdot}s$.

We summarize the transfer characteristics in *Figure 29*. On the left panel we plot transistor's transfer characteristics for different channel length. Channel width is 200 μm for all devices. We can notice how the ON current of transistors nicely scales with the ratio W/L (channel width to channel length) according to the saturation equation. When the transistors channel length decrease by a factor of 2, the saturation current increase by the same factor. The leakage current for all device is consistently lower than 100 pA. ON/OFF ratios of the devices are determined by the scaling of saturation currents and are in any

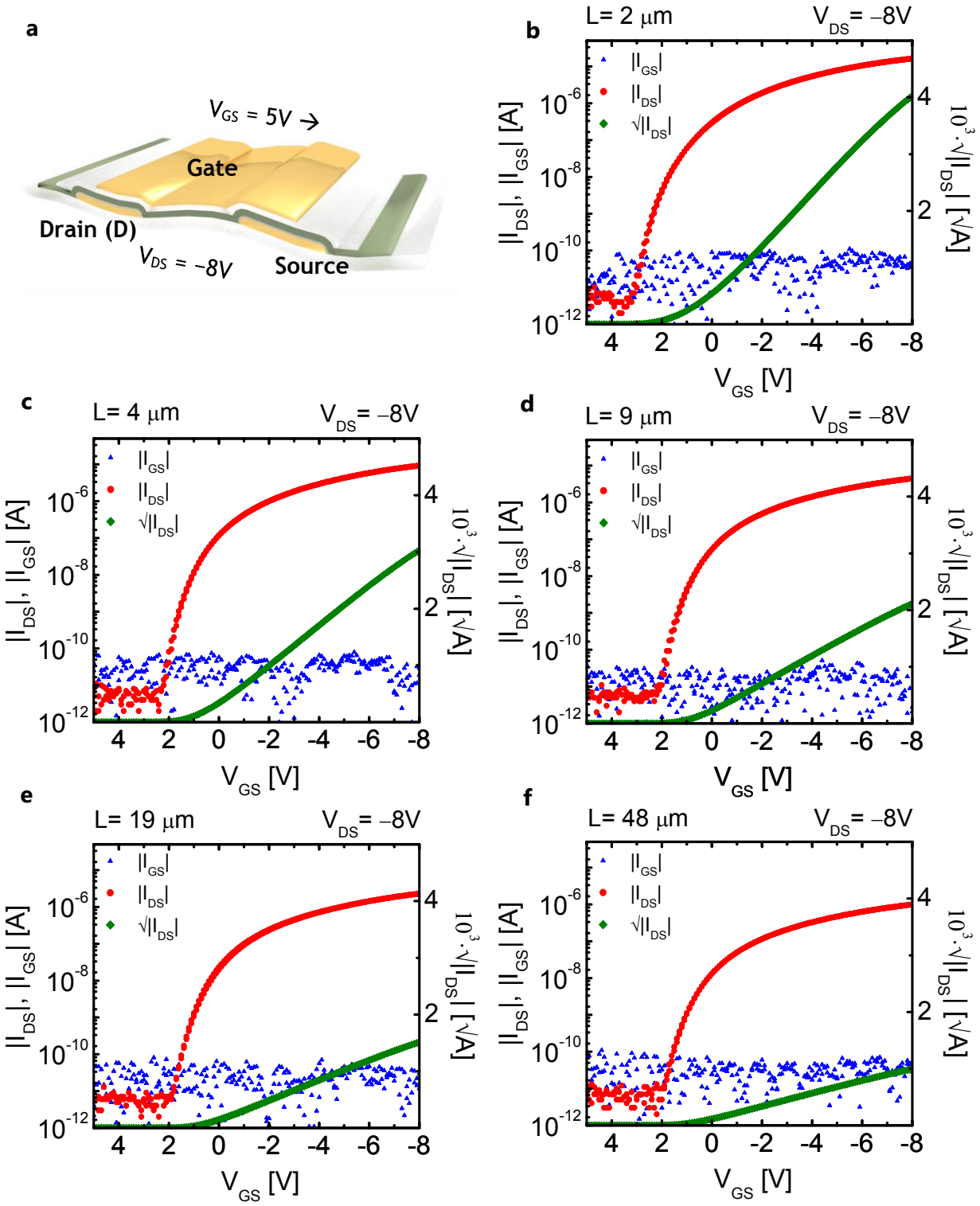


Figure 28: (a) Illustration for contacts and voltage applied on the ultrathin film transistors. (b)-(f) Transfer characteristics of bottom contact transistors with varying channel length from 2-48 μm. I_{DS} (red) and I_{GS} (blue) are plotted against the left logarithmic scale while the square root of I_{DS} (green) is plotted linearly on the right scale.

case larger than 10^5. In the short channel case, the ratio can easily reach to 10^7 with a relatively low W/L value of 100. In *Figure 29*b an accumulative representation of the average mobility (red) and threshold voltage (blue) is plotted. The plot represents approximately 50 devices with different channel lengths. We can see that the threshold voltage variation, which is an important parameter for circuit application, is relatively small and ranges between 0.1-0.2 V. The threshold voltage itself is roughly 1V and seems independent in the channel dimensions. As far as the device mobility is concerned, we can detect almost constant mobility with channel length. The average mobility is approximately 0.2 $cm^2/V{\cdot}s$ with small variation of only 0.01 $cm^2/V{\cdot}s$ (5%) in the short channel case. For the long channel lengths, mobility variation increases to 0.04 $cm^2/V{\cdot}s$. This fact might be related to increased number of impurities as the channel length increases. The high mobility we achieved in the short channel case allows us to operate the devices in higher frequencies. According to equation (12) our transistors can achieve frequency response of several hundreds of kHz where the highest frequency calculated was of 1 MHz.

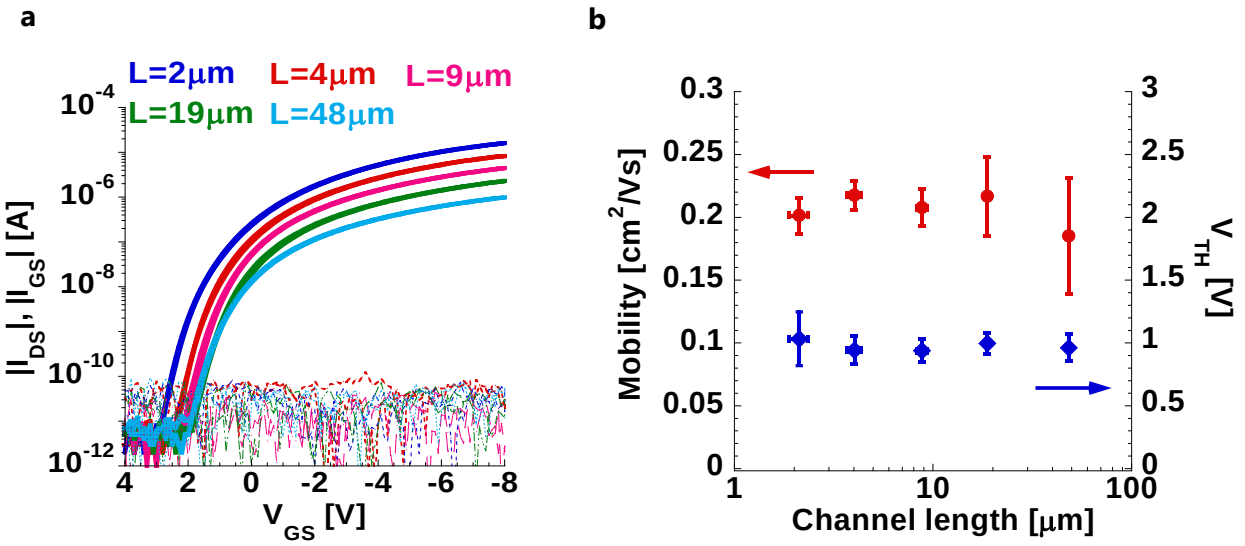


Figure 29: (a) Transfer curves of different channel lengths for channel width of 200 μm. Consistent reduction of saturation current and shift in threshold voltage is observed as channel length increase. (b) Summary of transistors V_{TH} and mobility as a function of channel lengths. 5-10 transistors were sampled for each channel length.

4.2.3 Output characteristics

Transistor's output curve is an important device characteristic. The output curve shows the relation between the source and drain voltage and the source and drain current. It can reflect the effective resistance of the devices in saturation and linear regimes. In *Figure 30* we present devices' output curves for the different channel lengths. Here again, the channel lengths vary from 2 μm to 48 μm and channel widths are fixed to 200 μm. Gate dielectric thickness is 120 nm. The measurements were done using parameter analyzer while sweeping the drain source voltage for different gate voltages (*Figure 30*a). Results are plotted in *Figure 30*b-f for channel lengths of 2 μm, 4 μm, 9 μm, 19 μm and 48 μm, respectively. In the long channel case (L≥ 9 μm) we can see nice linear curve in the linear regime as $V_{DS} \propto I_{DS}$ at low drain voltages. In the saturation regime, the output resistance ($\partial V_{DS}/\partial I_{DS}$) gets very high (especially for long channels) which is a desirable property for transistors used as an ideal current source. The output saturation resistance at low gate voltage (-2V) ranges from 50 MΩ for the short channel case up to 15 GΩ for the long channel case. The short channels suffer from lower output resistances due to short channel effects. At high gate voltage, the saturation output resistances ranges from 1 MΩ for the short channel case up to 50 MΩ for the long channel case.

Another interesting analysis of the device output curve is the contact resistance of the device. From quick observation on the short channel cases (L= 2 μm, L= 4μm) we can detect that I_{DS} does not follow linearly the change in V_{DS}. This phenomenon can be hardly observed in the long channel case. This deviation from the ideal case is related to the existence of contact resistance in the injection from the metal contacts to the semiconductor. In order to quantify this resistance we use the transfer length measurement (TLM). A schematic of the TLM principle is plotted in *Figure 31*a. When we plot the total resistance of the device as a function of the device channel length we expect it to follow the equation:

(15) $$R_T = R_C + R_{sheet} \cdot \frac{L}{W} \quad [54]$$

Here, R_T is the total resistance ($\partial V_{DS}/\partial I_{DS}$, calculated in the linear region), R_C the total contact resistance and L and W are the channel length and width respectively. We calculated the linear total resistance ($V_{DS} = -0.5V$) of the transistors with channel lengths between 2 μm and 48 μm for different gate voltages. The results are plotted in *Figure 31*b for $V_{GS} = -4V$ (blue), $V_{GS} = -6V$ (orange) and $V_{GS} = -8V$ (red). The contact resistance for each gate voltage is the intercept of each linear line and it depends on the gate voltage. The lower contact resistance is obtained for the highest applied gate voltage ($V_{GS} = -8V$) and is approximated to be 5.5 kΩ·cm. The highest calculated contact resistance was 6.8 kΩ·cm for $V_{GS} = -4V$. Two other quantities that could be extracted from the TLM method are the sheet resistance and transfer length of the transistors. The sheet resistance stands

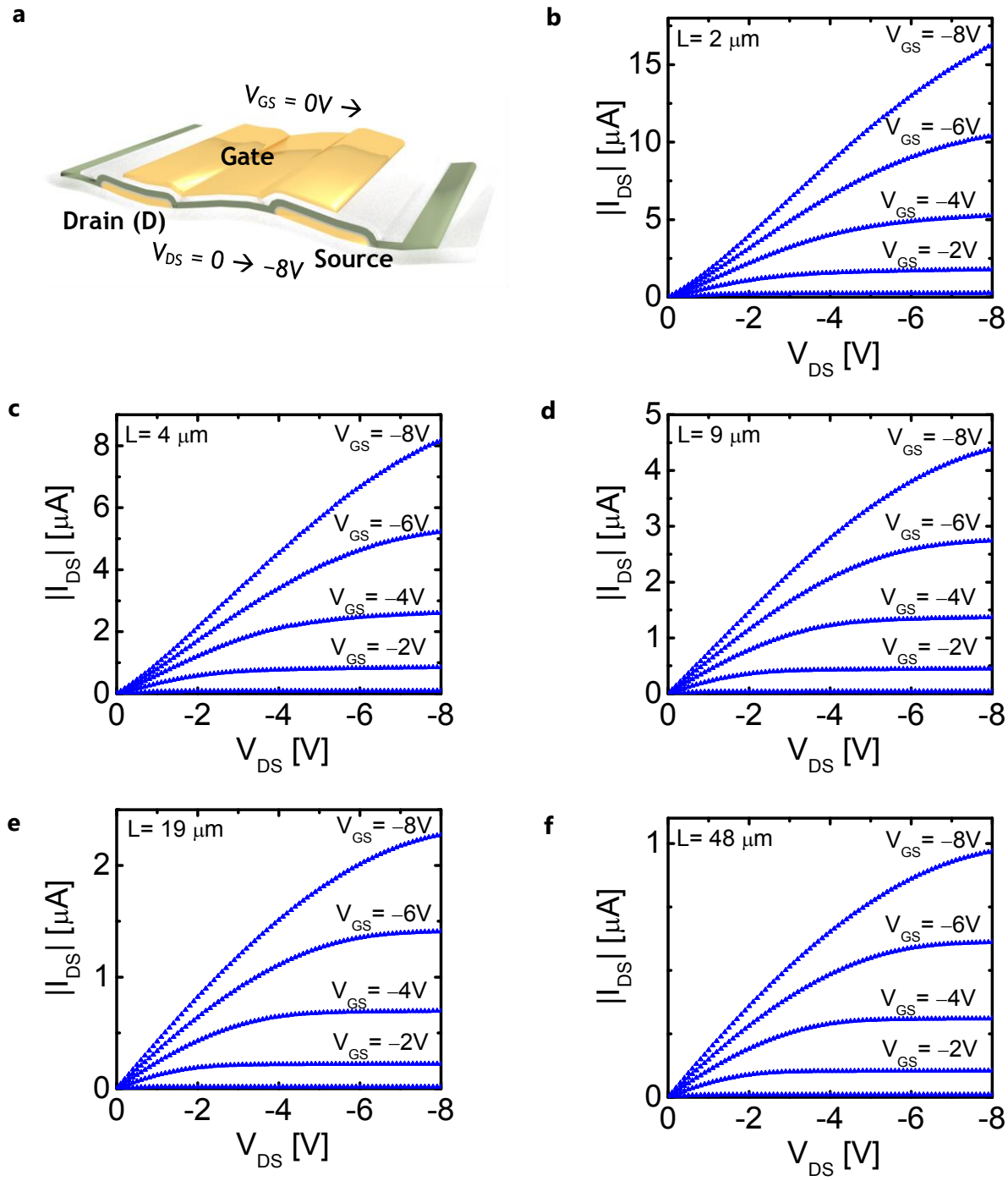


Figure 30: (a) Illustration for contacts and voltage applied on the ultrathin film transistors. (b)-(f) Output characteristics of bottom contact transistors with varying channel length from 2-48 μm. I_{DS} is plotted Vs. V_{DS} on a linear scale for different gate-source voltages.

for the channel resistance which is mainly affected by the pristine properties of the semiconductor in the transistor's channel. The sheet resistance changes from 30 MΩ/□ to 56 MΩ/□, depending on the gate voltage. The transfer length of a transistor is the contact

are where 2/3 of the charge carriers are being injected from. The transfer length gives us information on the effectiveness of the charge transmission from the contacts to the semiconductor. From this value we can deduct the minimum 'finger' size we can utilize for our transistors. Using the transmission line measurement, the transfer length, L_T, is approximated by the line intersection with the x-axis. For our devices, the transfer length was approximately 1 μm which allows us to implement small 'finger' size with very low parasitic capacitance.

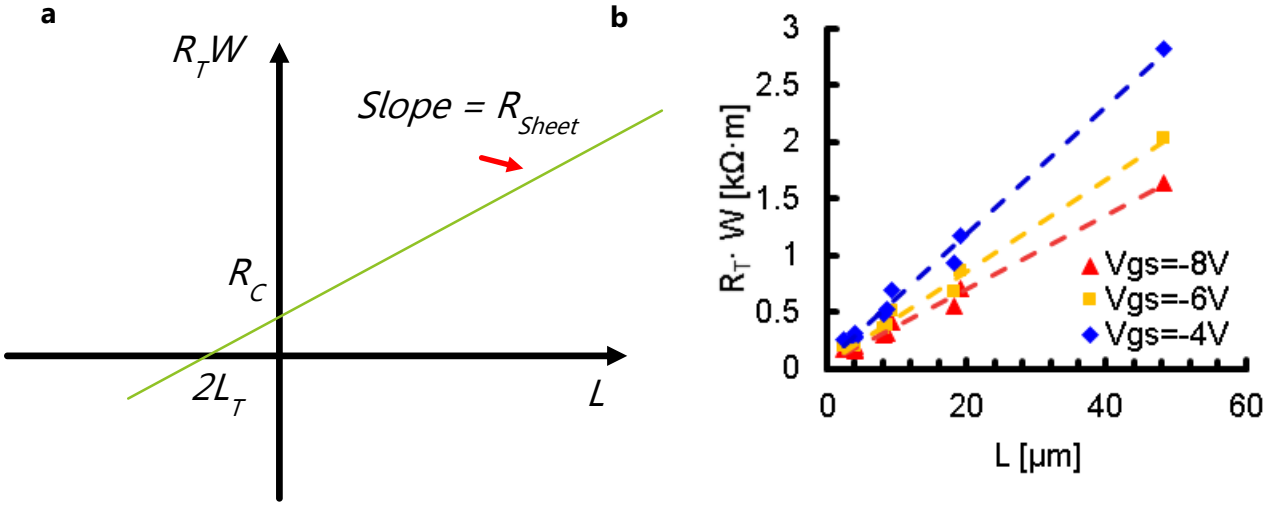


Figure 31: (a) Schematic illustration of contact resistance calculation using the TLM method. (b) Plot of the total channel resistance vs. channel length for different gate-source voltages. Lines intercepts represent the contact resistance for each condition.

4.2.4 Frequency response

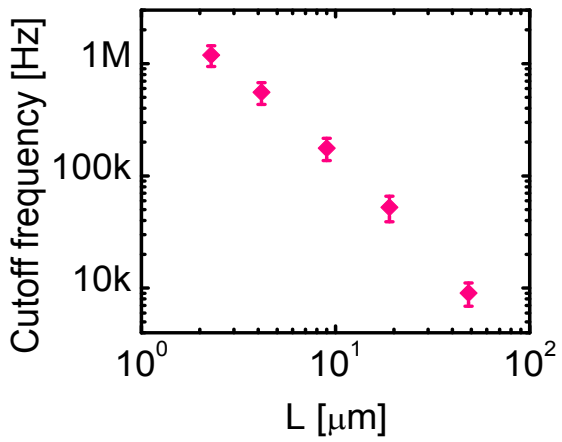
In chapter 3 we gave the theoretical background for calculating transistor characteristics and bandwidth. We showed that transistor cutoff frequency is estimated by the relation:

$$f_T \approx \frac{\mu \cdot (V_{GS} - V_{TH})}{2\pi L(L + 2L_C)} \quad (16)$$

where μ is the transistor's field effect mobility, V_{GS} and V_{TH} are the gate-source and threshold voltage respectively, L is the channel length and L_C is the physical overlap between transistor's gate and source. As mentioned earlier, transistor's channel dimensions play an important role in determining its maximum frequency, which is

defined as the frequency where the transistor current gain equals to unity. Here, we summarize the theoretical cutoff frequencies of our fabricated transistors which demonstrate values exceeding 1 MHz.

a



b

Channel length	Cutoff frequency	
	Average	Maximum
2 μm	1.2 MHz	1.6 MHz
4 μm	550 kHz	760 kHz
8 μm	170 kHz	240 kHz
19 μm	50 kHz	70 kHz
48 μm	9 kHz	13 kHz

Figure 32: (a) Average cutoff frequency value of transistors with increasing channel length. (b) Summary of values obtained from frequency calculation. Average and maximum values of the different channel lengths are presented.

We performed the theoretical cutoff frequency estimation for 75 transistors with different channel lengths from 2 μm to 48 μm. Mobility and threshold values were extracted from transistors' transfer curves while channel length and gate-source overlap were measured using optical microscope. The values for the gate-source overlap averaged to L_C=4.5 ± 0.1 μm that represent good patterning uniformity and actual parasitic capacitance of $C_{GS} = C_{GD} = W \cdot L_C \cdot C_{OX} \approx 400\ \mu m \cdot 4.5\ \mu m \cdot 25 \frac{nF}{cm^2} = 0.45\ pF$ between gate and source. The average total parasitic capacitance of the channel is only ~0.9 pF. Average value of mobility was 0.18±0.03 $cm^2/V{\cdot}s$. We calculated the theoretical frequency for each transistor using its actual mobility and channel overlap, according to equation (16). We plot the results in *Figure 32*a. The cutoff frequency is presented as a function of the channel length in a log-log scale. We see a clear improvement of more than 2 orders in cutoff frequency when reducing the channel length down to 2 μm. The consistent power-low increase ($f_T \propto 1/L^2$) indicates that our mobility and threshold values maintain their value when decreasing the channel length. This is another indication that the contact resistance in our devices is negligible and does not affect much their performance.

*Figure 32*b exhibits the importance of channel dimensions scaling for improving frequency response. Here we summarize the values obtained for the different channel lengths by comparing the average and maximum frequencies achieved. The maximum

frequency we could obtain is 1.6 MHz which is the maximum value obtained on ultrathin substrates. The average value for 2 µm also exceeds the 1 MHz cutoff value (standard deviation ~0.2 MHz) which validates the consistency of device performance. Long channel lengths (e.g. 19 µm and 48 µm) obtain frequencies in the kHz region. The kHz frequency range is, in many cases, not sufficient for multiplexing numerous signals from large area sensor arrays. It is important to note that the theoretical cutoff frequency represents the frequency where transistor gain equals to 1 and does not reflect the practical maximum bandwidth of a circuit utilizing those devices. For an amplifier circuit, for example, the f3dB point is of importance and is much lower than the cutoff frequency value. We will evaluate an amplifier circuit frequency response in chapter 8.2

4.2.5 Transistors uniformity

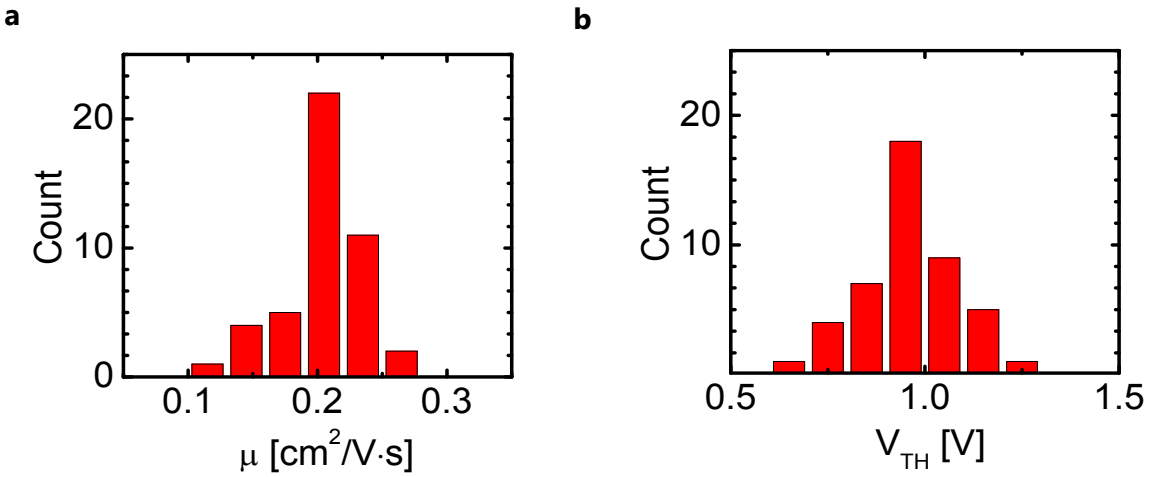


Figure 33: Transistor count for (a) mobility and (b) threshold voltage for transistors fabricated on 2.5x2.5 cm^2 (Total device area is demonstrated in Figure 34a).

In the view of circuit implementation and practical applications, uniformity and reproducibility of device characteristics are of utmost importance. Transistors should be reliably patterned and fabricated to allow consistent circuit design without failure, especially in the case of organic electronics for large area applications. For our device fabrication we chose in advance techniques that are suitable for uniform fabrication over large area: photolithography is a well-established method for reliable large area patterning; chemical vapor deposition and thermal evaporation are uniform methods for material deposition and are limited only by the chamber size and vapor distribution; self-assembled monolayer application is possible on large areas with suitable solution containers. By applying those methods for transistors' fabrication we expect high degree of uniformity over large areas.

In order to evaluate characteristics uniformity we fabricated transistors over an area of 2.5x2.5 cm^2 (*Figure 27*a) with varying channel lengths on different device locations. Transistors' channel lengths are from 2-48 μm and channel width is uniform for all devices at 200 μm. Gate dielectric thickness is 120 nm and applied drain voltage is $V_{DS}=-8V$. We made a histogram for devices' mobility and threshold voltage in order to demonstrate the variation of devices. It is important to notice that the devices' histograms presented in *Figure 33* consist of 50 different devices with different channel lengths. Nevertheless, a very uniform distribution can be observed. In *Figure 33*a, the mobility distribution is aggregated in 0.03 $cm^2/V{\cdot}s$ bins and shows that most of the devices are within 10% deviation from the average value of 0.2 $cm^2/V{\cdot}s$. In *Figure 33*b the threshold voltage distribution shows a uniform behavior for the different channel lengths where most of devices are within 0.3V from the average value of 1V.

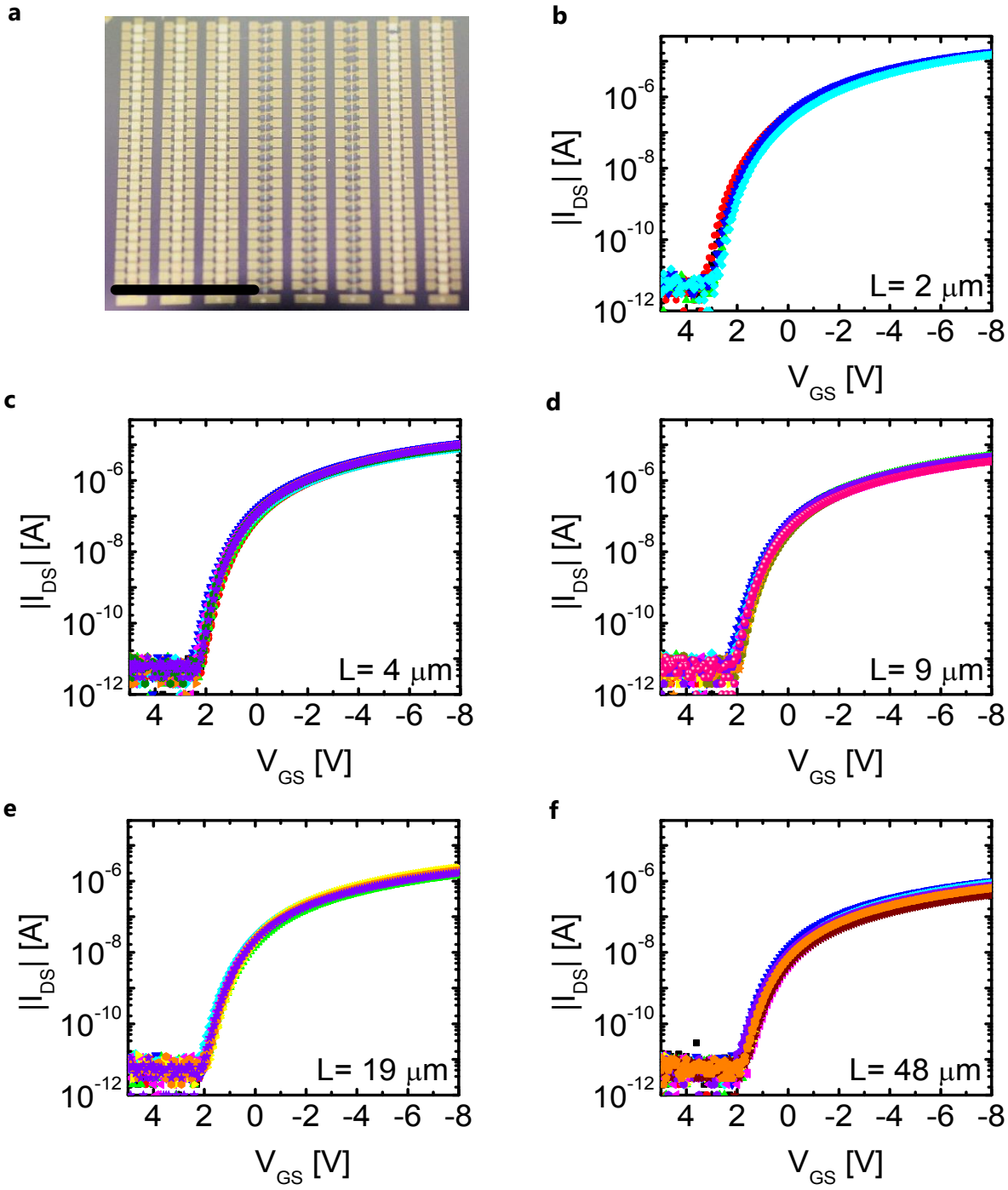


Figure 34: Transistor uniformity. (a) Photograph of the fabricated sample, consists of approximately 70 working transistors. Scale bar is 1 cm. (b)-(f) Transfer curves of bottom contact transistors with varying channel length from 2-48 μm.

For more graphic demonstration, we plot the transfer curves of 10 devices from each channel length in *Figure 34*b-f. From this plot we can evaluate the uniformity of the transfer characteristics in each channel dimensions. We can detect very uniform performance among transistors with the same channel length. Similar OFF and ON currents provide reliable ON/OFF ratio for the device and almost identical sub-threshold swing, threshold voltage and mobility allow same working frequency for the specific channel length. The mobility and threshold distribution and the uniform representation of the transfer curves reassures the uniformity of our devices on relatively large area and paves the way for reliable fabrication of large area electronic devices and circuits.

4.3 Discussion

Our optimized device structure has shown good short channel transistor mobility in bottom contact architecture, low contact resistance, low operation voltage and excellent uniformity. The simultaneous achievement is demonstrated for the first time on ultrathin films. The successful implementation is an important step for improvement of ultrathin devices and can be attributed to our selection of materials and processes. Following are some of the important design elements that led us to those successful results:

- *Top gate architecture and vapor deposited parylene diX-SR as gate dielectric*

The utilization of the top gate layout for bottom contact devices offers the advantages of the staggered structure of an increased charge injection area to the semiconductor. In this architecture the electrical field is applied from the top of the device and charges are injected from the entire area of contacts (*Figure 35*a). On the contrary, in the bottom gate structure charges are mainly injected from the source and drain lateral dimensions as the electrical field is masked to affect only in the region between contacts (*Figure 35*b). The injection area in top gate devices can be modified more effectively with SAM [129] which facilitate charge carrier transmission without affecting device dimensions. Furthermore, larger interface area provides better stability and durability of this sensitive and crucial region in case of external stresses.

Nevertheless, the top gate-bottom contact structure is not very common in literature. One of the reason is the deposition method of the gate dielectric. The gate dielectric is a very important layer in the transistor structure and should be formed uniformly and reliably over the channel area. Reliable dielectric layer allows low leakage current and reduced power consumption, uniform and reproducible performance over different fabrication batches and small device hysteresis. Among the common approaches for fabrication of gate dielectric one can find metal oxide formation, spin coating and drop casting [10,41]. In many cases those approaches limit the structure to the bottom gate layout. Metal oxide layer can be very reliably formed in anodization processes or plasma

treatment but require the gate to be deposited as the first layer of the transistor. Oxides can also be deposited using sputtering methods but can cause damage the thin film substrate or the semiconductor [10]. Sputtering of metal oxide directly on the semiconductor can cause irreversible damage to the sensitive layer and degrade device performance. For deposition of dielectric layer on top of the semiconductor using spin

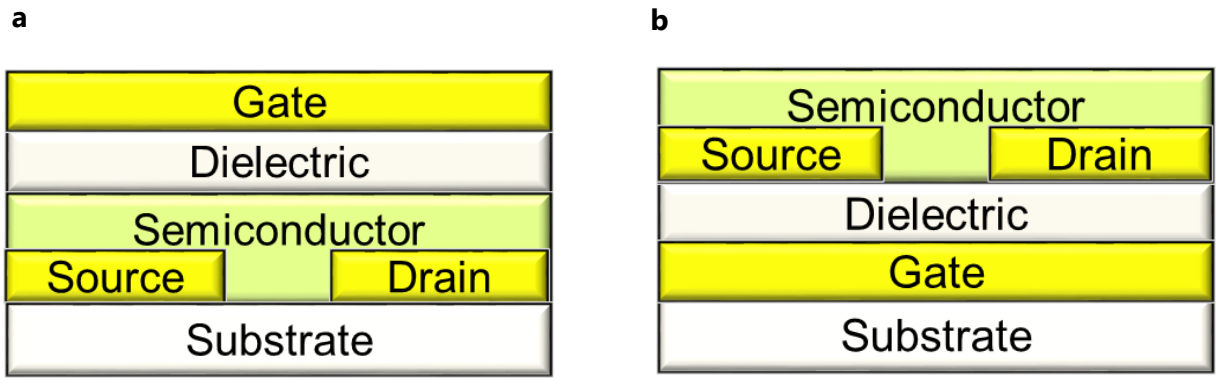


Figure 35: Bottom contact OTFTs: (a) bottom contact – top gate and (b) bottom contact – bottom gate architectures.

coating of drop casting, the selection of solvents is very important to prevent damage to the semiconductor [34]. For example, organic solvents such as ethanol or isopropanol which are used for dissolution of dielectric materials, causes severe damage for certain organic semiconductors. By the use of spin coating or drop casting, film uniformity and coverage over large area should be considered.

The choice of parylene diX-SR as our gate dielectric was a key point in the simultaneous achievement of uniform, low voltage devices on ultrathin films. Parylene diX-SR has a low dielectric constant of ε_r=3.06 and high breakdown voltage. This allows parylene diX-SR to serve as a very good insulator for gate dielectric and provide very low leakage currents. Furthermore, parylene diX-SR can be deposited using chemical vapor deposition on any surface in a uniform and reliable way. This important characteristic of this gate dielectric allows us an important degree of freedom in choosing the appropriate device layout to work with. For the bottom contact devices, top contact is advantageous in terms of durability and charge injection area and the use of parylene diX-SR dielectric enabled the implementation of this structure in our case.

Parylene diX-SR has additional characteristics that improve our devices even further. First, this material is not dissolved by organic solvents or developer and is compatible with photolithography process. This allows us to form the top gate layer using photolithography in high accuracy and reliability. Second, parylene diX-SR can be vapor deposited at ultrathin layers in a uniform, pinhole free manner. Using high vacuum parylene U-diX coater (KISCO Ltd.) layers of 100 nm and below can be formed over large device areas. Thin and uniform dielectric layer allows reduction of operation voltage while maintaining low leakage and good device performance. The complementary choice of

parylene diX-SR and top gate – bottom contact structure was a key factor in the successful implementation of short channel, uniform and low operation voltage transistors on ultrathin films.

• *Parylene diX-SR as substrate*

For realizing large area and ultrathin electronic devices on plastic foils, the choice of substrate is critical. Substrates should be ultrathin (~1 μm) but yet durable and easy to handle. Another requirement is the feasibility to form large sheets to allow the manufacturing of devices simultaneously over large area. The ultrathin film is easy to wrinkle and change its properties during device fabrication. In *Figure 5*a (section 3.1), we give examples of common flexible substrates used for electronic device fabrication. It can be easily seen that the ultrathin foil has different properties than its thicker companions. We showed how our substrate formation and properties enabled the reliable fabrication using photolithography. In addition, surface roughness and hydrophobicity play an important role when one tries to fabricate active devices on those substrates. Organic semiconductors are known to be sensitive to those properties during deposition which affect the final device performance. Hydrophobicity and low surface roughness are considered to improve semiconductor formation during evaporation and lead to better device mobility.

Parylene diX-SR as substrate in the top gate structure provides many advantages. One of the unique material properties compared with other thin plastic film is its surface roughness. Parylene diX-SR has surface roughness of a few nanometers (1.5 nm < Ra < 3 nm, 2 nm < RMS < 4 nm) when deposited using CVD [60]. As a comparison, this value is considerably low in relation the commercially available 1.2 μm PEN sheet (88 nm RMS [16]), and comparable to thick 75 μm polyimide substrate (2.4 RMS [60]). The small surface roughness allows good metal and semiconductor deposition on top of the substrate and reliable electronic device fabrication. Another important property of parylene diX-SR is its hydrophobicity. We measured water contact angle of 83° which indicated a nearly hydrophobic surface. The surface energy could be reduced by annealing the substrate at 120°C and obtain contact angle of 86°. When we utilize the top-gate structure for device fabrication, the semiconductor is deposited directly on the substrate, and its formation would determine the charge transport properties in the channel. Low surface roughness and surface energy improve semiconductor deposition and contribute to transistor's performance in the bottom contact-top gate architecture.

The choice in parylene diX-SR as substrate enabled reliable fabrication techniques using photolithography and high quality semiconductor formation in the top gate structure. Parylene is also a durable material that is used in the biomedical field as an encapsulation or passive recording electrodes [62]. When utilizing the top gate structure, parylene diX-SR has good properties for semiconductor deposition. Small surface

roughness and nearly hydrophobic surface provide excellent compatibility for electronic device manufacturing on ultrathin films.

• *Contacts modification on ultrathin films*

Contacts modification is an important process step for bottom contact devices. The injection barrier is considered higher in the bottom contact structure because of work function and different surface energies of the metal and the gate dielectric. This modification was found to be more challenging than in the rigid substrate case. In section 4.1 , we experimented several methods that were proven effective on rigid substrates. However in the ultrathin case we found that only PFBT SAM could obtain performance improvement on the ultrathin film. The high energy involved in plasma treatments increases surface energy and roughness and degrades the semiconductor quality on the substrate. On the other hand, application of PFBT SAM involves dipping the sample in ethanol-based for 2 hours which was found to be compatible with device fabrication on ultrathin films.

The reliability of PFBT was proven to be excellent in the thin film transistor structure. We could detect uniform contacts modification over large area that led to an enhanced device performance at all channel lengths. Pentafluorobenzenethiol SAM changes gold work function from roughly −5 eV to −5.5 eV and reduces the injection barrier between the metal and the semiconductor (DNTT work function: −5.4 eV [72]). In addition, we demonstrated that PFBT reduces the surface energy of gold and allows better semiconductor formation. By using this modification, we could reduce contact resistance to ~5.5 kΩ·cm (from originally 50 kΩ·cm without modification), which is a comparable value to top contact devices with the same electrode material and semiconductor [33]. We also found our that the transfer length of our devices (the contact area from which 2/3 of charge carrier are injected) is only ~1 μm. This value is much smaller than previously reported values in top contact devices (~10 μm [33]) and allows us reduction of parasitic overlap to enhance device's cutoff frequency.

Pentafluorobenzenethiol self-assembled-monolayer modification is a critical factor in our device fabrication and in achieving high device performance. With a simple, yet effective method we could change gold properties to have lower surface energy and deeper work function to facilitate charge injection to the channel. Our results showed that the gold modification was compatible to ultrathin films and could achieve a high degree of uniformity. In addition, good mobility could be demonstrated with very small channel length and source and drain widths which can increase cutoff frequency of devices to a theoretical value of 1 MHz.

5 Mechanical Stress Evaluation

For practical applications, devices have to sustain large amounts of stress, especially in the large area and ultrathin case. Stress can be applied by many forms: environmental, such as thermal or pressures changes; mechanical, such as in bending or stretching of devices, and others. The ultrathin films are inherently more fragile and easy to tear than their thicker companions and hence more susceptible to stress. Furthermore, transistor application in the bottom gate structure was considered less robust than the top contact case due the small injection area to the channel. Here we will test our devices upon thermal annealing and mechanical bending to realize the device stability under those conditions. Transistors will be annealed to check their maximum temperature durability without failure and their characteristics dependence when temperature rises. Bending down to small radii until complete device crumpling will be introduced to the devices to evaluate their performance after large mechanical deformation. These evaluations are important characterization of devices before the application for real-life instruments.

5.1 Bending tests

5.1.1 Apparatus

Mechanical stability of organic transistors is a well-studied research. Thin film transistors on flexible substrates have intrigued scholars to evaluate their minimum radius of curvature without fail [16,130,131]. The effect of bending on semiconductor properties during compressive and tensile stress was also investigated thoroughly [40,42,132,133]. However, most of the devices that were tested featured long channel and top contact devices. Here we test the mechanical durability of our ultrathin, short channel device upon bending in various radii of curvatures and an ultimate crumpling test. We will evaluate the change in transistors characteristics, such as mobility, ON/OFF ratio and threshold voltage, and compare the results between the different channel lengths utilization.

The mechanical test apparatus includes transistors on ultrathin, 2.5x2.5 cm^2 parylene diX-SR substrate in the architecture of *Figure 26*. Gate dielectric thickness is 120 nm which allows low operation voltage of 8V. Transistors were fabricated with channel lengths between 2 μm – 48 μm and channel width of 200 μm. source and drain width was kept < 4 μm to reduce the parasitic capacitance during transistors operation. After fabrication, transistors were encapsulated with a 1 μm parylene diX-SR layer using CVD deposition. The encapsulation enhances the mechanical stability of devices by locating them on the device neutral plane and reducing the effective stress they experience [134]. The thinness of our original devices allows such an encapsulation while still keeping our devices

ultrathin with only ~2 µm of total thickness. We delaminated the devices from the supporting silicon substrate after encapsulation and initiated the mechanical bending tests. The evaluation included bending to radii of 5 mm, 2 mm and 0.6 mm, both perpendicular and parallel to the channel direction (*Figure 36*). In order to obtain the desired stress, we rolled the ultrathin film on cylindrical metal rods for each bending radius for the entire device area. After each bending step, the transfer characteristics of devices were taken to investigate potential degradation. We extracted important parameters for device operation, such as threshold voltage, ON/OFF ratio, leakage current and mobility for this investigation and compared the behavior between short and channel length case.

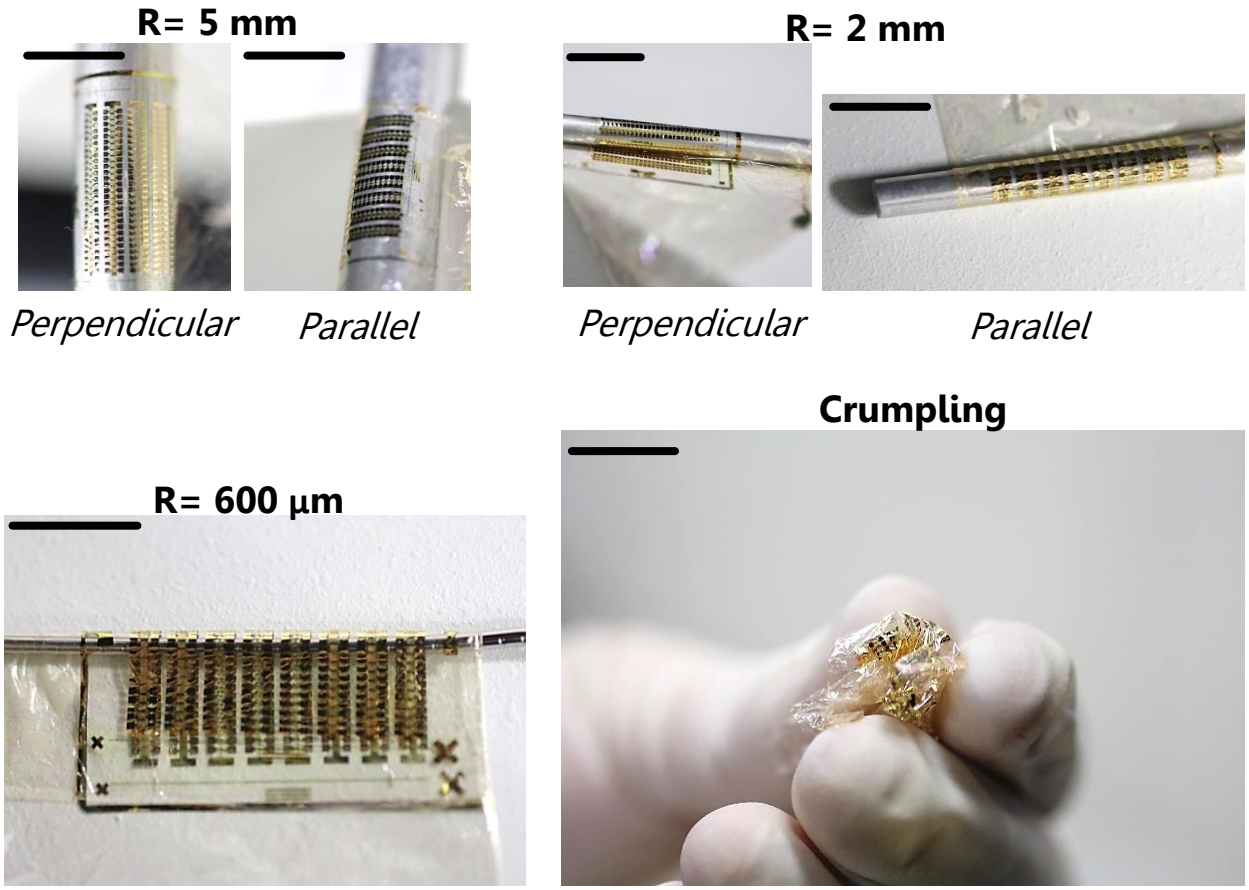


Figure 36: Photographs of the mechanical tests on the ultrathin film transistors. Parallel and perpendicular bending to the channel direction were tested on 5 mm and 2 mm bending radii. Additional bending at 600 µm and several crumpling tests were also performed on the same sample. Scale bar is 1 cm.

5.1.2 Electrical evaluation

In *Figure 37* we plot transfer characteristics of transistors after each bending step. The entire device photograph, in its free standing form, is presented *Figure 37*a. Transfer curves of transistors with channel lengths of 2 μm (*Figure 37*b), 4 μm (*Figure 37*c), 8 μm (*Figure 37*d), 19 μm (*Figure 37*e) and 48 μm (*Figure 37*f) after combined stress cycles (perpendicular and parallel to channel orientation) represent the characteristics change during bending stress. We can notice that no significant change in transistors ON/OFF ratio is observed. OFF current of devices with short channel lengths seems to suffer more from bending to small radii. However, this increase does not degrade by much the functionality of the transistors as a switching device. Another noticeable observation is that the transistors turn-on voltage is shifted slightly to the positive direction. ON current and subthreshold swing are kept unchanged as a result of the extreme bending and generally only slight differences can be observed for the various channel lengths. More quantitative analysis of those changes will be brought in the following paragraphs.

First we analyze the effect of bending on essential parameters for circuit and switching implementation – leakage current and ON/OFF current. Leakage current is important for power consumption and circuit stability while the device ON/OFF ratio in saturation determines the detectability of transistors when they are being used as sensors or switching elements. In *Figure 38* those parameters are summarized for channel lengths < 10 μm. *Figure 38*a (red columns) and *Figure 38*b (green columns) plots the maximum leakage current and ON/OFF ratio respectively, as a function of the bending radius for a transistor with channel length of 2 μm. Same applies for channel lengths of 4 μm and 9 μm in *Figure 38*c-d and *Figure 38*e-f respectively. As a general rule, there is a minor trend in the leakage current behavior as we reduce channel dimensions. Maximum leakage current is kept at ~100 pA for all cases and bending radii where the maximum current for 0.6 mm bending in the 4 μm channel length transistor. Due to the fact this increase is not permanent and the maximum leakage current decreases after the next bending step (crumpling) we can regards this increase as a singularity and not as a general trend. In principle, leakage current should not be affected negatively when channel dimensions decrease because the effective leakage path gets smaller when reducing channel length. When examining the ON/OFF ratio behavior in the short channel cases, we can observe decrease of roughly 1 order of magnitude in channels smaller than 5 μm. The short channel transistors seem to suffer more than the long channel devices from bending stress in small radii. The decrease in ON/OFF ratio is derived from an increase in the OFF current of the devices, as we can detect form *Figure 37*b-c. This increase in OFF current is related to changes in contact areas which are more significant in the short channel case. After this degradation due to extreme bending and crumpling, the ON/OFF ratio of the devices can be still higher than 10^5 in short channels. We expect that this value keeps our transistors suitable for applications in various fields.

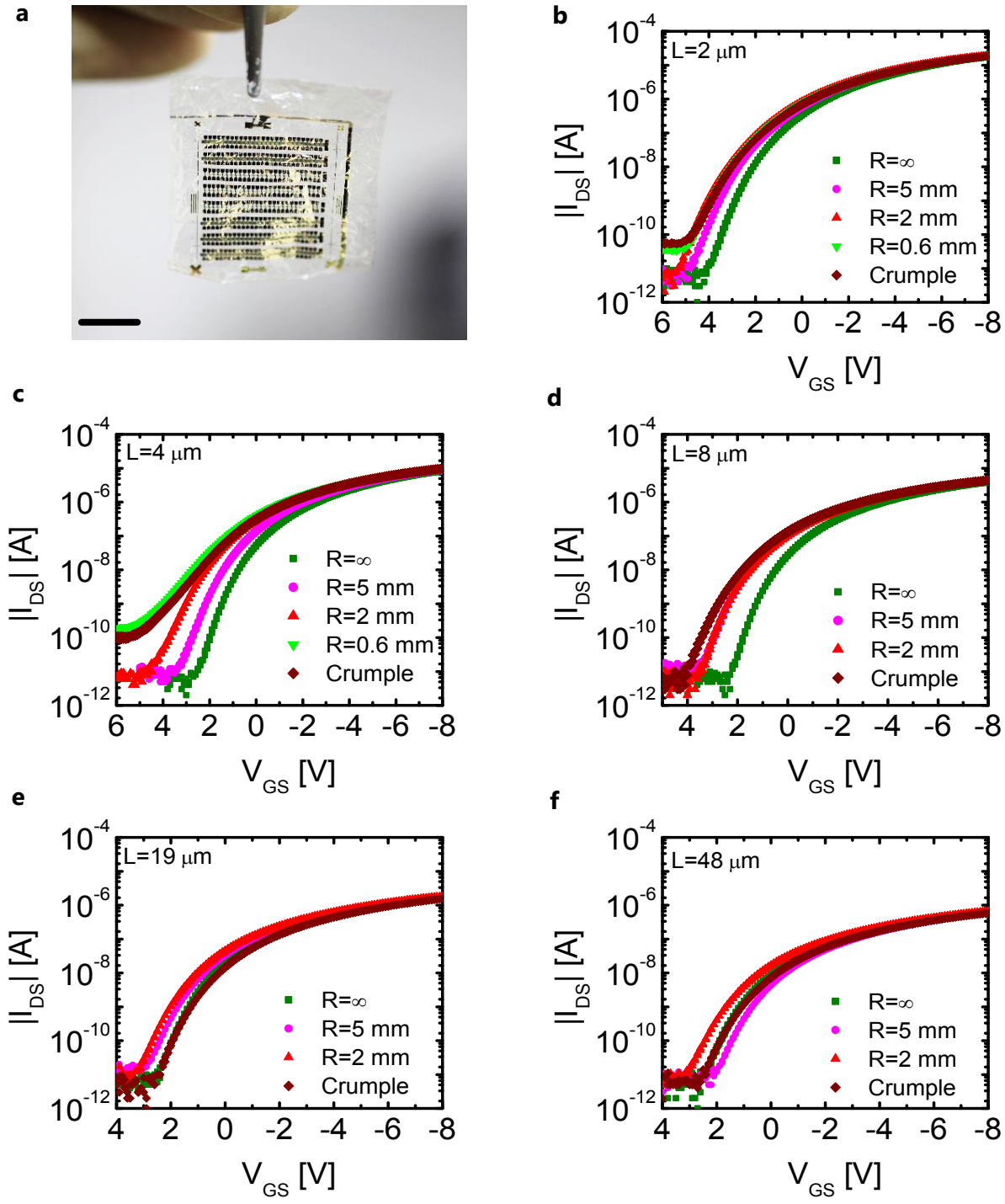


Figure 37: Bending tests. (a) Photograph of the free-standing device after the entire bending tests series. Scale bar is 1 cm. (b)-(f) Transfer curves of bottom contact transistors with varying channel length from 2-48 μm after bending tests steps. R=∞ represents the initial state.

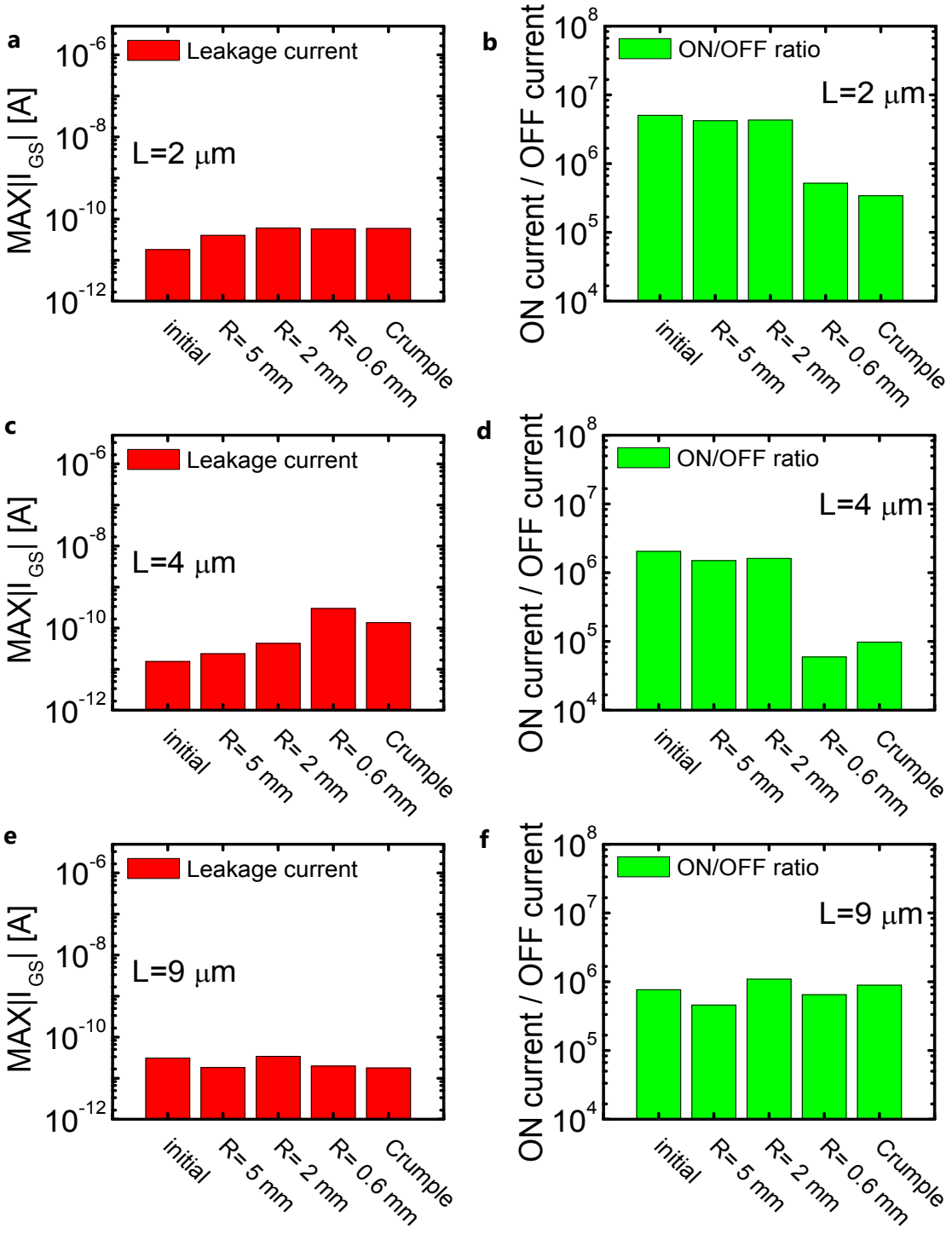


Figure 38: Leakage current and ON/OFF ratio trends for short channel transistors after bending tests. Insets (a), (c) and (e) show the change in the maximum leakage current after bending tests steps. Insets (b), (d) and (f) plot the change in ratio between the transistors' off current and maximum on current after bending tests steps.

5.1.3 Bending orientation

Another interesting aspect of quantitative bending tests, is the bending direction in relation to the channel. Changing the bending directions applies different stresses on the channel area. It was demonstrated that perpendicular and parallel bending does not show substantial differences until bending radii of 1 mm, for top contact devices and long channel layouts [130]. We try to examine this issue also in the bottom structure architecture with varying channel lengths. We have conducted systematical bending tests in 5 mm and 2 mm radius in parallel and perpendicular bending direction to the channel (*Figure 36*). In *Figure 39* we summarize the results for 5 channel lengths between 2 μm and 48 μm. *Figure 39*a and *Figure 39*c show the change in mobility after parallel and perpendicular bending for 5 mm and 2 mm bending radius respectively. Similarly, *Figure 39*b and *Figure 39*d plot the change in threshold voltage after parallel and perpendicular bending for 5 mm and 2 mm bending radius respectively. The initial values represent the

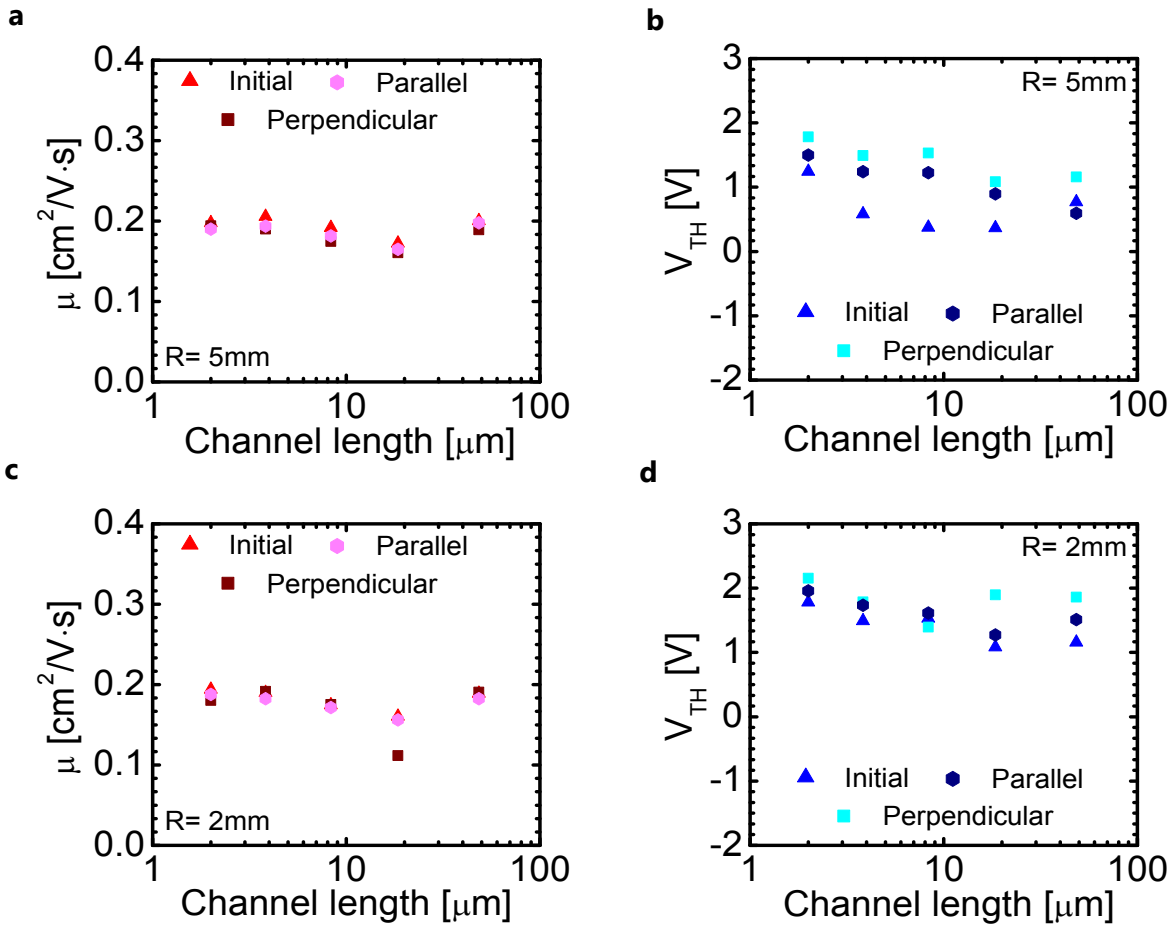


Figure 39: Perpendicular vs. parallel bending in relation to channel orientation. Insets (a) and (b) plot the mobility and threshold values respectively for 5 mm bending radius for transistors with different channel lengths. The initial value and values after perpendicular and parallel bending are presented. Similar information for bending radius of 2 mm is presented in insets (c) and (d).

values before the tests in the specific bending radius. Also, please note that bending in 5 mm bending radius is the first bending experiment in this set.

We detect that mobility of devices does not change for perpendicular and parallel bending orientations until 2 mm. There is no observable difference when changing the bending direction in relation to the channel. Also, no difference is demonstrated as we change the channel length from 2 μm to 48 μm. When we examine the effect of bending on the threshold voltage, it seems that in some cases there is an initial effect for bending the device, however, this change is not related to the bending direction and only slight change is observed between the orientations. From these results we can conclude that there is no specific trend with channel length when it comes to variations in mobility and threshold voltage sown to 2 mm bending radius. Also, we could not distinguish any significant contrast between bending in the perpendicular and parallel bending at these radii.

5.1.4 Characteristics summary

In *Figure 40* we bring a summary of the average device characteristics as they are affected from the entire set of bending tests (5 mm bending radius, 2 mm bending radius, 0.6 mm bending radius, crumpling). In *Figure 40*a presented a photograph of the ultimate crumpling test. We conducted this crumpling test several times before measurement to ensure uniform effect of crumpling on the entire device. We plot the mobility variation for the channel lengths under test before and after the mechanical bending evaluation set in *Figure 40*b. We identify a change of roughly 10% in the effective saturation mobility, regardless transistors' channel lengths, as a result of bending. Mobility variation was maintained or slightly decreased after bending. Maximum leakage current shows no specific trend after bending (*Figure 40*c) as the shortest (2 μm) and longest (48 μm) channel lengths exhibit similar increase in maximum leakage of approximately 2 orders of magnitude. The intermediate channel lengths shows virtually no change in leakage current and maintain low leakage < 100 pA. We assume that the changes in $|I_{GS}|$ are caused from local faults or contaminations in the channel area rather than a real trend of channel length dependence. In *Figure 40*d, change of roughly +1V is observed for the threshold voltage of transistors. We see slightly lower change rate in the long channel lengths (L > 10 μm) which implies that those variations are caused from changes in charge distribution near contact areas. Effect of contacts becomes less significant as the channel length increases due to their relative dimensions. ON/OFF ratio of devices with shorter channel lengths degrades more than in the long channel devices. Devices with 2 μm and 4 μm channel lengths can change their ON/OFF ratio by 1 order of magnitude after extreme crumpling (*Figure 40*e). Nevertheless, ON current of the transistors at $V_{GS}=-8V$ maintains very nicely after extreme mechanical bending stress on the film and no change is detected in ON current for all channel lengths (*Figure 40*f). This property is very

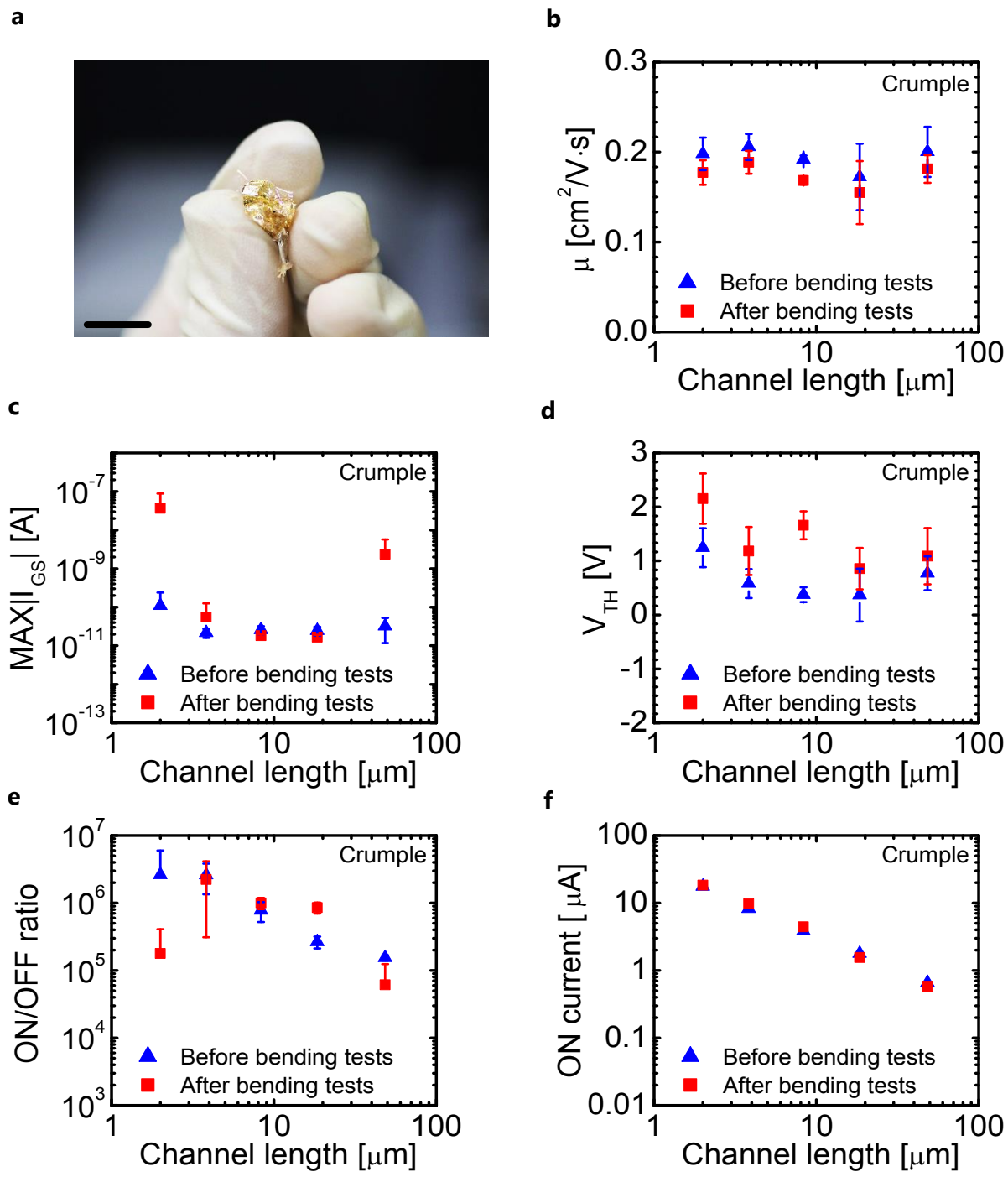


Figure 40: Effect of bending tests. (a) Photograph of the crumpled device at the end of the bending tests series. Scale bar is 1 cm. (b) Mobility, (c) maximum leakage current, (d) threshold voltage, (e) ON/OFF ratio and (f) maximum 'ON' current before and after the entire series of bending tests (including crumpling) are plotted as a function of channel length.

important for applications which require constant current levels such as sensors or current sources. From *Figure 40*e and *Figure 40*f we can deduct that the change in ON/OFF ratio is

originated from increase in OFF current of transistors which is related to contact area deformation and un-gated regions which has larger effect the shorter channels case.

In summary, we can conclude that the bottom contact staggered structure, which allows larger injection area than the coplanar structure, makes our long channels devices durable and mechanically stable similarly to previous reports on long channels in the top contact staggered structure. The extended injection area prevents failure of devices due to changes in contact area. Additionally, we observed some variations in performance of devices with short channel lengths due to bending. Nevertheless, we demonstrated that those variations are not crucial for device functionality and our short channel devices can maintain their relevance for large variety of applications even after extreme bending.

5.2 Discussion

Organic transistors flexibility and mechanical stability are amongst the most appealing points of this technology. The relatively disordered structure of small molecules or polymeric semiconductor allows the device to be durable to larger strains without failure. Nevertheless, organic transistors are still susceptible to certain amounts of stress which normally can reach to a few percent. Mechanical stability of organic TFTs was studied under compressive or tensile stress and on various substrates and their mechanism of failure was investigated [40,42,132]. In *Figure 41* we demonstrate the bending mechanism

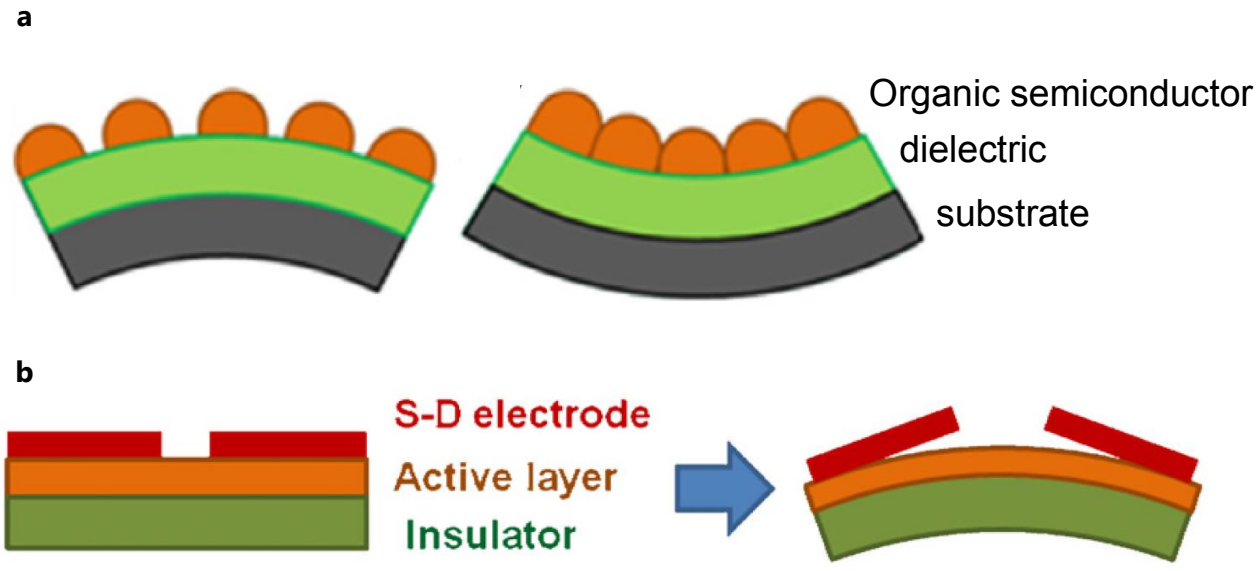


Figure 41: (a) Tensile (left) and compressive (right) stress on transistors layer as a result of bending. Organic semiconductor is denoted in orange, dielectric layer in light green and substrate in grey. (b) Illustration of contact delamination in top contact devices during bending. Illustration were adopted from [40].

of transistor's layer, adopted from [40]. The orange circles in *Figure 41*a represent the semiconductor grains under tensile and compressive stress. We can see that tensile stress can cause separation of semiconductor grains from each other which leads to degradation in device performance. On the other hand, wen the device is compressed and grains can get closer to each other which results in reduced degradation in device mobility and even an increase of this value in some cases. Another degradation mechanism is analyzed in *Figure 41*b. Here we see that the interface of the semiconductor with the source and drain contacts is of great importance for device stability. While bent, due to the different bending stiffness of the thin layers might lead to detachment of the electrodes from the semiconductor surface. This delamination acutely hinder the charge

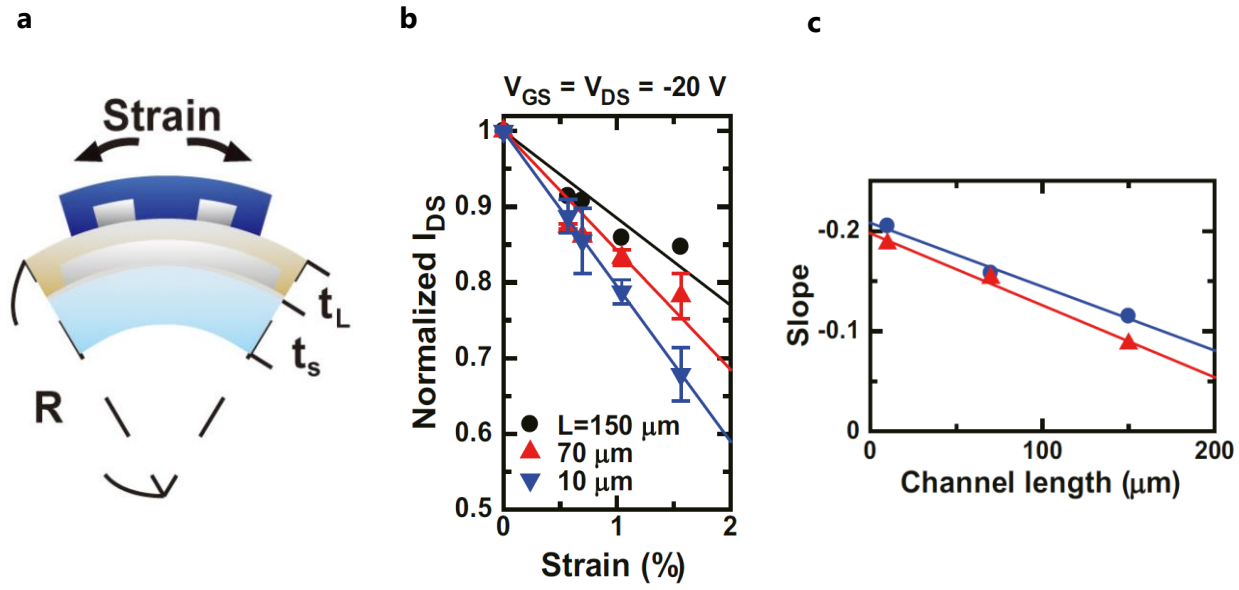


Figure 42: (a) Illustration of bottom gate – bottom contact structure under bending dtress. Substrate thickness and dielectric thickness are t_S and t_L respectively. (b) Normalized drain current as a function of strain applied for different channel lengths. (c) Slope of the curves presented in (b) for p (blue) and n (red) semiconductors, as a function of channel length. All images were adopted from [135].

injection from the contacts to the semiconductor, increases contact resistance, and lead to severe degradation in effective mobility.

Short channel, bottom contact transistors presents further challenges and issues for device stability under mechanical stress. First, the most common architecture for bottom contact devices is the bottom contact-bottom gate structure due to the compatibility with large variety of dielectric layers and semiconductors. In this structure, the injection to the semiconductor is made through a relatively small area ('point injection'). Due to its small area, under mechanical stress this point of injection becomes the most critical component in keeping device performance. Contact delamination or grain separation in the vicinity of this area might lead to a fatal device failure or severe performance degradation. In

Figure 42 we refer to an illustration of the stress applied on the bottom gate-bottom contact structure and experimental results related to device degradation, adopted from [135]. In *Figure 42*a an illustration of the device presents the tensile stress on the transistor with layer thicknesses of t_S for substrate and t_L for gate and dielectric, under bending radius of R. The tensile stress increases as the layer is located further from the neutral plane of the device and small injection areas are more affected from this strain than larger ones. In *Figure 42*b we see how transistors with different channel lengths degrade with increasing strain, as reported in [135]. We notice that from 0.5% strain degradation of ON current occurs between 5%-10% depending on the channel length. As mentioned earlier, contact area is a crucial point for device stability and its relative weight in total device conductivity increases as channel length decreases. Hence, damage to contact area as a

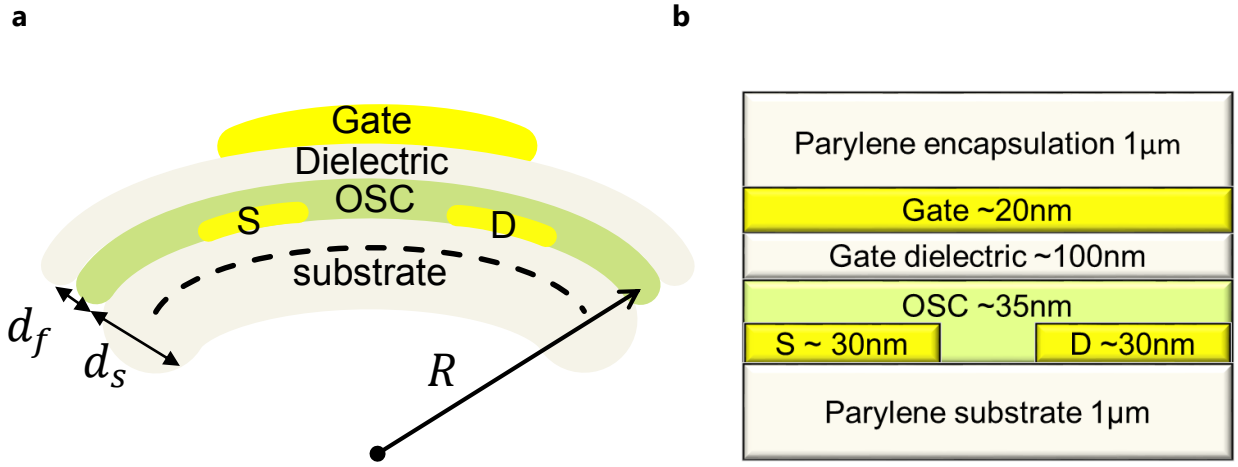


Figure 43: (a) Top gate – bottom contact transistor under bending in radius R. Substrate thickness is d_s and semiconductor thickness is d_f. Channel is assumed to be in the top of the semiconductor as a more strict condition. Dashed line represents the imaginary neutral plane. (b) Encapsulated ultrathin top gate – bottom contact transistor. The neutral plane is approximated to be in proximity to the channel.

result of strain affects more on shorter channel lengths. According to these reported results differences can be seen even between channels of 150 μm (black), 70 μm (red) and 10 μm (blue). This result is emphasized in *Figure 42*c where the slope of I_{DS} degradation as a function of channel length is plotted. The results show the degradation slope of p-type semiconductor devices (blue) and their n-type companions (red) [135]. Clearly, short channel devices seem to suffer more from the applied bending stress in this case due to the increase in contact resistance.

For enhancing the stability of our devices we chose a strategy which comprises from the following main points: First, we implemented the bottom contact-top gate staggered structure which provides larger charge injection area and advantageous channel location over the coplanar structure. Due to the gate location and direction of the electrical field,

the injection is made from the entire area of contacts. Additionally, in this structure the channel is located closer to the neutral plane than in the coplanar structure, which provides better strain immunity. Illustration of the bent staggered device is presented in *Figure 43*a. Estimation of the device neutral plane is given by the dashed black line. The illustration is not to scale. We can clearly see that the channel is located directly on the substrate and affected only by its thickness (d_s) and its own dimensions (d_f), in contrary to the bottom gate structure where the dielectric thickness increases the strain applied on the channel. Second important consideration we implemented is the reduction of substrate thickness. Our devices are fabricated on only 1 μm thick parylene substrate which dramatically reduces the effective strain applied on the channel. During bending the induced strain on channel is given by [133]:

(17)
$$S = \left(\frac{d_f + d_s}{2R}\right)\frac{(1 + 2\delta + \gamma\delta^2)}{(1+\delta)(1+\gamma\delta)} \quad ; \quad \delta = {d_f}/{d_s} \;, \quad \gamma = {E_f}/{E_s}$$

where R is the radius of curvature of device, d_s and d_f are the substrate and semiconductor thickness as denoted in *Figure 43*a. E_s and E_f are their corresponding Young's moduli. For the 1 μm substrate and the appropriate values of our materials [16,136] we obtain that S=0.6% at R=100 μm. As shown earlier in *Figure 42*b, this strain can already cause certain degradation for short channel devices. Thus we engaged the third design approach and encapsulated our devices with an identical material and thickness (*Figure 43*b). When encapsulated with material of the same properties as the substrate, and thanks to the fact that our transistors consist of only ultrathin layers, we can locate the mechanical neutral axis of the device very close to the channel and significantly reduce the strain on channel. The neutral axis of a composite layer structure is given by [137]:

(18)
$$Z_0 = \frac{\sum_{i=1}^{n} E_i d_i \left[\sum_{j=1}^{i} d_j - {d_i}/{2}\right]}{\sum_{i=1}^{n} E_i d_i}$$

Where E_i and d_i are the Young's modulus and thickness of each of the n layers. By the encapsulation process and device thicknesses denoted in *Figure 43*b, we obtain the neutral plane at $Z_0 \cong 1.09\ \mu m$. This value ensure maximal strain of only S=0.025% on channel. The precise encapsulation step was enabled by the use of CVD process, both for the substrate and encapsulation, and the choice of our materials. Additionally the initial thinness of our devices offers this encapsulation without deviating from our ultrathin device concept (total device thickness with encapsulation is roughly 2 μm).

In conclusion, we analyzed how our simple and effective strategy for device fabrication can yield a negligible strain on channel area and enhance short channel device stability under severe mechanical bending stress. The strategy is composed of three important principles: choice of the appropriate device architecture and materials, reduce substrate thickness and device encapsulation. This combined approach allows our devices to perform well after bending, almost regardless on the channel dimensions as we showed

in the mechanical bending tests section. We demonstrate for the first time how short channel devices can offer both large bandwidth, conformability and mechanical stability to allow practical utilization on any shape.

6 Thermal Stress Evaluation

6.1 Thermal stability tests

6.1.1 Apparatus

In order to use OTFTs for practical applications, environmental and thermal stability are of utmost importance. For example, in the biomedical field, large area sensor sheets can be placed on internal organs, such as the brain or the heart, or on our skin and clothes. While environmental stability can be improved by various encapsulation techniques, the thermal stability of the device is an inherent property which is difficult to enhance by external means, especially in the ultrathin film case. Thermal stability is important for devices that are exposed to harsh environmental condition or during sterilization processes which involves temperatures greater than 100°C. Thermal and environmental stability of organic transistors has developed substantially in recent years and excellent air stability was reported, featuring DNTT as a promising material for utilization in real life applications [81]. The thermal stability of DNTT was further investigated to demonstrate sterilization processes on plastic foils, without causing significant damage to the active components [82]. By introducing diphenyl derivatives to the DNTT molecule, an improved thermal stability of up to 250°C could be obtained on flexible substrates, to sustain even more severe environmental conditions [83].

Although high performance and environmentally stable OTFTs have been reported previously, the fabrication of those devices on ultrathin films (~1μm) was not demonstrated yet. High frequency organic circuits were fabricated on rather thick films or rigid substrates, which make them difficult to implement as large area conformable devices. Thermally and environmentally stable OTFTs have been characterized on long channel devices in the top contact architectures, neglecting the effect of channel length reduction as temperature rises. The bottom contact structure also carries additional challenge as the semiconductor is deposited on low surface energy metal contacts [138]. For the ultrathin substrate case, only low operational frequency OTFTs were demonstrated. In this section we study the thermal behavior of our short channel, bottom contact transistors fabricated on ultrathin (1 μm thick) parylene diX-SR films. We quantitatively evaluate the transistors' performance as channel dimensions decrease and annealing temperature rises up to 190°C. The theoretical cutoff frequency (equation (12)) is estimated for various channel lengths (2.5 μm – 48 μm) in the bottom contact architecture and can reach to more than 100 kHz at elevated temperatures. We also show cyclic stability of devices by maintaining transistors' performance after few thermal cycles.

For the thermal tests series we fabricated transistors on ultrathin, 2.5x2.5 cm^2 parylene diX-SR substrate in the architecture of *Figure 26*. Gate dielectric thickness is 120 nm which allows low operation voltage of 8V. Transistors were fabricated with channel lengths between 2 µm – 48 µm and channel width of 200 µm. source and drain width was kept < 4 µm to reduce the parasitic capacitance and obtain higher cutoff frequency values. After fabrication, transistors were encapsulated with a 1 µm parylene diX-SR layer using CVD deposition. Transistors were kept on the thermally conductive silicon wafer, as fabricated, to ensure uniform and direct contact with heater. Devices were annealed using hot plate for 30 minutes at elevated temperatures and then allowed to cool down to room temperature. Initially and after each annealing step, electrical characterization was performed by semiconductor analyzer (Agilent Technologies 4156C) in air to identify performance change (procedure is described in *Figure 44*). The Effect of annealing environment (N2 vs. air) was analyzed by performing heating steps in N2 glove box (O_2 < 9 ppm, H_2O < 1 ppm) and in ambient conditions. Transistors were annealed until they fail to show transistor characteristics.

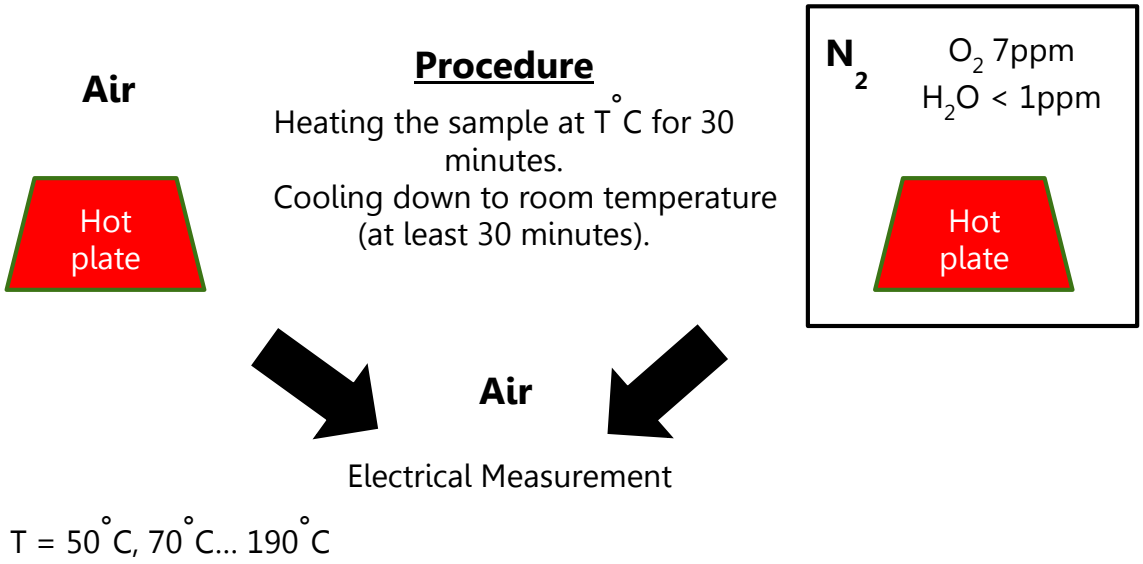


Figure 44: Process flow of thermal stability measurement tests. Devices were encapsulated and tested under ambient and N_2 conditions for performance changes.

6.1.2 Electrical characterization - Air Vs. N_2 environment

Representative transfer curves of devices with channel lengths of 2 µm, 4 µm, 19 µm and 48 µm annealed in N_2 glove box (O_2 < 9 ppm, H_2O < 1 ppm) are plotted in *Figure 45*a-d respectively. Curves plot color indicates the annealing temperature. Initial transistor performance showed saturation mobility of ~0.2 $cm^2/V{\cdot}s$ with low operation voltage (V_{GS}=−8V). Threshold voltage was estimated to ~1V. Contact resistance was evaluated using the transfer line method (TLM) to be 6 kΩ·cm. As temperature rises we detect a consistent reduction in ON current, especially above 70°C. In addition, a generally

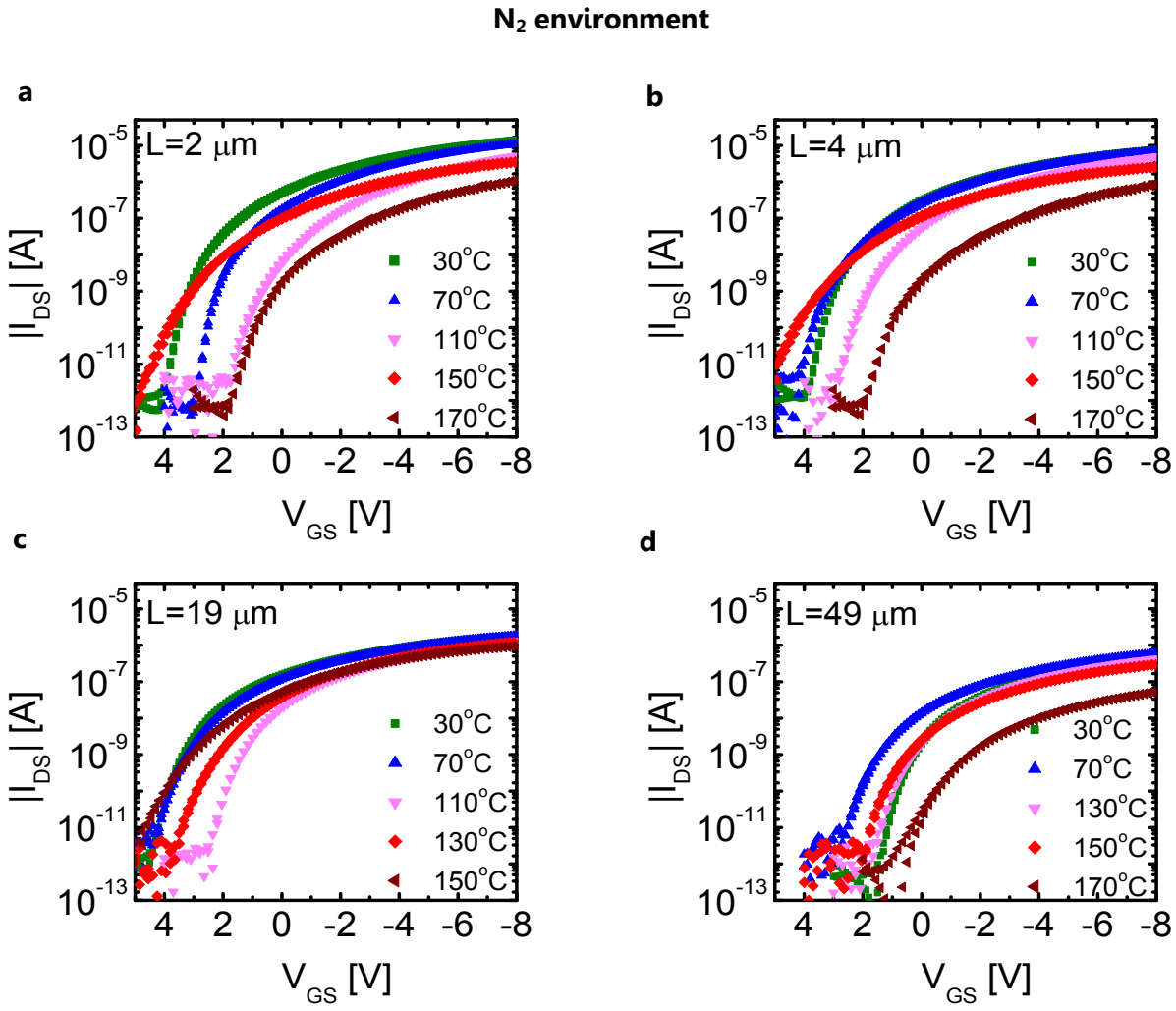


Figure 45: Thermal tests results in N_2. Transfer curves of transistors with channel lengths of (a) 2 μm, (b) 4 μm, (c) 19 μm and (d) 48 μm are plotted for different annealing temperatures.

negative shift in turn-on voltage is also apparent in elevated temperatures. Similar trend was detected for devices annealed in air. In *Figure 46*a-d results of transfer characteristics of transistors with channel lengths of 2 μm, 4 μm, 19 μm and 48 μm respectively are plotted. Curves colors indicate the annealing temperature before measurement. Similar trends for reduction of ON current and threshold voltage shift are observed in this case as well. The main difference between the two annealing conditions (N_2 and air) is the ultimate annealing temperature before failure. As a general rule, devices annealed in N_2 showed better durability and could function up to 170°C where transistors that were treated in air could operate only up to 150°C.

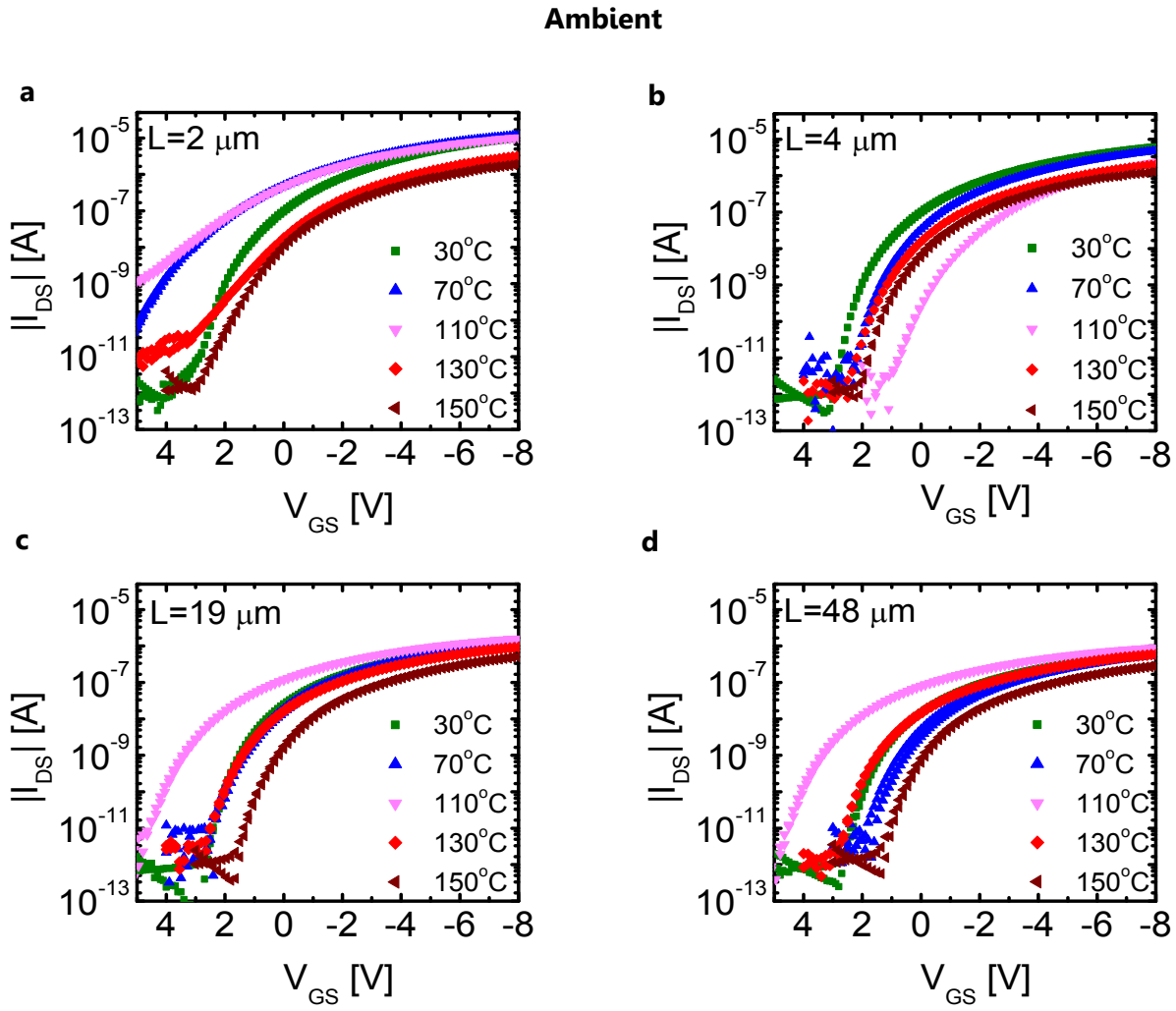


Figure 46: Thermal tests results in air. Transfer curves of transistors with channel lengths of (a) 2 μm, (b) 4 μm, (c) 19 μm and (d) 48 μm are plotted for different annealing temperatures.

6.1.3 Analysis

We summarize some of the important transistors' characteristics in *Figure 47*. In *Figure 47*a and *Figure 47*b we compare the maximum leakage current of devices with different channel lengths when annealed in air and in N_2 respectively. We observe no noticeable difference in leakage currents as a result of annealing, regardless the test environment. Also, no trend can be identified with channel length while leakage current can be kept < 1 nA for all channel dimensions. We compare the ON current behavior in different environments with temperature for various channel lengths in *Figure 47*c (air) and *Figure 47*d (N_2). First we note that the long channels (L > 10 μm) present more stable performance up to 150°C in both environments. This trend is comparable to previous

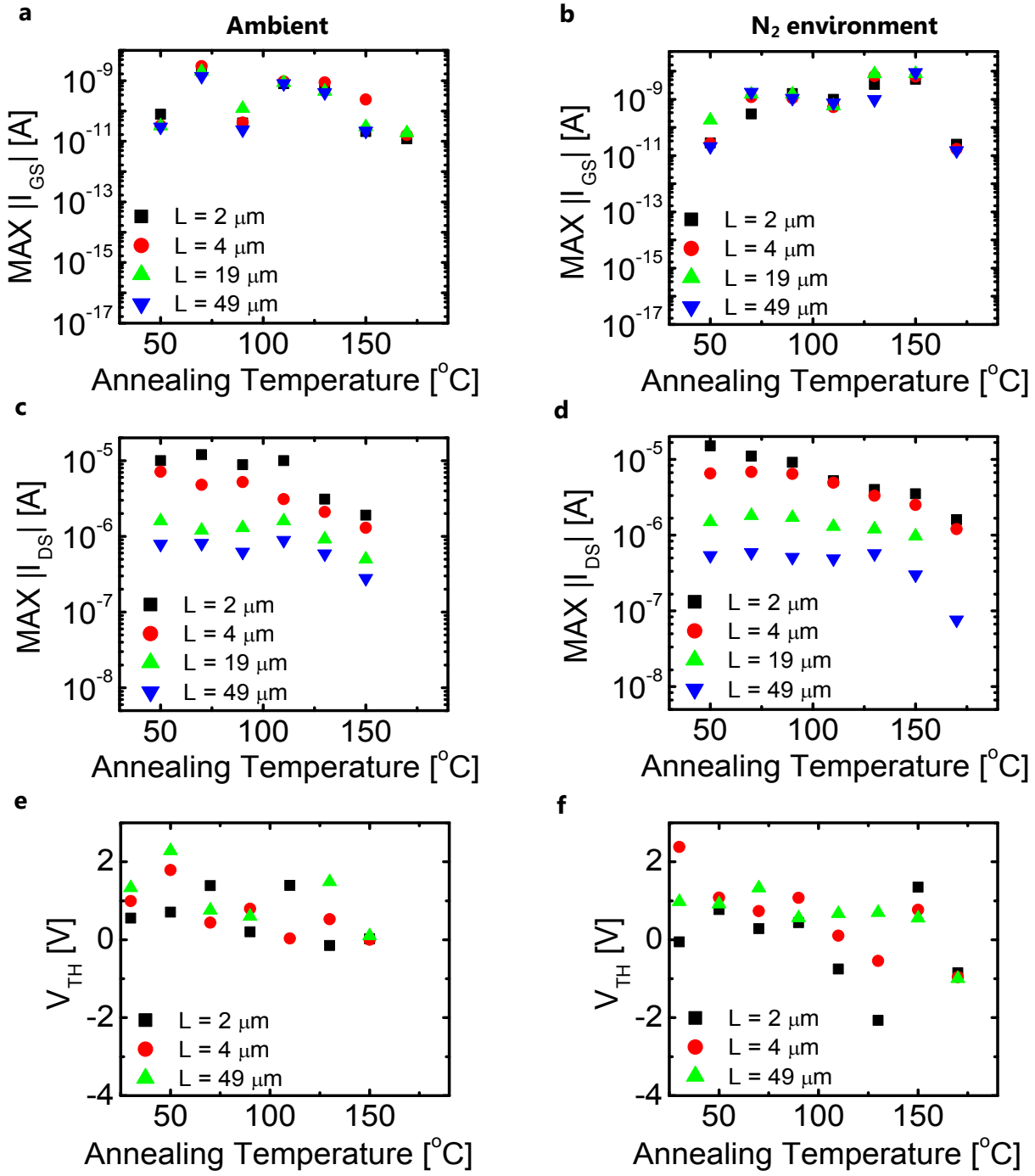


Figure 47: Comparison of annealing effects in air and N_2. Insets (a), (c) and (e) represent the maximum leakage current, maximum 'ON' current and threshold voltage respectively of devices with different channel lengths, annealed in air. Similarly insets (b), (d) and (f) represent the maximum leakage current, maximum 'ON' current and threshold voltage respectively of devices with different channel lengths, annealed in N_2.

reports on DNTT based transistors [60,82]. Transistors with the shortest channels (L= 2 μm) begin to show degradation in ON current at 130°C when annealed in air. When

annealed in N_2, similar devices show earlier degradation already at 110°C. In the 4 μm channel case, similar degradation pattern can be observed between the two annealing conditions. In all cases, devices which were annealed in air stopped working and showed very low ON (< 10 nA) current above 150°C where the same happened to the N_2 annealed devices only above 170°C. From comparing the ON current, we can conclude that the trends are similar and the main effect of the environment is on the ultimate device annealing temperature before failure. Comparison of threshold voltage is plotted in *Figure 47*e (air) and *Figure 47*f (N_2). Here we see that device threshold voltage is generally shifted to more negative values in both cases. Long channel devices have slightly more

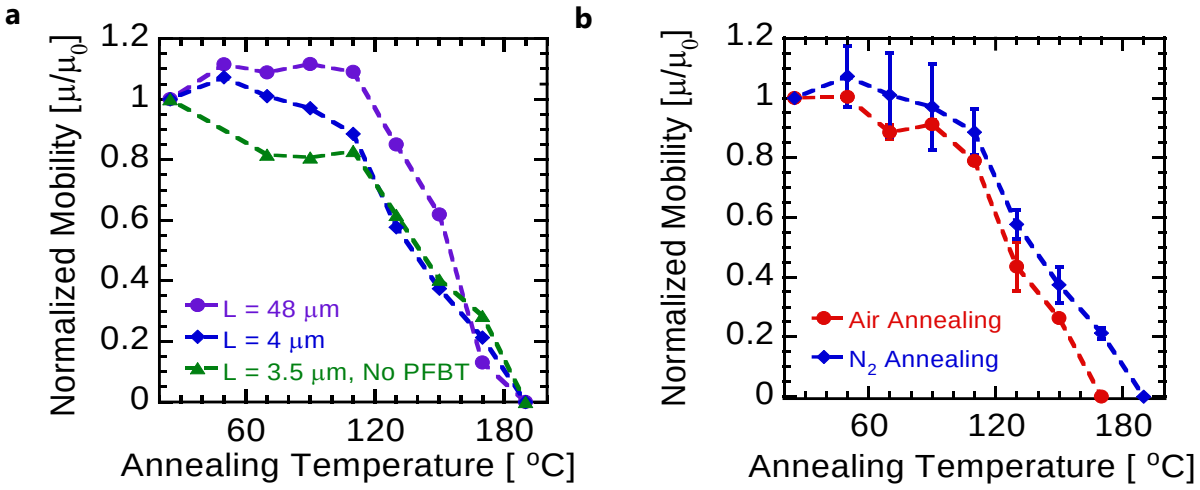


Figure 48: Mobility trend with annealing temperature. (a) Normalized mobility (μ_0 is the mobility in 25°C before annealing tests) for different channel lengths, annealed in N_2 environment. Transistor with no PFBT treatment is presented in green. (b) Comparison of mobility trend in air (red) and N_2 (blue) for PFBT treated transistor with 4 μm channel length.

predictable trend than the very short channel case. In summary, although we detected a few minor differences between annealing inside and outside the glove box, no significant change is apparent and devices can be annealed in air and obtain similar degradation behavior. The most significant parameter change is the failure temperature of devices which is lower in approximately 20°C when annealed in ambient conditions.

Normalized mobilities of devices as a function of annealing temperature are plotted in *Figure 48*. In *Figure 48*a we demonstrate the normalized saturation mobility of devices with short and long channel lengths. Initial mobility before annealing is considered as 1. As a reference, we also show device performance without PFBT treatment. We recognize that the relative mobility of the short channel lengths tend to degrade in more significant manner as temperature rises. Transistor with 48 μm channel maintain its performance (and even slightly improves) up to 110°C while the degradation in the 4 μm devices starts already at 70°C. At high temperatures, device degradation becomes similar for all cases and it might mot be related to channel dimensions (T> 150°C). The control device without PFBT shows worse degradation than the treated which implies that PFBT degradation

does play an important role in degrading device mobility when annealing. *Figure 48*b demonstrates an average mobility comparison between air (red) and N_2 (blue) annealing of 4 μm channel transistors. Although the transistors were encapsulated with 1 μm thick, thermally stable parylene diX-SR, one can identify almost constant degraded performance in the devices annealed at air. As an organic layer with limited barrier properties (moisture vapor transmission – 0.09 g·mm/m^2·24h at 37°C, oxygen transmission – 2 cm^3·mm/m^2·24h·atm at 23°C [136]), parylene encapsulation cannot provide a perfect barrier for preventing penetration of air molecules even at 50°C, which results in deteriorated performance upon heating the devices in air.

According to equation (12), we calculate the theoretical cutoff frequencies of devices with different channel lengths and plot them in *Figure 49*a. We present PFBT treated devices with 2.5 μm (red), 4 μm (blue), and 48 μm (purple) channel lengths and PFBT-untreated short channel transistors with 3.5 μm (green) channel length. As one can expect, devices with short channel lengths achieve higher cutoff frequencies. Transistors treated

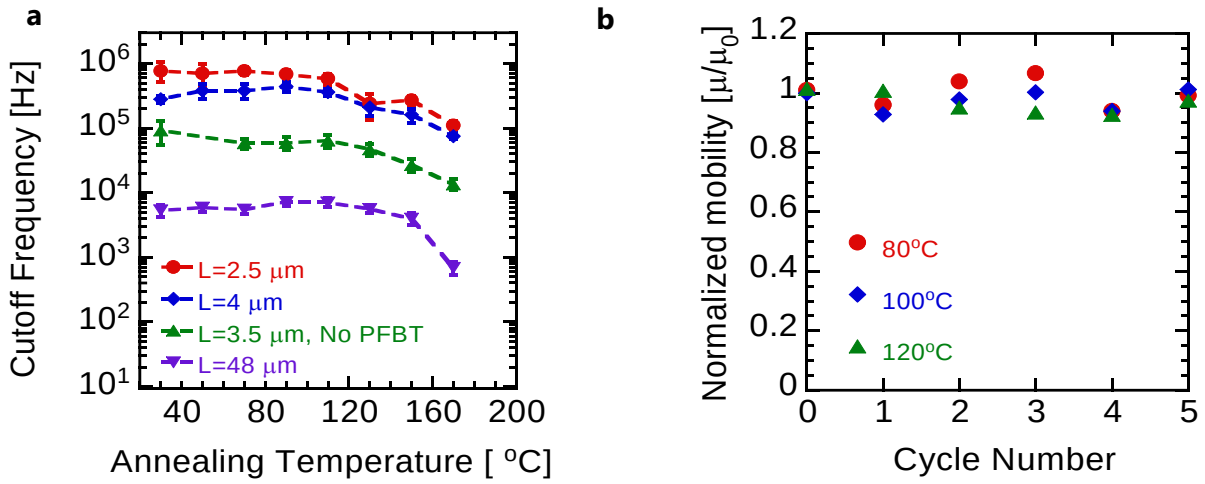


Figure 49: (a) Theoretical cutoff frequency of bottom contact transistors with different channel lengths after annealing at elevated temperatures. (b) Cyclic stability of 4 μm channel transistors. The normalized mobility of transistors that were repeatedly annealed at 80°C (red), 100°C (blue) and 120°C (green) is presented as a function of cycle number.

with PFBT obtain larger bandwidth than those which were not treated and with the same channel dimensions. Interestingly, devices with short channel can maintain high frequencies even after annealing at temperatures as high as 170°C. Transistors with 2 μm channel length obtain cutoff frequencies larger than 100 kHz at this temperature.

Cyclic thermal stability is crucial for transistors operation at high throughput rates and harsh environmental conditions such as thermal sterilization. Using a post annealing step at a specific temperature (i.e. stabilization temperature), we present a method to maintain transistors performance constant at temperatures lower than this temperature. We annealed devices at 150°C in glove box for 30 min. After their cooling down time (approximately 30 min), we performed electrical characterization. Later we repeatedly

annealed the devices at lower temperatures in N_2 environment. We evaluated cyclic heating tests at 80°C, 100°C and 120°C (*Figure 49*b). After cooling down to room temperature, we measured their effective mobility and transfer characteristics (Agilent

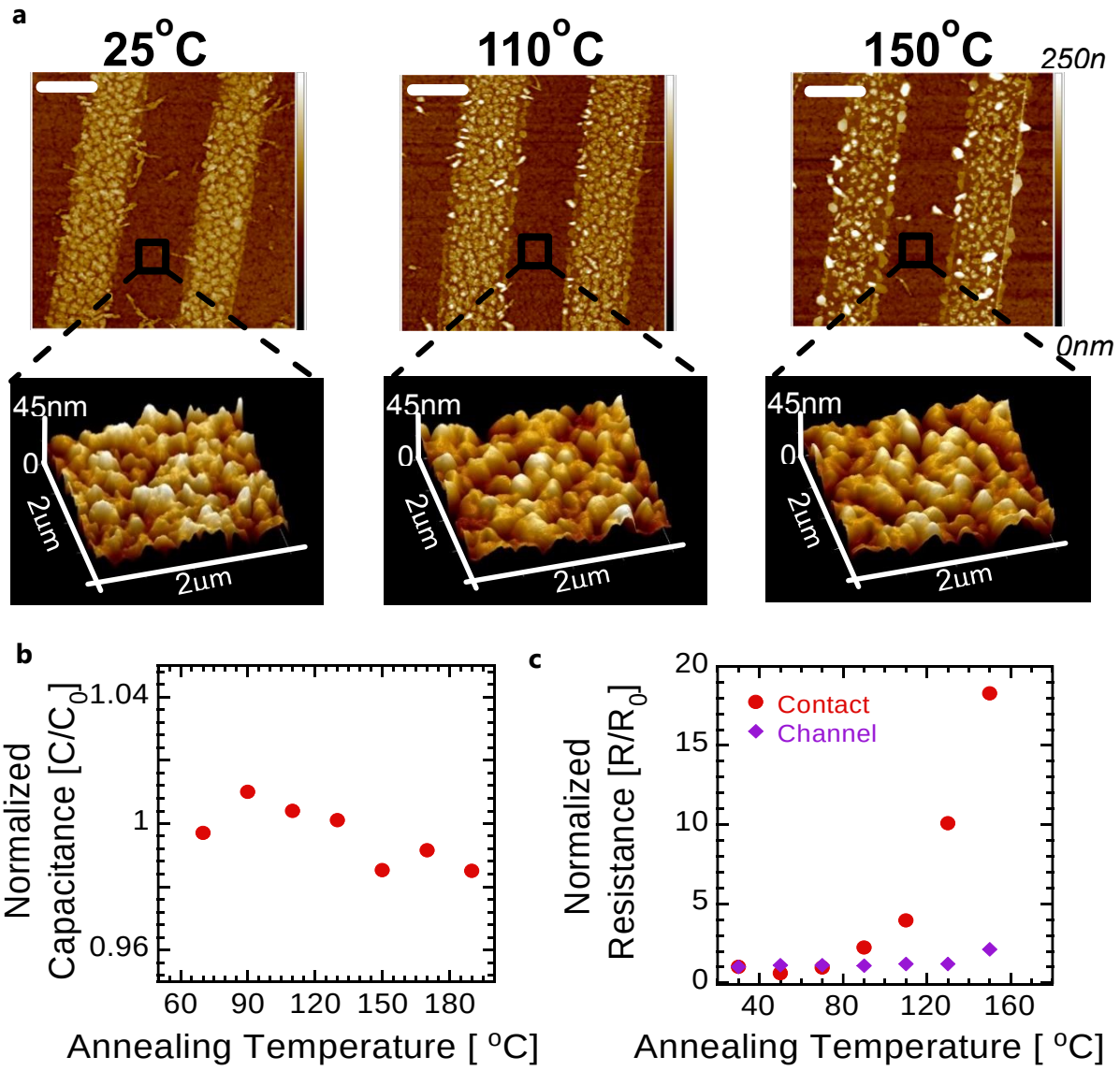


Figure 50: (a) AFM images of channel (upper, 15 µm2) and contact areas (lower, 2 µm2) measured at room temperature after annealing steps. For reference, the initial scan before annealing is presented (left column). Scale bars correlate to 3 µm. Relative changes in (b) parylene diX-SR capacitance and (c) device typical resistances as a function of annealing temperature.

Technologies 4156C). Devices with channel lengths of 3.5 µm were tested and the mobility was compared between the different cycles. We can observe device stabilization as mobility did not change more than 8% between cycles of various temperatures. Moreover, mobility converged into similar values after 4 cycles, even at different annealing temperatures, which implies a stable charge transfer mechanism at this level. This

stabilization ensures reliable transistor operation at temperatures lower than or equal to 120°C and under repeated heat cycles.

In order to gain better understanding on the thermal degradation mechanism, we observed the layer topology change using ex-situ atomic force microscopy (Bruker MultiMode V). We scanned DNTT on a transistor area of 15 μm^2 after each annealing step in N_2. In Figure 50a, we can identify a substantial change in semiconductor morphology on contact area as heating temperature increases. The arithmetic average of absolute values (R_a) increased from 18 nm at room temperature to approximately 29 nm at 150°C. The root mean squared value (R_q) was also dramatically affected by annealing. Rq values were changed from 22 nm to 35 nm at 150°C on top of the gold surface. This morphology change was not observed on the channel area which remained virtually unchanged (Figure 50a bottom row). Roughness measurements at room temperature obtained R_a and R_q values of 6.2 nm and 8.4 nm respectively while those values slightly decreased to 4.7 nm and 6.3 nm at high temperatures (150°C). The variation in roughness changes between the DNTT on the channel and contact area may imply on different degradation mechanisms between the two areas upon heating.

We carried out electrical measurements in order to detect changes in the substrate characteristics and channel area. Changes in the parylene diX-SR layer were investigated by measuring the capacitance of a MIM structure while annealing it up to 180°C. Parylene diX-SR thickness was approximately 500 nm in this layout with initial capacitance of 15.9 pF at 1 kHz. Capacitance values were almost constant and did not change in more than 2% even at the highest temperature measured (Figure 50b). On the other hand, transistor resistance showed a distinct trend between the channel and contact regions. Using the TLM method, we plot the channel and contact resistances as a function of temperature in Figure 50c. Here we can recognize a substantial difference between the two typical resistance values. While the sheet resistance remains practically unchanged up to 150°C due to the thermally stable parylene dix-SR substrate, the contact resistance clearly increases at high temperatures.

In summary, thermal stability of short channel organic transistors was investigated on ultrathin (1 μm) plastic substrates. Short channel devices, modified with PFBT self-assembled monolayer, were found to be durable up to 170°C with maintaining operation frequency above 100 kHz. The cyclic tests show that thermal annealing can stabilize mobility and operational frequency below the stabilization temperature. Using atomic force microscope, we observed topology change in contact areas after annealing above 110°C, which we relate to reordering of semiconductor molecules on the gold surface. This phenomenon increases contact resistance and degrades performance of bottom contact transistors, especially in the short channel case.

6.2 Discussion

Note in *Figure 49*a that cutoff frequency maintains larger than 100 kHz even after annealing at 170°C. This becomes possible mainly because of the thermal stability of parylene diX-SR (Figure 50b) and relatively constant channel resistance (Figure 50c). Thermal stability of OTFTs have been intensively examined for the device structures with the long channel and the top contact geometry [8,26,27] since these are less sensitive to changes of contact resistance induced by thermal processes. Indeed, we observed in AFM characterization (Figure 50a) large change in morphology on contact areas after the annealing above 110°C and, for this reason, the short channel devices degrade more rapidly than the long channel transistors (*Figure 48*a). However, their small lateral dimensions and moderate change in mobility kept their bandwidth large at high temperatures.

It is interesting to note that the utilization of PFBT does not seem to cause further degradation in device mobility over temperature. Gold modified surface with PFBT were reported to change their work function when increasing temperature above 100 °C and make them more shallow [124]. The thermally-modified work function might increase the charge injection barrier and reduce the effective mobility value. However, from *Figure 48*a we see that contact-modified and unmodified devices with same channel lengths have similar mobility degradation trend when increasing temperature. The green curve represents the normalized mobility of a transistor with 3.5 μm channel length that was not modified by PFBT. The blue curve plots the normalized mobility behavior of a contact-modified device with 4 μm channel length. Both devices show very similar mobility trend at temperatures above 110°C and hence it seems that PFBT modified devices do not suffer further degradation as a result of changes in the SAM layer. Future investigation should be conducted to reveal the mechanism behind this observation.

We would like to emphasize that the choice of materials and transistor structure was essential to simultaneously achieve high cutoff frequency (> 100 kHz) and high temperature tolerance (less than 10% of mobility change at 100°C) for OTFTs on ultrathin films. First, parylene diX-SR was chosen as a thermally stable material with high melting temperature (303°C [28]) and low water absorption rate (< 0.1% during 24 hours [25]). Second, both the top gate metal layer and parylene diX-SR gate dielectric layer are functioned as an encapsulation layer. It is interesting to note that the OTFTs with the bottom contact structure exhibit reasonable thermal stability equivalent to those with top contact structure. In the top contact structure, the semiconductor is deposited solely on a dielectric layer which allows a uniform molecular growth and orientation. On the other hand, in the bottom contact structure the semiconductor is deposited on two different materials, namely, the semiconductor and the metal contacts. In this case the semiconductor has two different growth modes which create barrier in charge transfer

mechanism [18]. The organic semiconductor is more sensitive to dewetting phenomena upon heating on top of the metal areas [15,16]. The non-uniformity of the film and the dewetting tendency on metals are expected to affect more the charge mechanism degradation in the bottom contact structure compared with the top contact one. Nevertheless, the choice of thermally stable materials for the substrate, gate dielectric and semiconductor could maintain device performance even in the bottom contact structure.

7 Ultrathin circuits

7.1 Pseudo-CMOS architecture

7.1.1 Circuit design

The pseudo-CMOS design have recently been proposed as a design library for organic electronics, compensating differentiation in threshold voltage and the lack of reliable, environmentally stable complementary technology [139,140]. The design allows fabrication of high level circuit elements, such as inverters and logic gates, with the use of only p-type OTFTs. Using the pseudo-CMOS architecture one can realize higher device

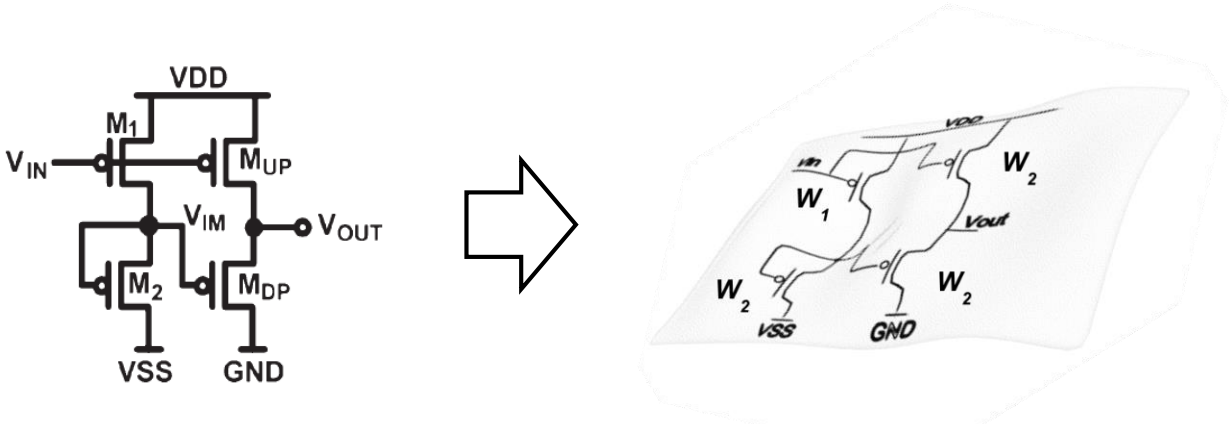


Figure 51: Pseudo-CMOS D-type inverter design [139] (left) and an illustration of inverter on the ultrathin, flexible film. The symbols W_1, W_2 denote the channel widths of the corresponding transistors.

gain and adjust the operation point of circuits. In addition, pseudo-CMOS design provides lower power consumption compared with other p-type only technological implementations. As an elementary and essential cell design, the pseudo-CMOS inverter is often used to demonstrate logic operation and ring oscillators.

The pseudo-CMOS inverter, when based on p-type technology, comprises of two important components: the pull up network, where input voltage is inserted (M_1 and M_{UP} in Figure 51) and from two functional transistors that are used to adjust switching point and provide the inverters load (M_2 and M_{DP} in Figure 51). For a p-type inverter, V_{DD} is a positive supply voltage that determines the inverter's high level output voltage. V_{SS} is another supply voltage that is used to compensate for V_{TH} degradation or change switching point of the circuit. V_{SS} is usually set to 0V or smaller to provide strong circuit pull down. The actual switching voltage of the inverter is determined by the sizing ratio of M_2/M_1, here defined as $\alpha = W_2/W_1$.

Here, we will test the viability of pseudo-CMOS technology for the bottom contact, parylene based transistor. We will apply the pseudo-CMOS inverter with short channel lengths on ultrathin films and evaluate its performance. We will measure the inverter's gain with different architectures, inverters' uniformity and their thermal stability. Switching voltage adjustment by double gate structure can be found in the appendix.

7.1.2 Inverter fabrication

We designed four pseudo-CMOS inverters on a 30 mm^2 area using a CAD VectorWorks Ltd. software (Figure 52a). The design is based on the layout proposed in Figure 51. Each of the transistors in the logic unit is based on the single transistor structure we described earlier with 70 nm parylene diX-SR gate dielectric. We chose to fabricate this set of inverters with $\alpha=3$, previously reported as a successful design rule [140]. The input transistor, M_1, has W_1/L_1 ratio of 1500 μm/3.5 μm. Other transistors in the design has

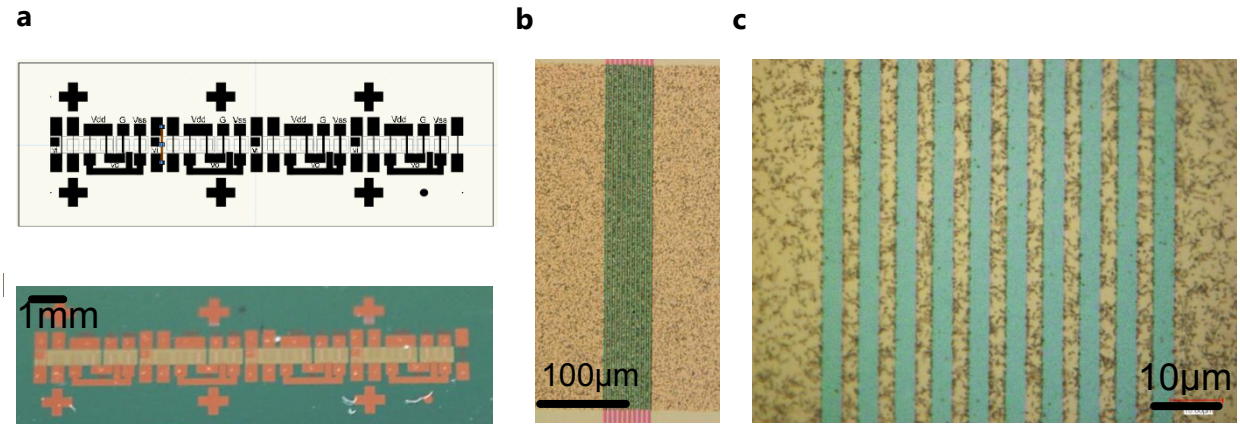


Figure 52: (a) Circuit design (top) and fabricated device (bottom) of 4 pseudo-CMOS inverters. (b) Magnification of semiconductor area and (c) channel area of transistor with W/L=4500 μm/3.5 μm. Inverters were fabricated with identical α value of 3.

larger channel width of $3W_1$ with the same channel length. Microscopic image of the semiconductor area and magnification of channel region of M_2 are plotted in Figure 52b and Figure 52c respectively.

Transfer characteristics of the 4 pseudo-CMOS inverters are plotted in *Figure 53*. We scan the input voltage from 0V to 10V and changed the supply voltages. V_{DD} ranged from 3V to 8V (denoted on graph) and in all cases $V_{DD}=-V_{SS}$. The GND pad was connected to the measurement setup's common port. *Figure 53*a-d present the transfer curves of the inverters as they appear from left to right in the circuit design (Figure 52a). The plotted voltage scans (red) focus on the switching regime of the inverters and are made with 10 mV scan step size. The right hand side y-axis represents the inverter absolute gain (blue), defined as $|GAIN| = \left|{}^{dVout}/_{dVin}\right|$, on a linear scale.

We observe uniform transfer characteristics of the pseudo-CMOS inverter cells fabricated on 30 mm^2 area. The 4 inverters show uniform switching point of 7.1±0.3V with supply voltage of $V_{DD}=-V_{SS}=8V$. The maximal gain obtained for this supply voltage ranged from 35 to 47 which corresponds to uniform gain level of 32±1 dB. Operating in lower voltages yielded lower gain but still showed uniform characteristics. For example, for $V_{DD}=-V_{SS}=5V$, switching voltage was 4.2±0.2V and maximum inverters' gain was 29±2 dB. Those results are amongst the highest gain achieved for pseudo-CMOS inverters [31,139,140]. We also note that our inverters maintain their functionality even with low operation voltage of only 3V and obtain good gain characteristics.

The uniformity of inverters and their high gain were primarily determined by our transistor regularity. To allow high inverter gain, operation regimes of the transistors should be correctly aligned by similar threshold voltage. The small variation we demonstrated in section 4.2.5 (e.g. *Figure 34*) could guarantee the correct working points of transistors. Moreover, device uniformity over 4 different inverters was achieved thanks

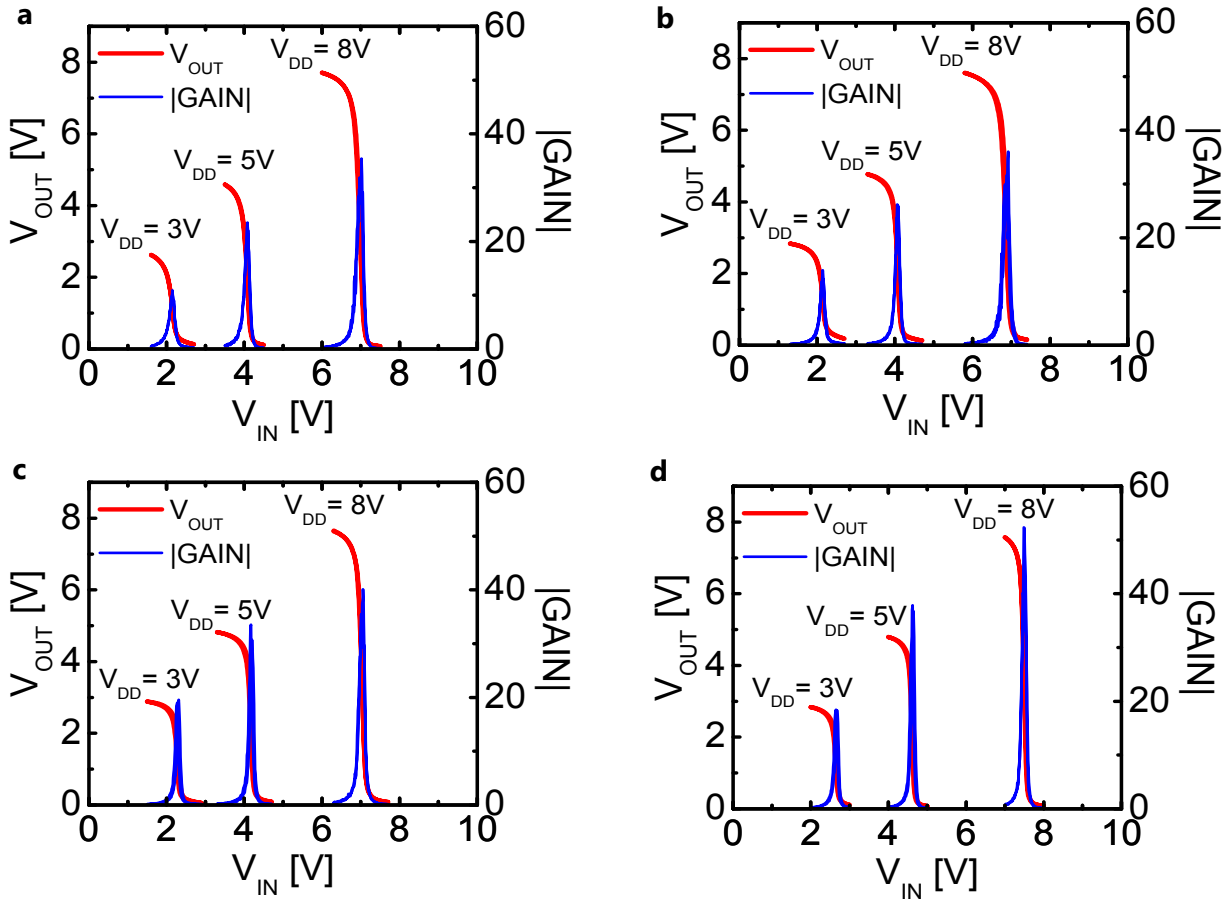


Figure 53: Uniform output characteristics (red), gain (blue) and switching voltage of the four pseudo-CMOS inverters, (a)-(d), presented in Figure *52*. Data are presented for supply voltage (V_{DD}) of 3V, 5V and 8V. Voltage scan step is 10 mV.

to the common characteristics of 16 transistors on the same substrate. This uniformity is represented by standard variation of only 0.3V in threshold voltage of varying channel widths, operating at 8V. Nevertheless, in this device characteristics we notice that the trip point (where $V_{IN}=V_{OUT}$) is far from the high gain voltage due to the specific pseudo-CMOS design we utilized. As future prospect, further optimization and simulation of device structure will be needed.

7.1.3 Post-annealing gain enhancement

In chapter 7, we demonstrated how post annealing process can change our single transistor characteristics such as mobility, threshold voltage and ON current. We also demonstrated that our transistors showed very good durability up to 170°C without fail. Furthermore, important aspects of device characteristic for circuit implementation, namely operation frequency and cyclic stability, could be maintained even at high temperatures and several cyclic tests. An interesting aspect is the functionality of those devices in logic gates upon thermal annealing. In this section we will test the behavior of inverters when annealed up to 150°C. Inverter gain and switching point will be examined and compared to initial values.

Figure 54a plots initial inverter characteristics of a tested device with $\alpha=3$. The double sweep shows very clear repetition of the transfer curve with no hysteresis and switching point of 7.5V. The inverter was composed of transistors which were fabricated with 85 nm gate dielectric by CVD of parylene diX-SR in high vacuum. The W_1/L_1 of the input transistor was determined to be 1500 μm/ 3.5 μm. We fabricated 3 different inverters with $\alpha=3$, 6 and 10 and tested them for before and after annealing steps. The highest initial gain was obtained for the ratio of $\alpha=3$ which corresponds to previous results [139,140].

We annealed the devices in N_2 environment from 70°C to 150°C and evaluated their transfer characteristics for gain and switching point. In Figure 54b we plot the inverters' gain development upon the post annealing steps. The different α values are denoted by the different colors for $\alpha=3$ (red), $\alpha=6$ (blue) and $\alpha=10$ (green), According to this plot, inverters gain seem to increase with temperature for all α values obtaining up to 170% at 150°C. The highest gain for $\alpha=3$ could reach 15 which is 150% enhancement from the original value. After reaching the maximal gain at 150°C, we annealed the inverters at the 100°C for 5 annealing cycles to check its stability at the same temperature. In accordance with the single transistor cyclic stability, inverter's gain was not changed compared with the first cycle. We detected similar behavior for the switching voltage. In addition to the single transistor thermal stability, this test assures that inverters can improve their performance with device annealing and keep this performance stable upon additional annealing steps.

In *Figure 55* we give a more descriptive plot of inverters characteristics with changing temperature. Each row represents a specific α value as it appears in the bottom left corner

of the graphs. In the left column we record the double V_{OUT}-V_{IN} sweep of devices for different annealing temperatures. The right column shows the gain behavior for different temperatures, denoted in different colors. We note that the switching voltage is negatively shifted as we enlarge α. Switching voltage changes from ~7.5V with α=3 to

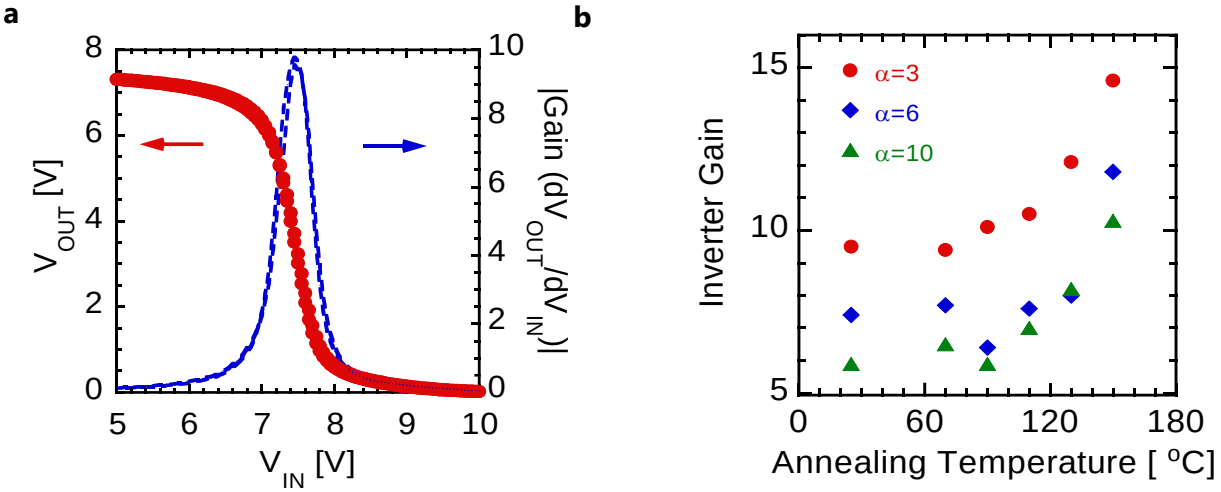


Figure 54: (a) The transfer characteristics (V_{out} vs. V_{in}, red curve) of the fabricated inverter with 3.5 μm channel length and $\alpha=W_2/W_1=3$. Inverter gain (dV_{out}/dV_{in}) is plotted in blue where maximum gain of 9.5 at 7.5V is obtained. (b) Inverter's gain increase as function of annealing temperature for 3 different inverter architectures.

~6.5V with α=10 at room temperature. At the right column, we can also clearly observe the gain reduction for large values of α at 30°C.

Generally we detect very consistent switching voltage, even after device annealing. The best consistency with temperature was identified for α=6. Only one anomaly was observed in the case of α=10 and 130°C. Here we see a shift in the maximum gain voltage. However, after an additional annealing step the switching point retained its original position. The reason for this consistency is the uniform behavior of devices upon annealing. Under small variation of the threshold voltage, the switching voltage is mainly affected by the 'synchronization' of transistors when moving from one operation mode to another. As long as the relation between threshold voltages is kept identical we can expect similar switching properties.

We can conclude then the thermal stability of the pseudo-CMOS inverter is improved by a simple post-fabrication annealing. The inverter gain is strongly influenced by the threshold voltage and the saturation resistance of the transistors. After annealing, we could see negative threshold shift (*Figure 45*) and an increased output resistance (R_{DS}) that enhances the inverter load and in turn improves the total gain. This emphasizes the importance of thermally stable short channel transistors as we can improve inverter gain by a annealing in addition to keeping the high frequency operation of circuits. In accordance with the single transistor stabilization process, the inverter gain shows stable

performance after cyclic tests at temperatures below 150°C which demonstrates the process reliability.

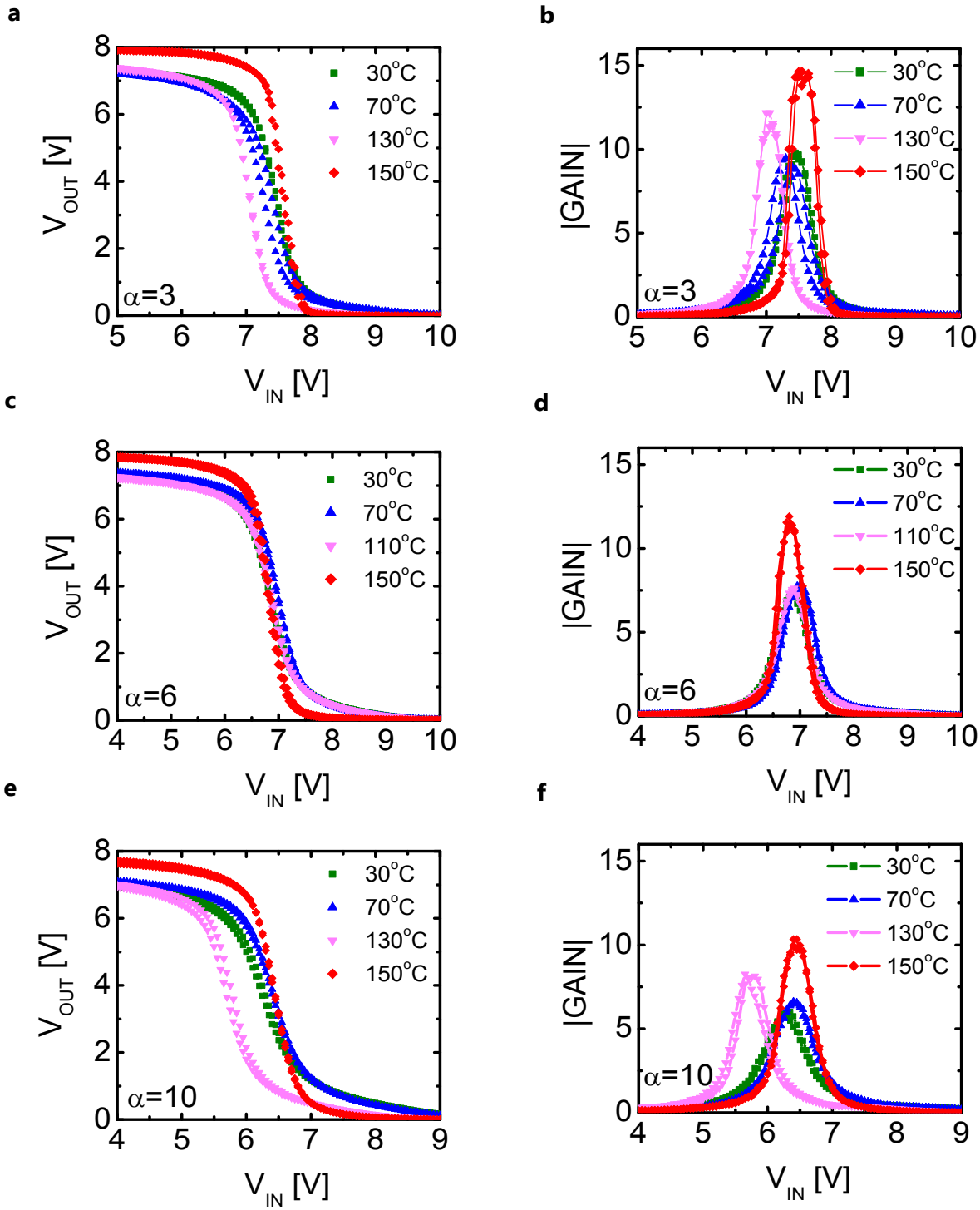


Figure 55: Transfer characteristics and absolute gain, $|dV_{out}/dV_{in}|$, are plotted for α=3 [(a) and (b), respectively], α=6 [(c) and (d), respectively] and α=10 [(e) and (f), respectively]. The effect of post-annealing can be noted at different temperatures according to the color set.

7.1.4 Threshold voltage control by double gate structure

For circuit applications, control of threshold voltage is crucial for their proper operation [114,141–143]. Correlation of threshold voltages between different circuit components is essential for correct operation modes and current/voltage levels. For organic transistors, shift of threshold voltage may occur over time due to environmental and molecular changes. This change over time creates improper functioning of the circuit and affect its reliability. For this reason, post-fabrication controlling and tuning of threshold voltage is important for organic circuit operation.

For thin film transistors, the double gate architecture is a common method for threshold voltage control after device fabrication. In this layout, the charge distribution in the channel is manipulated by two gates simultaneously (*Figure 56*a). In this sense, one gate is utilized for device switching and determination of transistor operation modes while the other gate is fixed to provide the desired spatial charge distribution and threshold voltage. We have realized a symmetric structure of thin film layers, consisting of thin gate (20 nm of gold) and gate dielectric (60 nm of parylene diX-SR) around the transistor channel (*Figure 56*a). After transistor fabrication we tested the double gate

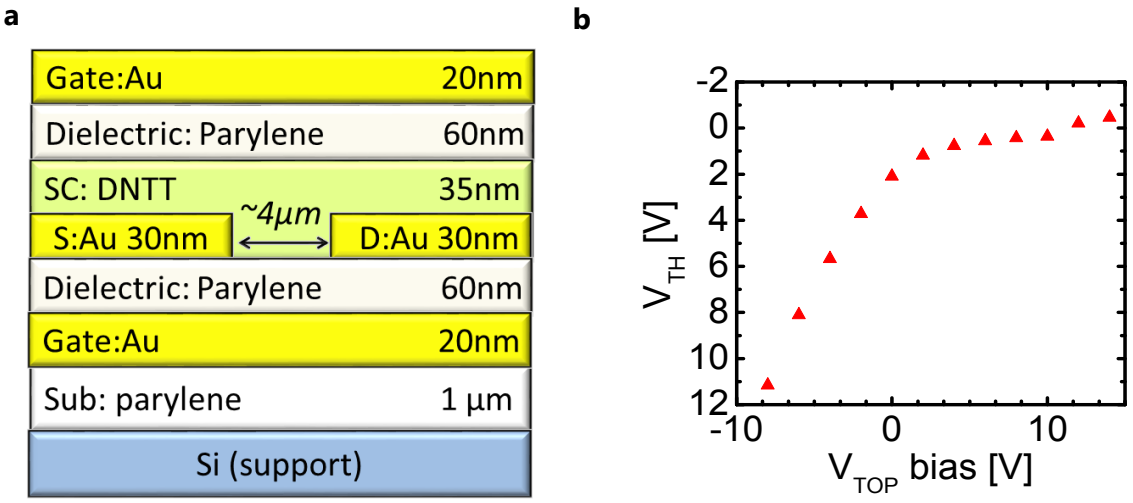


Figure 56: (a) Transistor architecture in the double gate structure. (b) Systematic shift in threshold voltage as top gate voltage changes. Threshold voltage in a wide range from 12V – 0V can be achieved.

structure by applying a constant bias voltage on the top gate (V_{TOP} bias) and scanning for the transfer curve of the OTFT. By changing the value of the bias voltage we could detect a clear shift in threshold voltage, as plotted in *Figure 56*b. The shift in threshold voltage occurs as a result of change in the accumulated charge carriers in channel; when negative bias voltage (top gate) is applied, concentration of holes in channel increases and the transistor can operate already in positive bottom gate voltages. The double gate method allows us to tune the threshold voltage between +12V to 0V while changing the bias voltage from –10V to +10V.

In *Figure 57*a we present the transfer curve (double sweep) trend as the top gate bias voltage changes. We can identify the shift in threshold voltage of the curves as the top voltage turns more positive. Note that the 'OFF' current of the transistor is higher when we apply negative top gate bias due to the additional charges induced in the channel. Accordingly, 'ON' current at –8V is higher. Larger hysteresis in negative bias voltage is observed in the transfer curve of the transistor. This phenomenon is related to the increased number of charges that are trapped in the channel at negative bias. In this case, additional conduction path is formed that maintain the high current in the reverse sweep. In positive bias the range for controlling the threshold voltage is smaller, however we can get high ON/OFF ratio for the device and low hysteresis.

In order to show the application for circuit, we fabricated a Pseudo-CMOS inverter based on the double gate principle. We fabricated similar circuits to the description in Section 7.1.2 , with the addition of top gate for all transistors. The transfer characteristics of the circuit with different bias voltages are plotted in *Figure 57*b. We can detect a systematic change in switching voltage of the circuit as we apply positive bias on the circuit. Bias of 20V locates the switching voltage of the circuit at ~2V where bias of 10V makes the inverter switch at ~3.7V, under supply voltage of V_{DD}=8V. We can also observe a change in gain of the inverters as a result of this bias. This method of changing the switching point by application of double gate is important for circuit design and performance. For example, it can change the gain and stability of a closed loop amplifier As we will show later in Section 7.2.4

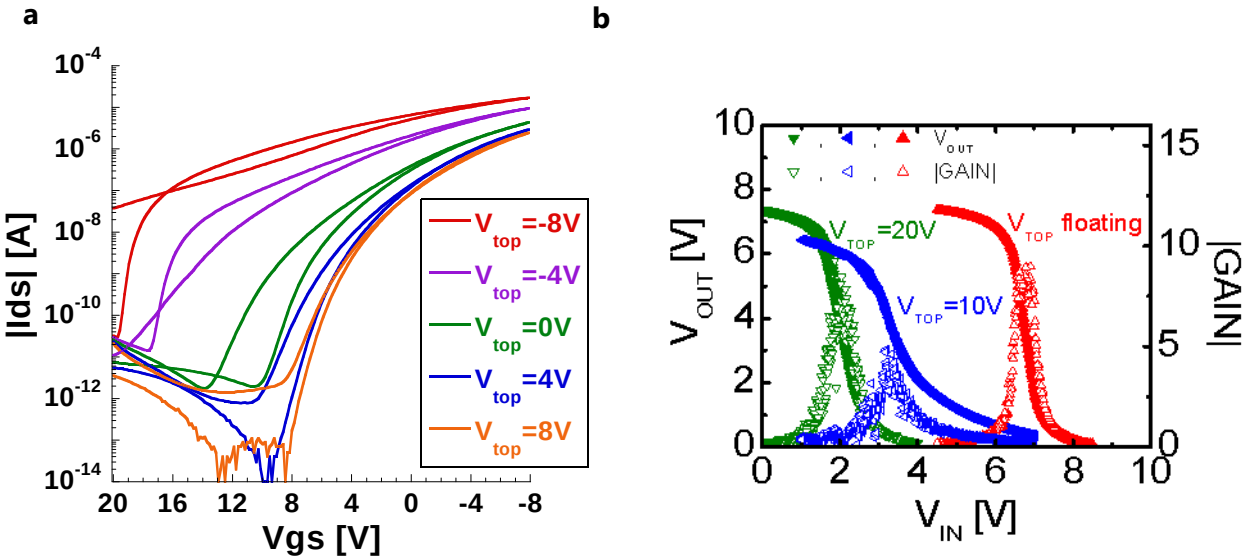


Figure 57: (a) Transfer curves of the double gate structure while changing the top gate voltage bias from –8V to +8V. Shift in threshold voltage and change in hysteresis properties is observed. (b) Change of top gate voltage of all transistors to 10V (blue) and 20V (green) shifts the original output curve (red) to the negative direction and creates preferable switching voltage.

7.2 Amplifier fabrication

7.2.1 AC coupled amplifier

For fabrication of amplifiers for bio-signal measurements, reliability of signal is of utmost importance. Any distortion in the amplified signal is undesirable and can lead to misinterpretation of the acquired data and wrong conclusions. Although previously reported pseudo-CMOS inverter based amplifiers show phenomenally high gain of more than 100 times signal amplification, they have poor frequency response [31]. The reported amplifiers show band pass behavior at roughly 20-100 Hz where signals in other frequencies are amplified at different rates. Using pseudo-CMOS as preliminary amplifier near the recording site would distort the recorded signal and lead to wrong information temporal information. Recently the AC coupled design was adopted by Fuketa et al. [144] who demonstrated good low-pass filter behavior with constant frequency response up to ~40 Hz. The AC coupled design (Figure 59) allows higher amplifier gain than the diode-load inverter based amplifier and reliable frequency transmission. However, the main disadvantages of this amplifier is the low cutoff frequency (~40 Hz) and the large area required by a capacitor implementation.

Here we demonstrate an improved frequency response for the AC coupled amplifier design and reduced area implementation. The desired frequency range for biological information from the body is estimated to be not higher than 600 Hz for neural activity recording [145]. We will use the high frequency characteristic of our short channel

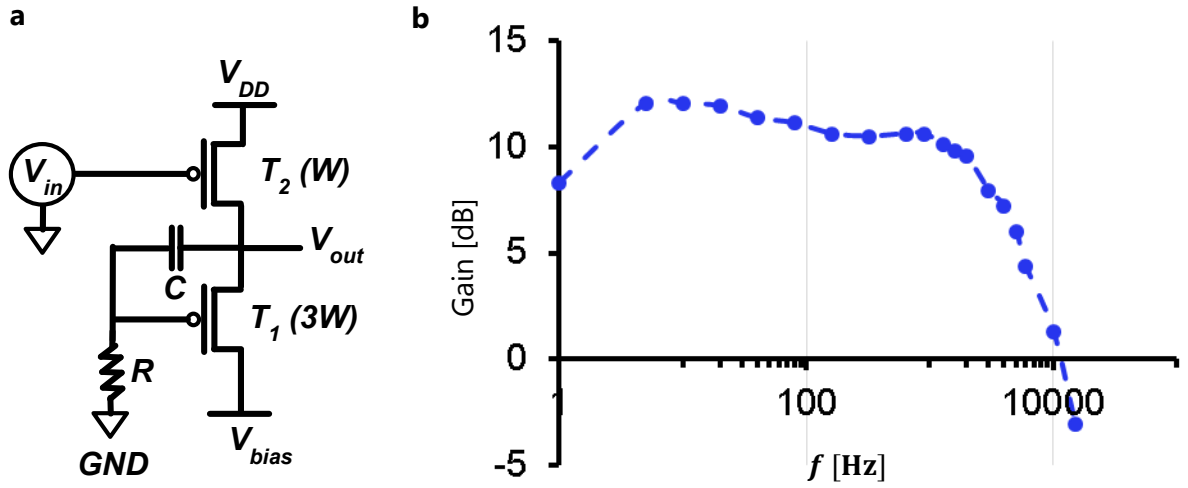
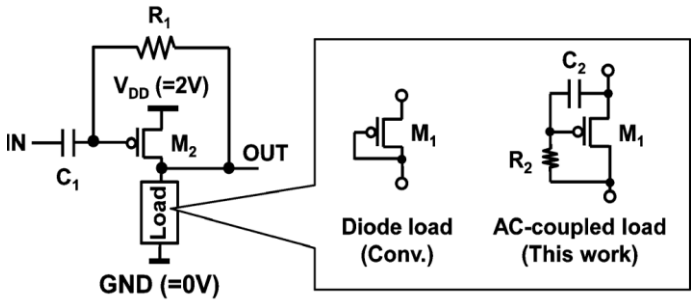


Figure 58: (a) Circuit schematic of AC coupled amplifier utilizing bottom contact, short channel transistors. W and 3W denote the channel widths of the implemented transistors. R and C are external resistor and capacitor with values of 6.8 MΩ and 100 nF respectively. (b) Frequency response of the fabricated amplifier demonstrating nominal gain of ~12dB and flat low pass band behavior up to 2.5 kHz.

transistors to enhance the amplifier bandwidth. In addition, we will utilize a high capacitance technology with anodizing aluminum oxide in a multilayered structure. The entire device will be integrated with direct fabrication on a 1 μm thick parylene diX-SR substrate, allowing implementation of large area amplifier fabrication in a cost effective manner.

In Figure 58 we present a proof of concept to the amplifier fabrication using the bottom contact transistor on ultrathin films. We connected two short channel transistors with 3.5 μm channel length and channel width of 5000 μm and 15000 μm (W and 3W in Figure 58a respectively). The transistors were fabricated on 1 μm parylene diX-SR film. Through an external circuit connection, we integrated fixed value ceramic capacitor and resistor in a lead arrangement to realize the amplifier circuit. The capacitor and resistor values were 100 nF and 6.8 MΩ respectively. V_{DD}=6V and V_{BIAS}=-7V and GND port was connected to the common circuit ground. Input voltage was generated with signal generator as a biased AC signal of 5±1V. Output voltage was recorded using an oscilloscope and gain was calculated using the relation $20\log|{}^{V_{OUT}}/_{V_{IN}}|$ where V_{OUT} and V_{IN} are the output and input AC signal amplitudes respectively. The gain measurement are plotted in Figure 58b. We see that a uniform frequency behavior with amplifier gain of 12 dB can be achieved in the range of 1-2500 Hz. The amplifier presents good signal gain and relevant frequency response for any *in-vivo* signal. Practically, the fabricated ultrathin amplifier is a hybrid implementation of an amplifier and a low pass filter in the appropriate frequency range for biological signal measurements, on one device.



$$A = \frac{g_{m2}}{g_{ds1}+g_{ds2}}$$

$$f_L = \frac{1}{2\pi RC}\frac{g_{m2}}{g_{ds1}+g_{ds2}}$$

$$f_H = \frac{g_{ds1}+g_{ds2}}{2\pi CL}$$

Figure 59: AC coupled amplifier design and basic equations as they appear in [144].

7.2.2 Fabrication on ultrathin film

7.2.2.1 Utilizing parylene diX-SR capacitors

For fabrication of the amplifier, entirely on the ultrathin film we need to transfer the external capacitor and resistor to the parylene diX-SR substrate, in addition to the inverter's transistors (M_1 and M_2 in Figure 59). For the resistor utilization, we chose to fabricate a weak transistor (small W/L) and operate it in its OFF state (V_{GS}>0). In this way, we can obtain a resistor of several MΩ for circuit implementation. For the capacitor fabrication we should choose a reliable, ultrathin film compatible and high capacitance per area technology. One of the most natural methods is to implement an ultrathin

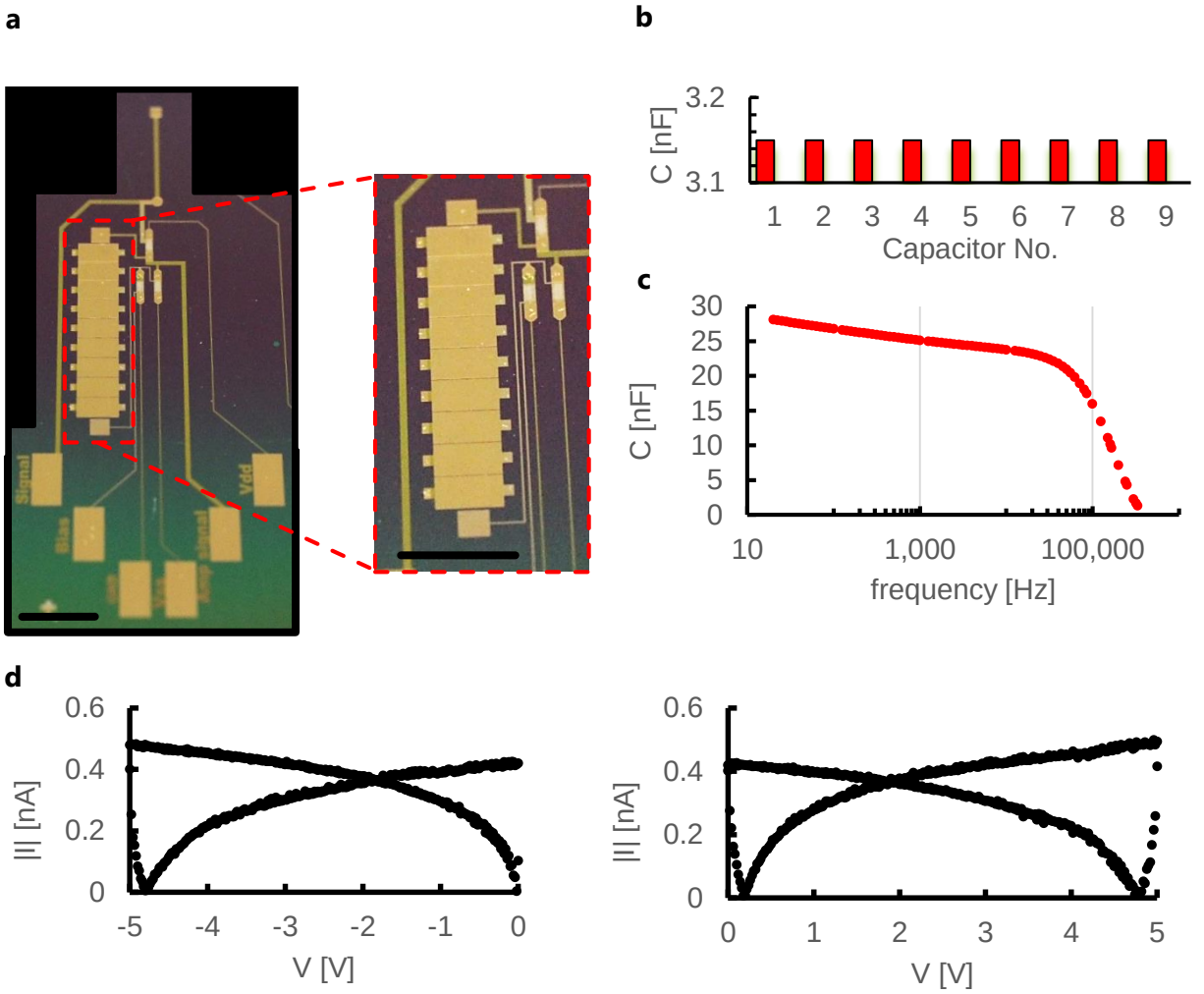


Figure 60: (a) Amplifier (left) and magnified capacitor (right) optical photographs. Scale bar is 5 mm. Capacitor consists of 9 small capacitor elements which are connected in a post fabrication step to improve device yield. (b) Basic capacitors capacitance and (c) final capacitor frequency response. (d) Absolute leakage current of capacitors with negative and positive bias between –5V and +5V.

parylene diX-SR which can be easily integrated with our transistors' structure. The capacitors can be fabricated in the same layer as the transistors' gate dielectric and save time and process complexities. However this implementation suggests relatively low capacitance per area (~50 nF/cm^2) for reliable fabrication over large area (see Appendix for details). On the other hand, metal oxide technology provides high capacitance per area for reliable implementation over large area [16]. Metal oxides often have large dielectric constants and can be reliably deposited with small thicknesses in the order of 10 nm.

Parylene capacitor can be used in the amplifier circuit in an effective manner. The parylene diX-SR can be deposited using high vacuum CVD process in ultrathin films (< 100 nm) and provide good capacitance per area values. Another important advantage of using parylene capacitors in our case is the ability to integrate the capacitor during the transistor fabrication (in the same step of the gate dielectric) and save time, cost and process complications. In *Figure 60a* we demonstrate a possible fabrication of parylene capacitor as part of the amplifier design. The capacitor consists of 9 small capacitive elements of 2x3.5 mm^2 which are connected in an additional post-fabrication step after validating their yield. The need in this type of post fabrication connection arised from the fact the parylene is deposited outside the cleanroom and dust contaminations used to reduce the capacitor yields when reducing dielectric thickness. Nevertheless, we could fabricate reliably 9 working elements with identical capacitance of 3.15 nF each (*Figure 60*b) utilizing 60 nm parylene layer. This value represents capacitance of 45 nF/cm^2 for the dielectric layer. By connecting the nine elements together we could achieve total capacitance of approximately 28 nF over area of 65 mm^2 (*Figure 60*c). The capacitor shows excellent I/V curve in a scan between −5V and +5V (*Figure 60*d). A symmetric response was recorded with low leakage current between capacitor plates with the maximum of 500 pA.

Although the parylene diX-SR capacitor shows very good characteristics, its main disadvantage compared with the selected implementation of AlOx capacitor is its size. Parylene diX-SR is a low-k dielectric material (dielectric constant ~3) and with deposition of ~50 nm, capacitance of ~50 nF/cm^2 can be achieved. In the following we will present an alternative technology, presenting higher capacitance per-area to reduce amplifier size.

7.2.2.2 Utilizing AlOx capacitors

AlOx is a good candidate for integration on large area with our amplifier circuit. AlOx was shown to be suitable for fabrication on ultrathin films and provide large capacitance per area (~100 nF/cm^2) on flexible substrates [7]. In order to operate our amplifier with a low transmission frequency starting at 1 Hz, a value of at least 100 nF should be obtained for the integrated capacitor. This value is realized both from the theoretical calculations and from the circuit demonstration we conducted with external components. However, the value can be also tuned by reducing amplifier gain and increasing resistance value (Figure

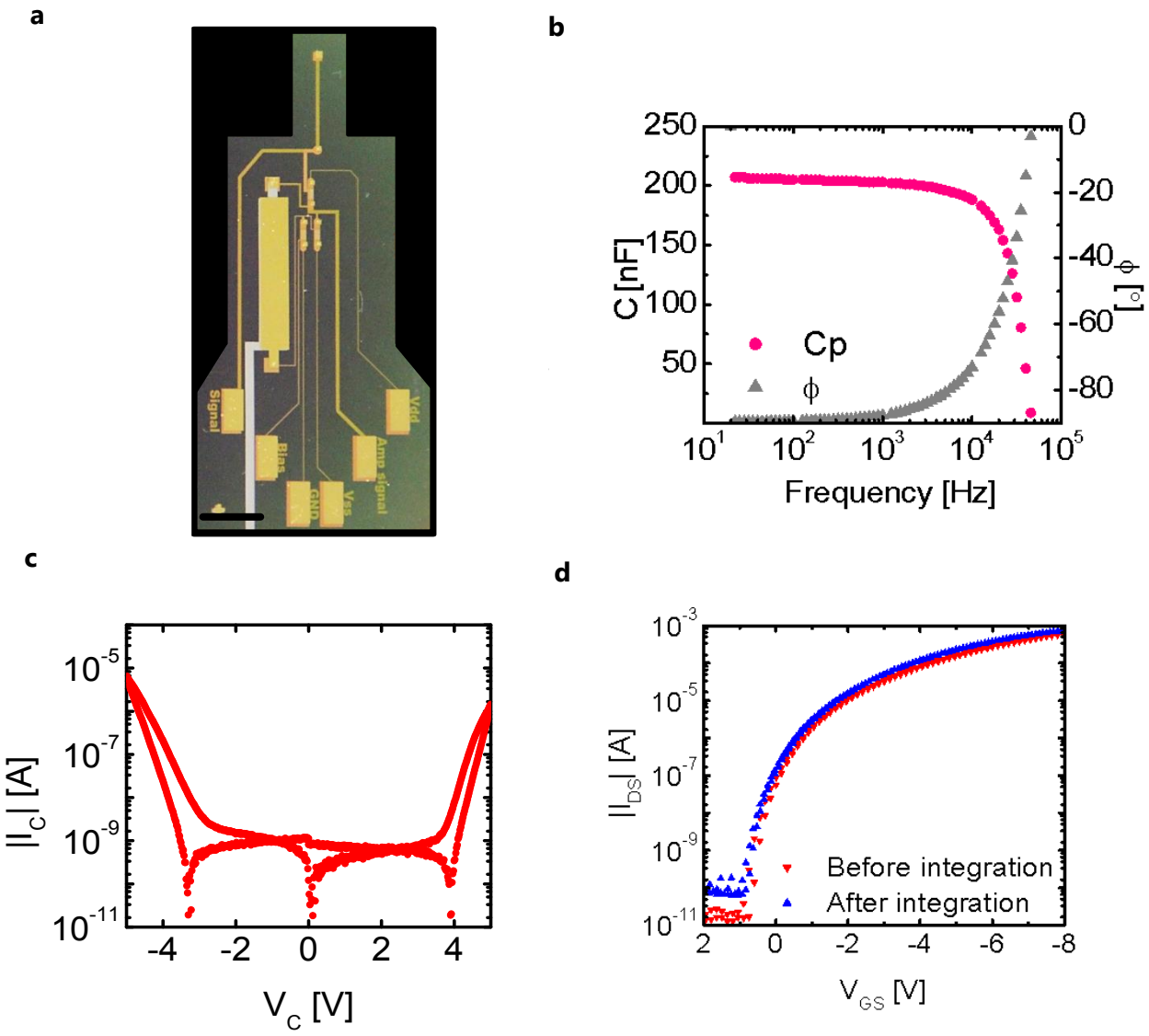


Figure 61: (a) AlOx capacitor integrated amplifier optical photograph. Scale bar is 5 mm. (b) AlOx capacitance value (pink) and the impedance phase (grey) versus frequency. (c) Capacitor I/V curve between -5V to 5V. (d) Transistor transfer characteristics before (blue) and after (red) anodization process.

59). In addition, the capacitor should have low leakage current at the operation voltage between 5-8V, according to the operation voltage of our transistors. The AlOx in our process is estimated to be in thickness of between 10-20 nm for anodiztion voltage of 7-10V. Those values predict that the AlOx capacitor should have approximately 10 times larger capacitance per area than the parylene implementation. As a result, we chose to fabricate our devices with the AlOx technology and reduce the effective amplifier size significantly.

We designed a process to form an AlOx layer that will meet all those requirements. For increasing the reliability of the process we adopt the anodization technique. Anodization forms a metal oxide layer on top of an anodic metal layer by introducing a chemical reaction between ions in the solution and the metal (see appendix for details). Anodization is a reliable process over large area and can form the dielectric layer in various thicknesses, determining the layer's capacitance and breakdown voltage. For our requirement of operation between 5-8V, anodization voltage of at least 7V should be conducted. The breakdown voltage is calculated by the anodization voltage added to the native oxide voltage drop (~1.6V). These conditions yield a capacitance per area of 500 nF/cm^2 for the AlOx capacitor. Hence, we designed the total area of capacitor to be of 60 mm^2 and obtain 200 nF for the circuit. In *Figure 61*a, we present the integrated circuit of the amplifier on the ultrathin film. The capacitance frequency dependence is plotted in *Figure 61*b and shows a capacitance value of 200 nF up to 10kHz, which matches our area expectations.

The two inverter transistors were designed to have large W/L of 25000 μm/ 3.5 μm to increase their transconductance value and frequency response. Mobility of devices was estimated to 0.1 cm^2/V·s. Dielectric thickness was 60 nm and transconductance approximately 0.2 mS. The resistor-like transistor was designed and fabricated with smaller W/L of 2000 μm/ 20 μm to increase its resistance. The maximal transconductance of this transistor was 6 μS. In *Figure 61*c, the I/V scan of the capacitor determines the voltage range of the capacitor between -5V and 5V as the current does not exceed 10 μA at those voltage level. We set this value as a result of the saturation currents of transistors during circuit operation which is between 100 μA to 1 mA.

An important issue for the integration of our transistors with AlOx capacitor is the process compatibility. Our transistors are based on photolithography process which involves basic solutions for development and organic solvents for lift off process. An of one component's process on the other. During our integration we have found out that the AlOx is very sensitive to the developer and PFBT solution. When fabricated first, the capacitor was damaged heavily after completing transistors fabrication. On the other hand, when we fabricated the capacitor after forming the transistors, we hardly noticed any change in transistors performance. In *Figure 61*d, we plot a typical transistor transfer characteristics before (blue) and after (red) the anodization process. Before forming the

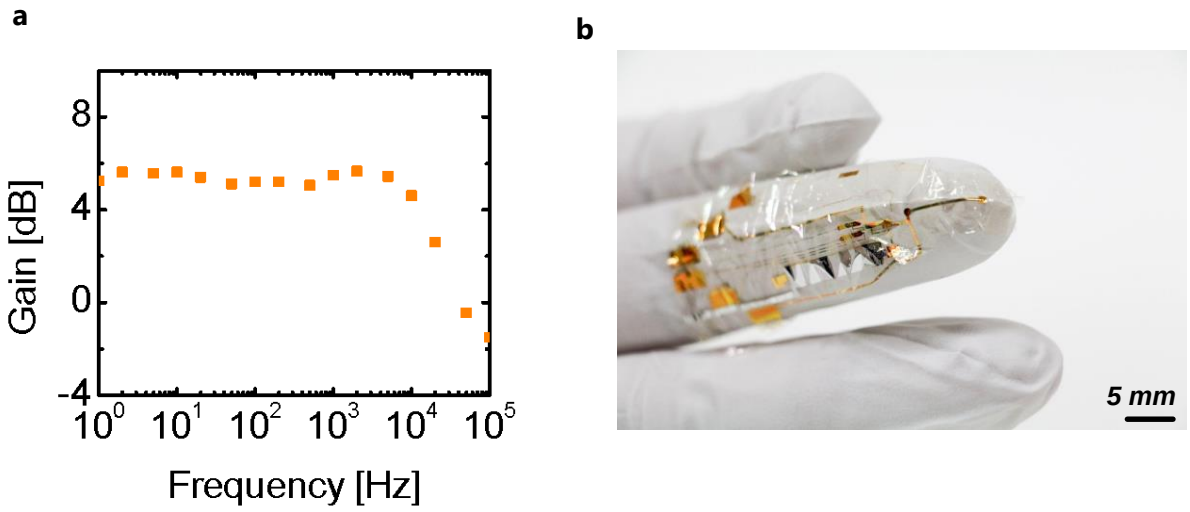


Figure 62: (a) Integrated amplifier frequency response demonstrating flat band pass behavior up to 25 kHz with nominal gain of 5 dB. (b) Device after delamination on a human finger.

important factor is the order of which we will fabricate the elements to prevent damage AlOx, we encapsulated the transistors with 500 nm of parylene and evaporated 60 nm of Al using thermal evaporation. During anodization, the devices were soaked in an aqueous solution (pH 6) for several minutes until the process is completed. We detect slight increase in ON/OFF ratio after anodization and similar ON current and mobility which shows the compatibility of our transistors with the process.

The integrated design was tested as an amplifier circuit on the ultrathin film. We supplied $V_{DD}=-V_{SS}=7V$ and connected GND and V_{BIAS} to the common port. Input voltage was generated with signal generator as a biased AC signal of 3±0.1V. Output voltage was recorded using an oscilloscope and gain was calculated using the relation $20\log|{}^{V_{OUT}}/_{V_{IN}}|$ where V_{OUT} and V_{IN} are the output and input AC signal amplitudes respectively. The gain measurement are plotted in *Figure 62*a. We see that a uniform frequency behavior with amplifier gain of 5 dB can be achieved in phenomenal frequency range, from 1 Hz up to 25 kHz. Unity gain of the device is approximated to 45 kHz. This constant amplification to such a frequency range is the highest achieved for organic amplifiers on flexible substrates. In *Figure 62*b a conceptual image of future application of the amplifier on a human finger is presented after delamination from the sacrificial substrate.

7.2.3 Design optimization

The successful amplifier fabrication we demonstrated on ultrathin films enables proceeding towards a real biological measurement device. For practical application, device size is an important issue. For example current ECoG arrays resolution, used for

clinical purposes on humans and even brain machine interfaces, is approximately 1 cm [146] but efforts are being made to allow higher spatial resolution for those devices. The active size of the amplifier we proposed in previous section is approximately 135 mm^2 which is slightly bigger than required for ECoG devices. We aspire for a design which will allow reliable amplification close to the recording site in the highest resolution possible.

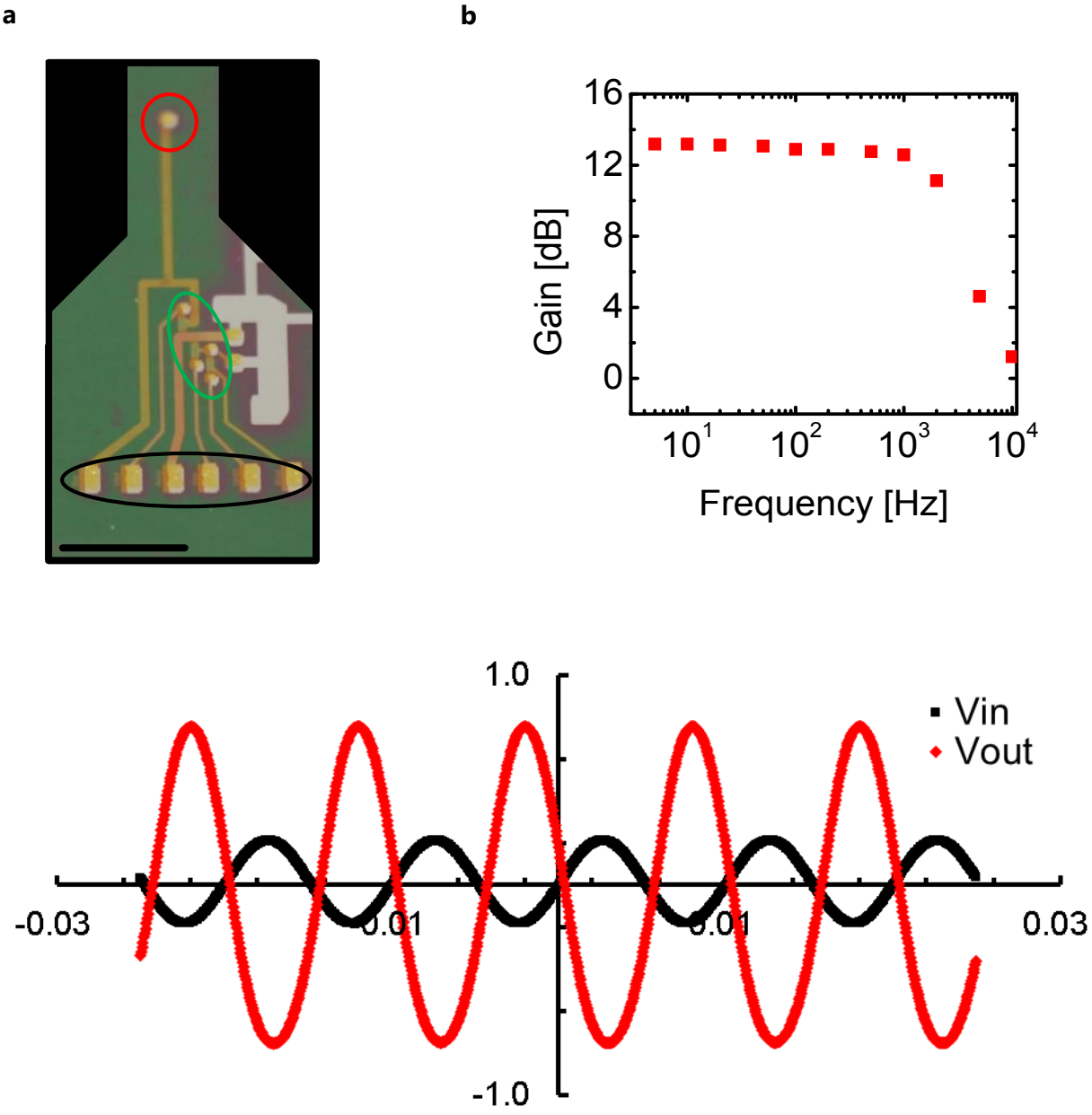


Figure 63: (a) AlOx capacitor (light grey component) and the integrated amplifier with reduced area photograph. The transistors are fabricated in the green ellipse area and contacts are circled by the black ellipse. Recording electrode is marked in red. Scale bar is 5 mm. (b) Integrated amplifier frequency response demonstrating flat band pass behavior up to 3 kHz with nominal gain of 13 dB. (c) Temporal response of the input signal (black) and output signal (red) from the amplifier at 100 Hz.

For that purpose, we would like to reduce the component with the largest area in our circuit – the capacitor. The current size of the AlOx capacitor is 60 mm^2 and provides 200 nF in a single capacitor layer. The choice of AlOx has already increased the capacitance per area of the device and it also allows multilayer structure to boost it even further. By anodizing the top layer of aluminum capacitor we can fabricate another capacitor in parallel and increase the capacitance per area. With keeping this in mind we moved forward to our next, miniaturized amplifier design.

Our advanced design is based on a capacitor with an area of only 10 mm^2. We also reduced the size of connectors and transistors and created a reduced effective amplifier area of only 30 mm^2. In *Figure 63*a, a photograph of the fabricated amplifier demonstrates the active transistor area (green ellipse) and the AlOx capacitor (light grey component). The intended electrode for signal recording (red circle) and contacts (black ellipse) are also presented. By anodizing with 7V, we can realize a capacitance of 500 nF/cm^2 and obtain capacitance of 50 nF for the designed capacitor. As a first step we will try to realize the amplifier with this value of capacitance and in case that the frequency response would not suffice, we will increase our capacitor by multilayer structure. We also reduced the length of connectors to be less than 5 mm to create a small amplifying element that can be later connected to external wiring by bonding techniques [147].

For transistors fabrication, we realized devices with W/L of 15000 µm/ 3.5 µm for the inverter circuit, which represent lower transconductance of 0.1 mS. The lower W/L is supposed to provide higher transistor gain due to an increased inverter load, but also degraded frequency response due to decrease in transconductance. Dielectric thickness was set to lower value of only 45 nm to enable lower operation voltage. The resistor-like transistor was designed and fabricated with smaller W/L of 1500 µm/ 20 µm to increase its resistance and presents maximal transconductance of 5 µS.

The integrated design was tested as an amplifier circuit on the ultrathin film. We supplied $V_{DD}=-V_{SS}=3V$ and connected GND and V_{BIAS} to -3V and 5V respectively. Input voltage was generated with signal generator as a biased AC signal of 2.5±0.4V. Output voltage was recorded using an oscilloscope and gain was calculated using the relation $20\log\left|{}^{V_{OUT}}/_{V_{IN}}\right|$ where V_{OUT} and V_{IN} are the output and input AC signal amplitudes respectively. The gain measurement are plotted in *Figure 63*b as a function of input voltage frequency. We see that a uniform frequency behavior with amplifier gain of 13 dB can be achieved up to 3 kHz. Unity gain of the device is approximated to 10 kHz. In *Figure 63*c, the temporal response of the amplifier at 100 Hz is plotted. We see clear amplification of input signal in an inverse type amplifier with no phase shift. This frequency range allows recording of the entire spectrum of electrical signals generated from the body. The fabricated device shows relevant gain-frequency performance for *in-vivo* recording and exhibits the unique characteristic of ultrathin film implementation.

7.2.4 Closed loop ultrathin amplifier

For the realization of an analog pre-amplifier for biomedical application, one of the most important requirements is a stable and un-biased performance. Measurement from a living body introduces noises due to external electrical signals or movements which affect device performance. To prevent these phenomena, the design of such amplifier usually includes a closed-loop design for signal stabilization, and an input capacitor to remove DC levels from the circuit (*Figure 64*a). We realized the circuit, based on the design in section 7.2.3 , by adding a feedback resistor (implemented by a low W/L transistor) and an input capacitor. The fabricated device appears in *Figure 64*b. Total area of the active circuit is estimated to be 40 mm^2. For process simplicity, we considered parylene capacitors with lower capacitance per area. The total capacitance of each capacitor (C_1, C_2) was 4.2 nF. With the implementation of lower gain and large resistors, a good frequency response in lower frequencies could be obtained. Before the evaluation of the full closed-loop circuit we measured the amplifier maximal gain without the input capacitor. The measurements were conducted by bypassing the input capacitor to evaluate the internal gain of the circuit. With biasing the input voltage at ~2V, we could the maximal gain from each amplifier. The results have demonstrated excellent uniformity of circuits over area of 16 cm^2 (*Figure 64*c).

The amplifier response was recorded in a closed loop configuration with input capacitor to filter DC bias. By introducing the input capacitor, the amplifier circuit is stabilized in a working point between the supply voltage and GND, regardless the input bias. Stabilization point should accord with the point where DC voltage $V_{out}=V_{in}$ to allow the correct feedback loop. We measured the temporal response at 1 kHz and present it in *Figure 64*d. We can see clear 90° phase between input (black) and the amplified output signal (red). The inverted response implies on a good frequency behavior at high frequencies. To evaluate the performance in the entire spectrum, we measured gain characteristics at different frequencies and plotted them in *Figure 64*e. The amplification is almost constant on a nominal value of 6dB in most of the frequency range important for biological signals. We calculated that f_{3dB} of the amplifier is 3 Hz at the lower cutoff and 3 kHz at the high frequency range. These characteristics prospect reliable amplification, in closed-loop configuration, for any of the signals generated from the human body.

For more specific applications where size is of priority, we suggest an even more compact design. The total circuit size in this configuration is only 15 mm^2 which is suitable for high resolution recording arrays. In this design we propose AlOx capacitors of 2 mm^2 and 5 mm^2 for the circuit (C_1) and input (C_{in}) capacitors respectively. The capacitance of these capacitors are 10 nF and 25 nF in anodization process of 7V. For easy tuning of amplifier gain in closed loop, we utilized the double gate structure. As we showed in 0, adding double gate to the design can change the inverter working point and adjust it to the $V_{out}=V_{in}$ curve. For maintaining wiring number, we connected the ports for Vss and GND together. In *Figure 65*a we present a photo of the miniaturized design after fabrication. We provided V_{DD} of 5V to the circuit and with double gate voltage of 3V we

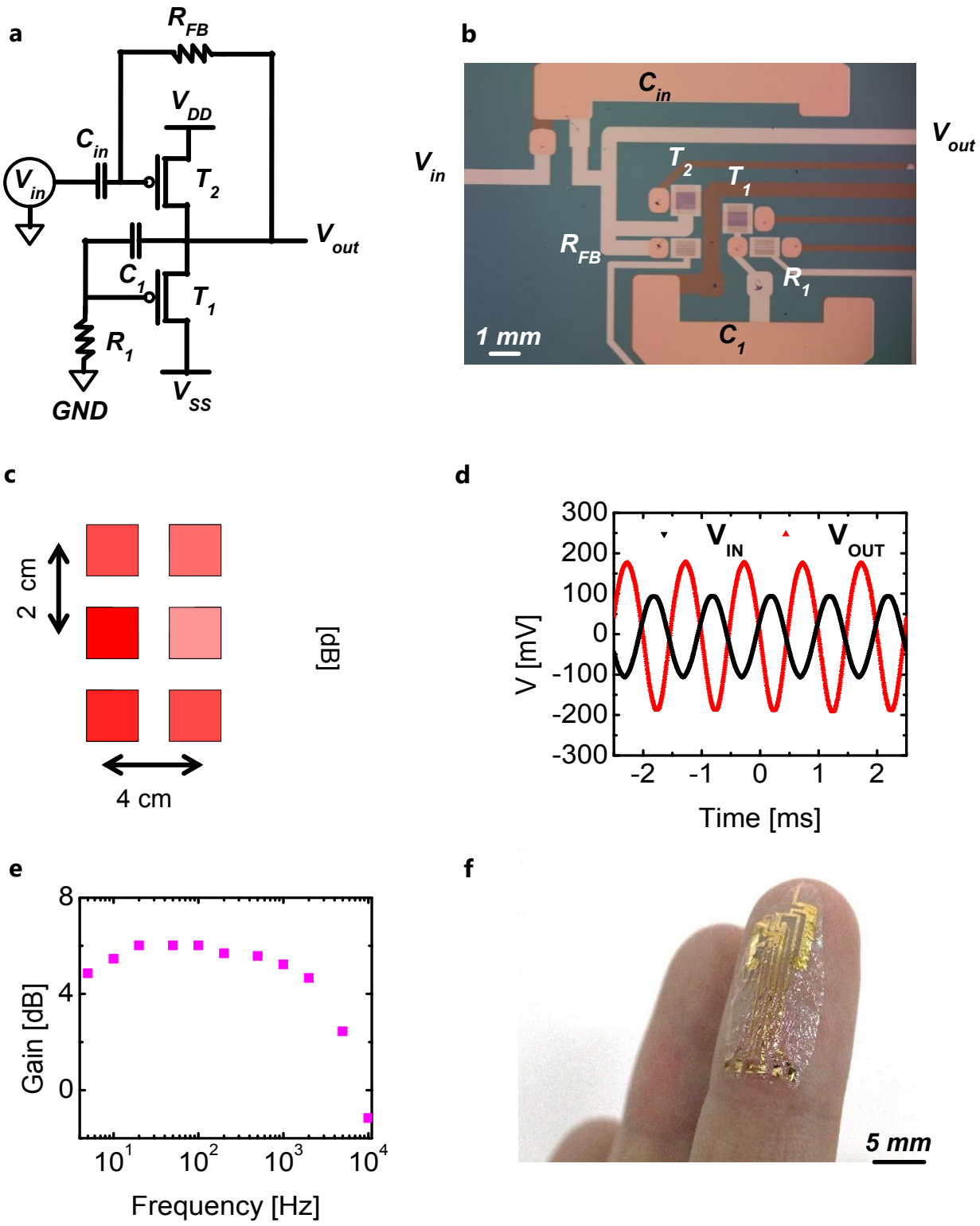


Figure 64: (a) Closed-loop design, including input capacitor and feedback resistor. (b) Implementation of the closed-loop design using the ultrathin film technology. (c) Distribution of closed-loop gain of amplifier over 16 cm^2, without input capacitor. (d) Temporal closed loop amplification at 1 kHz. (e) Spectral frequency response of closed loop amplifier, presenting up to 3 kHz of constant amplification. (f) Conceptual image of the ultrathin amplifier on human finger.

could get constant signal amplification in the range of 5Hz-700Hz (*Figure 65*b). The degradation in high frequency region might be in part related to the increased parasitic capacitance from the double gate configuration. Other considerations can be related to the higher leakage current in the AlOx capacitors compared with the parylene design, which changes the working point in the AC coupled design. Nevertheless, this amplifier presents the **smallest organic closed-loop amplifier** (active area - 15 mm^2) reported to date and presents good frequency response, suitable for most signals generated from a living body.

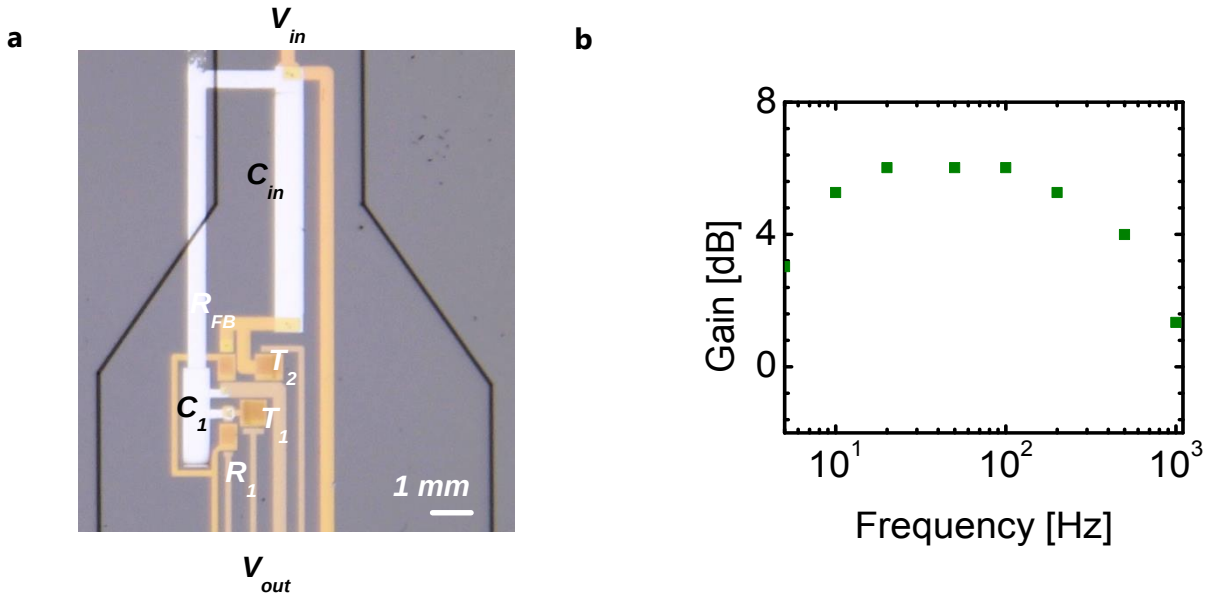


Figure 65: (a) Miniaturized closed-loop amplifier of only 15 mm^2. Notations correspond to *Figure 59*. (b) Frequency response of amplifier presents constant amplification between 5Hz to 700 Hz (f_{3dB}).

8 Large area application

8.1 Active matrix

One of the most appealing applications for flexible electronics is large area sensing sheet that can conform to any curvilinear object. Large area sensor arrays can detect signals from various environmental conditions and provide real-time monitoring for wide variety of parameters. For example, pressure signals can be detected from robotic arms in E-skin application; neural signals can be mapped from brain surfaces; thermal distribution of sensitive machinery can be detected in real-time and more. The sensing element should translate the detected signal into electrical signal which is monitored for realizing changes in the environmental conditions. Large area sensor sheets are characterized with large number of signals and hence should contain many input and output wire connections. A possible solution for this problem is to provide large area active matrix for selective addressing of each sensor by transistor switching. The active matrix solution reduces the wiring coming out logarithmically and provide good selectivity of sensors.

The transistor implementation in an active matrix should meet certain criteria for reliable implementation. In order to provide good signal selectivity, transistors should have large ON/OFF ratio and low leakage current. The high ON/OFF ratio provides good switching between transistor states and reliable cell selection. Each transistor channel in the matrix should have appropriate resistance for detecting the changes in the sensing element. Low leakage assures that additional signals would not interfere with the detected one. Additionally, for real-time detection of high rate signals, transistor should be able to switch frequently. Each transistor cell in the matrix should meet frequency demand of approximately $2 \cdot n \cdot f$ where n is the maximal number of sensors in a column/row and f is the maximal frequency of the detected signal. One more important consideration is transistors uniformity and yield over large area. Failure of one single cell would rule out detection from the corresponding row and column in the matrix.

With our implementation of bottom contact short channel transistors are expected to be able to meet all criteria for the active matrix application. We have shown that our transistors have high ON/OFF ratio (~107) and low leakage currents (MAX|IGS| in the order of 100 pA) when tested as single devices. Furthermore, the short channel implementation with small parasitic capacitance allows large bandwidth for transistor switching (cutoff frequency of at least 100 kHz). Transistors have proved good uniformity and yield in our single transistors measurements (*Figure 34*). Finally, the devices are compatible with ultrathin device implementation and are fabricated on 1 µm thick parylene diX-SR substrate and demonstrate excellent mechanical and thermal stability.

We have designed a bottom contact active matrix design which consists of 12x12 cells (144 transistors). The matrix was fabricated on a 1 µm parylene siX-SR, vapor deposited

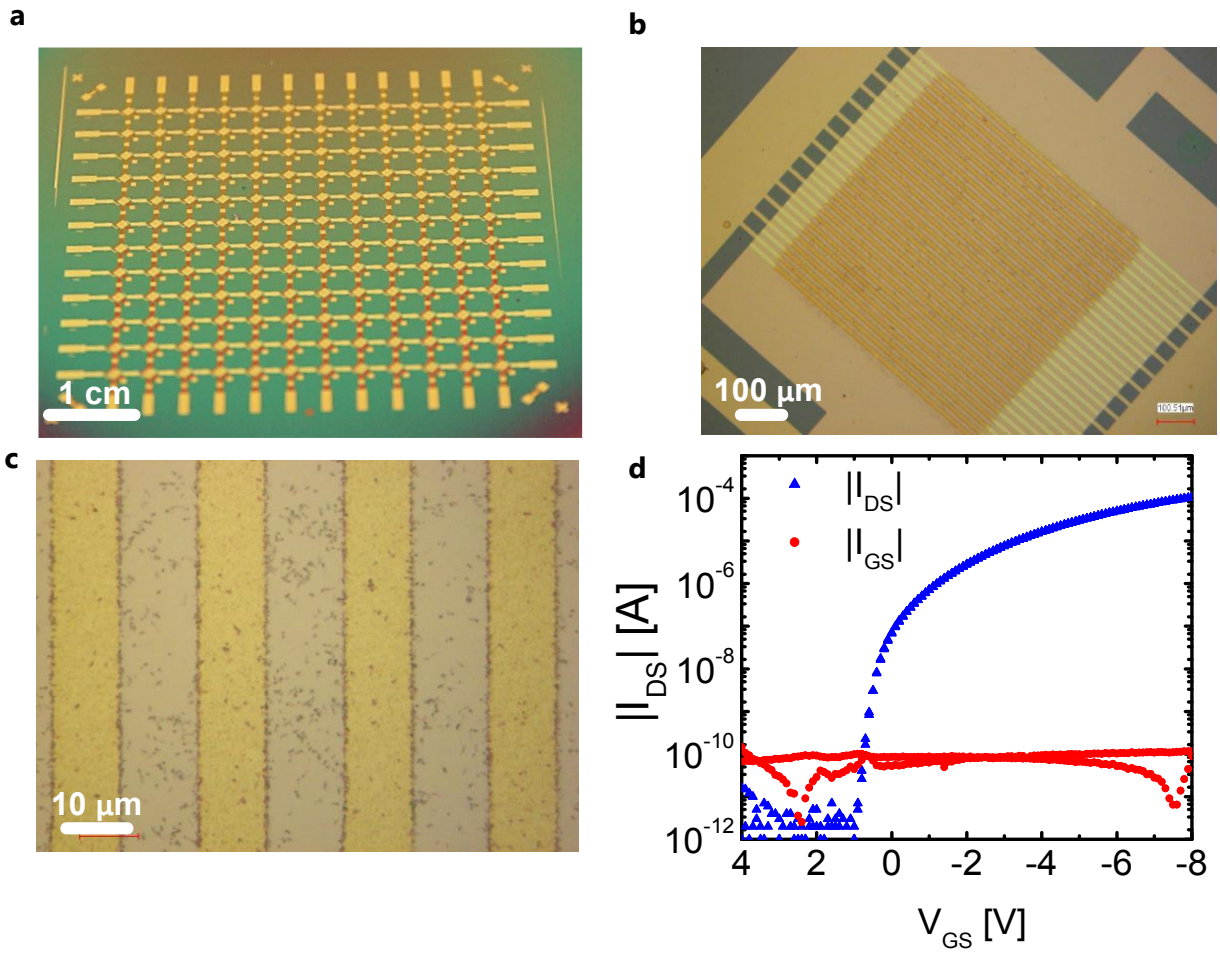


Figure 66: (a) Large area active matrix (6x6 cm^2) photograph. (b) Single matrix cell of organic transistor with W/L of 1500. (c) Magnified microscopic image of the channels area, presenting channel length of 13 µm and source/drain 'finger' width of 11 µm. (d) Typical transfer curve of a single matrix cell.

on Si/SiO_2 4" wafer. Device's total active area is 6x6 cm^2 and cells are connected through perpendicular source and gate lines (*Figure 66*a). We carefully designed the overlap between gate and source lines to be only 20x20 μm^2 in the intersection of each cell. In *Figure 66*b one transistor cell is presented. Each of the transistors has W/L of 20000 µm/ 13 µm and total active area of 720x720 μm^2. We reduced the 'finger' width in the active area to 11 µm for achieving low parasitic capacitance (*Figure 66*c). We evaluated transistor performance using auto-probing measurement system and acquired transfer and output characteristic of each cell.

Typical transistor transfer characteristics is plotted in *Figure 66*d. We observe high subthreshold slope of ~200 mV/dec and ON current of roughly 100 µA. Device operation voltage is –8V (parylene diX-SR dielectric thickness of 120 nm). Leakage current (I_{GS}, red curve) did not exceed 100 pA and ON/OFF ratio exhibit phenomenal value of 10^8. In *Figure*

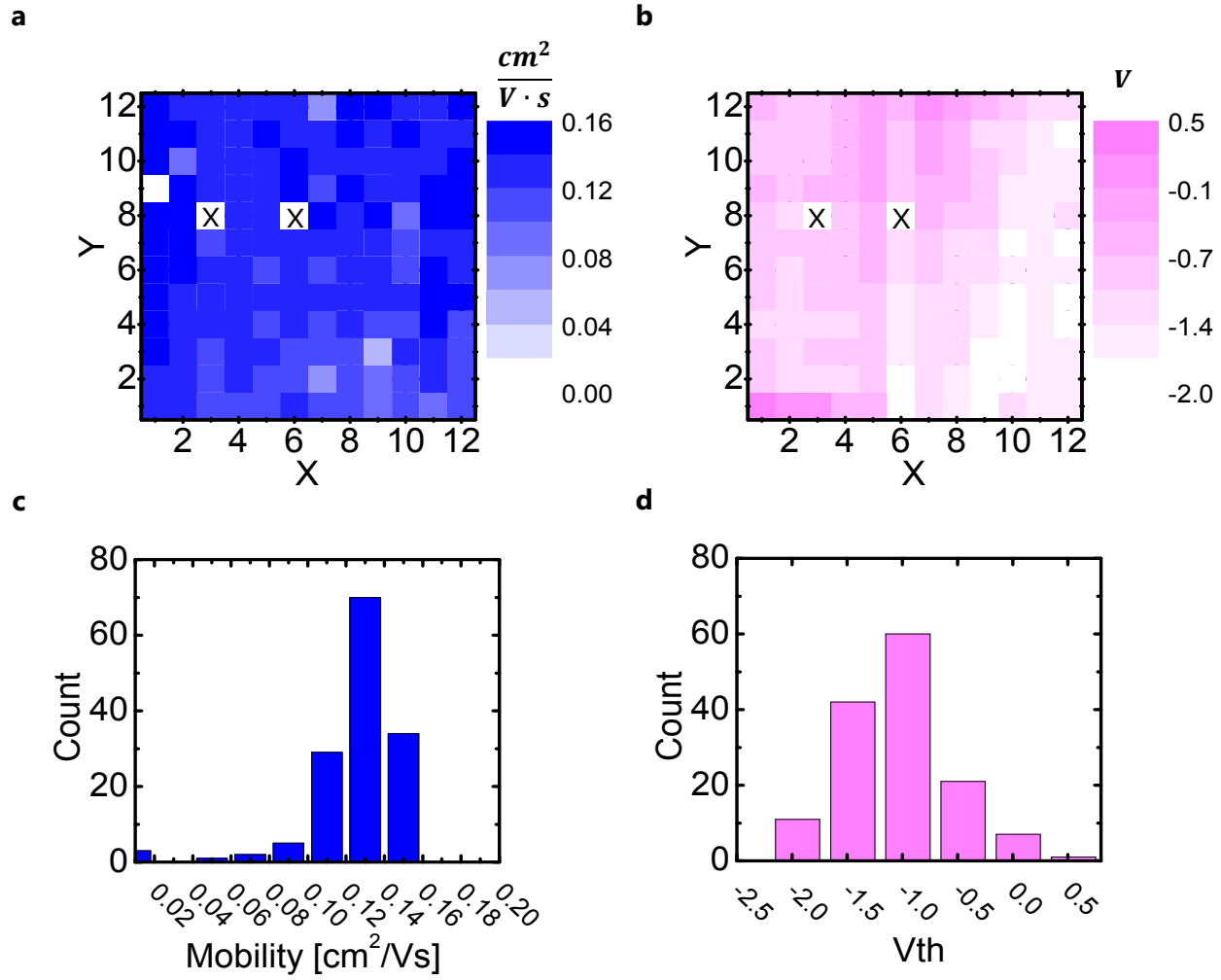


Figure 67: (a) Mobility and (b) threshold voltage spatial distribution of the active matrix presented in Figure 66. Values are presented according to the color scale bar near each matrix distribution. (c) Mobility and (d) threshold voltage device count are presented in a histogram plot.

*67*a and *Figure 67*b we plot the spatial distribution of transistors' mobility and threshold voltage respectively. The X and Y axis and their indices denote the cell number from 1 to 12. We can detect excellent uniformity and very high device yield (98.6%). Except from singular cells with low mobility and slightly lower mobility near the edges, most devices seem to exhibit high and uniform saturation mobility. The graph for distribution of threshold voltage also shows high degree of uniformity between –1.5V and –0.5V. For more detailed analysis of device uniformity we plot the histogram of device count as a function of their mobility (*Figure 67*c) and threshold voltage (*Figure 67*d). Roughly half of the devices have mobility between 0.11 $cm^2/V{\cdot}s$ and 0.13 $cm^2/V{\cdot}s$ and threshold voltage between –1.25V and –0.75V. Mobility average and standard deviation were calculated to be 0.12±0.019 $cm^2/V{\cdot}s$. Additionally, more than half of devices have ON/OFF ratio of 10^8 or higher and 84% of devices have ON/OFF ratio of at least 10^7. The maximum leakage

current of 90% of devices was smaller than 1 nA. The uniform data obtained from transistors and the high device yield allow reliable design of active matrix for large area sensing sheets on ultrathin films.

8.2 Large area pressure sensing sheet

We utilized the ability for realizing large area active matrix for the fabrication of pressure sensitive sheet. An active matrix with channel length of only 4 μm and W/L of 18,000 was fabricated using the bottom contact structure. Transistors yield was 98.6% (142/144). The transistors were connected to an external wiring via patterning of 12 wires of drains and additional 12 wires for gates. On transistors' source, for each cell, pads of 3x3 mm^2 were patterned to increase the contact area with the pressure sensitive sheet. The matrix was then encapsulated with an additional 1 μm parylene layer to prevent short circuit between connectors. Reactive ion etching was finally conducted to expose the designated connection area. The matrix was covered by a pressure sensitive rubber, topped with a 1 μm GND electrode. Device layout and stack are shown in *Figure 68*.

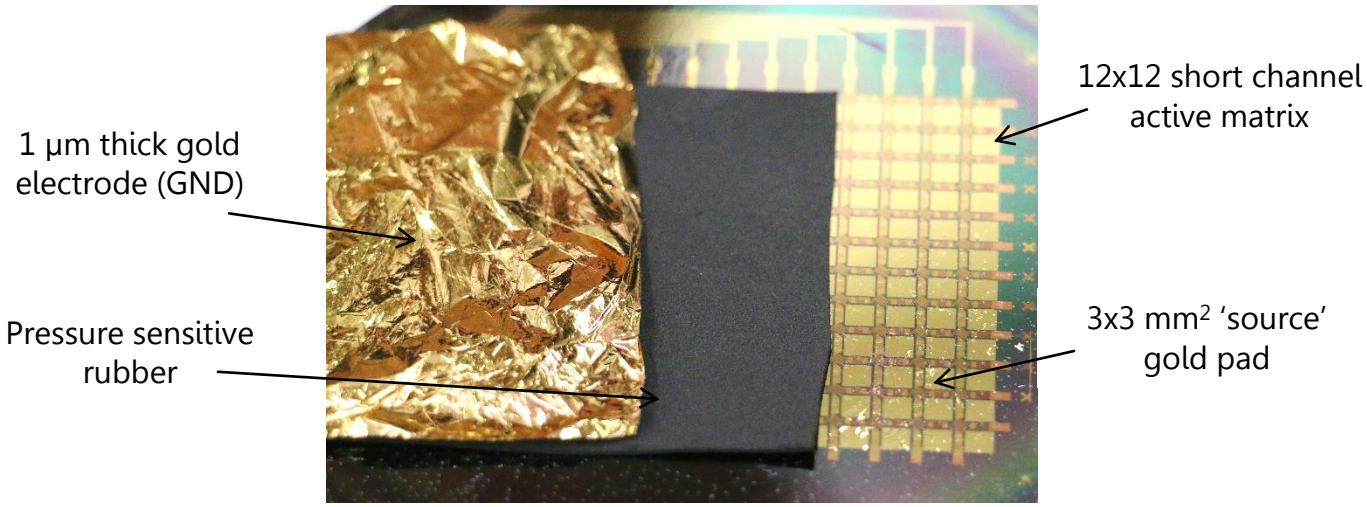


Figure 68: Layout of the pressure sensitive sheet based on short channel active matrix. Pressure sensitive rubber was mounted on top of the active matrix to control the resistivity upon pressure of the reading circuit. Circuit's GND was connected to a 1 μm thick gold electrode.

The entire wiring set (12 gate wires, 12 drain wires and GND electrode) were connected to a driving and reading circuit (UART ©). A voltage of -8V was applied to the 12 gates and drains in relation to the GND. The induced current was selectively read from the drain ports upon application of pressure. The current is determined by the application of a gate voltage larger than the threshold (-8V) and by the resistance between the source pad and GND. This resistance can be tuned by the pressure applied on the pressure sensitive sheet. In the initial state the lateral resistance of the rubber is several MΩ which limits the current flowing through the transistors. In correlation with the pressure on a specific cell, the

resistance of the conductive rubber decreases to a few kΩ which allows the conduction of current via the transistor. Currents up to 100 μA could be detected by the system.

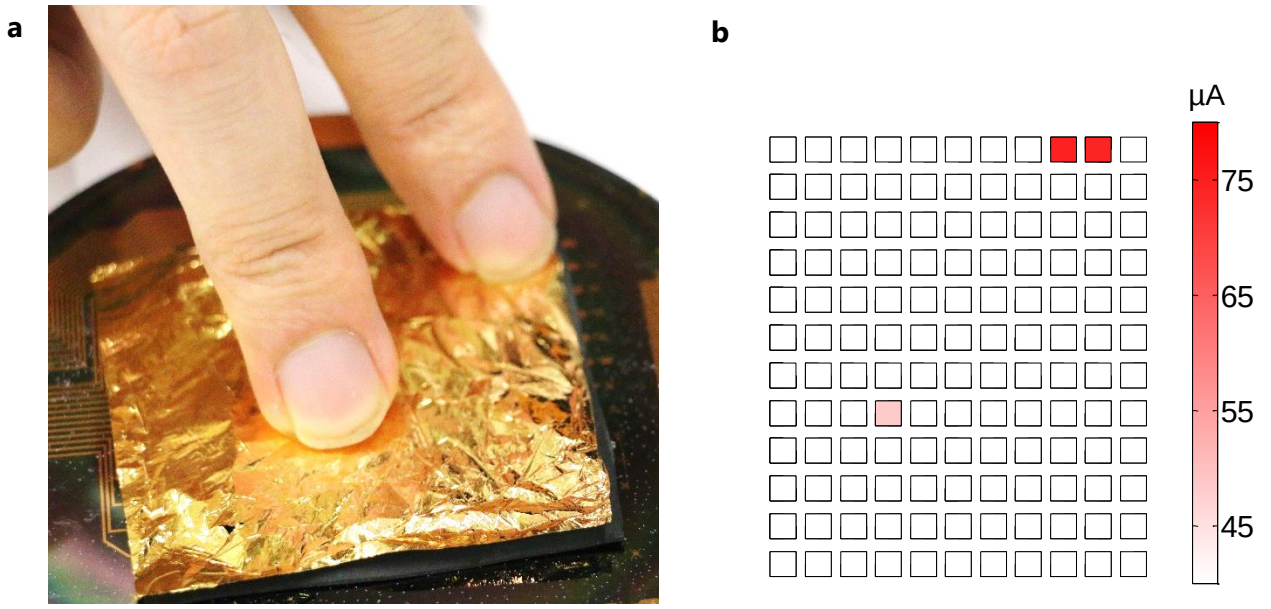


Figure 69: (a) Pressure applied on 3 cells and (b) their corresponding current readout. Slight pressure differences could be detected by the system.

In *Figure 69* the detection of pressure in multiple points is demonstrated. By using two fingers we applied different pressure on 3 different cells and measured the readout current. Stronger press was applied on the edge of the matrix which resulted in larger current readout. The ability to correctly distinguish between the different cells is attributed to three main merits of our devices: device uniformity, low leakage currents (~100 pA) and high ON/OFF ratio (~10^7). These properties have made our device suitable to practical large area sensor sheet and future applications which require high degree of selectivity and reliability.

9 Summary and Outlook

Our achievements in this study can be summarized into three main categories:

- **High frequency and conformable organic transistors**

  Our transistors demonstrate the highest theoretical value of cutoff frequency for organic devices on ultrathin films (record of 1.6 MHz). We have overcome challenges in photolithography patterning and contact modification on ultrathin films to realize channel lengths of only 2 μm with good carrier mobility for high frequency operation. The implemented top-gate structure allows better contact modification mechanism and smaller transfer length (~1 μm) which enabled reduction of the parasitic capacitance to less than 0.5 pF per channel.

- **Reliable and uniform electronics on large area**

  The proposed fabrication method exhibits high degree of reliability, device yield (98.6% of 144 transistors) and uniformity (~15% standard deviation in mobility) over large area active matrix (36 cm^2). The reliable patterning using photolithography and the selection of conformable, vapor deposited gate dielectric have major contribution to this achievement. Thanks to those properties, high gain and uniform pseudo-CMOS inverters and AC coupled amplifiers have been successfully manufactured on ultrathin films. AC coupled amplifiers could show the highest frequency response (f_{3dB} of 25 kHz, f_{unity} of 45 kHz) reported for organic devices. Closed loop design can reach uniform and stable amplification between 3Hz-3kHz.

- **Excellent device stability**

  The fabricated transistors presented extreme durability to severe mechanical and thermal stress. Bending down to radius of 600 μm and device crumpling were successfully demonstrated with slight performance change (< 10% in mobility). Transistors could also keep their cutoff frequency above 100 kHz after annealing at 170°C and showed very good cyclic stability at 120°C. This is the first demonstration of such high degree of stability, both for mechanical and thermal stresses, of short channel organic transistors (< 5μm channel length). We attribute this excellent performance to the utilization of thermally stable materials in the bottom contact-top gate structure.

  In the following table we summarize our device characteristics in terms of single transistor and circuit performance. The table summarizes recent state of the art research on organic thin film transistors on flexible, freestanding substrates:

Table 2: Recent state of the art studies on organic thin film transistors, fabricated on flexible freestanding plastic substrates [16,24,25,130,131].

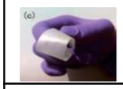
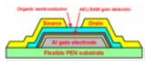
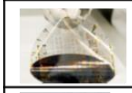
Source	Contact /Thickness	Cutoff frequency*	Operation voltage	Mechanical stability	Inverter gain	Amplifier Gain/ f_{3dB}
	Bottom / 60μm	N/A	60V	R=1mm	40dB	N/A
	Top / 26μm	5kHz	2V	R=0.1mm	32dB	N/A
	Top / 125μm	7MHz	4V	N/A	N/A	N/A
	Bottom / 25μm	12MHz	18V	N/A	12dB	N/A
	Top / 75μm	250kHz	2V	N/A	52dB	40dB/ 100Hz
	Top / 2μm	30kHz	3V	Crumple	N/A	N/A
	Bottom / 2μm	1.4MHz	8V	Crumple	38dB	6dB/ 3kHz

Table 2 presents the advantages of our technology on ultrathin films where both high cutoff frequency and high performance circuits could be achieved. Cutoff frequency surpassed the MHz regime, presenting an advancement towards the best reported frequency response on thin films. In addition, low operation voltage circuits with large gain and excellent frequency response could be demonstrated.

The simultaneous achievement of those three important components is unique and presents a major contribution towards the realization of practical imperceptible electronics on large areas. As a future prospect we expect that the proposed reliable technology would be implemented to a variety of applications, such as:

- *Large area sensor sheets*

Our proposed uniform and environmentally stable electronic devices can be readily utilized as switching elements for large area sensor sheets. We demonstrated large area active matrix, consists of more than 140 transistors which will be able to allow switching of sensing elements. The environmental and thermal stability offer wide range practical utilization opportunities in various fields. The high frequency of the devices enables real-time recording and multiplexing of rapidly changing signals. The imperceptible substrate

we utilize can afford implementation on any 3-dimensional shape, including human organs. The devices are mechanically and thermally stable to be used directly on skin or, if properly encapsulated, inside the human body.

- *Ultrathin electronic circuits*

The uniformity of devices allows reliable implementation of circuits, as we demonstrated here for pseudo-CMOS inverters and AC-coupled amplifiers, in large numbers and on large areas. For example, an imperceptible amplifier array can be realized using our method. In sensing applications, amplification of signals near the recording site has a critical effect on the signal-to-noise ratio and can improve it dramatically. The large area applicability of the technology will allow the realization of amplifier arrays for signal improvement of numerous sensing elements. The amplification bandwidth of devices is practically not limited for most sensing applications and can reach to as high as 25 kHz. Moreover, basic circuits such as rectifiers, band-pass filter, ring-oscillators and others can be implemented on the ultrathin film. The size of the circuits can be dramatically reduced by the successful integration we demonstrated with ultrathin, area efficient passive elements such as the AlOx capacitor.

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