博士論文(要約)

Study on carrier transport properties and performance improvement of ultra-thin body Germanium-on-insulator MOSFETs

（極薄 Germanium-on-insulator MOSFET のキャリア輸送特性と性能向上に関する研究）

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Germanium (Ge) metal-oxide-semiconductor field-effect transistors (MOSFETs) have been regarded as promising devices for the future logic large scale integrated circuits (LSIs), because of the higher mobility than silicon (Si). In order to realize high quality Ge MOSFETs on Si platform for further scaling, high quality and ultrathin-body (UTB) Ge-on-insulator (GeOI) structures are mandatory. In this research, we focus on the fabrication technique for the ultrathin body GeOI with good crystal quality, good uniformity in large area and superior Ge/Buried Oxide (BOX) interfaces simultaneously. The GeOI MOSFET devices based on these UTB substrates are also demonstrated.

First, we have demonstrated a novel method to fabricate GeOI substrates based on epitaxial Ge films grown on III-V compounds wafers. The wafer-level formation of high quality GeOI substrate is realized by direct wafer bonding technique and high selective etching between III-V compounds and Ge. The plasma post oxidation process was introduced to improve the Ge/BOX back interface. By using the fabricated GeOI structures, p- and n-MOSFETs with the GeOI thickness down to 20 nm was fabricated and the electrical characteristics were evaluated. The normal p- and n-MOSFETs operations on the thin body GeOI structures have been confirmed in the inversion mode and the accumulation mode, respectively. The peak effective hole and electron mobility of 122 and 235 cm^2/Vs, respectively, have been obtained. Furthermore, the GeOI film thickness dependence of the electrical characteristics and effective mobility has been systematically investigated. The mobility of the present devices higher than that of the Smart Cut devices with Ge/SiO$_2$ interfaces is attributable to the better back interfacial properties by the GeO$_x$/Ge interfacial layers.

In order to improve the crystal quality as well as the interfacial quality of commercial Smart Cut GeOI, a novel way to realize UTB GeOI substrates, where the high quality surface layers of Smart-Cut GeOI is utilized for UTB structure through a layer transfer technology and a GeOI thinning process by the combination of RIE and thermal oxidation, has been proposed and demonstrated. Here, since the GeOI layers become upside down from the original GeOI substrates to utilize the surface layer with good crystal quality, this GeOI is named the flipped GeOI. The GeOI thickness dependence of the physical properties including the GeOI crystal quality, strain effect and surface roughness was systematically evaluated between the original and flipped GeOI. The flipped GeOI fabricated and thinned by the present method has exhibited better crystal quality than the original one, with preserving the good thickness uniformity in the UTB region. Furthermore, UTB GeOI pMOSFETs on the flipped GeOI have been realized with the thickness down to 11 nm. The flipped GeOI has higher mobility than the original GeOI at a given GeOI thickness. The effective peak hole mobility enhancement factor of the flipped GeOI against the original one amounts to 1.51 and 1.29 for GeOI thickness of 20 nm and 11 nm, respectively. These results mean that the interface properties of the buried oxide interface as well as the crystal quality are quite important for the mobility of UTB GeOI p-MOSFETs.

In order to discriminate the influences of the back interface passivation and the crystallite quality on the device characteristics, the electrical properties as well as the thickness dependence of UTB GeOI MOSFETs with the different back interfaces have been fabricated and evaluated. The interfacial quality has been found to be critical to the GeOI effective mobility than the crystallite quality in the thin GeOI MOSFETs ranging from 30 nm down to 10 nm. Even the crystallite quality near back interface of flipped GeOI should be better than that of original GeOI, the worse interfacial quality of flipped GeOI without passivation would compensate the improvement of crystallite quality and cause the degradation in mobility at a given thickness. However, as the GeOI thickness reduces down to around 10nm, the mobility among the different interfaces exhibits the similar decreasing dependence on the GeOI thickness, indicating that any other scattering mechanisms than MOS interface charges at the back interface would dominate the mobility in this UTB region.

Furthermore, based on the proposed flipped GeOI substrate, mobility improvement of UTB GeOI MOSFETs by GeOI thinning using plasma oxidation is demonstrated. Room temperature plasma oxidation in ECR is optimized and utilized for precisely control the GeOI thickness with low damage and low thermal budget, which is critical in Ge MOS interfacial quality.7-nm-thick GeOI MOSFETs are successfully demonstrated by the present technique with peak hole mobility amounts to 116 cm^2/Vs. The flipped GeOI thinned by plasma oxidation exhibit highest mobility at a given thickness, and the enhancement factor is becoming larger as the thickness reduced.

The combination of the novel digital GeOI etching technique by plasma oxidation with the flipped GeOI formation by direct wafer bonding has realized the high quality ETB GeOI pMOSFETs with T_{GeOI} ranging from 25 nm to 2 nm. Successful device operation of back gate GeOI MOSFETs with GeOI thickness down to 2 nm and the front gate ones down to 4 nm have been demonstrated. The effective hole mobility with a wide range of GeOI thickness, down to 2 nm, is systematically studied and analyzed through the surface carrier concentration (Ns), temperature and back bias dependencies from the viewpoint of the scattering mechanisms, for the first time. The systematic hole mobility data with T_{GeOI} from 25 nm to 2 nm have clearly shown the continuous mobility decrease with a reduction in T_{GeOI}, which can be explained by the enhanced thickness fluctuation scattering and phonon scattering, particularly for T_{GeOI} less than 10 nm.