論 文 の 内 容 の 要 旨

論文題目 Study of Network Rigidity Coordination of Dielectric Thin Films for Scalable and Reliable Ge MOS Device

（高信頼性微細 Ge MOS デバイスの実現に向けた誘電体薄膜中のネットワーク強化に関する研究）

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The recent years of researches on GeO_2/Ge interface passivation technics have enable the operation of high mobility Ge MOSFET for the first time, which might be the dawn of a new generation of IC application with Ge channel. However, the remaining concerns are still critical. Namely, (1) the poor thermal and chemical stability of GeO_2/Ge stack must be improved; (2) the equivalent oxide thickness (EOT) must be reduced to below 1 nm without degrading the interface; and (3) the long term reliability of Ge MOS device must be ensured for real application. These three concerns are among the most critical challenges on bringing Ge back to future.

In this work, I will address the above concerns by designing new dielectric materials for MOS devices formation. The key to the dielectric designing is to manipulate the structure of oxides by the formation of ternary alloys. This is because the bonding configuration in the ternary oxide might be changed from the binary oxides and such change would bring about significant influences on the material and electrical properties of the gate dielectric.

Under this guiding principal, a new material, metal oxide doped GeO_2 (M-GeO_2), was proposed for the robust interfacial layer (IL) on Ge gate stack. Drastic improvements in thermal and chemical stability were obtained without any cost of interface properties by small amount of suitable doping like Y or Sc. The significant improvements in material stability were discussed from the network modification of GeO_2 by doping.

A new ternary high-*k* dielectric, yttrium scandate ($YScO_3$), is also proposed for the gate stack formation in the sub-nm EOT region. A higher *k*-value and sufficient energy gap is observed for $YScO_3$, which is a pronounced advantage over its binary compounds. The *k*-value improvement is also discussed from the structural change and denser packing of the ternary oxides. The $YScO_3$ also inherit the interface aware properties of its binary compounds, which enable it to be used on an ultra-thin IL. The 0.5 nm EOT and very high electron peak mobility is demonstrated by $YScO_3$/Y-GeO_2/Ge stack.

Based on the good initial properties, the reliability assessment of the Ge MOS device is also carried out in terms of both pre-existing trap in the as-prepare gate stacks and trap generation under high electric stress field (E_{stress}). It is found that the hole trap is the major concern among the pre-existing traps, which is controllable by the gate stack process condition such as high oxygen pressure. While, the trap generation behavior in the Ge stack is dominated by the intrinsic rigidity of the dielectrics network. Y or Sc-GeO_2 can effectively suppress the trap generation under high E_{stress} comparing to pure GeO_2. Based on this knowledge, we demonstrated significant reliability improvements in Ge MOS devices.