博士論文 （要約）

Study of Network Rigidity Coordination of Dielectric Thin Films for Scalable and Reliable Ge MOS Device

（高信頼性微細 Ge MOS デバイスの実現に向けた
誘電体薄膜中のネットワーク強化に関する研究）

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By

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Abstract

The recent years of researches on GeO_2/Ge interface passivation technics have enable the operation of high mobility Ge MOSFET for the first time, which might be the dawn of a new generation of IC application with Ge channel. However, the remaining concerns are still critical. Namely, (1) the poor thermal and chemical stability of GeO_2/Ge stack must be improved; (2) the equivalent oxide thickness (EOT) must be reduced to below 1 nm without degrading the interface; and (3) the long term reliability of Ge MOS device must be ensured for real application. These three concerns are among the most critical challenges on bringing Ge back to future.

In this work, I will address the above concerns by designing new dielectric materials for MOS devices formation. The key to the dielectric designing is to manipulate the structure of oxides by the formation of ternary alloys. This is because the bonding configuration in the ternary oxide might be changed from the binary oxides and such change would bring about significant influences on the material and electrical properties of the gate dielectric.

Under this guiding principal, a new material, metal oxide doped GeO_2 (M-GeO_2), was proposed for the robust interfacial layer (IL) on Ge gate stack. Drastic improvements in thermal and chemical stability were obtained without any cost of interface properties by

small amount of suitable doping like Y or Sc. The significant improvements in material stability were discussed from the network modification of GeO_2 by doping.

A new ternary high-*k* dielectric, yttrium scandate ($YScO_3$), is also proposed for the gate stack formation in the sub-nm EOT region. A higher *k*-value and sufficient energy gap is observed for $YScO_3$, which is a pronounced advantage over its binary compounds. The *k*-value improvement is also discussed from the structural change and denser packing of the ternary oxides. The $YScO_3$ also inherit the interface aware properties of its binary compounds, which enable it to be used on an ultra-thin IL. The 0.5 nm EOT and very high electron peak mobility is demonstrated by $YScO_3$/Y-GeO_2/Ge stack.

Based on the good initial properties, the reliability assessment of the Ge MOS device is also carried out in terms of both pre-existing trap in the as-prepare gate stacks and trap generation under high electric stress field (E_{stress}). It is found that the hole trap is the major concern among the pre-existing traps, which is controllable by the gate stack process condition such as high oxygen pressure. While, the trap generation behavior in the Ge stack is dominated by the intrinsic rigidity of the dielectrics network. Y or Sc-GeO_2 can effectively suppress the trap generation under high E_{stress} comparing to pure GeO_2. Based on this knowledge, we demonstrated significant reliability improvements in Ge MOS devices.

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Chapter 1

Introduction

1.1 High mobility channel material for future MOS device

1.2 Requirements for gate stack design in Ge MOS device

1.3 Objective and organization of this work

Overview

Due to the physical limitation on Si MOSFET dimensional scaling, Ge is emerging as an advanced channel material in substitute of Si to achieve higher device operation speed. The design of the gate dielectric is the most critical concern to ensure a sufficiently passivated Ge interface and high carrier mobility in the channel. Significant progresses have been reported recent years on the preparation of high quality GeO_2 on Ge, which yield a well passivated Ge interface and high carrier mobility over Si universality. Though GeO_2 has been believed to be the best candidate for the interface passivation, advanced gate dielectrics are still needed to improve several vital properties of Ge MOS device. Namely, the thermal and chemical robustness of the GeO_2/Ge stack must be improved. The scalability of the equivalent oxide thickness to deep sub-nm region must be ensured. And finally, the long term reliability of the Ge MOS device must be evaluated. This work will investigate the various dielectrics oxides in terms of the above requirements. A structural viewpoint on dielectric oxides is to be developed for controlling the material and electrical properties of the Ge MOS device.

1.1 High mobility channel material for future MOS device

Since the first demonstration on silicon in 1959 by Dawon Kahng and Martin M Atalla in Bell Lab,[1] metal-oxide-semiconductor field-effect-transistors (MOSFET) has been one of the most used electronic devices in the world. The logic, memory, power and radio-frequency (rf) circuits all utilize the MOSFET structure as their basic units.[2-5] It is not hard to sketch a basic configuration of MOSFET (**Figure 1.1**).[6] A MOSFET is basically an three-terminal device where the channel resistance between two contacts are controlled by the third.[6] In detail, the carriers flow from the source to the drain, and the control terminal is the gate, which can manipulate the channel resistance by capacitively coupled

electric field. Despite this simple schematics of the MOSFET structure, the understanding and improvement the MOSFET are not easy challenges.

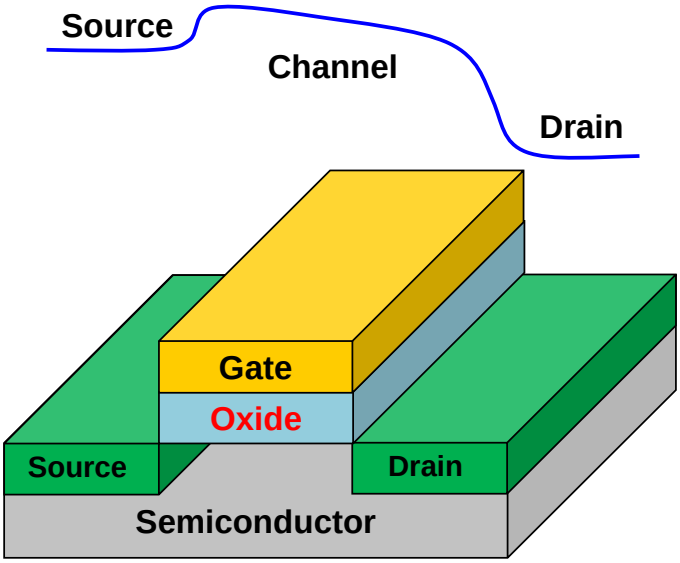


Figure 1.1 Schematics of a MOSFET with planar structure. There are three terminals for the device, the source, the drain and the gate. The carriers are injected from the source to the drain through the semiconductor channel, which is controlled by field applied through gate electrode.

Ever since the proposal of MOSFET concept in 1930s[7, 8] and the first demonstration in 1959,[1] progressive achievements have been made by the relentless works. In the recent decades of MOSFET researches, people have been focusing on shrinking the device size due to two fundamental reasons.[9-12] Firstly, the smaller the devices are, the larger amount of them can be integrated in a circuit. With a fixed cost of entire wafer process, the average cost of a single function can be reduced by larger amount of devices. Secondly, the smaller device can offer faster switch delay for the logic function, thereby to achieve higher speed of the circuit. **Table 1.1** lists in detail the size scaling results of the devices with constant electric field.[13] With the shrinkage of the device size, the shorter switch delay, smaller power dissipation and larger number of transistors are obtainable, which is beneficial to

improve the speed and the total number of functions on a single chip. Therefore, the scaling of the device size is the major trend for the MOSFET technology development for the recent decades.

Table 1.1 scaling effect on the device parameters with device sized reduced by a factor K. Here α is a scaling factor which is larger than 1.[13]

Parameters	Expressions	Scaling
Saturated I_d	$I_d=V_{sat}W_gC_{ox}(V_g-V_{th})$	K
I_d/gate wide	I_d/W_g	1
Gate capacitance	$C_g=\varepsilon_0\varepsilon_{OX}L_gW_g/t_{OX}$	K
Switch speed	$\tau=C_gV_{dd}/I_d$	K
Clock frequency	$f=1/\tau$	1/K
Chip area	A_{chip}	α
Integration	N	α/K^2
Power per chip	$P=fNCV^2/2$	α

To utilize the aforementioned benefits of smaller devices, semiconductor enterprises have managed to reduce the device size by half in about every 3 years, following the prediction by Moore's low.[14] **Figure 1.2** shows the international technology roadmap for semiconductors (ITRS) technology node of logic and memory devices,[15] which basically reflects the half pitch scale of a single MOSFET. The blue squares represent the technology nodes which have already been achieved and the red circles are those expected in the near future.

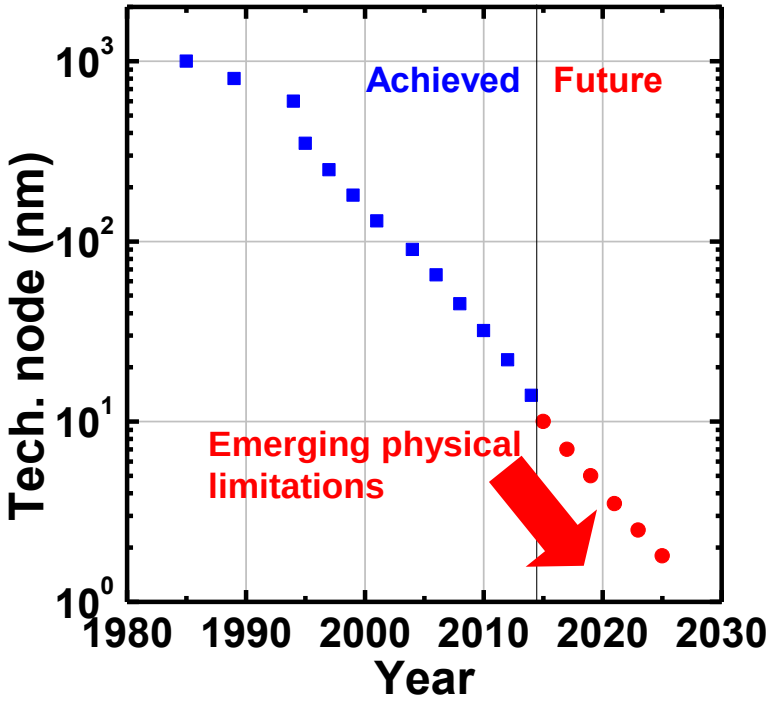


Figure 1.2 ITRS technology node of device scaling by years.[15] The half reduction of the device dimensions has been successfully carried out every 3 years so far, but further reducing the device size to a few nm will inevitably face the physical limitations.

Regardless of the success on device scaling so far achieved, the simple reduction of devices size is no longer a viable choose for future since many intrinsic limitations emerge when the devices are in only several nm size. In the horizontal direction, short channel effect appears when the source and drain depletion regions take a substantial proportion of the channel length, featuring large source drain leakage current.[6,16] In the vertical direction, to have sufficient control of the channel field by the gate bias, the thickness of the gate insulator is expected to be decreased with smaller device size, which inevitably results in a large gate leakage current (J_G), limiting the further scaling of the oxide thickness.[17, 18] Furthermore, the heavily doped source and drain region need to be more shallowly profiled with scaling of the device to maintain a high on current,[18, 19] which is a great challenge for the doping technics concerning the solubility limitation. These intrinsic limitations,

together with overwhelming production cost, make the further device size scaling virtually unattainable and useless.

Alternative approaches have been investigated to extend the semiconductor development in the More Moore era as summarized in **Figure 1.3**.[13] These approaches are dealing with either device topology, gate insulator materials, or channel materials. Among them, replacing Si with high mobility (μ) semiconductors and replacing ploy-Si/SiO_2 with metal gate/high-*k* dielectric might be a feasible choice for the MOSFET with high carrier mobilities and thin equivalent oxide thickness (EOT).

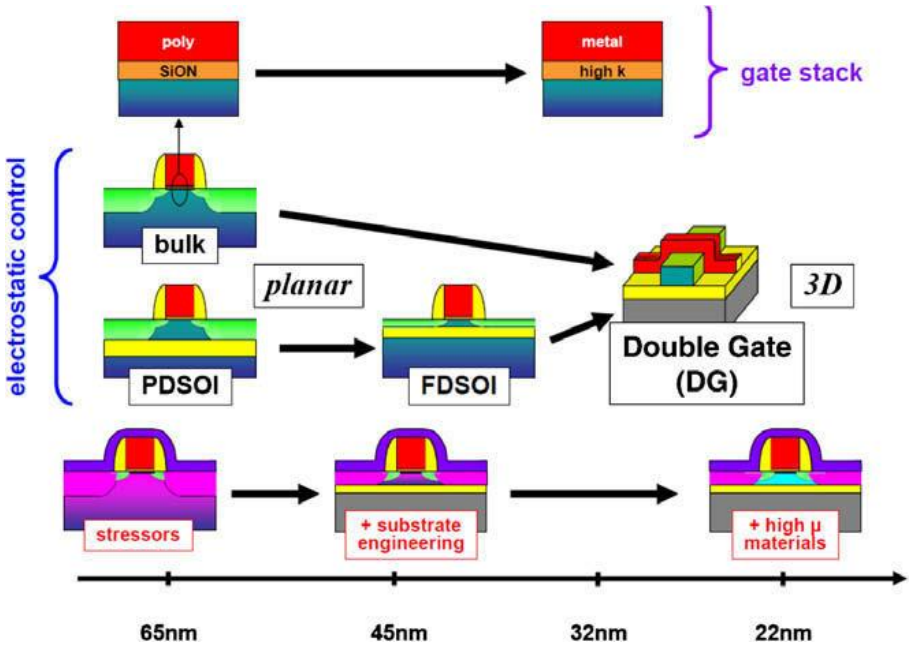


Figure 1.3 Schematics of various approaches to improve the device properties in the post dimensional scaling age.[13] The device structure, gate insulator material and channel material are all possible components that can be improved.

Various high-μ semiconductors have been investigated[20-23] to substitute Si as listed in **Figure 1.4**. Among them, germanium (Ge) has both high electron and hole mobilities over that of Si. It is notable that, though some group III-IV compound semiconductors have even higher electron mobilities, their hole mobilities are not satisfying. Thus, a balanced high electron and hole mobilities of Ge are a great advantage in terms of make the

complimentary MOS (cMOS) operations. Moreover, the low processing temperature of Ge makes it easier to be integrated in the existing Si technology. Therefore, Ge has emerged as the feasible channel material in replacement of Si.

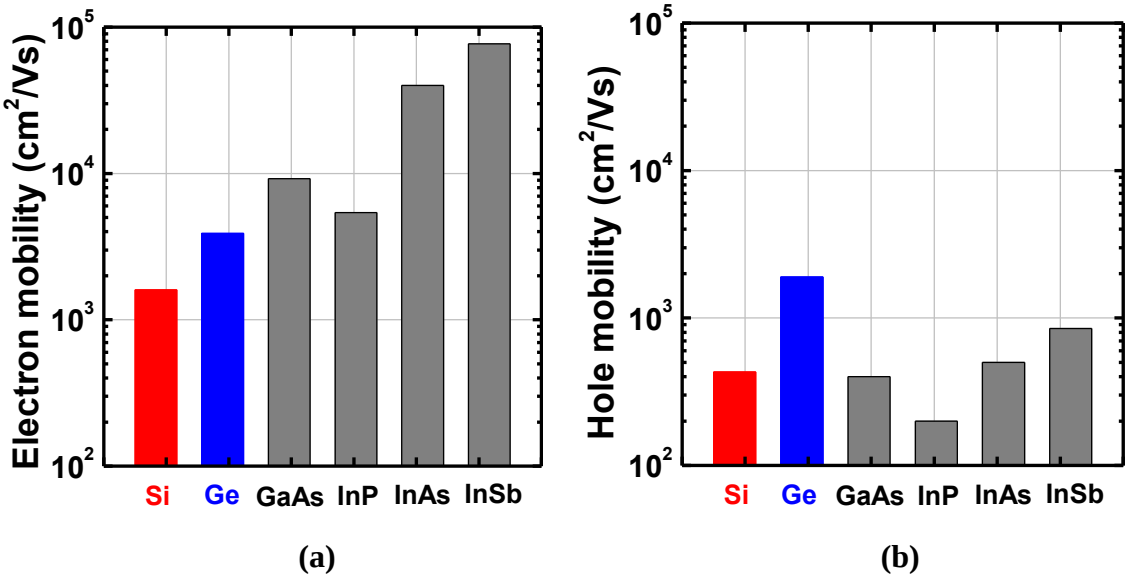


Figure 1.4 Bulk mobilities of **(a)** electron and **(b)** hole for various semiconductors. The striking advantage of Ge over the other semiconductor materials is that its electron and hole mobilities are higher than Si in a balanced way.

Ge is a lustrous, greyish-white matter in the group IV_b in periodic table. It has five natural isotopes, namely, 70Ge, 72Ge, 73Ge, 74Ge and 76Ge. The structure of crystallized Ge is diamond structure in cubic phase, which is the same with that of crystallized Si. The other physical properties of Ge at room temperature (RT, 300K) are listed in **Table 1.2** in comparison with Si.[24]

Table 1.2 Basic physical properties of Ge and Si at 300 K.[24]

Properties	Ge	Si
Density (g/cm^3)	5.323	2.329
Lattice constant (A)	5.658	5.431
Melting point (^oC)	937	1415
Dielectric constant	16.0	11.9
Band gap (eV)	0.66	1.12
Electron affinity, χ(V)	4.0	4.05
Breakdown field (V/cm)	$\sim 10^5$	$\sim 3 \times 10^5$

1.2 Requirements for gate stack design in Germanium MOS device

1.2.1 Intrinsically good interface of GeO_2/Ge

To ensure the high channel mobility, merely selecting a high-μ channel material is not enough, because the carriers in the channel are scattered by various mechanisms, namely, the Coulomb, phonon and surface roughness scatterings.[25] Among them, the Coulomb scattering is dominating the channel mobility under a low field, and is largely determined by the selection of gate oxides. Because, without a sufficient passivation of the dielectric/Ge interface, a large density of interface states (D_{it}) might exist, which act as scattering source to limit the channel mobility.[25] Therefore, the formation of a promising gate stack is one essential requirement for fully utilizing the high-μ of Ge. Germanium dioxide (GeO_2) was naturally considered as the gate dielectric for Ge gate stack formation[26] simply inspired by the successful SiO_2/Si system. As expected, very promising interface properties has been obtained by the growth of high quality GeO_2 through various methods thermally or chemically.[27-29] The D_{it} can be controlled at about 1×10^{11} $eV^{-1}cm^{-2}$ near the mid gap for these well prepared GeO_2/Ge gate stack.[27-29] Ge MOSFET operations have also been demonstrated with both electron and hole mobilities exceeding Si

universality[25] by GeO_2/Ge interface as summarized in **Figure 1.5**. Besides GeO_2, other dielectric materials with various deposition technics have also been investigated for Ge passivation, such as GeON,[30] GeOS,[31] fluorine,[32] silicon,[33] or direct high-k[34-37] passivation. However, on contrary to GeO_2/Ge interface, these passivation methods result in relatively higher D_{it}, which cannot yield high mobility for MOSFET operation. Therefore, we believed that GeO_2 was the best candidate for Ge interface passivation so far.

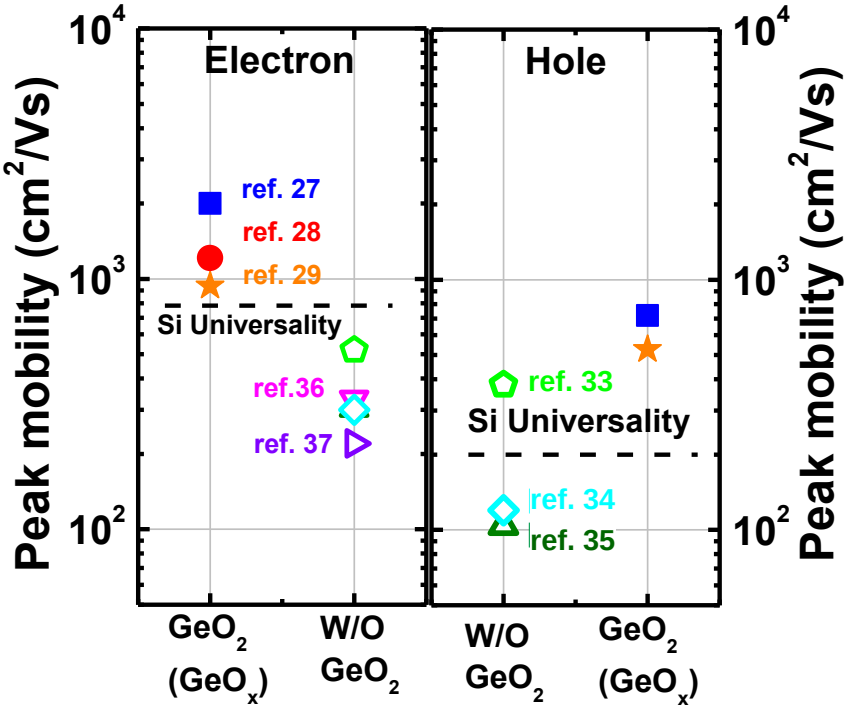
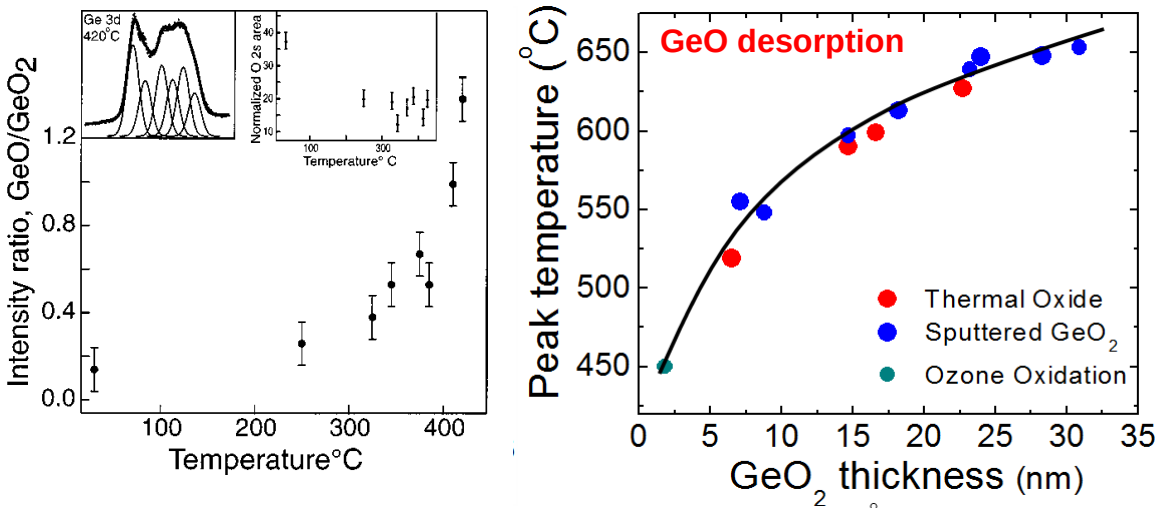


Figure 1.5 Channel mobilities in Ge MOSFET reported in the literatures with high quality $GeO_{2(x)}$/Ge interface[27-29] or with other dielectric passivation.[33-37] Both high electron and hole mobilities over that of Si universality[25] have been demonstrated by GeO_2/Ge interface. While with other passivation methods, the mobilities are relatively poorer.

1.2.2 Challenges for the Ge gate stack formation

Regardless of the promising properties of GeO_2/Ge interface, there are still critical concerns on utilizing GeO_2/Ge system for device application in a real scene. Firstly, GeO_2 is a relatively soft material comparing to SiO_2,[38] which makes GeO_2/Ge stacks thermally and chemically unstable. The formation of Ge monoxide (GeO) in the GeO_2/Ge stack is

observed from a relatively low temperature as shown in **Figure 1.6(a)**,[39] which reflects the reaction between GeO_2 and Ge. The formed GeO is then desorbed from the surface of GeO_2/Ge stack and is detectable in the thermal desorption spectrum (TDS). **Figure 1.6(b)** shows the GeO desorption peak temperature from GeO_2/Ge gate stacks as a function of initial thickness of GeO_2 according to previous reports.[40] GeO desorption occurs at a relatively low temperature, which is accompanied by the oxygen vacancy (V_O) formation and electrical properties degradation.[40]



(a) **(b)**

Figure 1.6(a) GeO component in the GeO_2/Ge gate stack as a function of annealing temperature.[39] The inset shows the typical fit with six components due to three species, Ge, GeO and GeO_2. Also shown in the inset is a plot of the intensity of the signal due to oxygen normalized by the beam current, indicating that the amount of oxygen remains essentially unchanged during the transformation. **(b)** GeO desorption peak temperature from GeO_2/Ge stacks as a function of GeO_2 thickness.[40] The desorption temperature is quite low, especially for thin GeO_2.

The highly hygroscopicity nature of GeO_2 is also a big problem. **Figure 1.7(a)** shows the thickness of GeO_2 as a function of immersion time in pure deionized water (DIW). On

contrary to water insoluble SiO_2, several nm of GeO_2 is immediately etched by DIW. The hygroscopic nature of GeO_2 incurs not only great trouble in the device process but also reliability issue with exposure to air as shown in **Figure 1.7(b)**.[41] Both thermal instability and water solubility are among the biggest obstacles against bringing Ge back to future in spite of superior GeO_2/Ge interface properties.

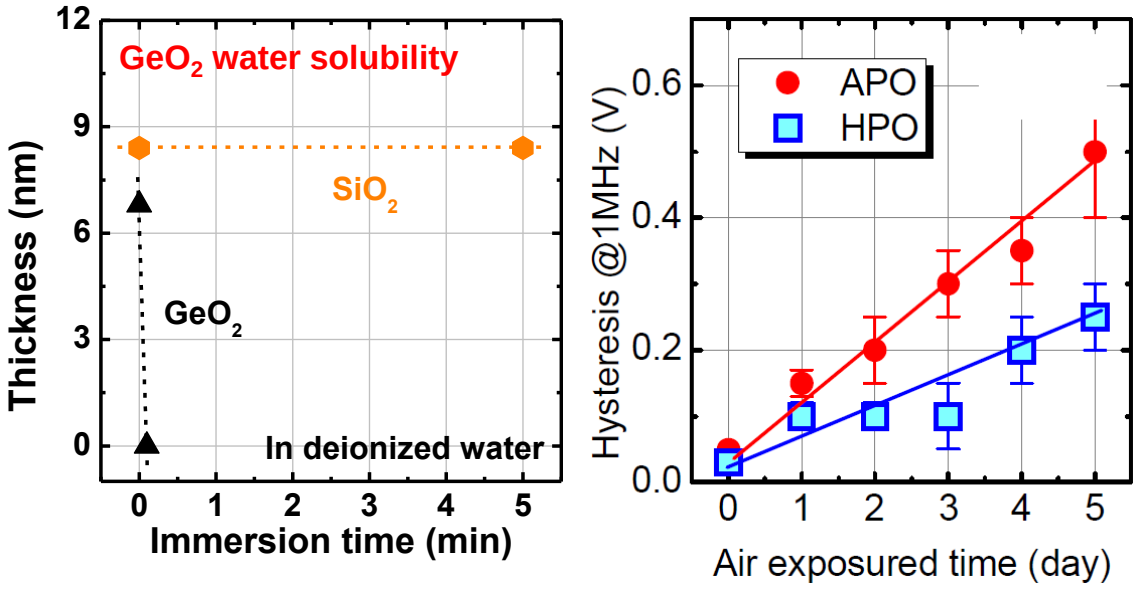
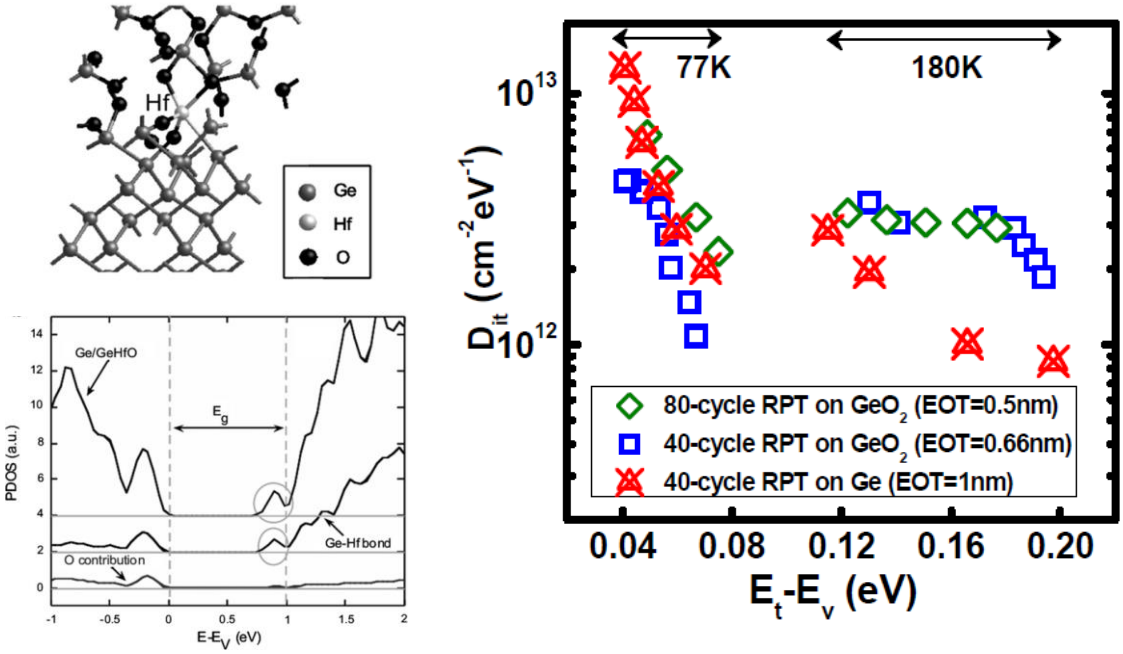


Figure 1.7(a) The thickness of GeO_2 and SiO_2 as a function of immersion time in DIW. SiO_2 is not etched by water, while GeO_2 is etched immediately. **(b)** Hysteresis of the *C-V* curves of GeO_2/Ge gate stack as a function of time with exposure to air.[41] Regardless of the good initial properties, the hysteresis increase a lot with air exposure.

Since the dielectric constant (k) of GeO_2 is about 5.2 to 5.9,[26, 42] it is naturally hard for GeO_2/Ge stack to achieve an EOT beneath 1 nm with affordable J_G. Therefore, only ultra-thin GeO_2 layer can be used as an interfacial layer (IL) between Ge and high-k dielectrics. The high-k/IL/Ge gate stack would be valid even for a real device application with very high switching frequency, because the high k-value is not reduced up to several

tens of GHz.[43] On the other hand, the biggest concern is the impact of high-*k* dielectrics on the interface. Due to the soft nature of GeO_2, considerable intermixing might occurs between the top high-*k* dielectrics and the GeO_2 IL in such bilayer stacks,[44, 45] which makes the interface properties highly sensitive to the high-*k* dielectric as well. Most conventional high-*k* dielectrics are expected to form a defect state by intermixing into GeO_2 IL as shown in **Figure 1.8(a)** (HfO_2 on Ge in this example).[46] Thus, the criteria for selecting proper high-*k* materials on sub-nm EOT Ge gate stack formation is more strict and comprehensive than that on Si. Without a proper high-*k*, the scaling of the EOT will inevitably be at the cost of D_{it} increase. This is the reason for the unsatisfying interface properties for very thin EOT Ge gate stack as reported in previous works (**Figure 1.8(b)** for a ZrO_2 as high-*k*, which is very similar to HfO_2[34]). Therefore, selecting a proper high-*k* oxide with interface awareness becomes a key to the EOT scaling in sub-nm region.



(a) **(b)**

Figure 1.8(a) First principle calculations on the defect state formation when conventional high-*k* dielectric (HfO_2 in this case) was intermixed with GeO_2 IL.[46] **(b)** D_{it} spectra of an aggressively scaled Ge stack with ZrO_2 as high-*k* (similar to HfO_2).[34] Though very thin EOT is demonstrated, the D_{it} is in the order of 10^{12} $cm^{-2}eV^{-1}$ near the mid gap (almost 10

times higher than the state-of-the-art low D_{it} in Ge stack), which is not satisfying for high mobility MOSFET application.

Moreover, it is reported in the previous literatures that the higher *k*-value in the transition oxides are always at the cost of the smaller band gap as shown in **Figure 1.9**.[47] For the low-*k* oxides like SiO_2, the band gap can be as wide as 9 eV. While, for the ultra-high-*k* oxide TiO_2, the band gap is only about 3 eV. The narrower band gap significant blurs the advantage of high-*k* dielectrics in terms of reducing J_G. Thus it is a great challenge to find a suitable combination of high-*k* value and sufficient band gap.

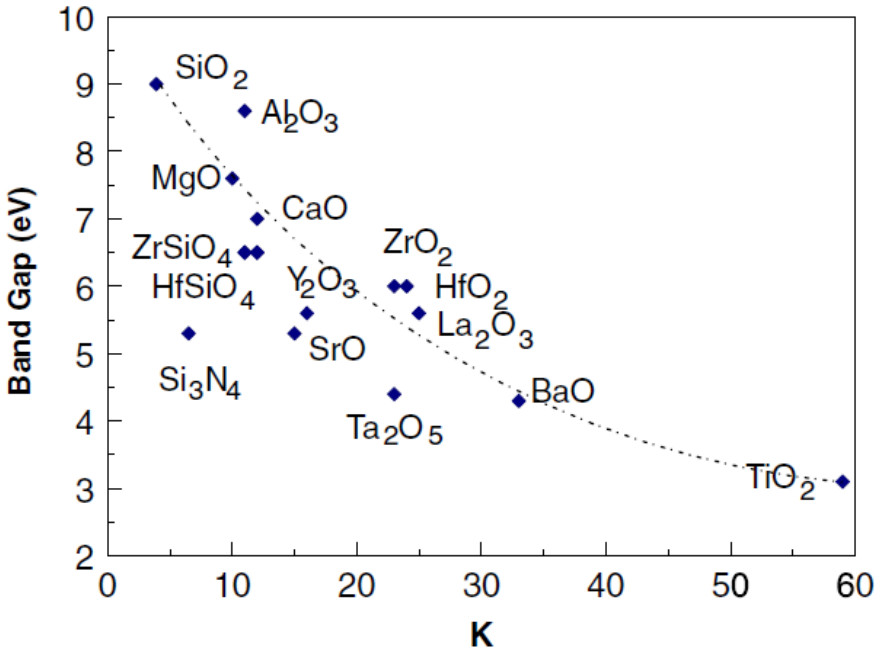


Figure 1.9 Band gap of various oxides as a function of the *k*-value.[46] The higher *k*-value is always at the cost of smaller band gap for normal transition metal oxides.

Finally, the promising initial characteristics of Ge MOS devices do not necessarily secure their long term reliability. Under an electric stress field (E_{stress}), electron or hole are injected into the gate dielectric and might be captured by some trap sites in the dielectric, which results in the shift of device parameters over time as schematically shown in **Figure 1.10(a)**.[48, 49] The D_{it} or bulk trap density might also be increased by the E_{stress}, which brings

about more severer shift of threshold voltage (V_{th}), the degradation of the trans-conductance (G_m) or the increase of J_G. A comprehensive understanding is not yet obtained on the long term reliability properties of Ge MOS devices. The reports so far indicate that the trapping is much severer for Ge MOS than that of Si counterpart (**Figure 1.10(b)**).[50] A systematic assessment on the Ge gate stack reliability is to be carried out to understand the reliability degradation mechanism and to improve the long term reliability projection.

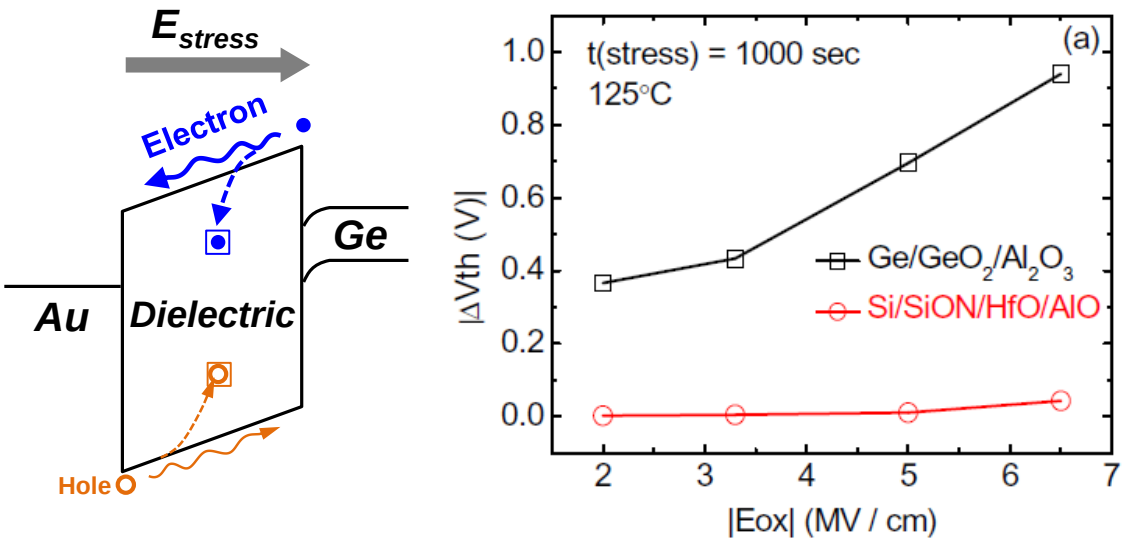


Figure 1.10(a) Schematics of the carrier trapping in Ge MOS device under and positive E_{stress}. The electrons are injected from the Ge to gate metal and the holes are injected in an inverse direction. Both might be captured by the trap sites in the dielectric. Similar situation can be expected for negative E_{stress}. **(b)** V_{th} shift as a function of electric field in Ge and Si stacks.[50]

1.3 Objective and organization of this work

In this work, I will focus on the gate stack formation on Ge in terms of aforementioned challenges. Under the presumption of (1) intrinsically good GeO_2/Ge based interface, I will discuss the (2) improvement of the thermal and chemical robustness of the GeO_2/Ge based

interface. (3) design of an interface aware high-*k* for EOT scaling of Ge gate stack, and (4) understanding and improvement of the reliability of Ge gate stack for long term application. It is important to note that all the challenges should be addressed simultaneously and the solution of one issue should not be at the cost of sacrificing another. The approaches in this work are not simple optimization of process, but the research into entirely new materials which are intrinsically good for Ge MOS device application.

In the first chapter, inspired by thermodynamics on metal oxides, yttrium oxide doped GeO_2 (Y-GeO_2) is investigated for interface passivation on Ge. Significant improvement of both thermal stability and water resistance was demonstrated in GeO_2/Ge stack by replacing GeO_2 with Y-GeO_2. The excellent electrical properties of Y-GeO_2/Ge stack with low D_{it} are presented as well as the enhancement of *k*-value in Y-GeO_2 layer, which is beneficial for further EOT scaling of Ge gate stack. Based on an systematic investigation of various metal oxides doping effect on GeO_2, a structural modification model was proposed to explain the material properties change in metal oxide doped GeO_2 (M-GeO_2).

In the second chapter, the proper high-*k* dielectric is designed for EOT scaling into deep sub-nm. Since many conventional high-*k* oxides cause interface degradation when they are intermixed with GeO_2 IL, the critical point here is to compromise the sufficient *k*-value with the awareness of the interface properties. An alternative approach for designing high-*k* oxide is proposed in this chapter, namely the formation of a ternary real high-*k* out of two promising binary medium-*k* materials. As an example, yttrium scandate ($YScO_3$) is demonstrated for gate stack formation on Ge, which enables the scaling down of the EOT to about 0.5 nm with affordable interface degradation. Ge n-MOSFET was also examined, which achieved the record high peak electron mobility (1057 cm^2/Vsec) in the sub-nm EOT region.

In the third chapter, the reliability assessment was carried out on Ge gate stack with good initial properties. This work focuses on the trap density pre-existing in the

as-prepared gate stack and the degradation of the dielectric under a high E_{stress}. It is found that though the initial trap density in the GeO_2 is controllable by process condition, the degradation of the dielectric under high E_{stress} is dominated by the intrinsically weak network of GeO_2. The relatively rigid network materials like Y or Sc-GeO_2 can suppress both interface degradation and trap generation under high E_{stress}. The impact of different high-*k* on the reliability of Ge gate stack is also assessed.

Though the aforementioned challenges are solved separately in each chapter, the underlying physical understanding is in common. In a word, by manipulating the structure of the oxides, both the material and electrical properties of the oxides might be improved. In the final chapter, I will summarize such structure/property relationships for the oxides on Ge gate stack and offer a guideline for the Ge gate stack design in deep-nm EOT region.

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Chapter 2

Rigidity coordination in GeO_2 network

2.1 Thermodynamics for interface reaction and thin films

2.2 Enhancement of thermal stability and hygroscopic tolerance in Y-GeO_2

2.3 Network modification model for metal oxide doped GeO_2

2.4 Concerns: interface defect bond and bulk immiscibility

Overview:

The thermal and chemical robustness of the GeO_2/Ge system is a vital concern in Ge gate stack formation. In this chapter, metal oxide doped GeO_2 (M-GeO_2) is proposed to substitute GeO_2 for a robust IL formation in Ge stack according to the thermodynamic consideration. It is found that yttrium doped GeO_2 (Y-GeO_2) can improve the thermal stability of GeO_2 by over 100^oC and reduce the water etching rate of GeO_2 by over 1000 times. The promising interface property comparable to the state-of-the-art GeO_2/Ge is also demonstrated.

To consistently explain the improvement of thermal and chemical stability, the modification of GeO_2 continuous random network (CRN) model is proposed, which build up a simple relationship between the network structure and various material and electrical properties. A systemic comparison on the material and electrical properties has also been carried out among different M-GeO_2/Ge stacks to further examine the MRN model. Two criteria for selecting desirable doping materials in GeO_2 are proposed. Firstly, metal cations with larger ionic radii are more preferable for their stronger influence on the GeO_2 network rigidity, which result in the higher thermal stability and water resistance. Secondly, metal oxides are necessarily to be unreactive with Ge substrate (typically trivalent oxides) to prevent the Ge-M metallic bond formation.

2.1 Thermodynamics for interface reaction and thin films

Regardless of its similarity with SiO_2, GeO_2 has been well known of its unstable thermal and chemical properties. It has been clarified that volatile germanium monoxide (GeO) are easily desorbed from GeO_2/Ge stack at a relatively low temperature.[1] **Figure 2.1** schematically shows the GeO desorption mechanism from GeO_2/Ge stacks under thermal process.[2] It is notable that the GeO desorption involves the oxygen vacancy (V_O) formation

at the bottom GeO_2/Ge interface, diffusion through the bulk GeO_2 and reaction at the top GeO_2 surface. Thus, the GeO desorption can deteriorate the electrical properties by generating a huge amount of both D_{it} and bulk defects. Related to the unstable nature of GeO_2, the water solubility is another big concern. It not only incurs difficulty in GeO_2/Ge based device process but also results in the degradation of GeO_2/Ge interface properties with exposure to atmosphere.[3, 4] Both thermal instability and water solubility are among the biggest obstacles against bringing Ge back to future in spite of superior GeO_2/Ge interface properties. Such unstable properties blur the intrinsically promising electrical properties of GeO_2/Ge interface and bring great difficulties in MOS application. Many attempts have been made to solve these issues, such as GeON or Al_2O_3 capping layer.[5, 6] However, these approaches are always at the cost of interface properties or EOT, which is also unwanted. Thus, an alternative material is needed beyond GeO_2 for a robust Ge MOS device application.

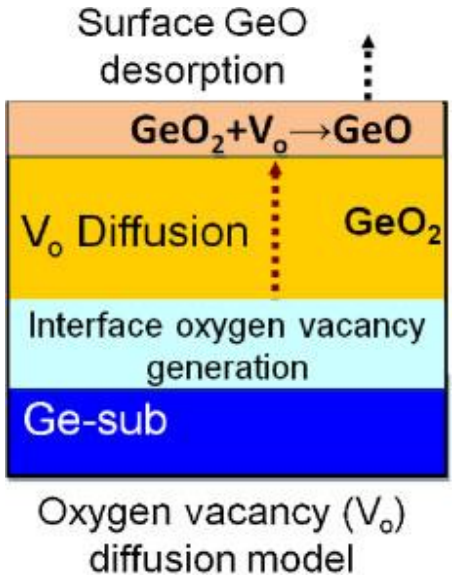


Figure 2.1 schematics of GeO desorption mechanism in GeO_2/Ge stacks under thermal process.[2] The GeO desorption process is accompanied by the V_O formation and diffusion throughout the GeO_2 layer, which result in drastic degradation of electrical properties.

A basic understanding on why GeO_2/Ge stack is thermally unstable must be obtained before any improvement work can be carried out. The Ellingham diagram of the metal oxide formation is an effective tool for analyzing the stability of metal oxides thermodynamically. **Figure 2.2** shows the Ellingham diagram for GeO_2 and SiO_2 formation under various oxygen ambient conditions calculated from thermodynamic data base.[7] Note that the ΔG^0 values are Gibbs free energy for the corresponding oxides formation and P_{O2} is the oxygen partial pressure in the annealing ambient which is named as oxygen potential.

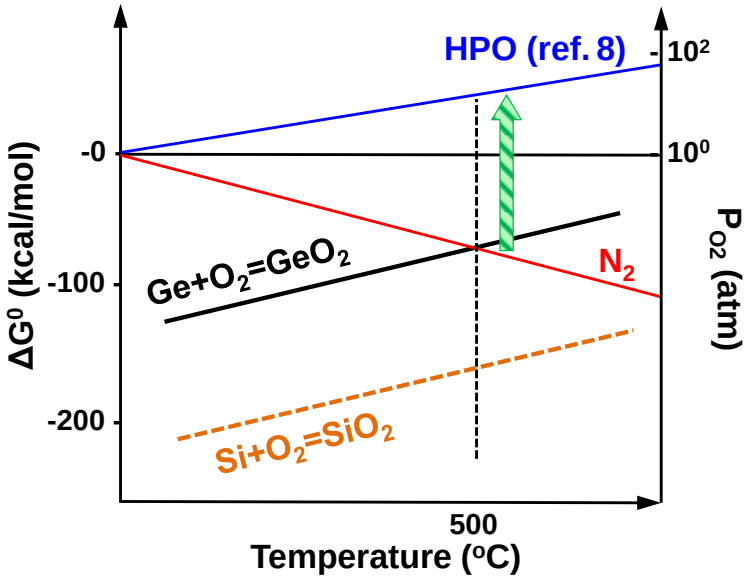


Figure 2.2 Ellingham diagram for GeO_2 and SiO_2 formation under various oxygen ambient conditions calculated from thermodynamic data base.[7]

In the Ellingham diagram, the region with ΔG^0 lower than ambient oxygen potential corresponds to a stable oxide. In the current example, GeO_2 should be stable at low temperature and SiO_2 is stable within all the range in Figure 2.2. On the contrary, the region with ΔG^0 higher than ambient oxygen potential in the diagram corresponds to the decomposition of the oxide, namely, the GeO desorption from GeO_2/Ge stack.

Quantitatively, such a relationship between the oxide stability, ΔG^0 and ambient oxygen potential in the Ellingham diagram can be summarized into the following equation:

$$\Delta G=\Delta G^0-RTln(P_{O2}) \quad (2.1)$$

The requirement for keeping a stable oxide is to ensure the sufficient energy gap (ΔG) between ΔG^0 and $RTln(P_{O2})$, like SiO_2. Inspired by the Ellingham diagram, high pressure oxidation (HPO) was invented as reported in the previous works,[8] which yields high quality GeO_2 growth on Ge. The reason for the success of HPO is that it can create the sufficient ΔG between ΔG_0 and $RTln(P_{O2})$ as indicated in Ellingham diagram as well (by the blue P_{O2} line in figure 2.2).

It is noticed that the sufficient energy gap ΔG might also be achieved by changing the oxide materials instead of P_{O2}. By lowering the ΔG_0 value of the oxide, the thermal stability can be improved in a given annealing ambient. There are various kinds of metal oxides having a lower ΔG^0 than that of GeO_2 as shown in **Figure 2.3**. Note that the reaction formulas have been normalized to one oxygen molecule for a fair comparison of ΔG^0. It is expected that by doping these metal oxide into GeO_2 the lower ΔG^0 can be obtained for the mixture and the thermal stability of GeO_2 might be improved. Therefore, the concept of M-GeO_2 is proposed and examined in this work for stable oxides formation.

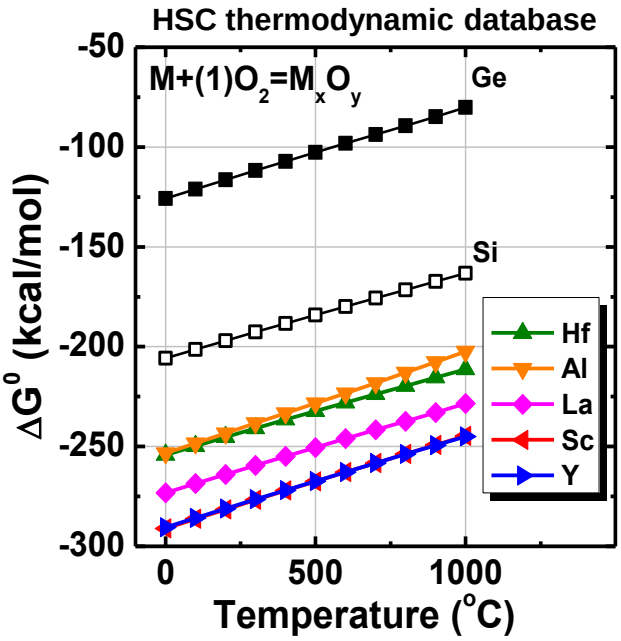


Figure 2.3 ΔG^0 for various metal oxides formation as a function of temperature. Note that the reaction formulas are normalized to one O_2 molecule.

Though the thermodynamics for the stable oxides formation are readily understood, a further concern is the validity of the thermodynamic understandings on the thin film and interface reaction. It is wondered if the thermodynamics built up based on the bulk material properties are applicable for the thin film reaction or not. Fortunately, it has been discussed in the previous works that the thin film or interface reactions are influenced by both bulk thermodynamics and interface energy.[9, 10] Let's consider the reaction between the oxides and semiconductors at the interface with sub-oxides as final products. Since the elementary semiconductor and the oxide do not have a same lattice constant or distance between atoms, it is natural to expect that strain might exist on the interface between them. It induces a negative Gibbs free energy for the interface reaction which favors the alloy (GeO_2/Ge reaction in this case) formation[10] in order to release the stress. Thus, one can expect that the thin film GeO_2/Ge interface reaction should occur more readily than that predicted by bulk thermodynamics. The interface energy would also be a possible explanation for existence of transition region (commonly referring to Ge sub-oxides between GeO_2 bulk

and Ge).[11] Nevertheless, for thin film reaction with several nm physical thickness, the thermodynamics still gives a correct direction experimentally.[8] Thus, for the thin film M-GeO_2/Ge, the change of the thermal stability is still expected to be in the same direction as bulk materials though the quantitative meaning might be partially lost.

2.2 Thermal stability and hygroscopic tolerance improvements in Y-GeO_2

2.2.1 Y-GeO_2/Ge gate stack formation

Y-GeO_2 was examined since Y_2O_3 has one of the lowest ΔG^0 among various oxides listed in figure 2.3. To investigate the bulk and interface properties of Y-GeO_2/Ge gate stack, p- and n-type Ge(111) wafer was used with resistivity of 0.6 Ω·cm and 0.7 Ω·cm, respectively. The Ge substrate was chemically cleaned by methanol (10 min in ultrasonic), 8% HCl (1 min) and 2% HF (3 min), sequentially, with DIW rinsing between each step. The smooth surface after wet chemical cleaning of Ge substrate was confirmed by atomic force microscopy (AFM) with RMS roughness at about 0.3 nm.

The gate stack fabrication process is shown in **Figure 2.4**. Y-GeO_2 was deposited on the Ge substrate by rf co-sputtering of GeO_2 and Y_2O_3 targets at the same time. The Y concentration in Y-GeO_2 was controlled by the sputtering power of both targets. Note that Ar/O_2 gas were supplied with 22/0.6 sccm during the sputtering. After deposition of Y-GeO_2 on Ge, the post deposition annealing (PDA) was carried out at 500^oC in N_2 ambient for 30 s. To study the electrical properties of Y-GeO_2/Ge stacks, Au and Al were deposited by vacuum evaporation for the gate electrode and substrate contact of the MOS capacitors (MOSCAPs), respectively, and the capacitance-voltage (*C*-*V*) and current-voltage (*I*-*V*) characteristics were measured at room temperature (RT).

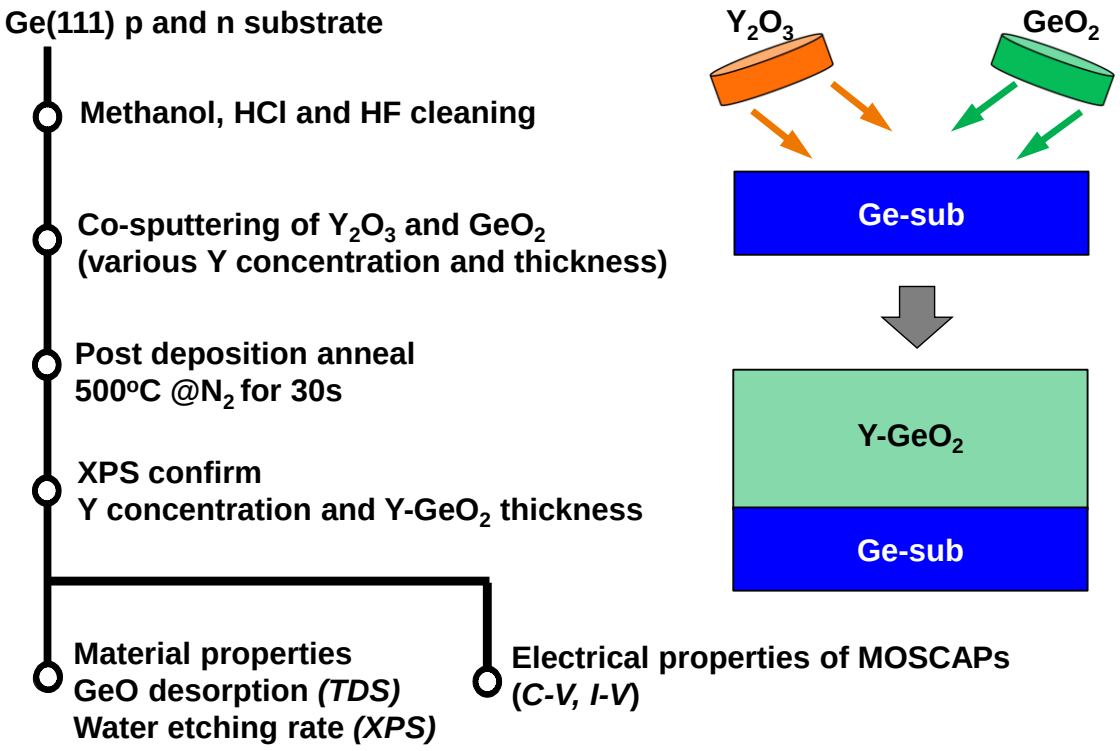


Figure 2.4 Y-GeO_2/Ge gate stack preparation process by rf co-sputtered technics. Note that the annealing process of this gate stack is pure N_2 ambient annealing in 1 atm pressure.

The Y atomic percentage (Y/(Y+Ge)) is calibrated by X-ray photoelectron spectroscopy (XPS). **Figure 2.5** shows the XPS core level spectra of Y3*d* and Ge3*d* from a (4 nm)Y-GeO_2/Ge stack.[12] The Y atomic percentage was calculated from the spectra as follows:[13]

$$Y\ per. = \frac{(I_{Y3d3/2} + I_{Y3d5/2}) / (S_{Y3d3/2} + S_{Y3d5/2})}{I_{Ge4+} / (S_{Ge3d3/2} + S_{Ge3d5/2}) + (I_{Y3d3/2} + I_{Y3d5/2}) / (S_{Y3d3/2} + S_{Y3d5/2})} . \qquad (2.2)$$

Here, *I* and *S* are the intensities and sensitivities of the corresponding XPS core level spectra peaks which are denoted in the subscript correspondingly. Note that the Ge3*d*3/2 and Ge3*d*5/2 are not deconvoluted from the Ge^{4+} signal because these two peaks are located very closely.

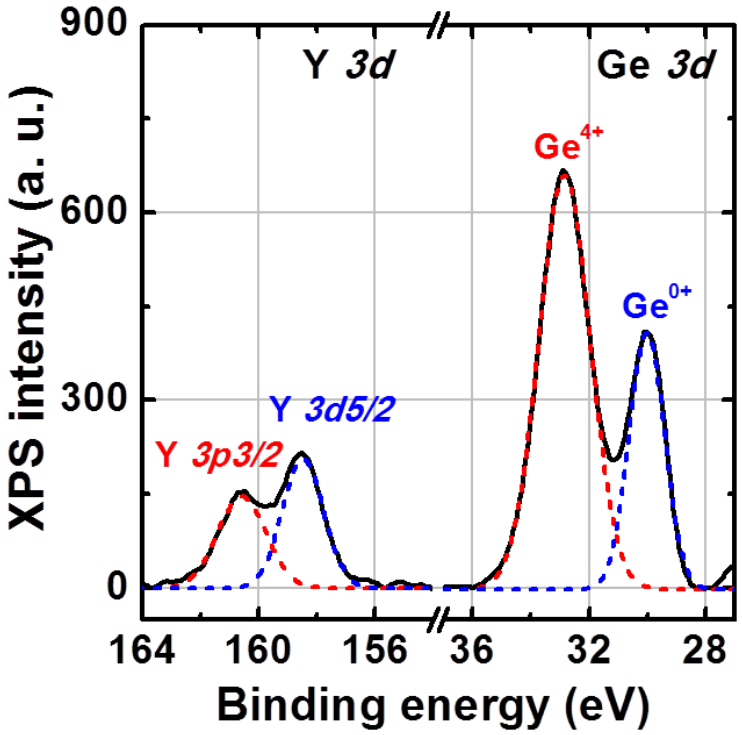
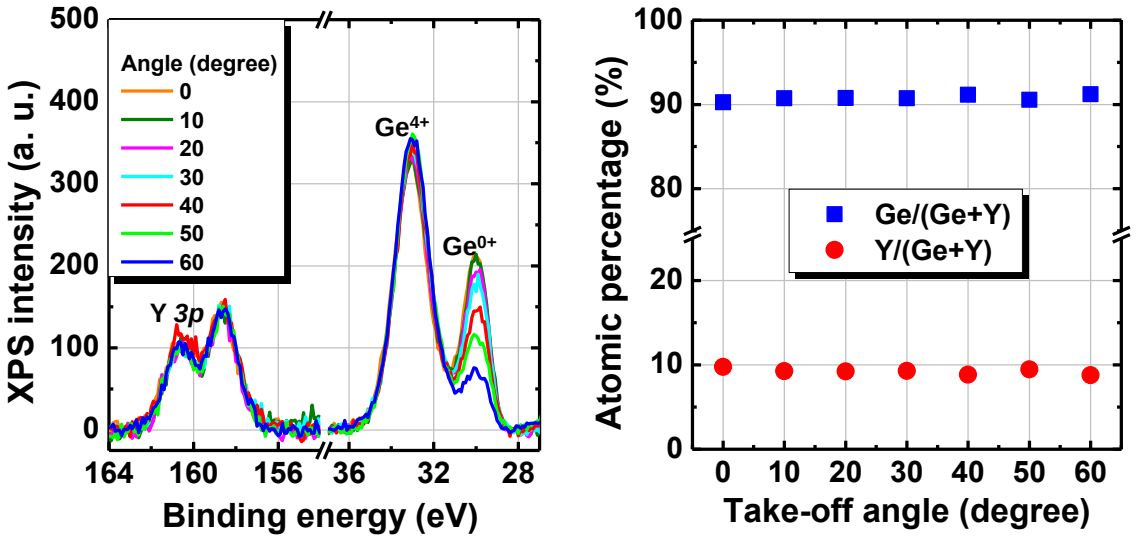


Figure 2.5 XPS core level spectra of Y3*d* and Ge3*d* from a Y-GeO_2/Ge stack. The spectra are deconvoluted as shown in the dotted curves.[12]

Comparing to thermally grown oxides, the uniformity of the deposited Y-GeO_2 thin film is an important property to be confirmed. The depth distribution of the Y component in Y-GeO_2 film was confirmed by angle-resolved XPS. **Figure 2.6(a)** shows the angle-resolved XPS spectra of Y-GeO_2/Ge stack. The intensity ratio between Ge$3d^{4+}$ and Y*3p* is not changed by changing the take-off angle. The atomic percentage of Y and Ge among metallic atoms as a function of take-off angle were calculated and shown in **Figure 2.6(b).** Since the different take-off angle corresponding to the different integration depth of the XPS signal, figure 2.6(b) indicates that Y component has a uniform depth distribution in the GeO_2 film. The surface morphology of Y-GeO_2 was also examined by atomic force microscope (AFM), the low RMS roughness (0.26 nm for (4 nm) Y-GeO_2/Ge stack with 10% Y) indicates a good uniformity of the deposited Y-GeO_2 film. The in-plain x-ray diffraction (XRD) is also measured, which shows the amorphous nature of the Y-GeO_2 after PDA

(data not shown). To maintain a low gate leakage current, the amorphous oxide is preferred over those poly-crystalized ones.



(a) **(b)**

Figure 2.6 (a) Angle-resolved XPS spectra of Y-GeO_2/Ge stack. The intensity ratio between Ge $3d^{4+}$ and Y *3p* is not changed by changing the take-off angle. **(b)** The atomic percentage of Y and Ge among metallic atoms calculated from the XPS spectra as a function of take-off angle.

2.2.2 Thermal stability and hygroscopic tolerance change by Y doping

The thermal desorption spectroscopy (TDS) was used to measure the GeO desorption features from Y-GeO_2/Ge stacks. TDS system (EMD-WA100S/W, ESCO Ltd) is made up of a lamp heater beneath the sample holder, a quadrupole mass spectrometer and an ultra-high vacuum chamber. By heating up the samples through the holder, the atom or molecule species are desorbed from the sample to the vacuum chamber, and finally analyzed by the mass spectrometer. **Figure 2.7(a)** shows the TDS spectra corresponding to GeO (M/z=90) from (3 nm) Y-GeO_2/Ge stacks with various Y percentage. The TDS spectrum from a (3 nm) GeO_2/Ge stack is also shown as a comparison. GeO desorption occurs from a certain temperature for each stacks, becomes faster with increasing

temperature and finishes when all the GeO_2 (or Y-GeO_2) is consumed by the GeO desorption. Thus, a peak appeared in the TDS spectrum for each stack. It is noticed that with small amount of Y doping, the GeO desorption temperature is significantly increased comparing to pure GeO_2 and higher Y percentage leads to higher desorption temperature. **Figure 2.7(b)** shows the GeO desorption peak temperature as a function of initial Y-GeO_2[14] and GeO_2 thicknesses (the data of GeO_2/Ge stack is re-plotted from ref. 2). SiO desorption from SiO_2/Si stacks are also shown for comparison.[15] It has been explained in the previous works that the thickness dependent of the TDS peak temperature in GeO_2/Ge stack comes from the V_O diffusion barrier effect of GeO_2.[2] It is notable that, at each thickness, Y-GeO_2/Ge stack shows obviously higher GeO desorption temperature than GeO_2/Ge stack, indicating a higher thermal stability of Y-GeO_2/Ge stack. The desorption behavior of Y-GeO_2/Ge stack is getting closer to the SiO_2/Si case with high Y concentration. It should be noted that the electrical properties would also benefit from the higher thermal stability due to the suppression of defects formation related to V_O.

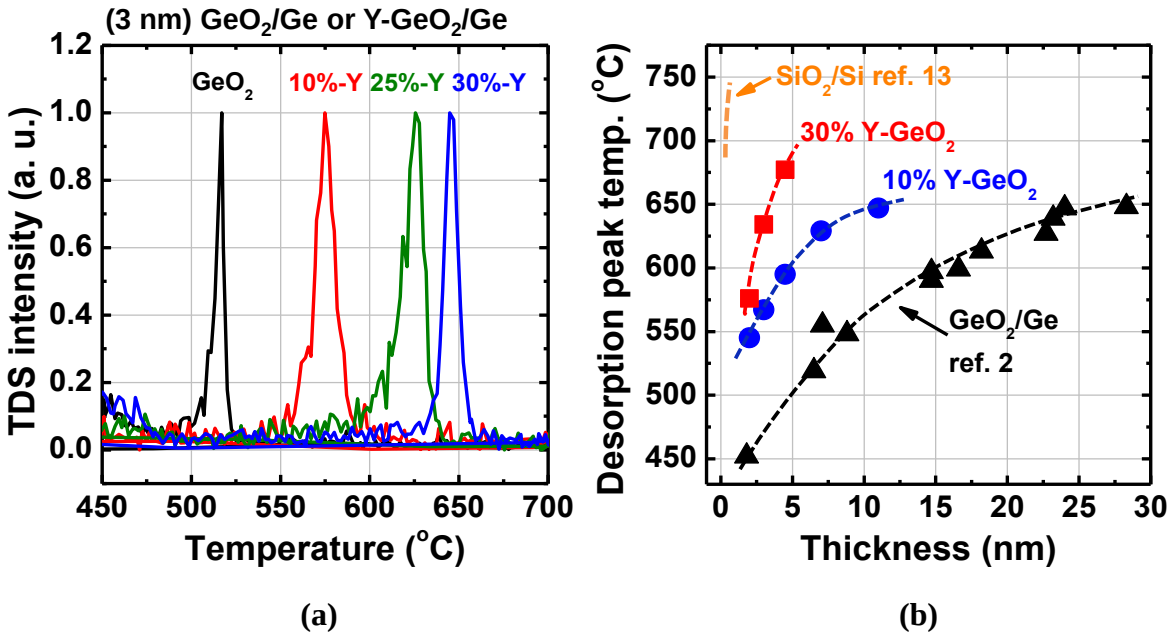
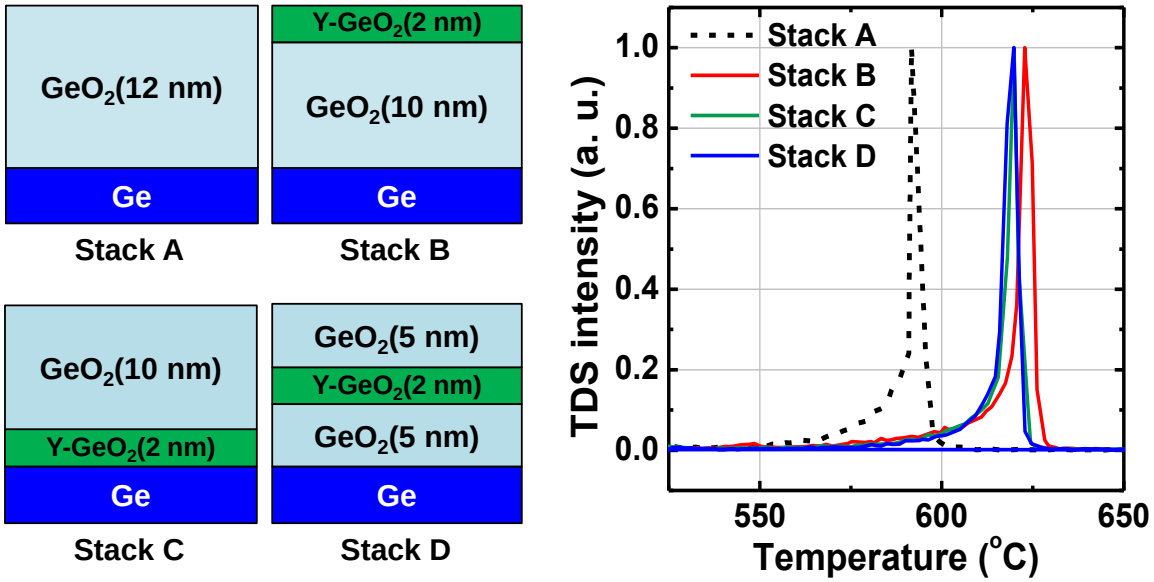


Figure 2.7(a) TDS spectra corresponding GeO (m/z=90) from Y-GeO_2/Ge and pure GeO_2/Ge stacks. Note that the thicknesses of the dielectrics are 3 nm in these stacks. **(b)**

TDS peak temperature corresponding to GeO as a function of initial Y-GeO_2 and GeO_2 thickness[14] (the data of GeO_2/Ge stack is re-plotted from ref. 2). Note that desorption of SiO from Si/SiO_2 is also shown for comparison.[15] The GeO desorption temperature is increased by the Y-doping.

The V_O formation at GeO_2/Ge interface and diffusion through GeO_2 bulk were believed to be the dominant mechanisms for GeO desorption.[2] To clarify the influences of Y doping on the Vo formation and diffusion, bilayer stacks were deposited as schematically shown in **Figure 2.8(a).** The Y is doped in different positions of the dielectric layer, namely, Y doped on the top(Y-GeO_2/GeO_2/Ge), on the bottom (GeO_2/Y-GeO_2/Ge) and in the middle, while the total thickness of the dielectrics is fixed at 12 nm. TDS spectra of GeO desorption from these bilayer stacks are shown in **Figure 2.8(b)** together with the spectrum of a (12 nm) GeO_2/Ge stack. As expected, the desorption temperatures of all the bilayer stacks are higher than that of GeO_2/Ge stack. However, the desorption temperature of all the bilayer stacks are almost the same regardless of the different positions of Y doping. Therefore, it can be concluded that the suppression of GeO desorption are mainly attributable to the limitation of Vo diffusion by Y-GeO_2.



(a) **(b)**

Figure 2.8(a) Schematic of bilayer stacks with top Y doping (10%Y-GeO2/GeO2/Ge), bottom Y doping (GeO2/10%Y-GeO2/Ge) and in the middle. (b) Corresponding GeO desorption spectra. The spectrum of a 12 nm Ge/GeO2 stack is also shown as reference.

It is note that, from the oxygen/V_O diffusion viewpoint, the upward diffusion of V_O equals to the downward diffusion of the atomic oxygen. Though atomic oxygen diffusion is the main contribution to the GeO desorption process, the Ge thermal oxidation process is majorly discussed in terms of molecular oxygen diffusion. To clarify the molecular oxygen diffusion in Y-GeO_2, thermal oxidation rate of Ge beneath a Y-GeO_2 layer is also examined by XPS. **Figure 2.9** shows the thickness change of GeO_2 as a function of oxygen annealing time at 550^{o}C for (2 nm) Y-GeO_2/Ge and GeO_2/Ge stacks. Almost no further oxidation can be observed in Y-GeO_2/Ge stacks, which supported that Y-GeO_2 is also a strong barrier against molecular oxygen diffusion and oxidation at the interface.

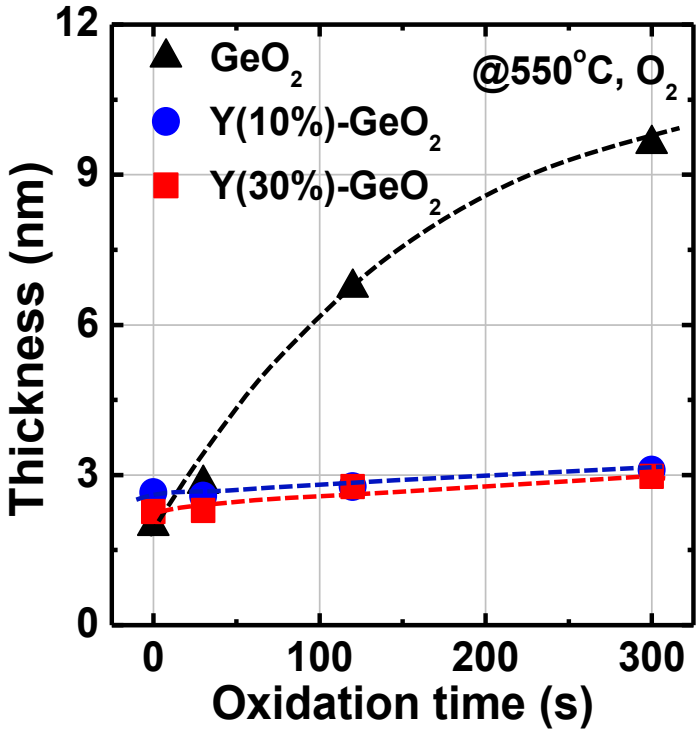


Figure 2.9 Thickness of GeO_2 regrowth in (2 nm) Y-GeO_2/Ge or GeO_2/Ge stacks as a function of time under 550°C O_2 ambient annealing. Regardless of the same initial thickness of Y-GeO_2 and GeO_2, the GeO_2/Ge stack shows significant regrowth of GeO_2, while Y-GeO_2 can block the further oxidation.

Since Y-GeO_2 has significantly changed the thermal stability of GeO_2, it is wondered if the hygroscopic nature of GeO_2 is changed as well. To study the influence of Y-doping in GeO_2 on the water etching properties, Y-GeO_2/Ge and GeO_2/Ge stacks were immersed into the 100% DIW, and the film thicknesses of Y-GeO_2 and GeO_2 with immersion time were measured by XPS, as shown in **Figure 2.10**.[14] It is found that the increase of Y concentration in GeO_2 drastically reduces the wet etching rate of Y-GeO_2 in water, while pure GeO_2 is dissolved in water immediately. The stronger water resistance of Y-GeO_2 will be beneficial not only for the device fabrication process but also for the hygroscopic tolerance of the gate stack.

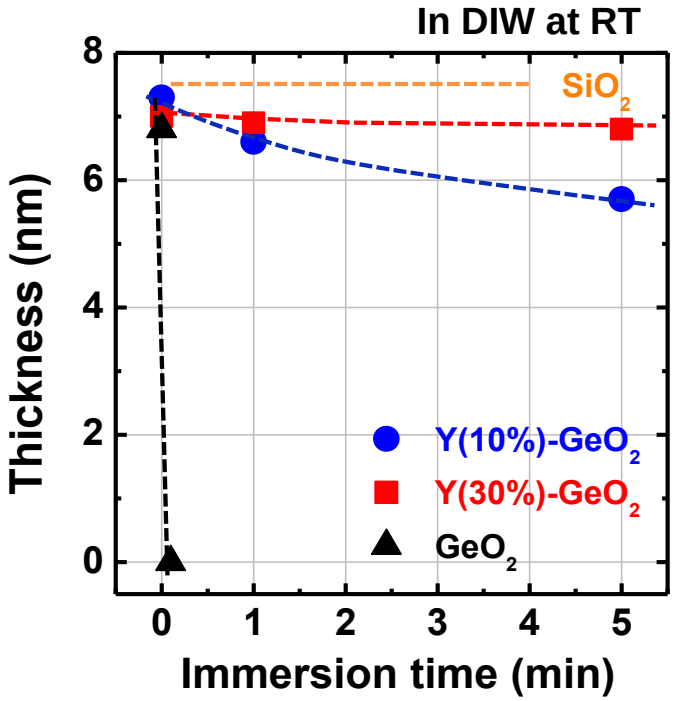
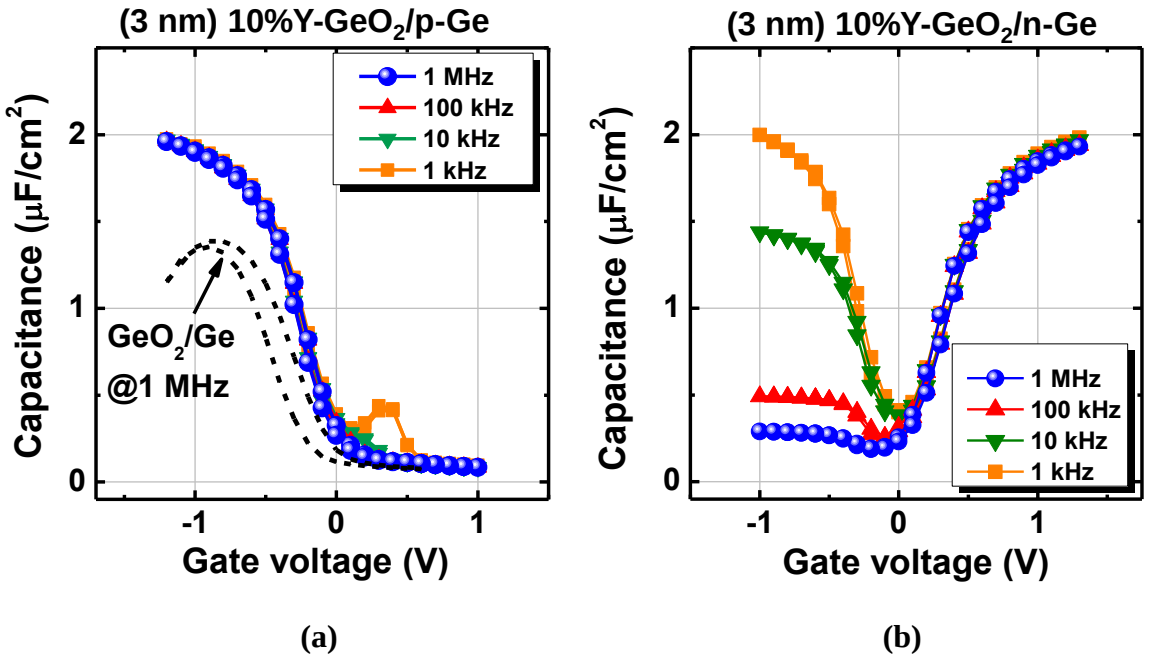


Figure 2.10 Thickness of Y-GeO_2 and GeO_2 as a function of immersion time in pure DIW. The solubility of Y-GeO_2 is drastically decreased. [14] Note that SiO_2 is insoluble in water.

2.2.3 Interface and bulk electrical properties of Y-GeO_2/Ge

To investigate the interface properties of Y-GeO_2/Ge stack, Au/Y-GeO_2/Ge MOSCAPs were fabricated and their electrical properties were measured. **Figure 2.11(a)** shows the bidirectional *C-V* curves of Au/10%Y-GeO_2/p-Ge MOSCAPs measured at RT, where PDA was carried out at 500^{o}C in N_2 ambient for 30s.[14] The physical thickness of Y-GeO_2 is 3 nm and EOT is estimated to be 1.45 nm. The 1 MHz *C-V* curve of pure (3 nm) GeO_2/p-Ge stack is also shown for comparison, the process of which was in a same manner with Y-GeO_2/Ge stacks. A drastic improvement of electrical properties is observed in Y-GeO_2/Ge stack, compared to the pure GeO_2/Ge stack. No hysteresis and frequency dispersion of *C-V* characteristics in Y-GeO_2/Ge stack indicates a low D_{it}. **Figure 2.11(b)** shows the bidirectional *C-V* curves of Au/10%Y-GeO_2/n-Ge MOSCAPs which have the same process condition as that of Au/10%Y-GeO_2/p-Ge MOSCAPs. [14] Note that the *C-V* characteristic of Y-GeO_2/Ge stack undergoes no obvious degradation with one week

exposure to atmosphere, which is attributable to a stronger hygroscopic tolerance as discussed in figure 2.10.



(a) **(b)**

Figure 2.11 (a) Bidirectional *C-V* curves of an Au/10%Y-GeO_2/p-Ge MOSCAPs measured at RT. The 1 MHz *C-V* curve of a sputtered (3nm) GeO_2/p-Ge stack is also shown for comparison. **(b)** Bidirectional *C-V* curves of Au/10%Y-GeO_2/n-Ge MOSCAPs measured at RT.

To quantitatively estimate the D_{it} spectrum of Y-GeO_2/Ge interface, low-temperature conductance method was carried out at 100 to 250 K. **Figure 2.12** shows the energy distribution of the estimated D_{it} in the Au/Y-GeO_2/Ge stacks with various Y concentrations. An extremely low D_{it} was achieved at 10%Y-GeO_2/Ge interface, which is close to the state-of-the-art low D_{it} at GeO_2/Ge interface prepared by HPO.[8] It is worth noting that the D_{it} distribution is in a symmetric U-shape across Ge band gap and not depending on PDA temperature up to 550°C, indicating good thermal stability of this stack. The low D_{it} might be originated from good thermal stability and hygroscopic tolerance of Y-GeO_2, which should effectively suppress the defects formation at the interface. The suppression of the

defect formation by Y-doping is in good accordance with theoretical calculations.[16] Further reduction of D_{it} can be expected by the optimizing the Y-doping concentration and PDA condition.

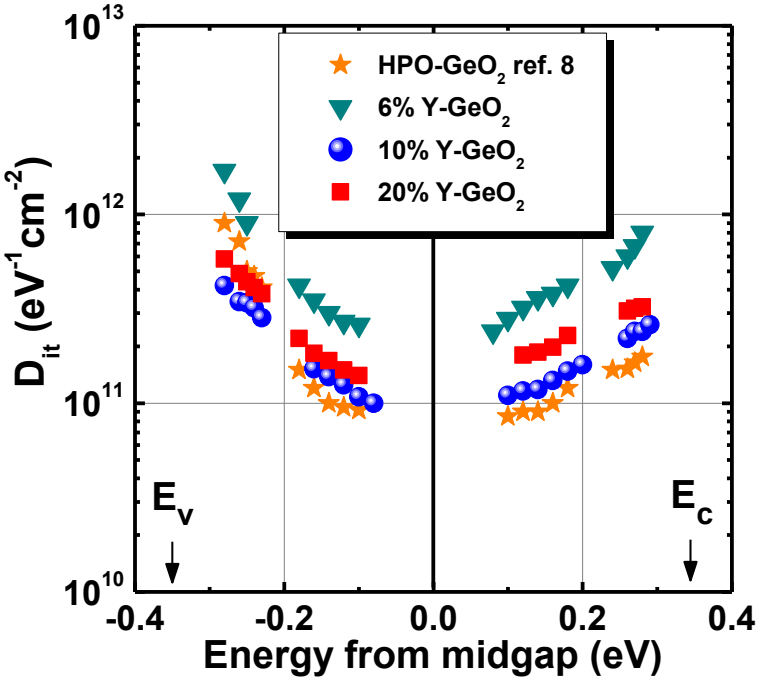
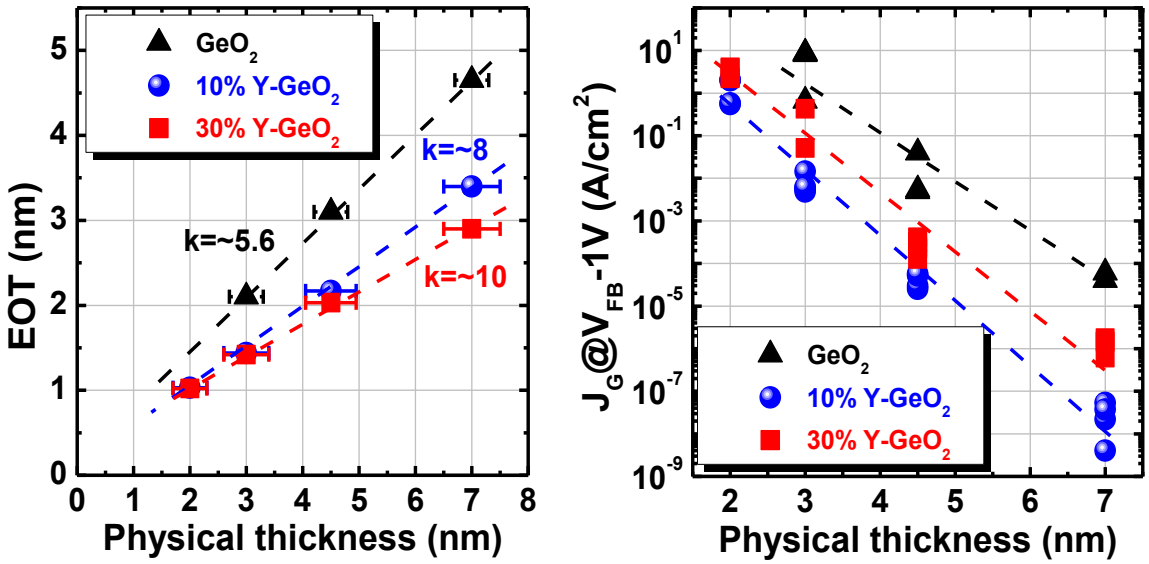


Figure 2.12 Energy distribution of the estimated D_{it} in the Au/Y-GeO_2/Ge stacks with various Y percentages measured by low-temperature conductance method. The state of art low D_{it} at GeO_2/Ge interface prepared by HPO is also shown for comparison.[8]

Since pure GeO_2 has a relatively low dielectric constant (k) (5.2~5.9),[17, 18] it becomes a bottleneck of the EOT scaling in GeO_2/Ge-based gate stacks. Another advantage of Y-doping in GeO_2 is the enhancement of k-value, which is beneficial for further EOT scaling. **Figure 2.13(a)** shows the EOT as a function of Y-GeO_2 and GeO_2 physical thickness.[14] k-value is increased to 8 and 10 for 10%Y-GeO_2 and 30%Y-GeO_2, respectively. It is noticed by a simple math that, the k-value improvements in Y-GeO_2 is higher than the linear combination of GeO_2 (5.2-5.9) and Y_2O_3 (~12). The reason for the non-linear increase of k-value will be further explained in section 2.3.3. The promising properties of Y-GeO_2/Ge stack offer not only superior interface properties with thermal

stability and hygroscopic tolerance, but also enhancement of *k*-value. Therefore, further EOT scaling of Ge gate stack into deep sub-nm range can be expected by using Y-GeO_2 as the IL between Ge and high-*k* dielectrics. **Figure 2.13(b)** shows the corresponding gate leakage current (J_G) as a function of the physical thickness. [14] The J_G of Y-GeO_2/Ge stacks are more than 3 orders of magnitude lower than that of pure GeO_2/Ge stacks prepared in a same manner, indicating the improvement of bulk properties with the suppression of GeO desorption. It is noticed, however, that the J_G of Y-GeO_2/Ge stack increases with an increase of Y concentration from 10 to 30%, indicating that an alternative leakage path might be formed by the excessive Y-doping. The explanation on the change of J_G as a function of Y percentage will be included in section 2.3.4.

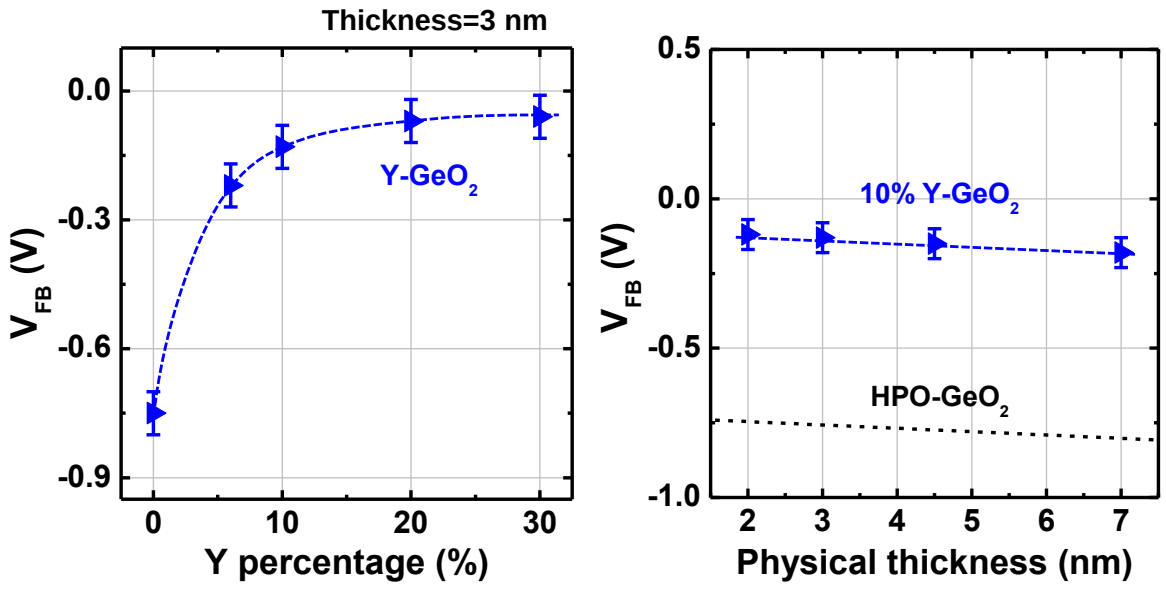


(a) **(b)**

Figure 2.13(a) EOT as a function of Y-GeO_2 and GeO_2 physical thickness. It is notable that the enhancement of *k*-value is observed by Y-doping in GeO_2.[14] **(b)** J_G as a function of Y-GeO_2 and GeO_2 physical thickness.[14]

In the final part of this section, I would like to comment on an interesting phenomenon about the flat band voltage (V_{FB}) in the *C-V* characteristics of the GeO_2/Ge based gate

stacks. A negative shift of the V_{FB} from its ideal value is frequently observed in pure GeO_2/Ge stacks, which has been discussed from the interaction with top metal electrode[19] or absorption of water related species[3, 20]. On the other hand, small amount of Y doping can effectively alleviates this negative shift. **Figure 2.14(a)** shows the V_{FB} in the *C*-*V* curves of GeO_2/Ge and Y-GeO_2/Ge stacks as a function of Y percentage. Since enhancement of water resistance is observed in Y-GeO_2/Ge stacks as shown in figure 2.10, it is reasonable to speculate that Y-GeO_2 can suppress the absorption of water related species. The suppression of V_O formation in Y-GeO_2 also reduces its interaction with top metal electrode. Thus, Y-GeO_2/Ge has a smaller negative V_{FB} shift than GeO_2/Ge. Further increase of Y atomic percentage beyond 10% doesn't cause more V_{FB} shift, indicating that the introduction of metal cations does not yield additional fixed change. A detailed estimation of fixed charge density is carried out using the V_{FB} dependence on the physical thickness of Y-GeO_2 as shown in **Figure 2.14(b)**. Note that the V_{FB} of pure GeO_2/Ge stacks prepared by HPO are also shown for comparison.[4] Generally speaking, if a certain amount of fixed charges exist in the gate dielectric, the V_{FB} should be obviously dependent on the thickness of the dielectrics (the larger thickness, the larger V_{FB} shift). For the Y-GeO_2, the V_{FB} dependent on thickness is so weak that very small amount of fixed charges can be expected in Y-GeO_2. The fixed charges in the Y-GeO_2 are considered to be locally (not uniformly) located in the film and can be estimated to be 1×10^{11} cm^{-2} from the slope of the line, which is as low as the state-of-the-art GeO_2/Ge stacks prepared by HPO. This small fixed charge density in Y-GeO_2/Ge stacks confirms that the no additional fixed change was created by the incorporated Y cations.



(a) **(b)**

Figure 2.14(a) V_{FB} as a function of the Y percentage in Y-GeO_2/Ge stacks. A negative shift of the V_{FB} from its ideal value is frequently observed in pure GeO_2/Ge stacks, while Y doping can effectively alleviate this negative shift. Note that the thicknesses of the dielectrics are 3 nm in these gate stacks. **(b).** V_{FB} of Y-GeO_2/Ge stacks as a function of the physical thicknesses of Y-GeO_2. A fixed charge density of 1×10^{11} cm^{-2} is derived from the slope of the line.

2.3 Network modification model for the metal oxide doped GeO_2

2.3.1 GeO_2 network and its modification by Y doping

The improvement on the thermal stability of Y-GeO_2 is qualitatively in agreement with thermodynamic expectation as discussed in section 2.1. On the other hand, the drastic change of water resistance is not expected by thermodynamics. Though both phenomena seem to be independent experimental observations, it is natural to think that both are originated from a same mechanism since they occur simultaneously on Y-GeO_2. Thus, in this section, I will try to establish a model which might explain the change of the material properties of Y-GeO_2 consistently.

Firstly, a fundamental discussion on the microscopic structure of GeO_2 is needed to clarify the unstable nature of GeO_2 and the prominent effect of Y doping. Stoichiometric amorphous GeO_2 has a similar local structure as amorphous SiO_2 as schematically shown in **Figure 2.15**,[21] featuring Ge-O_4 tetrahedral as the basic units of amorphous network. The Ge-O_4 tetrahedral unit shares a cornered oxygen atom with another unit, and each oxygen atom is thus bonded to two Ge atoms.

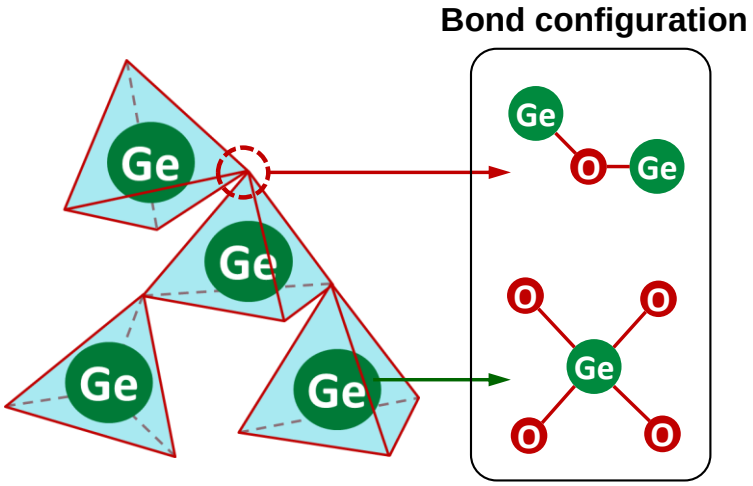


Figure 2.15 Schematics of amorphous GeO_2 structure. The bond configurations of Ge and O atoms are also shown (2-dimensional represent).

Let's consider what happens during the GeO desorption from GeO_2/Ge stack and GeO_2 etching by water. For GeO desorption, it can be considered that the following reaction occurs,

$$GeO_2+Ge=2GeO \quad (2.3)$$

Note that on the left side of this equation are two solids, while on the right side is a molecular in the ambient. It means that the solid material is dissociated into independent species with all the bonds connecting them broken. It is natural to expect that the energy barrier for this equation is related to both single bond energy and bond number.

Similarly, the water etching of GeO_2 might be written as the following equation,

$$GeO_2+2H_2O=Ge(OH)_4 \quad (2.4)$$

Again, the solid material on the left side (GeO_2) of the equation is dissociated into the separated species ($Ge(OH)_4$) in a water solution. An energy barrier of the reaction can also be considered here as a function of single bond energy and bond number.

To obtain a quantitative impression on how hard it is to dissociate GeO_2 through the above reaction 2.3 and 2.4, a new concept, the network rigidity, is created here by considering the average coordination number (N_{av}) and a pre-factor γ.

$$Network\ rigidity = N_{av} \times \gamma \tag{2.5}$$

N_{av} can be derived from the total number of coordination and number of atoms in a network. For GeO_2, the N_{av} value is 2.67, which is the same as that of SiO_2.[22] Note that the N_{av} value is obtained by dividing total number of coordination in a network with the number of atoms.[22] On the other hand, the pre-factor γ represents the strength and the constraint of a single coordination. Here we set the γ value to be 1 for SiO_2. According to the first-principles calculation on glass forming system,[23] the Ge-O bonding strength is much weaker (2.82 eV) than that of Si-O (3.48 eV) in spite of their similar structures, which means that it is easier to deform or dissociate a Ge-O bond than Si-O. Therefore, the γ value is smaller than 1 for GeO_2. It should be noted that the rigidity is a purely topological concept and the introduction of γ enables the use of this concept for dielectric properties discussions.

The energy consumption in dissociation of GeO_2 network should be proportional to the rigidity of the network. Thus, the dissociation rate of a network (either by thermal desorption or water etching) should be dependent on the total network rigidity as follows,

$$Dissociation\ rate \propto Exp[-\alpha (N_{av} \times \gamma)/kT] \tag{2.6}$$

Note that, since rigidity is a dimensionless value, a constant α with eV unit is included here (the value of α varies with different reactions). Thus, we established the relationship between the unstable properties of GeO_2 with that of its network topology information.

GeO_2 network is highly flexible. A flexible oxide might favor the Ge interface passivation,[11] but it also results in the unstable thermal and chemical properties. What is accomplished here by Y-GeO_2 is that, it enhances the rigidity of the network in a well-controlled manner to improve the thermal and chemical stability, while not too rigid to form a bad Ge interface. Let's investigate in detail on the role of Y in the Ge network.

Y doping is expected to change the microscopic structure of GeO_2 according to the modified random network (MRN) model as schematically shown in **Figure 2.16**.[24] Y-doping exists in the form of the Y^{3+} cation in the GeO_2 network, bonded to the nearest oxygen atoms according to MRN model. The Y-O bonding number is determined by the ratio of the Y^{3+} cation radii to the O^{2-} anion radii.[25] With a large Y^{3+} radii of 0.9 Å,[26] Y forms up to 7 bonds with the nearby oxygen atoms in GeO_2-Y_2O_3 ternary oxides, which has been confirmed by the observations on $Y_2Ge_2O_7$ and Y_2GeO_5.[27, 28] The coordination number of oxygen are increased simultaneously. Thus, the total N_{av} of the Y-GeO_2 network is necessarily increased to about 3 in 10% Y-GeO_2 by the introduction of Y-O bonds.

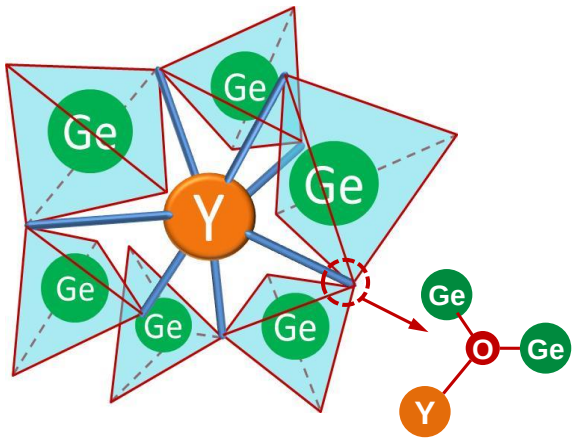


Figure 2.16 Schematics of MRN structure of Y-GeO_2. Due to the large amount of additional Y-O bond, some O atoms increase their coordination to 3 as well.

To quantitatively discuss the rigidity of the GeO_2 based oxide, a γ value of 0.8 is assumed for simplicity (the Ge-O single bond is 0.8 times the strength of Si-O single

bond[23]). The network rigidity of 10% Y-GeO_2 is derived by equation (2.5) by assuming a same value of γ with GeO_2 as shown in **Figure 2.17**. It is understandable that increasing the N_{av} value has a similar impact on the network rigidity with stronger single bond. Therefore, the higher N_{av} is expected to strengthen the Y-GeO_2 network significantly, thereby enhance the thermal stability, water resistance and electrical properties.[29]

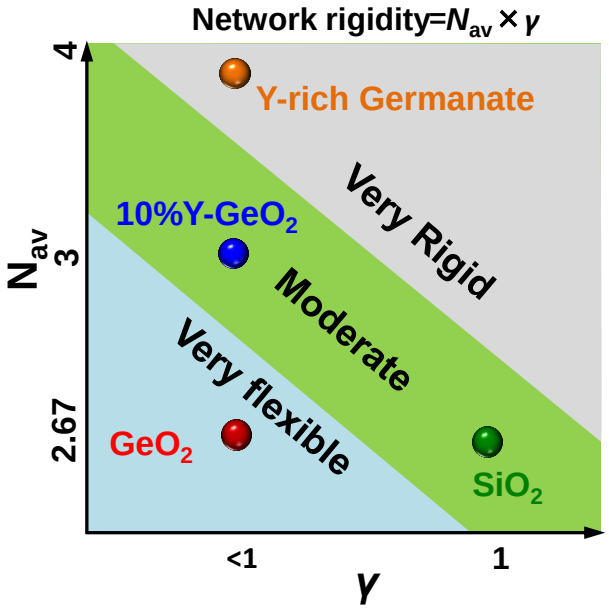


Figure 2.17 Network rigidity as a function of N_{av} estimated from the structures of Y-GeO_2 and GeO_2.[29] The better rigidity of Y-GeO_2 than the flexible GeO_2 network results in its both better thermal stability and water resistance. Note that the γ value is assumed to be 0.8 here for all the GeO_2 based oxides (γ=1 for SiO_2).

The network modification effect is experimentally observable from optical characterization of the thin films. Since the introduction of Y-O bond into the GeO_2 network is expected to change the bond configuration of GeO_2 according to MRN model, the bond vibrations should be changed as well. **Figure 2.18** shows the Fourier transform infrared spectroscopy (FTIR) absorbance spectra of GeO_2 and Y-GeO_2.[14] The peak corresponding to GeO_2 asymmetric stretching mode shifts to a lower energy and becomes

broadened. Two possible reasons for the peak shift of FTIR spectra can be considered. One is the decrease of Ge-O-Ge bond angle and the other is the increase of Ge-O bond length.

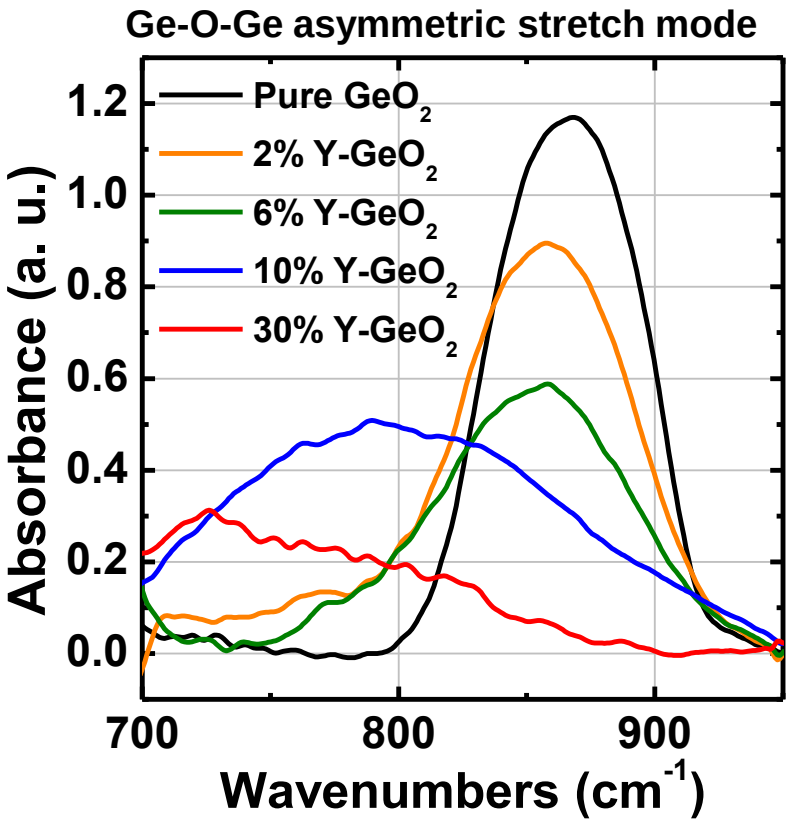


Figure 2.18 FTIR absorbance spectra of pure GeO_2 and Y-GeO_2.[14] The peak shift of asymmetric stretching mode in GeO_2 to lower energy is clearly observed with the increase of Y concentration. The thickness of the dielectrics are 40 nm

The extended x-ray absorption fine structure (EXAFS) measurement was also carried out to directly investigate the coordination configuration in the GeO_2 and Y-GeO_2 network. The estimated bond atom-atom distances in the GeO_2 and Y-GeO_2 network were derived by deconvolution of the spectra as shown in **Table 2.1**. It is noticed that the nearest Ge-O distance is enlarged by the Y incorporation, which supports the conclusion that GeO_2 network has been modified by the incorporation of Y atoms.

Table 2.1 atom-atom distances in the GeO_2 and Y-GeO_2 network measured by EXAFS

Material	Path	Distance (Å)
GeO_2	Ge-O	1.738±0.007
	Ge-Ge	3.163±0.023
Y-GeO_2	Ge-O	1.750±0.009
	Ge-Ge(Y)	3.178±0.054

Based on the Clausius-Mossoti (C-M) equation, the *k*-value of oxide is strongly related to both the ion species and the oxide structure as follows.[30]

$$k = \frac{1+8\pi(\alpha_m / V_m)/3}{1-4\pi(\alpha_m / V_m)/3} \tag{2.7}$$

Here, α_m and V_m are the molar polarizability and molar volume, respectively. For Y-GeO_2, the α_m is determined by the ion polarizability of Y^{3+}, Ge^{4+} and O^{2-} through the additive rule[30] and V_m is determined by the structure of Y-GeO_2. It is obvious from the C-M equation that a slightly denser packing of the structure can result in significant enhancement in *k*-value. The fact that Y-GeO_2 has a higher density than pure GeO_2 explains the increase of *k*-value demonstrated in figure 2.14(a).

In summary, the Y-O bond formation in the MRN network of Y-GeO_2 can reasonably explain both the rigidity enhancement of the network and the improvements in the thermal stability and water resistance.

2.3.2 Network modification effect of various metal cation species.

In the previous part of this section, we built up the MRN model to explain the eminent thermal and chemical stabilities of Y-GeO_2. However, Y does not stand alone on the thermodynamic diagrams (figure 2.3) as thermally stable oxides. In fact, several high-*k* metal oxides are possible candidate as doping materials in GeO_2 as well. The validity of MRN model is examined in various M-GeO_2/Ge stacks. After chemically cleaned by

methanol, HCl and diluted HF solution sequentially, M-GeO_2 was deposited on Ge substrate by radio frequency co-sputtering of GeO_2 and corresponding metal oxides targets. The M atomic percentage of all the samples in the following experiments was controlled to be (10±1)% in metallic atoms ratio (M per.=M/(Ge+M)) and confirmed by XPS.

The direct comparisons on the thermal stability and water resistance are good indications of the network rigidity of different M-GeO_2. **Fig. 2.19** shows the TDS peak temperature of GeO desorption from various M-GeO_2/Ge and pure GeO_2/Ge stacks.[12] The improvements of thermal stability are observable in all the M-GeO_2/Ge stacks. It is notable that the improvements of the thermal stability by different metal oxides doping, from lowest to highest, are in the order of Al_2O_3, HfO_2, Sc_2O_3, Y_2O_3 and La_2O_3.

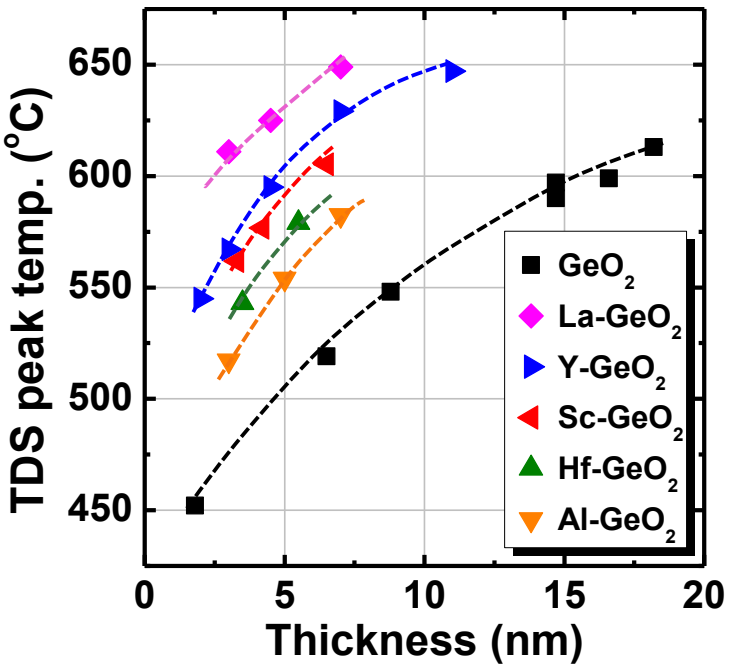


Figure 2.19 TDS peak temperature of GeO desorption as a function of initial M-GeO_2 and GeO_2 thickness.[12] The improvements of the thermal stability by different metal oxides doping, from lowest to highest, are in the order of Al_2O_3, HfO_2, Sc_2O_3, Y_2O_3 and La_2O_3.

To study the influence of different metal oxides doping on the GeO_2 in terms of water resistance, M-GeO_2/Ge and pure GeO_2/Ge stacks were immersed into 100% pure DIW and their thicknesses as a function of immersion time was measured by XPS as shown in

Figure 2.20.[12] GeO_2 is immediately dissolved in DIW while the etching rate of M-GeO_2 is drastically reduced. The stronger water resistance of M-GeO_2 will be beneficial not only for the device fabrication process but also for the electrical properties of the gate stack. Coincidently, the improvements of water resistance of M-GeO_2 among different doping species follows the same trend as their TDS peak temperature, which is, from weakest to strongest, Al_2O_3, HfO_2, Sc_2O_3, Y_2O_3 and La_2O_3.

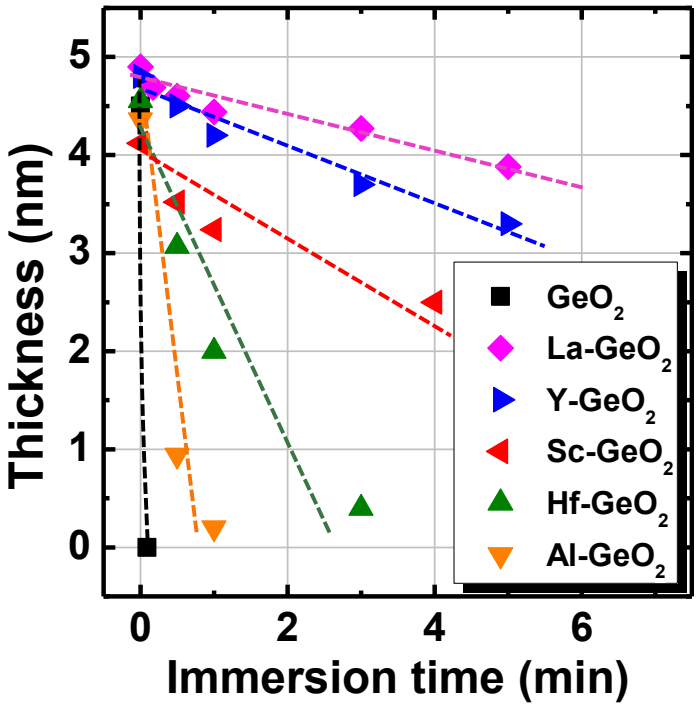


Figure 2.20 Thicknesses of M-GeO_2 and pure GeO_2 estimated from XPS as a function of immersion time in DIW.[12] The water resistance increase by different metal oxides doping, from weakest to strongest, is Al, Hf, Sc, Y and La.

The similar trends of thermal stability and water resistance improvements in different M-GeO_2/Ge stacks are also self-consistently explained by the MRN model discussed in the previous sections. The metal in doped metal oxides exist as M^{x+} (x is 3 or 4 for trivalent or tetravalent oxides, correspondingly) cation in the GeO_2 network and form M-O bond with the nearest O^{2-} anions, which should enhance the rigidity of the very flexible GeO_2 network as discussed in previous sections. The magnitude of this effect is therefore related

to the M-O bond number. **Figure 2.21** shows the expected M-O bonding number per M^{x+} cation as a fuction the M^{x+} cation radii according to literature reports.[25, 26, 31] Larger cations are prone to have higher M-O bonding number, therefore, exert stronger influence on the network of GeO_2, which leads to the higher thermal stability and stronger water resistance.

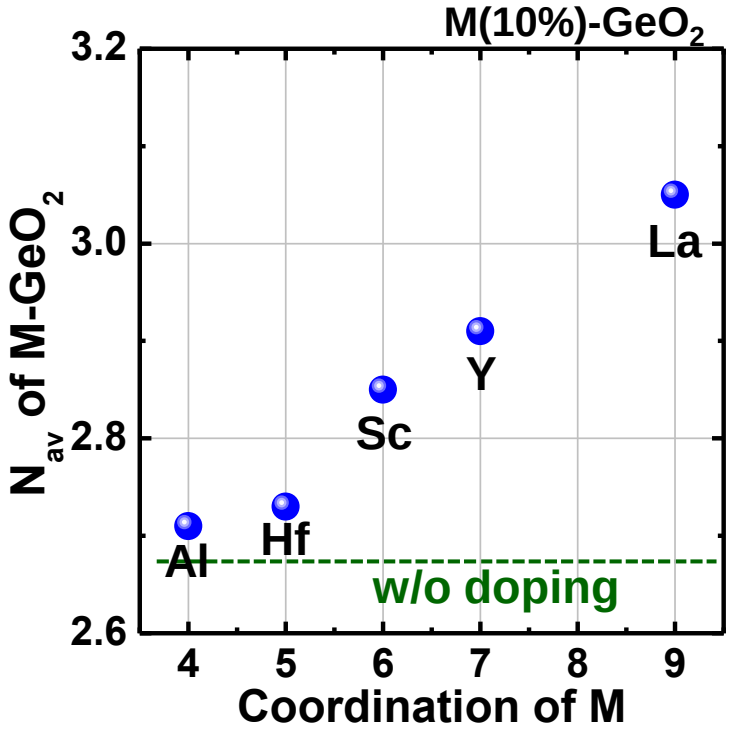


Figure 2.21 Expected coordination numbers of M cation in GeO_2 network and the corresponding N_{av} of the total network.[25, 26, 31] Note that the M percentage here is controlled to be 10% for all the M-GeO_2

A quantitative analysis on the material stabilities of various M-GeO_2 were carried out by applying the equation 2.6 on the detailed GeO desorption and water etching process for further understanding on the MRN model. According to equation 2.6, the relationship between GeO desorption peak temperature and N_{av} can be can be written as follows,

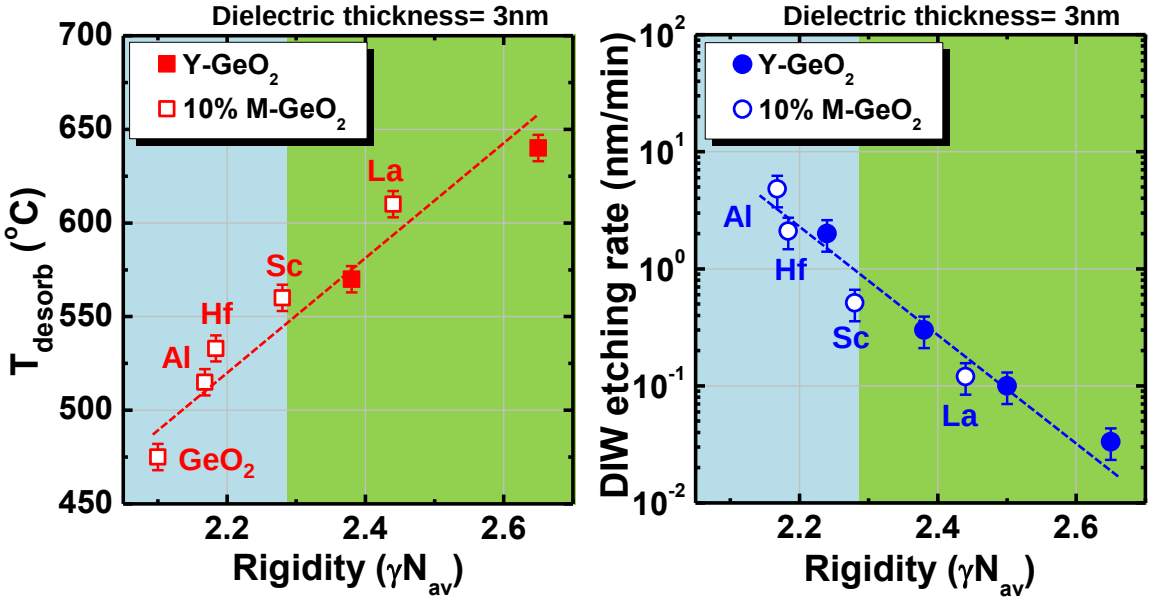
$$R_{TDS,peak} \propto Exp[-\alpha_{desorb}(N_{av} x_Y)/kT_{peak}] \quad (2.8)$$

Here, the $R_{TDS,peak}$ and T_{peak} are the peak desorption rate and desorption temperature, respectively. Since the $R_{TDS,peak}$ is almost invariant among all the M-GeO_2/Ge stacks with

same thickness of M-GeO_2 or GeO_2 (data not shown), the T_{peak} should be proportional to N_{av}. On the other hand, the water etching of GeO_2 occurs under the room temperature (T_0). Thus the etching rate $R_{etching}$ should be exponentially dependent on the N_{av} as follows,

$$R_{etching} \propto Exp[-\alpha_{etching}(N_{av} \times \gamma)/kT_0] \quad (2.9)$$

Figure 2.22 summarizes the T_{peak} and $R_{etching}$ as a function of N_{av}. The experimental data on T_{peak} and $R_{etching}$ fit the aforementioned relations with reasonable deviation, which further support the network rigidity criteria offered in the MRN model.



(a) **(b)**

Figure 2.22 (a) T_{peak} and **(b)** $R_{etching}$ as a function of N_{av}. Note that the T_{peak} are from the M-GeO_2/Ge and GeO_2/Ge stack with the same thickness (3 nm). Here, **γ** is assumed to be 0.8 for all the materials in the figure.

Finally, the various metal cations' modifying effect is also confirmed by the FTIR measurement as shown in **Figure 2.23**.[12] The FTIR peak corresponding to GeO_2 asymmetric stretching mode shifts to a lower energy and becomes broadened for all the M-GeO_2. The magnitudes of FTIR peak shift are in agreement with the enhancements of

material properties in the corresponding M-GeO_2/Ge stacks. It further supports the MRN model for various M-GeO_2.

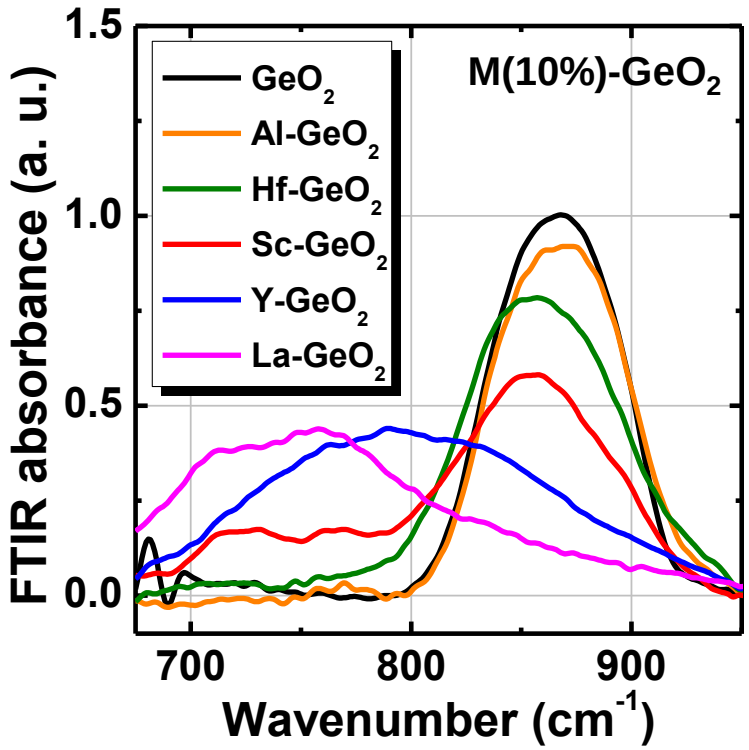


Figure 2.23 FTIR absorbance spectra of M-GeO_2 and pure GeO_2.[12] The peak shift of asymmetric stretching mode in GeO_2 to lower energy is clearly observed. The magnitude of this peak shift in different M-GeO_2 is an indication of how strongly the GeO_2 network is modified.

2.4 Concerns: interface defect bond and bulk immiscibility

2.4.1 Defect bond configuration between modifier and Ge

Since the electrical properties of M-GeO_2/Ge stacks are firmly related to the improvement of thermal stability and water resistance, it might be expected from previous result that a lower D_{it} is obtainable in M-GeO_2/Ge stacks. **Figure 2.24** shows the bi-directional *C-V* curves of the pure GeO_2/Ge and M-GeO_2/Ge stacks measured at room temperature.[12] It is notable that, at a given physical thickness of gate dielectrics, the maximum capacitance varies substantially among these gate stacks, which indicates that

the dielectric constant is changed significantly by doping. The change of dielectric constant is also partly understandable from the GeO_2 network modification and packing density change by doping as discussed in previous section. Al, Sc and Y doping improve the interface properties of the M-GeO_2/Ge gate stack featuring the negligible hysteresis and frequency dispersion in the *C-V* curves, which is in agreement with the expectation from thermal stability improvement. On the other hand, *C-V* curves of Hf-GeO_2/Ge and La-GeO_2/Ge stacks exhibit considerable hysteresis. It indicates that electrical properties of M-GeO_2/Ge stack are not simply determined by the thermal stability and water resistance.

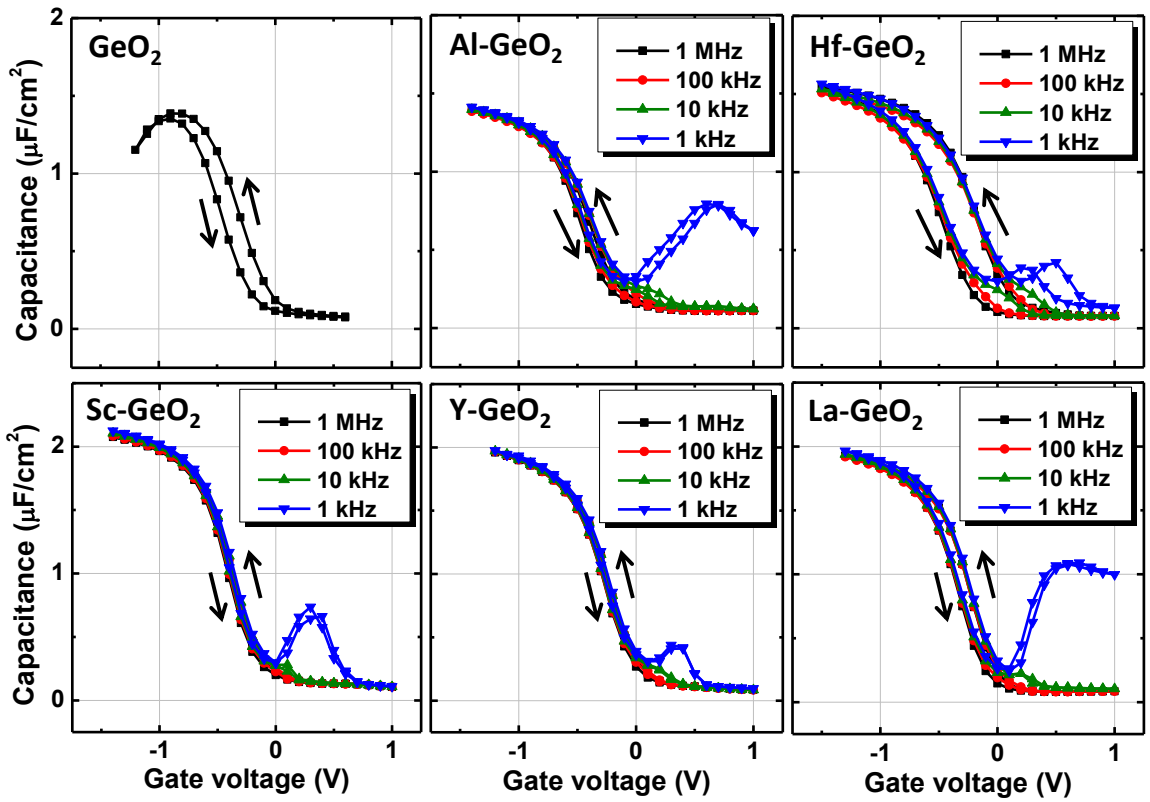


Figure 2.24 Bidirectional *C-V* curves of Au/GeO_2/Ge and Au/M-GeO_2/Ge MOSCAPs measured at RT: **(a)** GeO_2, **(b)** Al-GeO_2, **(c)** Hf-GeO_2, **(d)** Sc-GeO_2, **(e)** Y-GeO_2, **(f)** La-GeO_2.[12] Note that the thicknesses of the dielectrics are about 3 nm in these gate stacks.

To quantitatively estimate the D_{it} spectra of M-GeO_2/Ge stacks, low temperature conductance method was carried out at 100 to 250 K on both n-Ge and p-Ge substrates.

Figure 2.25 shows the energy distribution of D_{it} in M-GeO_2/Ge stacks derived from low temperature conductance method (closed symbols) and high-low-frequency capacitance method (open symbols).[12] It is notable that Y-GeO_2 and Sc-GeO_2 yield low D_{it} about 1×10^{11} $eV^{-1}cm^{-2}$ near the mid gap, which is close to the state-of-the-art low D_{it} at GeO_2/Ge interface prepared by high-press oxidation.[8] Hf-GeO_2/Ge stack, on contrary, has a significantly higher D_{it} (also the case for La-GeO_2).

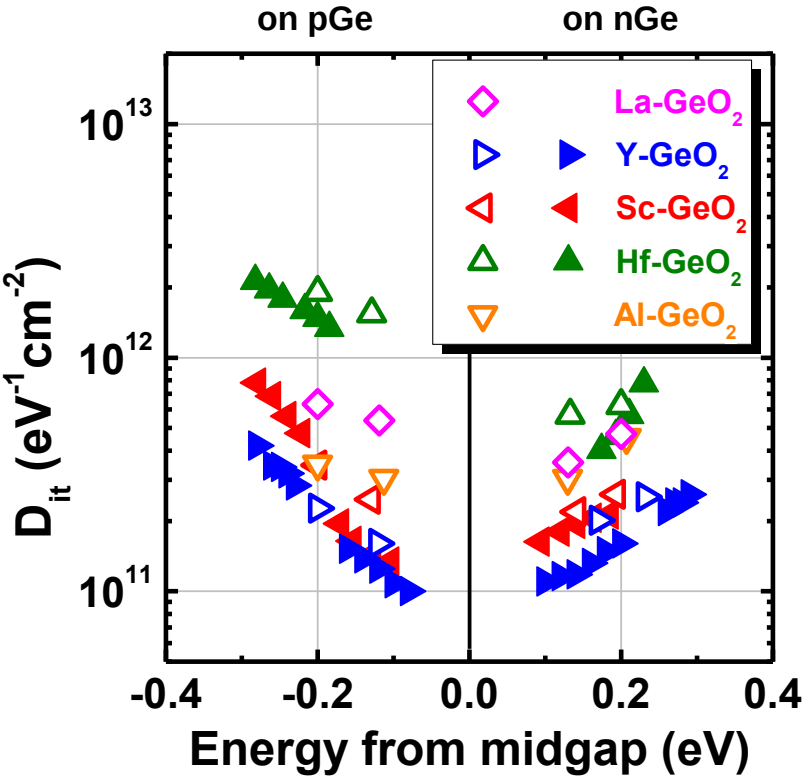


Figure 2.25 Energy distribution of D_{it} in M-GeO_2/p-Ge and n-Ge stacks derived from low temperature conductance method (closed symbols) and high-low-frequency capacitance method (open symbols).[12] It is notable that Y-GeO_2 and Sc-GeO_2 yield low D_{it} on Ge, which is close to the state-of-the-art low D_{it} at GeO_2/Ge interface prepared by high-press oxidation.[8] Hf-GeO_2/Ge stack, on contrary, has a significantly higher D_{it}, especially in the lower half of Ge band gap.

XPS measurements were carried out on the M-GeO_2/Ge stacks to identify this interface degradation mechanism observable for some M-GeO_2. As an example, the XPS results

from the Y-GeO_2/Ge (with good interface) and Hf-GeO_2/Ge stacks (with poor interface) are compared here. **Figure 2.26(a)** shows the Ge*3d* core level spectra from the Hf-GeO_2/Ge stacks with different thicknesses of the dielectrics.[12] The Ge*3d* spectrum of as-cleaned Ge substrate is also shown as a reference. The chemical shift of Hf-GeO_2 is about 3.1 eV with respect to Ge^{0+} peak, which is smaller than that of pure GeO_2 (about 3.5 eV). This smaller chemical shift of M-GeO_2 is originated from the second nearest-neighbor effect of M atoms through Ge-O-M bond configuration,[32] because of the stronger ionicity of M than that of Ge. **Figure 2.26(b)** shows Ge*3d* core level spectra from the Y-GeO_2/Ge stacks measured at the same condition for comparison. It is worth noting that Ge-Hf metallic bond is preferentially observable in Hf-GeO_2/Ge stack at a lower binding energy with respect to Ge^{0+} peak,[33,34] while no Ge-Y bond is found in Y-GeO_2/Ge stack. Regardless of different Hf-GeO_2 thickness, the XPS intensity of Ge-Hf metallic bond is almost same with respect to Ge^{0+} peak in all Hf-GeO_2/Ge stacks, which is a strong indication that the Ge-Hf metallic bond is locally distributed near the interface. The difference of bond configurations in the Y-GeO_2/Ge and Hf-GeO_2/Ge stacks is schematically shown in **Figure 2.26(c)**.[12] Y and Hf cations in the bulk network exist in the similar configuration as indicated in the MRN model. Although the interface is majorly passivated by GeO_2, introducing Hf near the interface results in Ge-Hf bond. Y doping, on contrary, is free from this concern. The degradation of Hf-GeO_2/Ge interface is attributable to the Hf-Ge bond, which is consistent with the first principle calculation.[31]

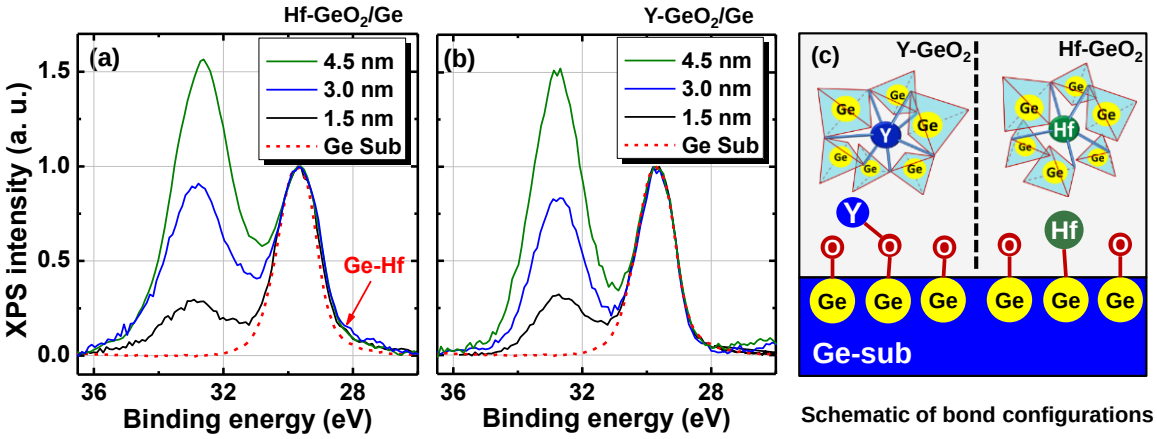


Figure 2.26 Ge3*d* core level spectra of **(a)** Hf-GeO_2/Ge and **(b)** Y-GeO_2/Ge measured by XPS,[12] Note that the spectrum of the as-cleaned Ge substrate is also shown in the dotted line for comparison. The Ge-Hf metallic bond is preferentially observed in Hf-GeO_2/Ge stack. **(c)** Schematic of the bond configurations in Y-GeO_2/Ge and Hf-GeO_2/Ge stacks.[12]

Thermodynamic considerations are required to understand the observation that M-Ge bond preferentially existed in Hf-GeO_2/Ge interface. By assuming that M-O or M-Ge single bond-strength is not changed from M_xO_y/Ge to M-GeO_2/Ge stacks,[35] the reason that Hf-Ge bond is energetically favorable are readily understood from thermodynamic calculations on M_xO_y/Ge interfacial reaction. The Y-Ge or Hf-Ge bond formation is related to the germanidation reaction at the interface. Within the accuracy of reference and thermodynamic database,[7, 35, 37] it is calculated as:

$$HfO_2 + 3Ge = HfGe_2 + GeO_2 \qquad \Delta G=-27 \text{ kcal/mol}, \qquad (2.10)$$

$$Y_2O_3 + 3.5Ge = 2YGe + 1.5GeO_2 \qquad \Delta G=152.8 \text{ kcal/mol}. \qquad (2.11)$$

Hf-Ge metallic bond is easier to form relating to the negative Gibbs free energy for germanidation, while the formation of Y-Ge bond is relatively hard from the thermodynamic viewpoint.

Similar Ge-La metallic bond can be experimentally observed in La-GeO_2/Ge stacks (data not shown), which explains the degradation in its *C-V* curves as well. However, it is

not likely for the La_2O_3 to react with Ge in the same way as equation 2.11 thermodynamically.[37] Instead, one possible reaction which might occur for La_2O_3 and Ge are written as follows,

$$La_2O_3+2Ge=1.14LaGe+0.43La_2Ge_2O_7 \quad (2.12)$$

Here, besides LaGe, the other product is a ternary alloy of La_2O_3 and GeO_2. Though there is no available thermodynamic data for this reaction, it is possible that the ternary alloy $La_2Ge_2O_7$ has a lower energy state than its binary compounds,[38] which offers a net energy gain for the reaction.

2.4.2 Defect bond configuration between network former and Ge

Besides the different M doping species, the interface properties of M-GeO_2/Ge stacks are also dependent on the percentage of doping experimentally. **Figure 2.27** shows the D_{it} at E_i-0.2 eV of Y-GeO_2/Ge stacks as a function Y percentage. Though small amount of Y doping can reduce D_{it} due to the suppression of GeO desorption (below 10%), it increases drastically with higher Y percentage. Since it has already been clarified in the previous sections that the existence of Y itself does not introduce the interface defect bond, such interface degradation with high Y percentage should be attributed to different mechanism instead of improper chemical bonds.

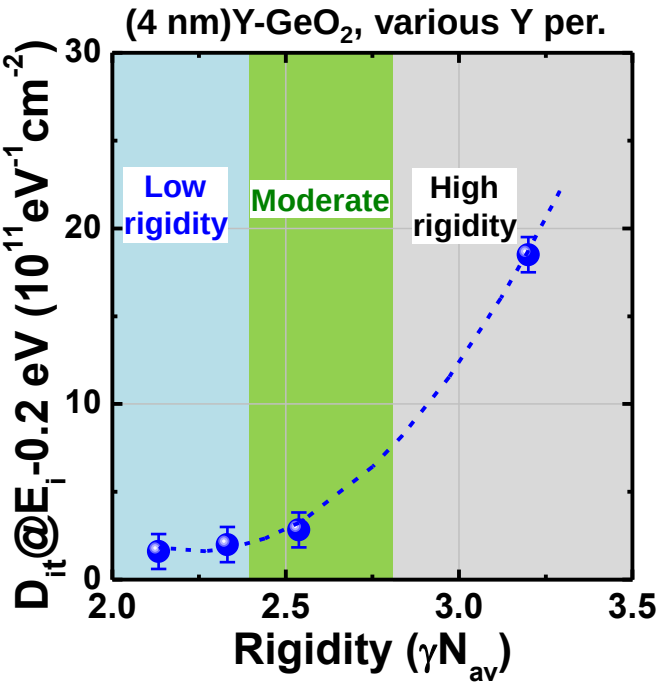


Figure 2.27 D_{it} at E_i-0.2 eV of Y-GeO_2/Ge stacks as a function Y percentage. Though small amount of Y doping is beneficial in terms of low D_{it}, it increases a lot with high Y percentage.

In fact, not all the chemically stable dielectrics can yield good interfaces on semiconductor. Silicon oxynitride (SiON) is a typical example of stable dielectric which have poor interface on Si.[39] The Ge interface degradation by high Y-percentage Y-GeO_2 might be attributable to a similar reason as SiON on Si, namely, the over-constraint of the oxide.[39] **Figure 2.28** schematically shows the degree of freedom and constrain in of atoms. The degree of freedom of each atom is 3, while the number constraint is dependent on the coordination between atoms (N_{av}, equally).[40] Too many coordination will result in a larger constraint number than the degree of freedom, which is called "over constraint".[39] Such an over constraint network will inevitably include some broken bond at the interface since not all the constraint can be satisfied by the arrangement of the atoms. The relationship between D_{it} and constraint has been summarized in the literatures as follows, [39]

$$D_{it} \propto (N_{av} - N_{av}^{*})^3 \quad (2.13)$$

Here, N_{av}* is the optimal average coordination number, which is below 3 for most dielectrics. In Y-GeO_2/Ge gate stacks, the N_{av} is larger than 3 when Y concentration is over 10%, which explains the observed D_{it} increment. From the constraint criteria, the low N_{av} value of 2.67 also explains why both GeO_2 and SiO_2 can offers sufficient passivation for Ge and Si. While, the unsatisfying interface properties in direct high-*k*/semiconductor interface are also explainable from much larger N_{av} value of the high-*k* oxides.

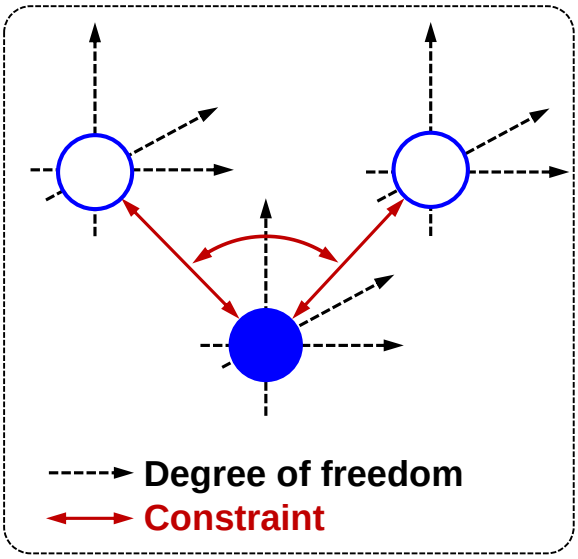
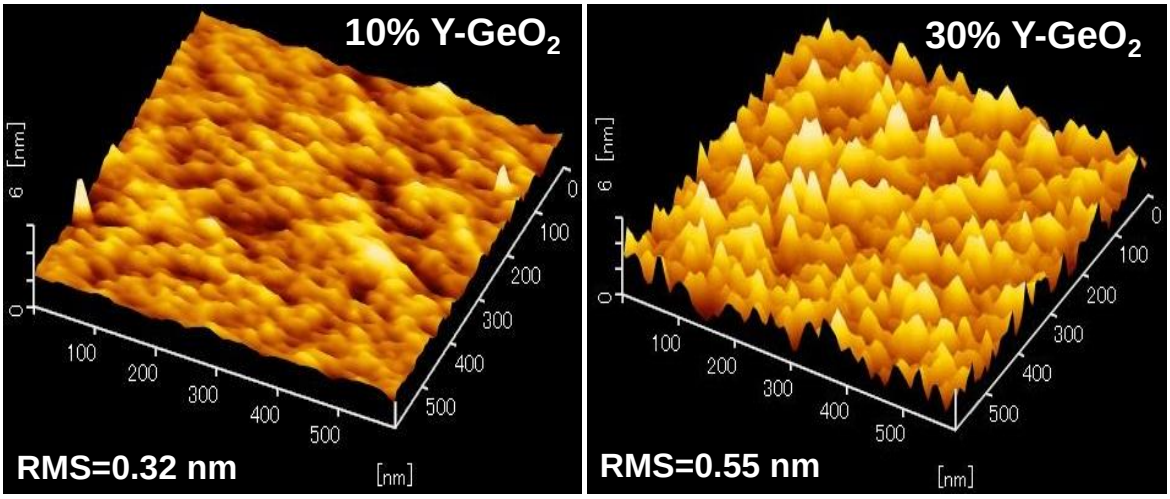


Figure 2.28 Schematics of the degree of freedom and constrain of atoms in a network. The degree of freedom is related to the number of atoms, while the number of constraint is determined by the number of the bond.

From the viewpoint of both interface bond and network constraint, it is not hard to understand the low D_{it} in 10% Y-GeO_2/Ge interface. Firstly, on the Y-GeO_2/Ge interface, the Y is bonded in a Y-O-Ge configuration to the Ge interface, which does not yield a gap states. Secondly, though the network rigidity of 10% Y-GeO_2 is higher than pure GeO_2, it is still flexible enough to avoid the over-constraint and dangling bond formation. Therefore, very low D_{it} is obtained in 10% Y-GeO_2/Ge.

2.4.3 Uniformity or immiscibility in bulk ternary oxides film

Besides the interface properties, it is found in the previous section 2.2.3 that the bulk electrical properties, especially J_G, are also dependent on the Y concentration (figure 2.13(b)). The J_G reduction by the small amount of Y doping is understandable from less V_O formation. On the other hand, the increase of J_G at high Y-percentage indicates that a different mechanism is dominating the J_G change. The water etching experiment reveals some hints on the reason for J_G increase at high-Y percentage. Y-GeO_2/Ge gate stacks with different Y concentrations are emerged in DIW and the AFM images are collected after water immersion as shown in **Figure 2.29(a) and (b)** for 4 nm 10% and 30%Y-GeO_2, respectively. It is found that 10%Y-GeO_2 is etched by DIW uniformly. While the surface of 30%Y-GeO_2 is roughened by DIW etching with some localized particles revealed, which indicates that the uniformity is degraded in 30%Y-GeO_2.



(a) **(b)**

Figure 2.29 AFM images of the top surface of **(a)** 10%Y-GeO_2 and **(b)** 30%Y-GeO_2 after 5 min immersion in DIW. The 10%Y-GeO_2 is uniformly etched by water, while 30%Y-GeO_2 shows some localized particles.

Such uniformity degradation under certain Y percentage can be explained in the ternary phase diagram of GeO_2-Y_2O_3 system, which is called immiscibility region as schematically shown in **Figure 2.30**.[41] The immiscibility region exists between pure GeO_2 and $Y_2Ge_2O_7$

on the phase diagram. When the GeO_2-Y_2O_3 ratio is located inside the immiscibility region, they cannot form a uniform material. Instead, phase separation would occur, which results into the Y-poor part and Y-rich parts in the oxide. Under the DIW etching, the etch rate of this two segregations are different. Therefore the surface is roughened by the DIW etching for 30% Y-GeO_2. The uniformity degradation also introduces an additional leakage path through the segregation boundaries, which might explain the increase of J_G for 30% Y-GeO_2 as shown in figure 2.13(b).

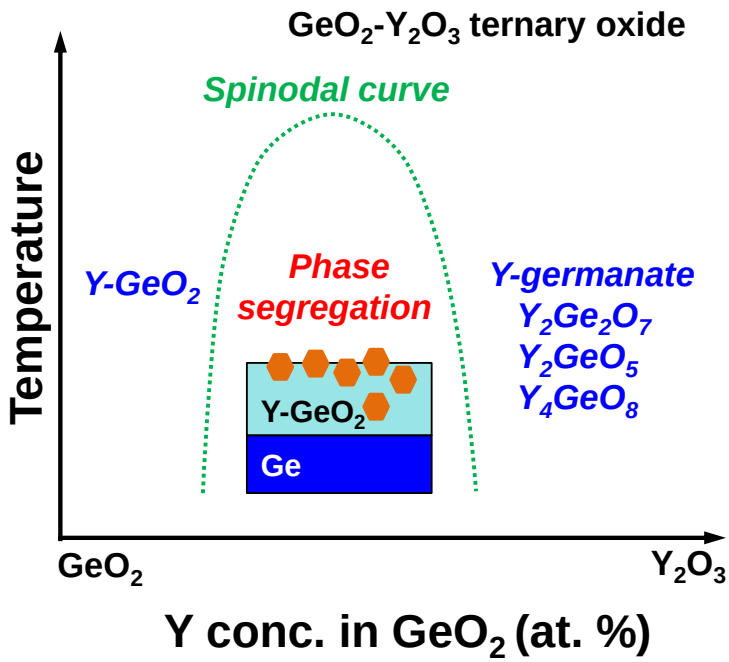


Figure 2.30 Phase diagram of GeO_2-Y_2O_3 ternary oxide.[41] Mainly three regions exist in the diagram, namely, Y-GeO_2, Y-rich germanate and phase segregation region.

2.5 Summary

In summary, inspired by thermodynamics in metal oxide formation, a new approach is proposed to enhance the thermal and chemical stability of GeO_2/Ge gate stacks by metal oxide doping. Y-GeO_2 provided both stronger water resistance and better thermal stability than pure GeO_2. Those are well understandable from a network modification viewpoint that the oxygen is more strongly bonded to the Ge and Y atoms, and thereby increase the

N_{av} in Y-GeO_2 network. Superior interface properties with low interface state density was also achieved in Y-GeO_2/Ge gate stack together with an enhancement of the *k*-value.

A systemic investigation has also been carried out on the network modification effect of various M-GeO_2 and M concentrations. It is found that a desirable M doping species should satisfy two semi-empirical criteria. Firstly, metal cations with larger ionic radii are more preferable for their stronger influence on the GeO_2 network, which result in the higher thermal stability and water resistance. Secondly, metal oxides are necessarily to be unreactive with Ge to prevent the Ge-M metallic bond formation. Combining the knowledge of this work and the literatures, transition metal cations can be categorized according to the two semi-empirical criteria as schematically shown in **Figure 2.31**. Firstly, under a certain PDA condition, larger or tetravalent cations are more reactive with Ge substrate than smaller or trivalent ones, which form the Ge-M metallic bond and result in the degradation of interface properties. Therefore, Al, Sc and Y doping survive Zr, Hf, La and some of the Lanthanide Rare-earth (Ln RE) due to less reactivity with Ge substrate and better interface properties of M-GeO_2/Ge stacks. Secondly, among unreactive cations, relatively large ones are more preferable due to a higher thermal stability offered by the network modification effect. Concerning the doping concentration, it is understood that a small amount of cation is the key to both material stability and good electrical properties. Higher M doping concentration would result in degradation of interface and bulk electrical properties due to over constraint and immiscibility, respectively.

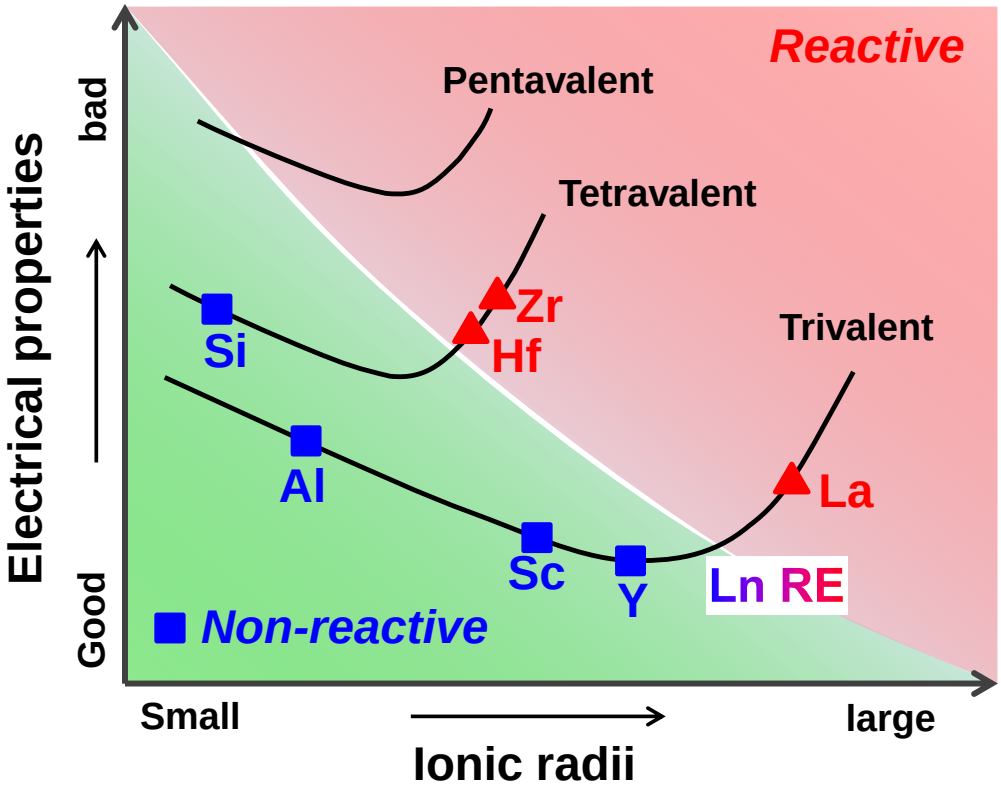


Figure 2.31. Schematic of two semi-empirical criteria for the interface properties in different M-GeO_2/Ge stack. The doping species that are reactive with Ge substrate are in the red region and the unreactive ones are in the blue region. Note that part of the Ln RE cations are reactive with Ge.

Thermally robust gate stack with deep sun-nm EOT can be expected by using suitable M-GeO_2 as an interfacial layer on Ge.

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Chapter 3

Selection of interface aware high-*k* dielectrics

3.1 Concerns on the high-*k* selection in Ge gate stack

3.2 Alternative ternary high-*k*: $YScO_3$

3.3 Demonstration of 0.5 nm EOT Ge gate stack

Overview

In the previous chapter, the formation of a thermally robust IL has been investigated. Improvement of thermal stability and hygroscopic tolarence of GeO_2/Ge interface was also demonstrated by Yttrium-doped-GeO_2 (Y-GeO_2) without any cost of interface properties. Therefore, GeO_2-based dielectrics, especially Y-GeO_2, are feasible interfacial layer (IL) between Ge and high-permittivity (*k*) dielectrics. However, with aggressive scaling of equavalent oxide thickness (EOT), the interface properties of Ge gate stacks become also highly sensitive to the top high-*k* dielectrics because the high-*k* dielectrics are readily intermixed with the ultra-thin GeO_2-based IL.[1, 2] Therefore, proper high-*k* dielectrics are needed for the deep sub-nm EOT Ge gate stack formation.

In this chapter, the interaction between the different top high-*k* dielectric and Ge interface is investigated in terms of intermixing and defect formation. Alternative high-*k* dielectric thin film yttrium scandate ($YScO_3$) is proposed for Ge gate stack formation. Significant enhancement of *k*-value was observed in $YScO_3$ comparing to both of its binary compounds, Y_2O_3 and Sc_2O_3, without any cost of interface properties. It suggests a feasible approach to design the promising high-*k* dielectrics for Ge gate stack, namely the formation of high-*k* ternary oxide out of two medium-*k* binary oxides. Aggressive scaling of equivalent oxide thickness (EOT) with promising interface properties is presented by using $YScO_3$ as high-*k* dielectric and yttrium-doped GeO_2 (Y-GeO_2) as interfacial layer, for a realistic demonstration of high-*k* gate stack on Ge. In addition, Ge n-MOSFET performance showing peak electron mobility over 1000 cm^2/Vsec in sub-nm EOT region was also demonstrated by $YScO_3$/Y-GeO_2/Ge gate stack.

3.1 Concerns on the high-*k* selection in Ge gate stack

3.1.1 Advantages and general requirements on the high-*k*.

The scaling of equivalent oxide thickness (EOT) is one important aspect of device scaling.[3-6] Thinner EOT can offer stronger control of the vertical electric field in the channel by the gate voltage (V_G), thereby improve the device properties. In detail, the drain current (I_d) in a MOSFET is directly dependent on the oxide capacitance (C_{ox}=ε_0/EOT) as follows,[7]

$$\text{In the linear region: } I_d = \frac{W}{L}\mu_{eff}C_{ox}(V_G - V_{th})V_d \quad \text{for } V_d \ll (V_G - V_{th}) \qquad (3.1)$$

$$\text{In the saturated region: } I_d = \frac{W}{2ML}\mu_{eff}C_{ox}(V_G - V_{th})^2 \qquad (3.2)$$

where W and L are the width and length of the channel. μ_{eff} and V_{th} are the effective mobility of the carriers and the threshold voltage. M is a function of doping concentrations. It is obvious that a higher C_{ox} (thinner EOT, equally) can result in larger I_d under a given gate voltage (V_G). Moreover, the short channel properties are also improved by thinner EOT thanks to the stronger electric control of the channel region.[6]

The insufficient *k*-value of GeO_2 (5.2-5.9) and Y-GeO_2 (8-10) makes it impossible for the sub-nm EOT gate stack formation using only GeO_2 or Y-GeO_2 as gate dielectric. A higher-*k* dielectric layer is needed above the GeO_2 or Y-GeO_2 interfacial layer (IL). There are several requirements on the material and electrical properties of the high-*k* dielectrics for Ge MOS devices as schematically shown in **Figure 3.1**. Namely, (1) the high-k dielectric should be uniform and armorphous to suppress the gate leakage current (J_G) since the it is deposited; (2) the oxide should have a high *k*-value and a sufficient band gap (E_g); (3) since the I_d is also directly dependent on the μ_{eff}, the introduction of the high-*k* should not be at the cost of interface properties. Without ensuring the above three requirements, there would be no meaning for improving the C_{ox} by high-*k* dielectrics.

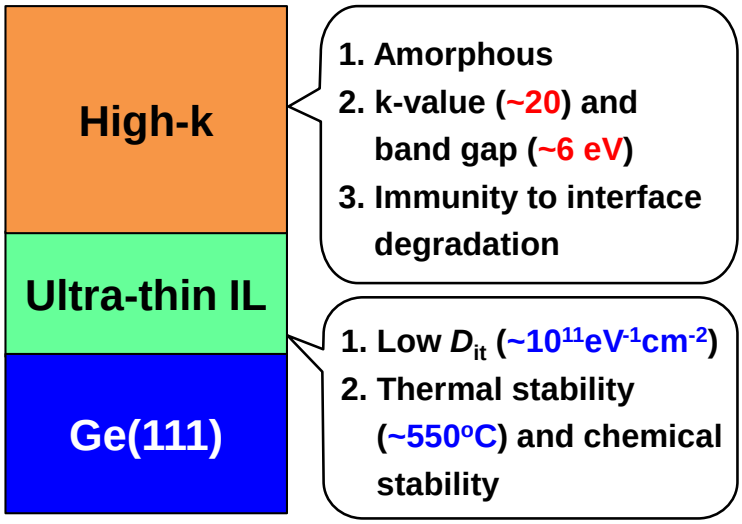


Figure 3.1 Schematic of basic Ge gate stacks structure for EOT scaling into sub-nm region. The requirements on the ultra-thin IL and high-*k* are listed with regard to both IL and high-*k*. The issue for the IL has been addressed in the chapter 2.

Though (1) and (2) are requirements simply on the properties of the dielectrics, (3) involve a complicated relationship between high-*k*, IL and semiconductor. Therefore I would like to spend more time on requirement (3) for a detail explanation.

It has been systematically investigated on the Si gate stacks that the interface awareness of the high-*k* is strongly related to the thermodynamics between the high-*k* dielectric and Si substrate.[8] Those chemically stable dielectrics are preferable for the interface aware high-*k* formation on Si. The chemical stabilities of dielectric/Si are considered in the following three reactions thermodynamically for the selection citeteria.[8]

$$Si+MO_x \rightarrow M+SiO_2 \quad (3.3)$$

$$Si+MO_x \rightarrow MSi_z+SiO_2 \quad (3.4)$$

$$M+SiO_2 \rightarrow MO_x+MSi_y \quad (3.5)$$

According to the Gibbs free energy (ΔG) of the three reactions, the high-*k* metal oxide can be catergoried in the following manner (**Figure 3.2**) for their stability on Si.[8] Note that in the bottom triangular phase diagrams, the conneted lines between two materials indicate

that the two materials are chemically stable with contact to each other. On the other hand, the reaction should occur for the two materials without a connecting line. It can be found that only the first configuration (left) can yield stable MO_x on Si, with ΔG of both reaction 3.3 and 3.4 being positve.

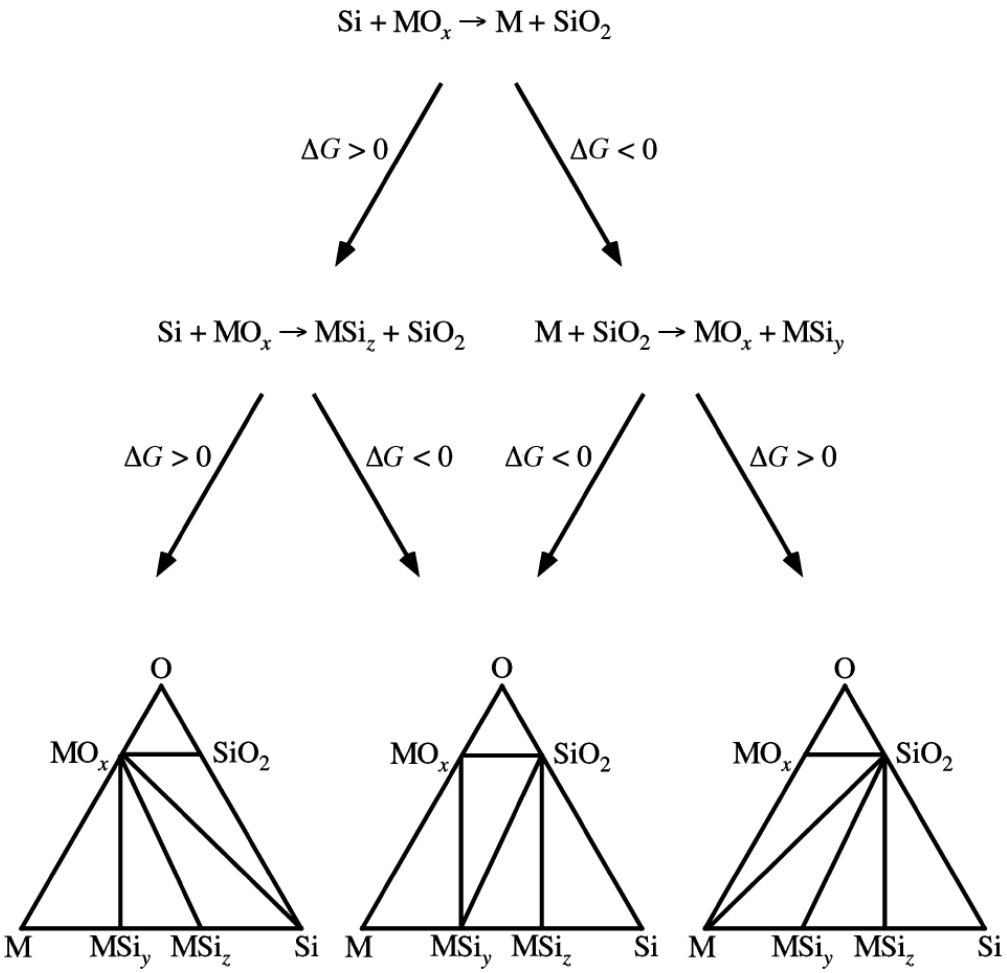


Figure 3.2 Flowchart for the selection of thermally stable metal oxides on Si.[8] In the triangular diagram, a solid line is plotted between every two materials which are not reactive with each other.

Similarly criteria can be used for identying chemically stable high-*k* oxide for Ge gate stacks. According to the literatures[9-11] and the discussions in the chapter 2, some conventional high-*k* oxides like HfO_2 becomes nolonger suitable for Ge gate stack formation since it increases the interface states density (D_{it}). In fact, the aforementioned

thermodynamic criteria (requirements 3) leave us a limited amount of "Ge friendly" cation species, namely, Al, Sc, Y, and some of lathanide rare-earth (Ln RE) (figure 2.31).

3.1.2 Intermixing behavior between high-*k* and GeO_2 IL

One might ask here that how strongly can the high-*k* dielectric influence the interface properties. In another word, when will the the interface properties becomes sensitive to the high-*k* dielectrics. If 0.5 nm of GeO_2-based IL can block any influence of high-*k* dielectrics on the interface with required annealing condition, then the discussion on the interface aware high-*k* would be meaningless.

So, here before the discussion on the interfacce aware high-*k* dielectric selection, I would like to clarify one important issue first: the intermixing between GeO_2 IL and the high-*k*, because it determines how strongly the high-*k* dielectric can influence the interface and how thin we can use for the IL. It has been reported qualitatively that, comparing to SiO_2, GeO_2 IL is weaker oxides in terms of blocking the cation diffusion from top high-*k* to the interface,[1, 2] which make the Ge interface more senstive to the high-*k* than the Si counterpart.

In this section, using Y_2O_3 as an example, the intermixing between the high-*k* and GeO_2 are invesitgated quantitatively, to clarify how signifiantly the high-*k* can influcence the interface. **Figure 3.3** shows the experimental design for this observation. GeO_2/Y_2O_3/Ge stacks (note that Y_2O_3 is at the bottom and GeO_2 is on the top) are deposited by sputtering and annealed in different PDA temparature to form an intermixing layer between GeO_2 and Y_2O_3 (the product is Y-GeO_2). After that, the gate stacks are immersed in diluted deionized water (DIW) (Methanol/DIW=20/1). Since only pure GeO_2 is etched by diluted DIW, the intermixing player Y-GeO_2 are remained and measurable by XPS.

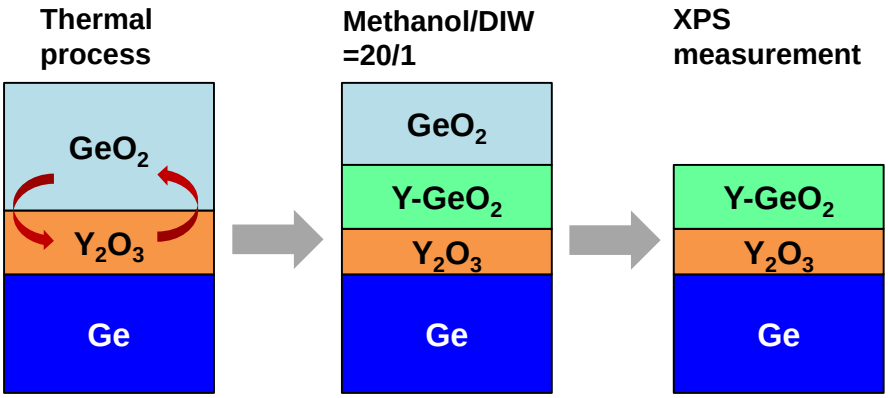
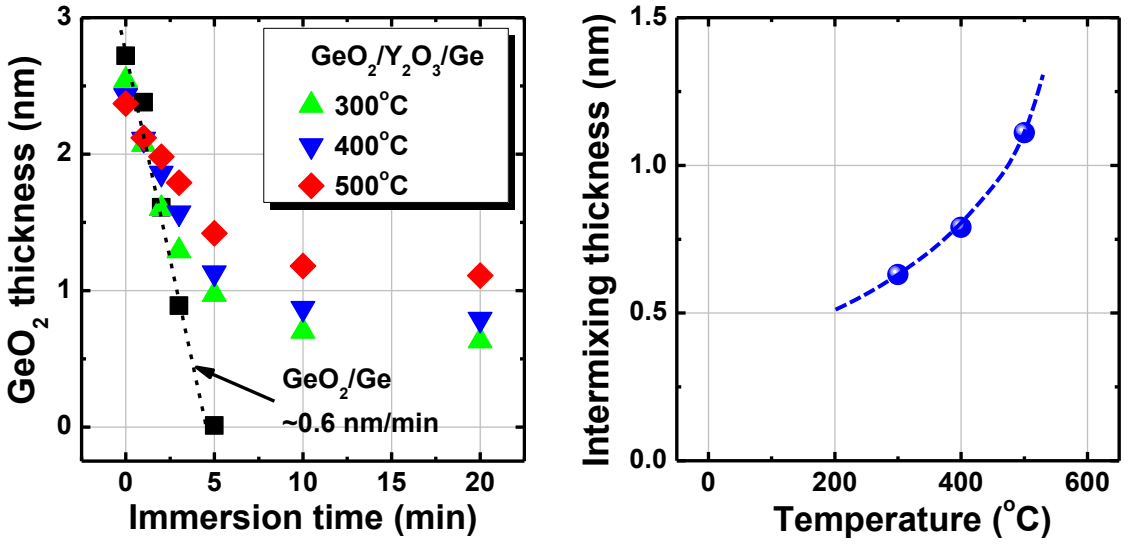


Figure 3.3 Experimal procedures to esitmate the intermixing thickness at the GeO_2/Y_2O_3 interface. The critial point here is the different DIW etching rate between the intermixed layer and pure GeO_2.

Figure 3.4(a) shows the thickness of the GeO_2 or Y-GeO_2 estimated from the XPS as a funtion of immersion time. As expected, pure GeO_2/Ge stack is completely etched in the diluted DIW, with an etching rate similar to the literature.[12] While, with the intermixing of Y_2O_3, the GeO_2 can not be completely etched, which is attributable to the Y-GeO_2 formtion by the Y_2O_3/GeO_2 intermixng. The thickness of the intermixing layer was extracted after 20 min immersion and plotted in **Figure 3.4(b)** as a funtion of annealing temperature. Over 1 nm of intermixing layer can be found in the stack after 500^{o}C annealing, which indicates that the intermixing between Y_2O_3/GeO_2 is much easier than the Y_2O_3/SiO_2 conterpart.[13] It should be noted that the thickness of intermixing is whitin the common thickness scale of an IL for sub-nm EOT gate stack (1 nm GeO_2 or Y-GeO_2 contibutes 0.7 or 0.5 nm EOT, respectively).



(a) **(b)**

Figure 3.4(a) GeO_2 thickness in $GeO_2/Y_2O_3/Ge$ stacks as a funtion of immersion time in diluted DIW. The results from a GeO_2/Ge stack is also shown as a reference. The remained GeO_2 layer after long time DIW etching is attributable to the intermixing between GeO_2 and Y_2O_3 (Y-GeO_2), which is not soluble in water. **(b)** The intermixing layer at GeO_2/Y_2O_3 interface as a funtion of annealing temperature.

It is found that, besides Y_2O_3, many high-*k* oxides share the similar intermixing property with contact to GeO_2. For the sub-nm EOT Ge gate stack with ultra-thin IL (about or below 1 nm), the high-*k* species can reach the interface easily, influencing the electrical properties. Therefore, for some high-*k* like HfO_2, even though an IL is prepared before HfO_2 depostion, Hf might still penatrate the IL and degrade the interface. **Figure 3.5** shows the bidirection *C-V* curves of HfO_2/Y-GeO_2/Ge gate stacks measured at room temperatrue (RT) with different Y-GeO_2 IL thickness. It is found that thick Y-GeO_2 IL ensures decent *C-V* curves, while reducing the Y-GeO_2 IL below 1 nm results in obvious degradation of the *C-V* curve. Such a interface degradation is not due to the Y-GeO_2 IL, because the results is even worse with 1 nm pure GeO_2 IL (also shown in **figure 3.5**).

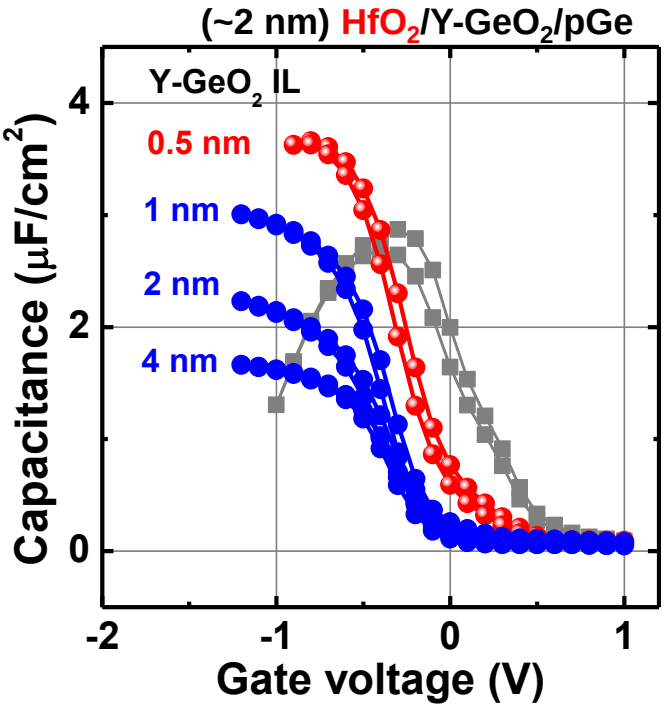


Figure 3.5 Bidirectional *C*-*V* curves of HfO_2/Y-GeO_2/Ge stacks with various Y-GeO_2 IL thicknesses measured at RT. It is notable that decent *C*-*V* curves are kept with Y-GeO_2 thickness over 1 nm, while thinner Y-GeO_2 thickness (below 1 nm) results in the degradation of the *C*-*V* curve. The HfO_2/(1 nm) GeO_2/Ge stack also shows poor electrical properties.

Thus, it can be concluded that the defect forming high-*k* dielectrics like HfO_2 can not be used directly on ultra-thin IL, even on the very robust Y-GeO_2. One popular approach is to block the reactive high-*k* species by inserting a diffusion barrier layer like Al_2O_3.[14] While in this section, an alternative attempt is made by creating a real high-*k* oxide out of thosed limited "Ge friendly" cations.

3.2 Alternative ternary high-k: $YScO_3$

3.2.1 Thin film $YScO_3$ preparation

To investigate the dielectric properties of $YScO_3$ on Ge, p-type Ge(111) wafer was chemically cleaned by methanol, HCl and diluted HF solution sequentially. Prior to the

deposition of $YScO_3$, ultra-thin Y-GeO_2 IL was deposited by rf co-sputtering GeO_2 and Y_2O_3 targets (Y/(Y+Ge)=10%) for interface passivation as described in the chapter 2. Then, $YScO_3$ thin film was deposited in-situ by rf co-sputtering of Y_2O_3 and Sc_2O_3 targets without breaking the vacuum. After the deposition of $YScO_3$/Y-GeO_2/Ge stacks, the post deposition annealing (PDA) was carried out at 500°C in N_2+O_2(0.1%) ambient for 30 s. The gate stack preparation is schematically show in **Figure 3.6**.

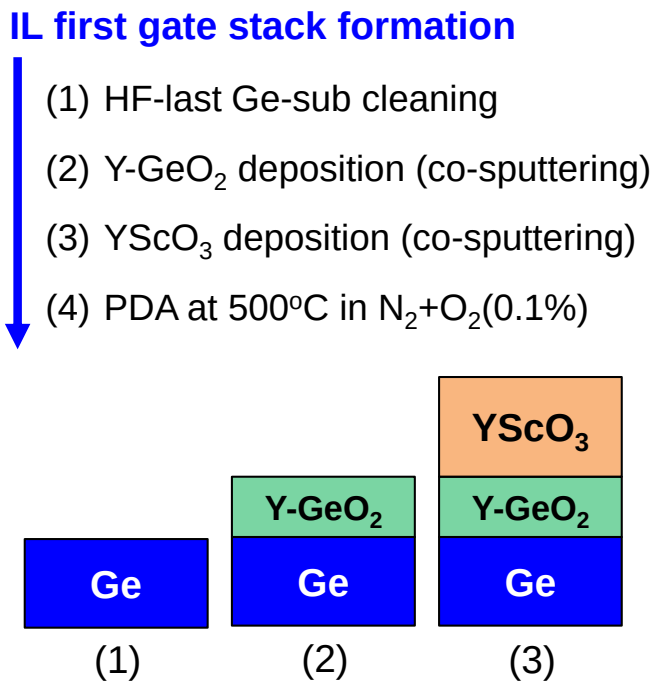
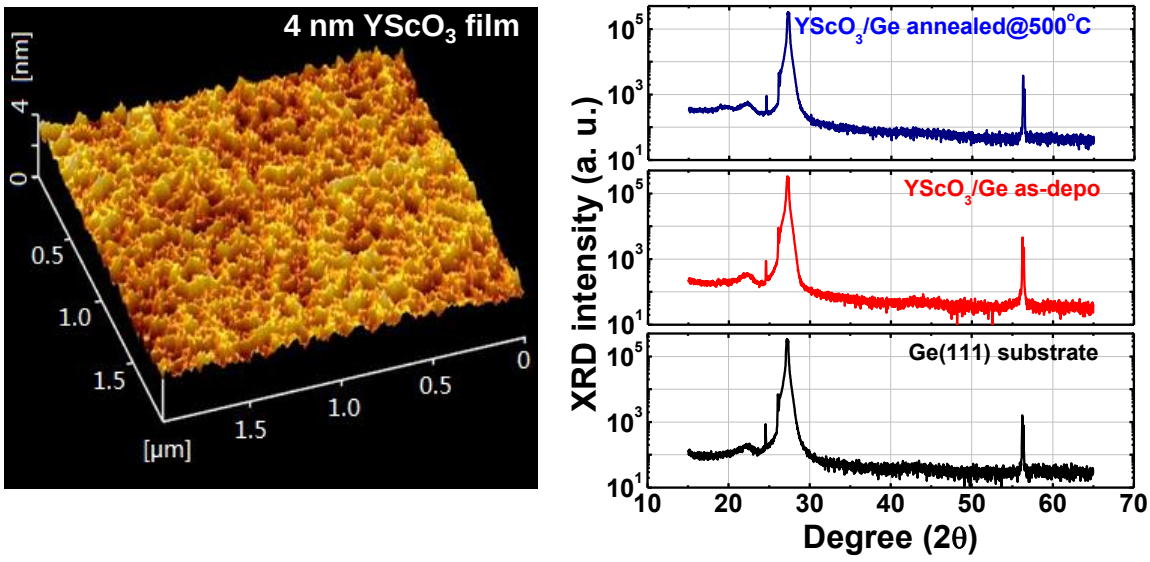


Figure 3.6 Schematics of $YScO_3$/Y-GeO_2/Ge gate stack process. Note that in the step 3, low sputtering power is preferred to reduce damage to the passivated interface.

Since the non-uniformity or poly-crystallinity of the dielectric film would results in the increase of J_G,[15] the uniformity and amorphous feature are examined firstly. The surface morphology of the annealed $YScO_3$/Y-GeO_2/Ge stacks was characterized by atomic force microscopy (AFM) as shown in **Figure 3.7(a)**. A smooth and featureless $YScO_3$ top surface was observed with RMS roughness of 0.3 nm in 2μm×2μm region can be observed for the annealed gate stack, which indicates a good uniformity of deposited $YScO_3$ thin film. The amorphous character of the annealed $YScO_3$ with relative larger thickness

(40 nm) was also confirmed by X-ray diffraction (XRD) as shown in **Figure 3.7(b)**. The XRD pattern of bare Ge(111) substrate is also shown for comparison. The diffraction pattern of anneal $YScO_3$/Ge, as-deposited $YScO_3$/Ge and Ge substrate is exactly the same. There is no diffraction peaks corresponding to the $YScO_3$ crystal can be found in the XRD spectrum, indicating the amorphous nature of the annealed $YScO_3$ film. The good uniformity and amorphous nature of $YScO_3$ is important for maintaining low leakage current in the Ge gate stack.



(a) **(b)**

Figure 3.7(a) AFM image of the top surface of 4 nm $YScO_3$/Ge stack after annealing. The RMS roughness is about 0.3 nm. **(b)** XDR pattern of (40 nm) $YScO_2$/Ge gate stacks (both annealed and as-deposited). The XRD pattern of Ge(111) substrate are also shown for comparison.

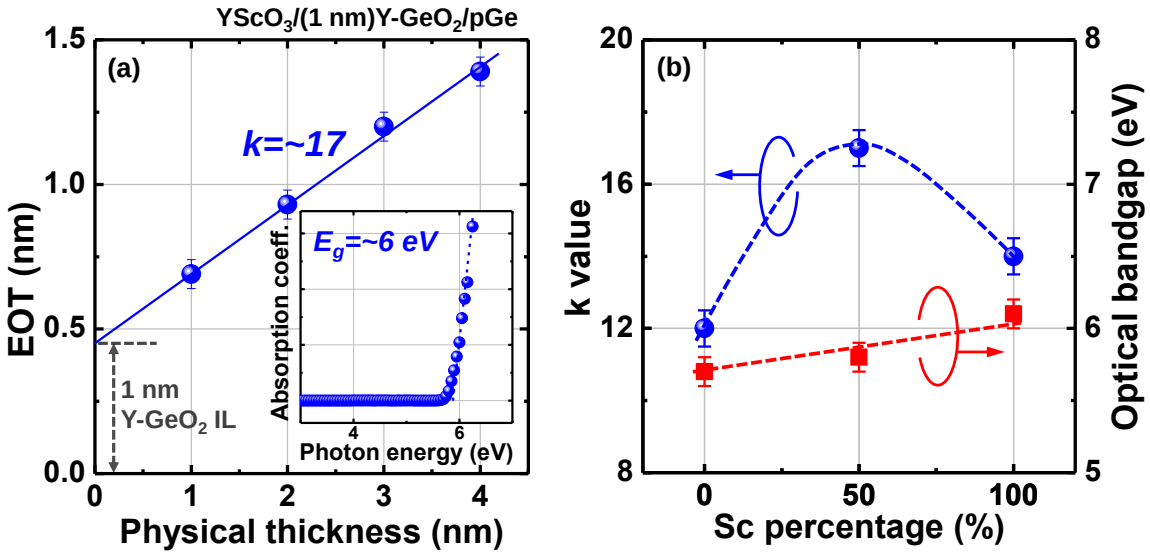
3.2.2 *k*-value enhancement in $YScO_3$ through structural change

To study the electrical properties of $YScO_3$/Y-GeO_2/Ge gate stacks, Au and Al were deposited by vacuum evaporation for the gate electrode and substrate contact of the MOS

capacitors (MOSCAPs), respectively, and the *C*-*V* and *I*-*V* characteristics were measured at RT.

The *k*-value of $YScO_3$ thin film is estimated from the *C*-*V* measurement on $YScO_3$/Y-GeO_2/Ge gate stacks with different physical thicknesses of $YScO_3$. **Figure 3.8(a)** shows the EOT of $YScO_3$/Y-GeO_2/Ge gate stacks as a function of physical thickness of $YScO_3$. Note that the physical thickness of Y-GeO_2 IL is fixed at 1 nm, which contributes 0.5 nm in the total EOT. *k*-value about 17 of $YScO_3$ is estimated from the slope of the linear fit. E_g of $YScO_3$ was also measured on a (40 nm) $YScO_3$/Ge stack by spectroscopic ellipsometry as shown in the inset of **Figure 3.8(a)**. The E_g of $YScO_3$ is estimated to be 5.8 eV, which is in agreement with previous reports.[16] The EOT scaling potential of the $YScO_3$/Y-GeO_2/Ge stacks is ensured by the high *k*-value and sufficient E_g of $YScO_3$.

From a common viewpoint, one might naturally expect that the mixture of two binary oxides should acquire a *k*-value which is the linear combination of the two compounds as well. However, it is not the case for $YScO_3$. Interestingly, a significant enhancement of *k*-value of $YScO_3$ over its binary compounds is noticed as shown in **Figure 3.8(b)**. More interestingly, regardless of the enhancement in *k*-value, E_g of $YScO_3$ is similar to that of Y_2O_3 or Sc_2O_3, which is against the common trend of *k*-E_g trade-off relationship as described in the figure 1.9 in chapter 1. The enhanced *k*-value and sufficient E_g are obtained in $YScO_3$ at the same time, which is a big advantage of $YScO_3$ over its binary compounds as high-*k* dielectric for Ge gate stacks formation.

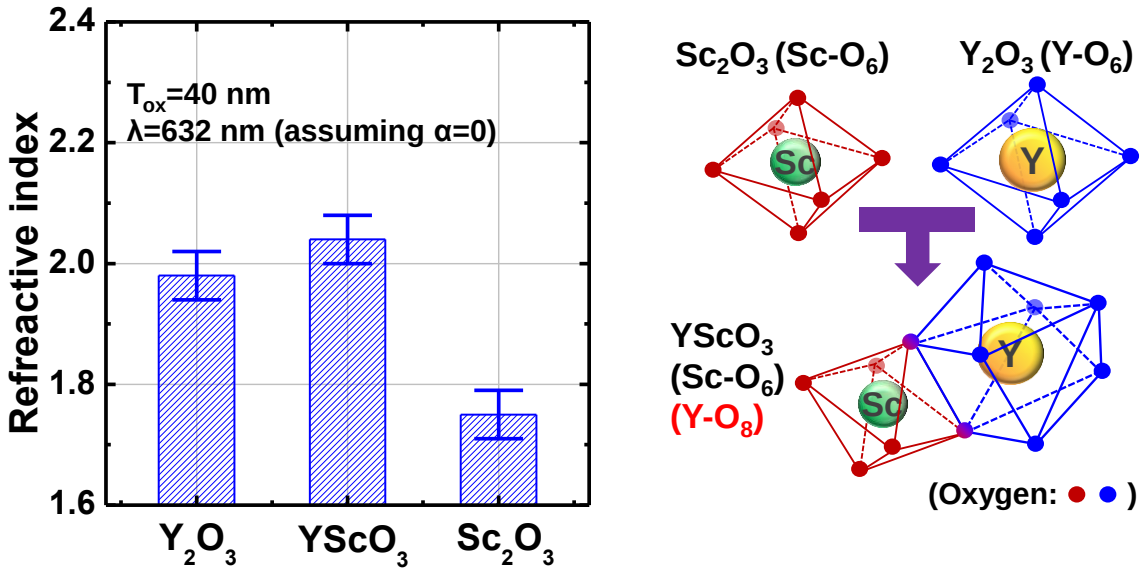


(a) **(b)**

Figure 3.8(a) EOT of $YScO_3$/Y-GeO_2/Ge gate stacks as a function of physical thickness of $YScO_3$. Note that the physical thickness of Y-GeO_2 IL is fixed at 1 nm, which contributes 0.5 nm in the total EOT. The inset shows the absorption coefficient (α) as a function of photon energy for a (40 nm) $YScO_3$/Ge stack. **(b)** *k* and E_g values of Y_2O_3, Sc_2O_3 and $YScO_3$. It is notable that $YScO_3$ enhance the *k*-value comparing to its both binary compounds.

To understand the origin of the *k*-value enhancement in $YScO_3$, reflective indices of Y_2O_3, Sc_2O_3 and $YScO_3$ are measured by spectroscopic ellipsometry on the (40 nm) Y_2O_3/Ge, Sc_2O_3/Ge and $YScO_3$/Ge stacks, respectively, as shown in **Figure 3.9(a)**. Note that the refractive indices are determined at λ=632 nm in this experiment and α is assumed to be 0 at this wavelength. $YScO_3$ shows higher refractive index than both Y_2O_3 and Sc_2O_3, which strongly indicates that $YScO_3$ has a higher packing density than Y_2O_3 and Sc_2O_3.[17] The denser packing of $YScO_3$ is evident from its structure reported in previous literatures.[18, 19] $YScO_3$ has a different structure with both Y_2O_3 and Sc_2O_3 as shown in the **Figure 3.9(b)**[18, 19]. Y_2O_3 or Sc_2O_3 has the Y-O_6 or Sc-O_6 octahedral as their basic unit, respectively. While in $YScO_3$, the relatively larger cation Y^{3+} will increase its coordination

to Y-O_8. On the other hand, the Y-O or Sc-O bond length is not largely changed from the binary compounds to $YScO_3$[18, 19]. This structural change enables a denser packing of the O atoms in the $YScO_3$.



(a) **(b)**

Figure 3.9(a) Refractive indices of Y_2O_3, Sc_2O_3 and $YScO_3$ measured by spectroscopic ellipsometry on the (40 nm) Y_2O_3/Ge, Sc_2O_3/Ge and $YScO_3$/Ge stacks, respectively. Note that the refractive indices are determined at λ=632 nm and α is assumed to be 0 at this wavelength. The higher refractive index of $YScO_3$ indicates a higher packing density. **(b)** Schematics of the coordination polyhedrons in Y_2O_3, Sc_2O_3 and $YScO_3$[18, 19].

It is notable that such a denser packing is common feature among various rare-earth scandate ($REScO_3$) according to the literature reports.[20] **Figure 3.10** summarized the densities of several $REScO_3$ and their corresponding binary compounds, Sc_2O_3 and RE_2O_3. The density of all the $REScO_3$ is higher than the linear combination of the two binary compounds, which indicates that the structure of $REScO_3$ is more densely packed than that of the binary compound.

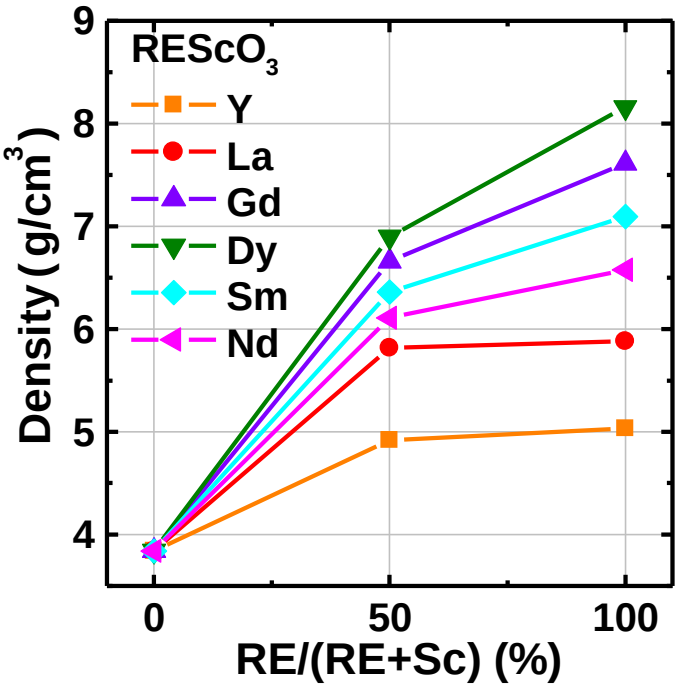


Figure 3.10 Densities of some $REScO_3$ and that of their binary compounds. Note that the densities of REScO3 are higher than linear combination of their binary compounds, which indicates that they are more densely packed.

The denser packing of $YScO_3$ (and other $REScO_3$) comparing to its binary compounds would result in a drastic increase of *k*-value as expected by Clausius-Mossoti (C-M) equation. **Figure 3.11** shows the *k*-value of $REScO_3$ and their binary compounds as a function of their α_m/V_m value. Note that the α_m of RE_2O_3, Sc_2O_3 and $REScO_3$ are derived from ion polarizabilities of RE^{3+}, Sc^{3+} and O^{2-} by the additivity rule,[21] and V_m is calculated from the structures of RE_2O_3, Sc_2O_3 and $REScO_3$.[18-20] The experimental *k*-values of RE_2O_3, Sc_2O_3 and $REScO_3$ are also plotted in the figure both from this work and literatures, which fit the prediction by C-M equation with small deviation. It is notable that the enhancement of *k*-value is also observable for the other rare-earth scandate ($REScO_3$)[22, 23], which might be attributed to the similar structural change and denser packing effect. Thus, we can

conclude that the denser packing of ternary oxides like $YScO_3$ can create high-*k* dielectrics out of two medium-*k* binary oxides.

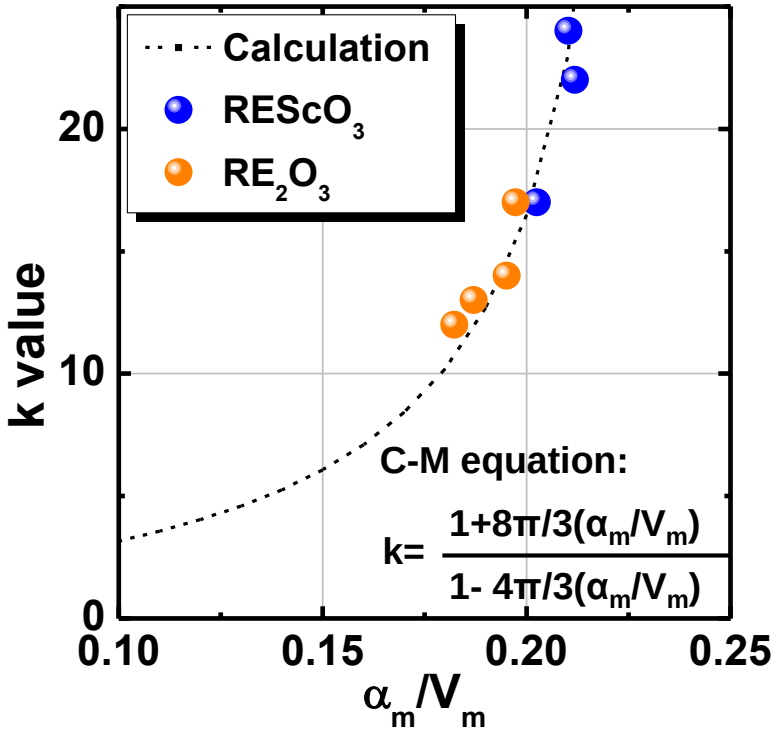


Figure 3.11 *k*-value of RE2O3, Sc2O3 and REScO3 as a function of α_m/V_m (ref. 18-21). The k-value predicted by C-M equation is also shown as a reference.

3.2.3 Interface awareness of $YScO_3$ due chemical stability

The remaining issue (and probably the most important issue) of $YScO_3$ is its impact on the Ge interface after the discussion of film quality and *k*-value. As discussed in the section 1 of this chapter, the interface aware high-*k* should be unreactive with Ge. It has been experimentally confirmed that both Y_2O_3 and Sc_2O_3 are unreactive species on Ge (data not shown). The reactivity between $YScO_3$ and Ge are also examined. **Figure 3.12** shows the Ge*3d* XPS core level spectra of (4 nm) $YScO_3$/Ge with different N_2 PDA temperature (for 30 sec). Note that the spectra are de-convoluted into the Sc*3p*, Y*4p* and Ge*3d* peaks at about 32, 30 and 26 eV, respectively. Referring to equation 3.3 and 3.4, GeO_2 should be form if any reaction occurs between $YScO_3$ and Ge at given annealing temperature. In fact,

there is no signal corresponding to the GeO_x can be found in these gate stacks. It should be noted that the signal at higher binding energy with respect to Ge 3*d* is attributed to Sc 3*p* peak, which is confirmed by $YScO_3$/Si stack deposited at the same condition. The XPS observation indicates that $YScO_3$ is chemically stable on Ge even at 600°C.

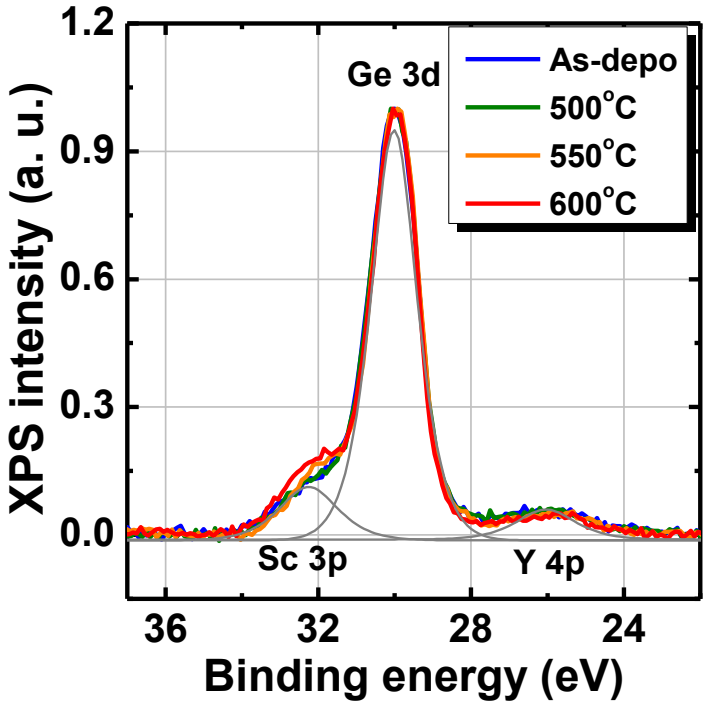


Figure 3.12 XPS spectra from 4 nm $YScO_3$/Ge gate stacks. The spectra are de-convoluted into Sc*3p*, Y*4p* and Ge*3d* peaks. Note that the spectra do not show obvious change with increasing the annealing temperature.

To examine the impact of $YScO_3$ on the interface properties, D_{it} of $YScO_3$/Y-GeO_2/Ge gate stacks with different Y-GeO_2 IL thicknesses was estimated by the high-low frequency capacitance method as shown in **Figure 3.13**.[24] D_{it} from the HfO_2/Y-GeO_2/Ge gate stacks is also shown for comparison. Note that the thicknesses of both $YScO_3$ and HfO_2 are fixed at 2 nm, while EOT of the gate stacks is changed by the Y-GeO_2 IL thickness. It is found that, with the decreasing of Y-GeO_2 IL thickness, D_{it} at $YScO_3$/Y-GeO_2/Ge gate stacks is almost unchanged. On contrary, HfO_2 drastically increases D_{it} with Y-GeO_2 IL thinner than 1 nm, which is attributable to the defect formation by Hf intermixing with IL.[11] Therefore,

we can conclude that, by combining two "IL friendly" medium-*k* components, real high-*k* dielectrics like $YScO_3$ can be formed also with "IL friendly" character, which is in a remarkable contrast with the conventional high-*k* dielectrics like HfO_2. It should also be noted that this "IL friendly" character of $YScO_3$ is valid for both Y-GeO_2 IL and GeO_2 IL (data not shown).

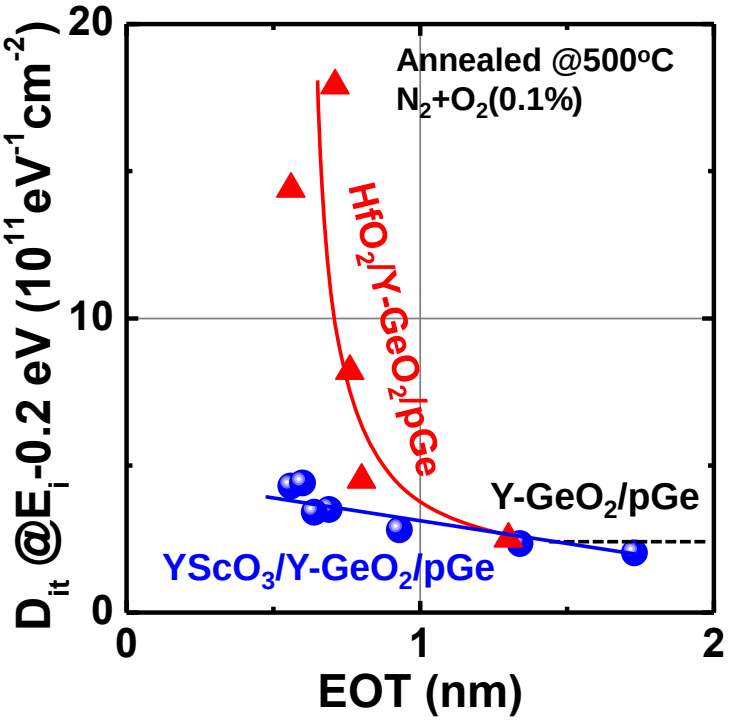


Figure 3.13 D_{it} at E_i-0.2 eV as a function of EOT in $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge stacks. Note that the thicknesses of both high-*k* dielectrics are fixed at 2 nm while the EOT is changed by Y-GeO_2 IL thickness. HfO_2 degrades the interface properties when Y-GeO_2 IL is thinner than 1 nm. On contrary, $YScO_3$ is immunity to interface degradation with ultra-thin Y-GeO_2 IL.

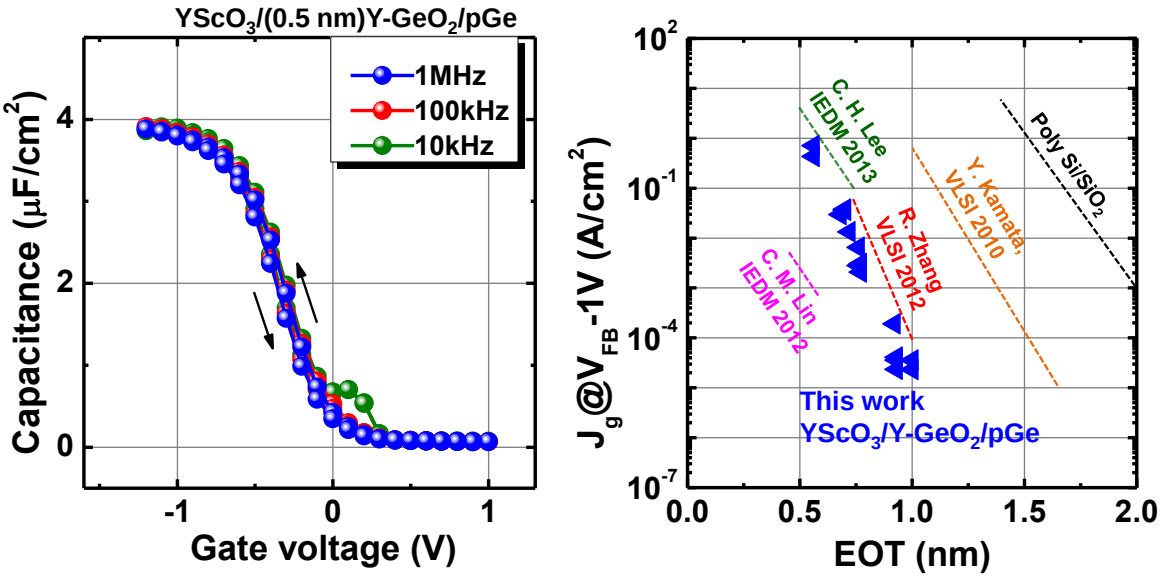
To summarize the results in this section, it is confirmed that $YScO_3$ is one of the desirable high-*k* dielectrics which satisfy all the three requirements suggested in the section 1 of this chapter. Thus, Ge gate stacks with deep sub-nm EOT and good interface can be

expected by using $YScO_3$ as high-*k*. It has to be pointed out that beside $YScO_3$, some other $REScO_3$ might have the similar properties.

3.3 Demonstration of 0.5 nm EOT Ge gate stack

3.3.1 Aggressive scaling of the EOT

Thanks to the "IL friendly" nature of $YScO_3$, EOT scaling can be carried out by aggressively reducing the Y-GeO_2 IL thickness. **Figure 3.14(a)** shows the bidirectional *C-V* characteristics of a $YScO_3$/(0.5 nm)Y-GeO_2/Ge gate stack measured at RT.[24] The EOT of this gate stack is about 0.5 nm. There is no obvious hysteresis or frequency dispersion, which indicates that the good interface properties are maintained regardless of the aggressive EOT scaling. The J_G at V_{FB}-1 V of the $YScO_3$/Y-GeO_2/Ge gate stacks as a function of EOT is also shown in **Figure 3.14(b)**.[24] With high *k*-value and sufficient bandgap of $YScO_3$, J_G is affordable even in the deep sub-nm EOT region, which is comparable to the state-of-the-art Ge gate stacks reported in the recent literatures.[14, 25-27]



(a) **(b)**

Figure 3.14(a) Bidirectional *C-V* curves of $YScO_3$/(0.5 nm)Y-GeO_2/Ge gate stacks with EOT about 0.5 nm measured at RT.[24] No hysteresis and frequency dispersion in *C-V* curves

indicates that $YScO_3$ does not degrade the Ge interface with only 0.5 nm Y-GeO2 IL. **(b)** J_G as a function of EOT in $YScO_3$/Y-GeO_2/Ge gate stacks.[24] Low J_G is observed which is comparable to the state-of-the-art Ge gate stacks.[14, 25-27]

3.4.2 Demonstration of the MOSFET operation

Since the electron mobility in Ge n-channel FETs is highly sensitive to interface properties,[27] we fabricated Ge n-MOSFET to verify out gate stack design for device applications. After HF-last cleaning, 30 nm Y_2O_3 and 500 nm SiO_2 were deposited to form the spacer and field oxides, respectively. Several channel lengths (W/L=90 μm/100–500 μm) were defined, and phosphorus (1×10^{15}/cm^2 dose) was implanted at 70 keV through the Y_2O_3 layer for source/drain (S/D) formation. Dopant activation was carried out at 600°C in N_2 ambient. $YScO_3$/Y-GeO_2/Ge gate stacks were prepared in a same manner as MOSCAPs. After gate stack formation, Al electrodes for the source, drain, and gate were formed by thermal evaporation. The main process flow and device schematics are shown in the Figure **3.15**.

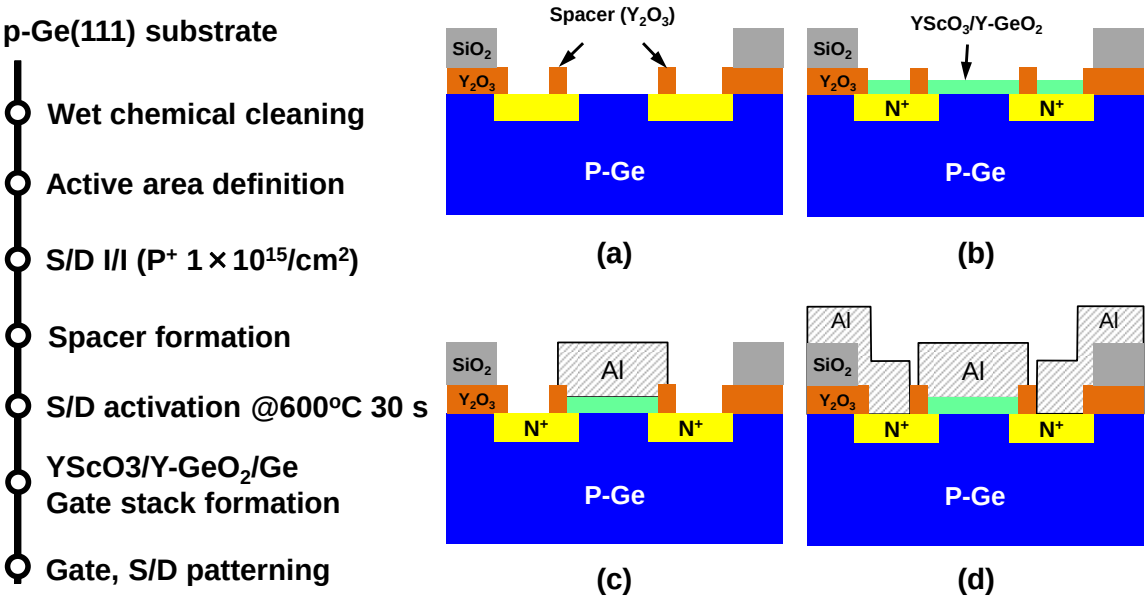


Figure 3.15 Process flow and schematics of Ge n-MOSFET with $YScO_3$/Y-GeO_2/Ge gate stacks. 30 nm Y_2O_3 and 500 nm SiO_2 were deposited to form the spacer and field oxides,

respectively. Several channel lengths (W/L=90 μm/100–500 μm) were defined, and phosphorus (1×10^{15}/cm^2 dose) was implanted at 70 keV through the Y_2O_3 layer for source/drain (S/D) formation. **(a)** Y_2O_3 was etched with HCl-based solution to form spacer; Dopant activation was done by RTA at 600^{o}C for 30 sec. **(b)** $YScO_3$/Y-GeO_2 deposition by rf co-sputtering and annealed at 500^{o}C N_2/O_2 (0.1%) for 30 sec. **(c)** Gate electrode patterning after Al deposition **(d)** S/D patterning.

Figure 3.16 shows the effective electron mobility (μ_{eff}) as a function of inversion carrier density (N_s) in the $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge n-MOSFETs where the Y-GeO_2 IL thickness is fixed at 1 nm. The μ_{eff} in the Y-GeO_2/Ge n-MOSFET (without high-*k*) is also shown for comparison. The $YScO_3$/Y-GeO_2/Ge n-MOSFET shows a moderate μ_{eff} loss with respect to that of Y-GeO_2/Ge when the EOT is greatly reduced. At a fixed EOT (0.8 nm), $YScO_3$/Y-GeO_2/Ge stack has much higher μ_{eff} over the HfO_2 counterpart, especially in the low N_s region. Since the mobility in low N_s region is mainly limited by the coulomb scattering,[29] it is readily understandable that the better interface offered by $YScO_3$/Y-GeO_2/Ge stack shows advantage over HfO_2 counterpart. The peak μ_{eff} in the $YScO_3$/Y-GeO_2/Ge n-MOSFET with EOT 0.8 nm is about 1057 cm^2/Vsec, which is so far the highest peak μ_{eff} for sub-nm EOT Ge n-MOSFET to our knowledge. Thus it is concluded that $YScO_3$ is a promising high-*k* dielectric for high mobility Ge n-MOSFET operation with thin EOT.

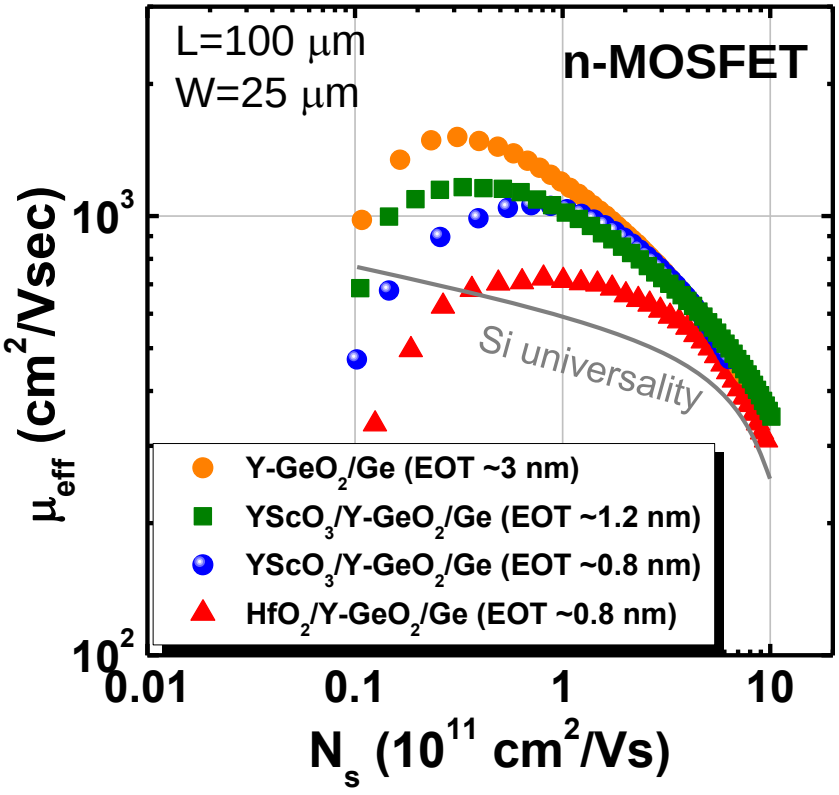


Figure 3.16 The μ_{eff} of $YScO_3$/Y-GeO_2/Ge n-MOSFETs where the Y-GeO_2 IL thickness is fixed at 1 nm. The μ_{eff} in the Y-GeO_2/Ge n-MOSFET is also shown for comparison[5]. The peak μ_{eff} of 1057cm^2/Vsec with EOT 0.8 nm is demonstrated in $YScO_3$/Y-GeO_2/Ge, which is the highest one in sub-nm EOT region due to the immunity to interface degradation.

Figure 3.17 shows the benchmarking of the peak electron mobilities of Ge n-MOSFETs.[24] Some results from the resent works are also shown as reference.[14, 27, 30-32] Comparing to the conventional high-*k* dielectrics, the advantage of $YScO_3$ is most obvious for the sub-nm EOT region since the mobility is not significantly degraded with reducing EOT. This result obtained for $YScO_3$/Y-GeO_2/Ge stack strongly suggested that $YScO_3$ is a promising high-k dielectric.

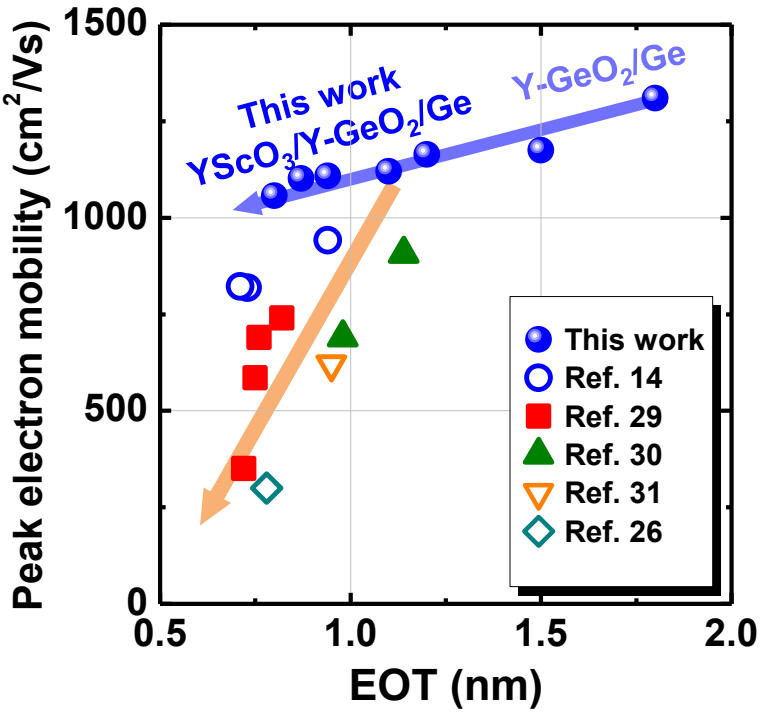


Figure 3.17 Benchmarking of peak electron mobility in Ge n-MOSFETs as a function of EOT.[14, 24, 27, 30-32] Comparing to other conventional high-*k*, $YScO_3$ shows moderate mobility degradation with reducing EOT.

3.4 Summary

The selection of a highly scalable and interface aware high-*k* has been discussed in this chapter after the designing of a promising IL. It is pointed out that the intermixing of high-*k* dielectric with GeO_2 based IL enables the high-*k* to exert a significant impact on the interface properties depending on the bond configuration of cation species in GeO_2-based IL. Thus, the procedure for the high-*k* selection here follows a "bottom up" manner, namely, selecting the cation species with defect free configuration on Ge and use this limited category of cations to assemble a real high-*k*.

It is found that ternary oxides made from two Ge friendly binary oxides are feasible high-*k* dielectrics for Ge gate stack formation in terms of both high *k*-value and "IL

friendly". The key point is the scandate formation of ternary oxides, in which a small cation radius Sc can enhance the density (reduce molar volume). This has lead us to the successful results, in spite of the fact that both binary oxides have medium-*k* values. $YScO_3$ is found to be a good example of desirable high-*k* material on Ge due to its "IL friendly" character and a high permittivity about 17. Based on these understandings, EOT scaling to about 0.5 nm was demonstrated by $YScO_3$/Y-GeO_2/Ge gate stacks with promising interface properties.

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Chapter 4

Reliability assessments on Ge MOS device

4.1 Dielectric degradation mechanisms in MOS device

4.2 Carrier trapping behaviors in GeO_2 based dielectrics

4.3 Dielectric degradation under high electric field

4.4 Demonstration of reliability improvements on Ge gate stack

4.5 Reliability assessment for sub-nm EOT Ge gate stack

Overview

Reliability of device for long term application is one of the most critical concerns for the MOSFET design and fabrication. Though prominent interface property and aggressive EOT scalability has been demonstrated in the previous chapters, the good initial properties do not secure the long term application since device parameter might be changed over time by the applied electric field. V_{FB} shift (or V_{th} shift, equally) under the electric stress field (E_{stress}) is one of the most important failure modes which limit the device performance and lifetime.[1, 2] The interface passivation can be degraded by the E_{stress} too, which results in the increase of interface state density (D_{it}) and the reduction of trans-conductance (G_m).[3] Insulating properties of the gate oxides might also be degraded under E_{stress} in terms of excessive gate leakage current (J_G) known as the stress induced leakage current (SILC).[4, 5] Such destructive change of device parameters comes up as a possible showstopper for the device application in the real scene, while no sufficient information has been reported for Ge.

In this chapter, the reliability degradation mechanisms of the Ge MOS device are discussed, and the possible approaches to improve the Ge MOS reliability are investigated as well.

Since the interface layer (IL) is especially susceptible to reliability degradation,[6] and for Ge MOS device, the IL is an essentially different component from the Si counterpart, a detailed investigation should be carried out firstly on GeO_2-based ILs. By measuring the MOS device parameter shifts, the trapping behaviors in GeO_2/Ge are analyzed in term of both pre-existing traps in the as-prepared gate stacks and trap generation by the E_{stress}. It is found that the initial trap density in the as-prepared Ge gate stack is related to the process condition. The reduction of oxygen vacancy (V_O) by high pressure oxidation (HPO)[7] can effectively reduce the hole traps. On the other hand, the trap generation under high E_{stress} is determined by the network rigidity of the dielectrics. Y or Sc-GeO_2 can suppress the trap

generation due to their enhanced rigidity of the network. The interface degradation under high E_{stress} is also found to be improved by doping.

The reliability assessment is also carried out for the sub-nm EOT $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge gate stacks. The impact of different high-*k* on the Ge MOS reliability is discussed.

4.1 Dielectric degradation mechanisms in MOS device

With the reduction of device dimensions, it becomes an increasingly critical problem that the device parameters change over time such as the degradation of G_m, the shift of the V_{th} and the increase of the J_G. It has been pointed out that such device parameter change is majorly induced by the charge trapping in the dielectrics.[1-5] The traps are classified into two types according to their formation mechanism, namely, the pre-existing traps formed during the gate stack process and generated traps under high E_{stress}.[8-10] Here, some basic understandings on these two types of traps are summarized according to the literatures.

In the gate stack process, the purity, stoichiometry and uniformity cannot be completely ensured. The inclusion of these charged defects might result in trap in the as-prepared gate stacks,[11, 12] which can capture the electrons or holes through Coulomb attraction. One of the direct impacts of the charge trapping is the shift of the V_{FB} (or V_{th}, equally) with time, which is understandable from the distortion of the band diagram as schematically shown in **Figure 4.1(a)** and **(b)** for the electron trapping and hole trapping, respectively. Note that the black lines indicate an ideal band diagram without any trapping, while the blue and red dotted lines indicate the distorted band diagram after the occurrence of electron or hole trapping, respectively. Note that these two schematics are reflecting the flat band condition of the gate stack. Now let's assume that the flat band condition should be maintained and charge trapping is introduced into dielectric. When electrons are trapped, the gate voltage (V_G) should be positively shifted to compensate the electric field generated

by the trapped electrons (otherwise the flat band condition is broken). Thus, a positive shift of the V_{FB} could be observed when electron trapping is dominant. The hole trapping, on contrary, results in a negative shift of the V_{FB}. The dependence of V_{FB} shift on the trap density can be written as follow,[13]

$$\Delta V_{FB} = \frac{qN_t}{C_{ox}} \tag{4.1}$$

Here, N_t, C_{ox}, q are the trap density, oxide capacitance and electron charge, respectively. Note that the traps are assumed to be near the dielectric/semiconductor interface.

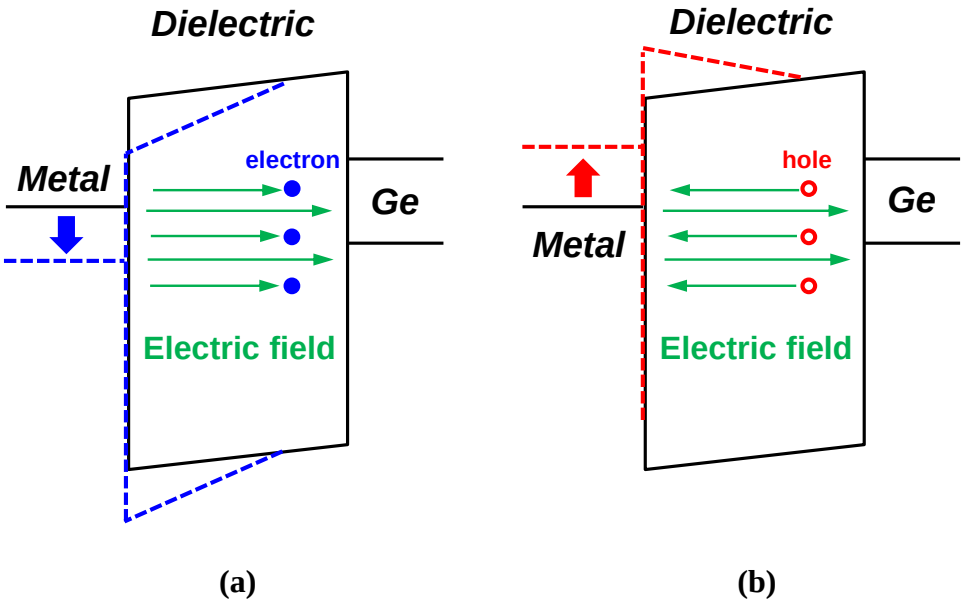


Figure 4.1 Band diagram of Ge gate stacks with **(a)** electron or **(b)** hole trapping. Note that the black lines denote the ideal gate stack without trapping, while the blue and red dotted lines stands for the band distorted by electron and hole trapping, respectively. Such distortion of band is originated from the electric field from the trapped carriers, which is compensated by the shift of V_G.

Though the effect of the electron and hole trappings are shown separately in the above schematics, both might exist in a same gate stack. Thus, the total V_{FB} shift after stress is a

combined effect of electron and hole trappings, and the direction and magnitude of V_{FB} shift is determined by the net charge trapping density. Since electron and hole traps have different cross-sections for the carriers,[14-16] the trapping rate of electron and hole might be different as well, which might result in a "turn around" V_{FB} shift as shown in **Figure 4.2** (for SiO_2/Si stacks, depending of the stress condition as well).[16]

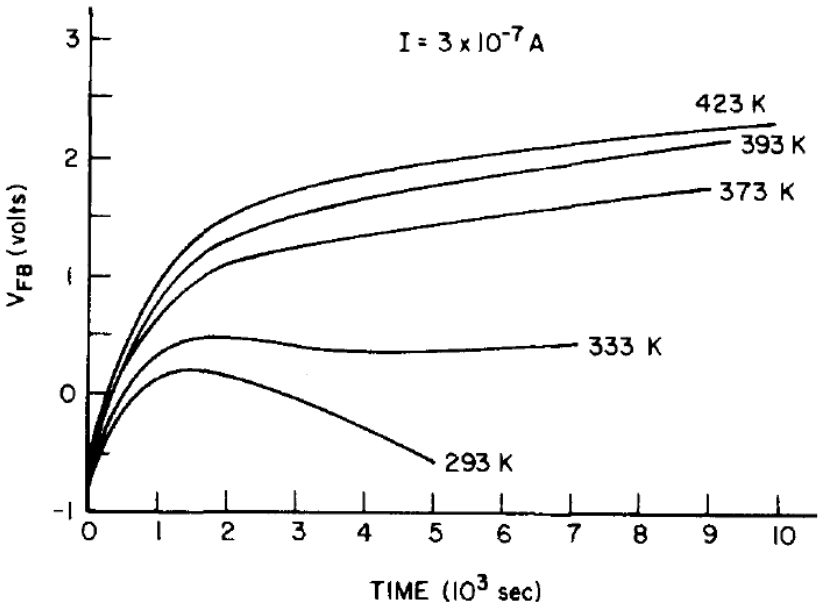


Figure 4.2 V_{FB} shift of Al/SiO_2/Si gate stack as a function of time under constant current stress of I=3×10^{-7} A (gate diameter=0.032 inch).[16] For room temperature stress (293 K), the electron trapping is dominant initially and then the hole trapping becomes the major component.

It must be emphasized that, to differentiate the contribution of pre-existing traps from that of newly generated traps, the applied E_{stress} field must be small enough,[8-10] because that an elevated E_{stress} field can create additional traps by bond breakings in the dielectrics. Though it is widely accepted that bond breaking in the dielectric is the origin of trap generation, the quantitative models to analyze such bond breaking process are so far controversial. There are basically two models for the bond breaking under E_{stress}, the carrier injection model[17] and the thermochemical model.[18] The carrier injection model explains

the bond breaking in the dielectrics from the injected carriers as schematically shown in **Figure 4.3**.[17] Under a negative V_G, the injected electrons are accelerated by the external electric field and obtain a considerable energy gain (ε_{gain}), which enables them to break the bond (especially Si-H) by ionization. It is a slightly different case under positive bias since the hole is facing a higher band offset than that of the electron. Therefore, the hole injection is triggered by the electrons.[19] Namely, the electrons are accelerated from the semiconductor side to the gate metal and excite the electron-hole pairs in the gate metal. The generated holes again can be injected from gate metal to the semiconductor interface and break the bonds as well.[19] The carrier injection model has successfully explained the reliability degradation mechanisms in the SiO_2/Si system.[17,19] However, the carrier injection model becomes less helpful when high-*k* dielectric is involved which shows different degradation behaviors with SiO_2 experimentally.

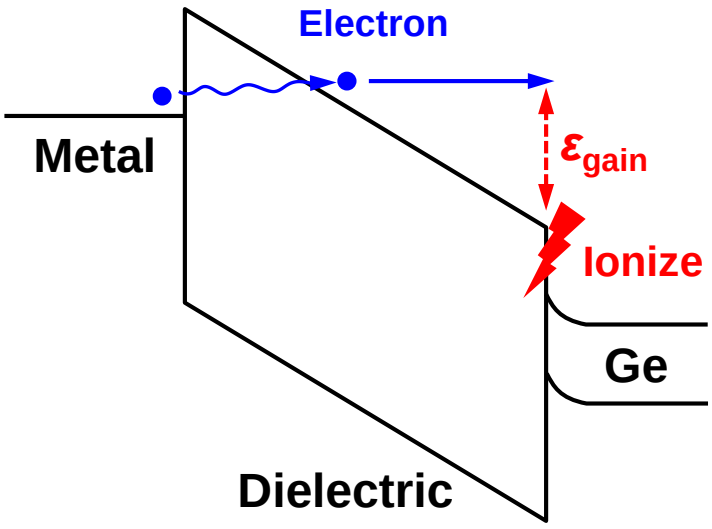


Figure 4.3 Schematic of carrier injection model for trap generation in the dielectrics under a negative E_{stress}.[17] The electrons from the gate metal are accelerated by the external electric field and acquire the sufficient ε_{gain} to break the bond near interface. For the positive E_{stress}, similar mechanism is involved except for that the holes are generated by the injected electrons.

Thermochemical model can analyze the reliability of the dielectrics with different *k*-values at better accuracy. **Figure 4.4(a)** schematically shows the thermochemical model in atomistic scale for the dielectric degradation mechanism of SiO_2.[18, 20] The chemical bonds are broken by the local electric field (E_{loc}, not externally applied field) and the ions are displaced from their original sites to form traps. The thermochemical model for the trap generation rate can be quantitatively expressed as the following equation,

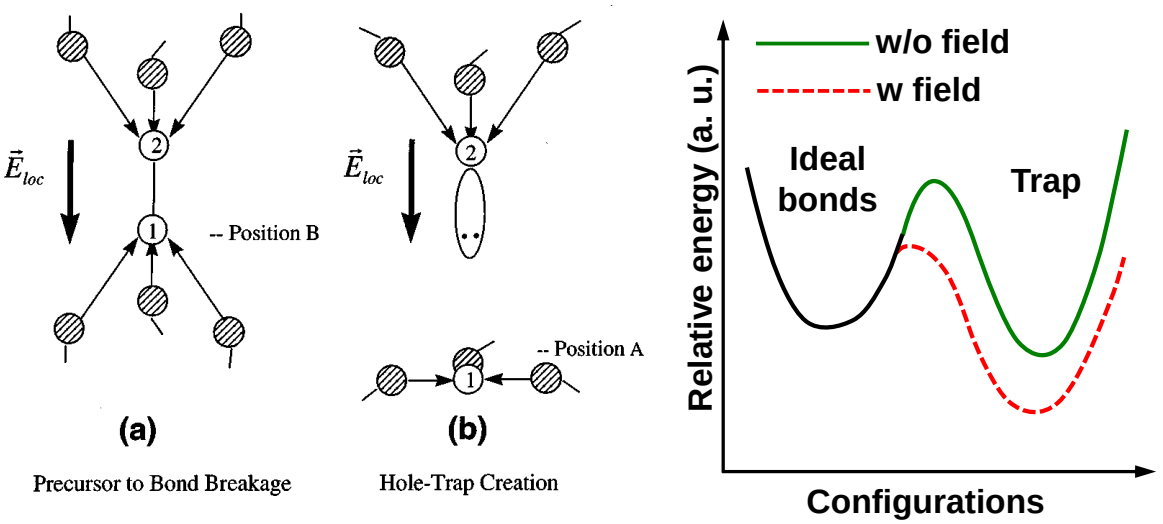
$$r = r_0 \, exp(-\frac{\Delta H_0 - \mu \cdot E_{loc}}{k_B T}) \tag{4.2}$$

where r_0 is a characteristic of collision (interaction) frequency, μ and T are the molecular dipole moment and temperature, respectively. ΔH_0 stands for the activation energy for bond breaking and ion displacement in the dielectric.

This equation reflects a basic physical picture of the trap generation in the MOS devices. In detail, the dielectric/semiconductor is a highly ordered system, while the trap sites can be seen as disorders from this ideal state. Thus, the entropy should favor the trap generation. Fortunately, the metal-oxygen bond forms an energy barrier here to stop the dielectric degradation immediately, which is reflected as an activation energy term ΔH_0 in the equation 4.2. On the other hand, with the local electric field and dipole moment, an additional energy μE_{loc} is given to lower the activation energy of bond breaking and ion displacement. Therefore, dielectric is degraded under electric stress.

It should be noted that, for the dielectric with higher-*k* than SiO_2, the value of E_{loc} is also larger, which makes it more susceptible to trap generation. This difference results in the *k*-value dependence of dielectric reliability, which is confirmed by experimental observations.[20] **Figure 4.4(b)** schematically shows the energy states corresponding to the ideal dielectric and trap generation with and without electric field. The equation 4.2 is more easily understandable by referring to this energy state configuration.

Since the dielectrics discussed in this work, including GeO_2 and M-GeO_2, have different *k*-values (higher than that of SiO_2), I will use the thermochemical model to analyze the experimental results in the following sections.



(a) **(b)**

Figure 4.4(a) Atomistic schematics of thermochemical model for dielectric degradation in SiO_2.[18, 20] The chemical bonds in the dielectric are broken by the E_{loc} (dependent on the dielectric thickness, V_G and *k*-value) and the ions are displaced from the original sites, which results in the generation of hole traps. **(b)** Schematically shows the energy states corresponding to the ideal dielectric and trap generation with and without electric field.

4.2 Carrier trapping behaviors in GeO_2 based dielectrics

4.2.1 Constant field stress on GeO_2/Ge based gate stacks

In following two sections, the reliability of two kinds of gate stacks were examined, namely, GeO_2/Ge stacks and M-GeO_2/Ge stacks. Both p-type and n-type Ge(111) substrates were used (from the same vender AXT) after HF-last cleaning, with the resistivity of 0.6 Ω·cm and 0.7 Ω·cm, respectively. The (4 nm) GeO_2/Ge stacks were formed by thermally oxidizing Ge substrates under various oxygen pressure (P_{O2}) from 1

to 70 atm. For the 1 atm O_2 oxidized GeO_2/Ge stacks, a low temperature O_2 annealing (LOA) were added to passivate the interface.[7] (4 nm) M-GeO_2/Ge (M for Al, Sc and Y, respectively) stacks were also prepared by radio frequency co-sputtering of GeO_2 and M_2O_3 targets in a same manner as described in chapter 2. The M atomic percentages of the samples are all controlled to be (10±1)% in the metallic atom ratio (M per.=M/(Ge+M)) unless specifically noted. After the deposition of M-GeO_2 on Ge, the PDA was carried out at 500^{o}C in N_2 ambient for 30 sec. Au and Al are used for these MOSCAPs as gate and substrate contacts, respectively. Note that all the stacks prepared here for the reliability tests have reasonably good interface properties as already systematically discussed in the chapter 2. The EOT of GeO_2 and Y-GeO_2/Ge stacks are 3 and 2 nm, respectively.

The constant E_{stress} experiments of both polarities were carried out at room temperature by applying positive and negative V_G on n-Ge and p-Ge MOSCAPs, respectively. This is because when the E_{stress} is applied on the accumulation region of Ge gate stack, the voltage loss in the Ge substrate can be minimized, and the E_{stress} is completely applied on the dielectrics. The *C-V* and *I-V* characteristics were recorded before and after the stress. Note that, in this work, the magnitude of the E_{stress} is defined as $E_{stress}=V_{OX}$/EOT for a fair comparison by considering the practical device operations with different EOT. Here V_{OX} is the oxide voltage ($V_{OX}=V_G-V_{FB}$), namely, the actual voltage applied on the dielectric. Under such a definition, the same magnitude of E_{stress} would correspond to the same amount of carriers in the channel for MOSFET operation.

It should be noted that this E_{stress} definition is not only a fair comparison concerning the real device application, but also compatible with the thermochemical model, because this definition of E_{stress} has compensated the *k*-value impact on dielectric reliability and the E_{loc} would be almost the same magnitude for the dielectrics with different *k*-values.

The detailed experiment procedures are schematically shown in **Figure 4.5**. Positive and negative V_G was applied on the n-Ge and p-Ge substrates at room temperature,

respectively, where Ge is in accumulation region with negligible voltage drop. The applied V_G forms an E_{stress} field on the dielectrics, and with a time interval, the V_G is scanned once to collect a *C-V* or *I-V* curve. It has to be noted that such a *C-V* or *I-V* scan out of stress level might result in the detrapping of the carriers.[21] To minimize the detrapping effect, the *C-V* or *I-V* scan is carried out rapidly (within 10 sec) and the V_{FB} value is collected in the downward *C-V* scan of the V_G.

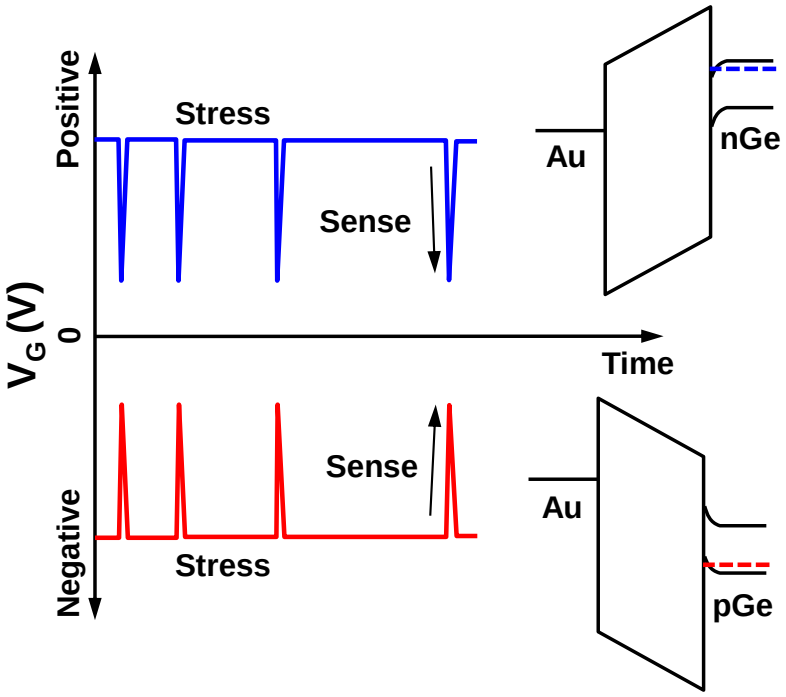
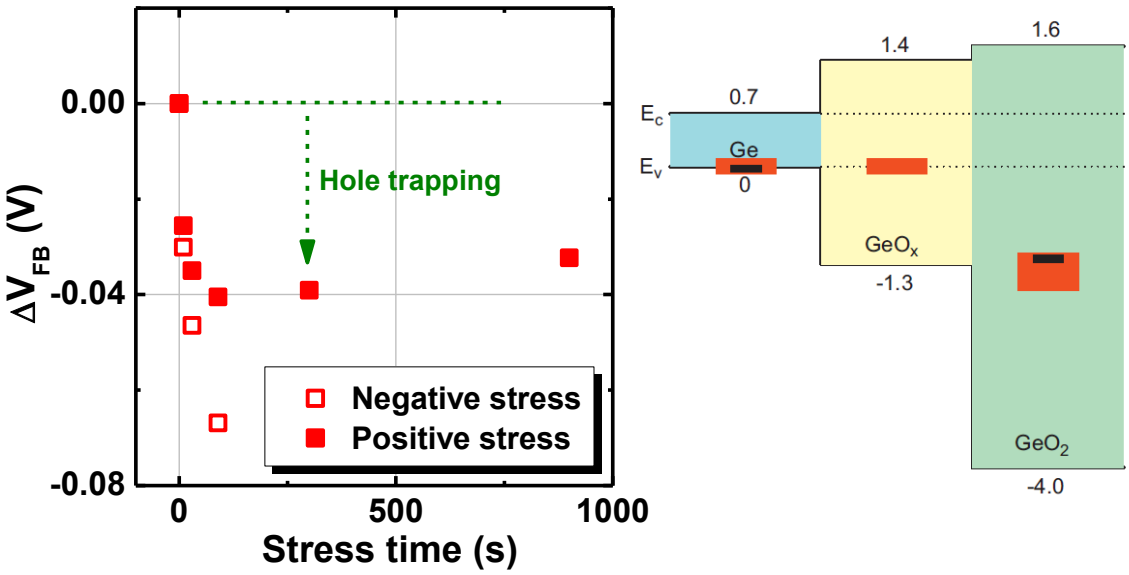


Figure 4.5 Schematics of the experimental procedures for E_{stress} on Ge with both polarities. Note that the *C-V* curves are collected along the scan direction indicated by the arrows.

4.2.2 Pre-existing trap species in GeO_2/Ge gate stack

Firstly, the pre-existing traps in the GeO_2/Ge based stacks are investigated under low E_{stress} (4 MV/cm) where trap generation should not occur. Namely, this low E_{stress} can only fill the pre-existing trap site by injected carriers, but not generating new traps. Before investigating various Ge gate stacks, let's examine the simplest one, 1 atm O_2 oxidized GeO_2/Ge stack first, to acquire a basic concept on which kinds of trap species to mind for

the following investigations. **Figure 4.6(a)** shows V_{FB} shift as a function of time for 1 atm GeO_2/n-Ge and p-Ge stacks under positive and negative E_{stress} (4 MV/cm), respectively. It is found that both polarities show a significant negative V_{FB} shift, which indicates that the large amount of hole trapping is the dominant trapping species in GeO_2/Ge stack. It has been reported by a first principle calculation that the V_O formation in the GeO_2 contributes significantly to the hole traps.[22] Especially for the V_O located close to the Ge interface (in transition region, GeO_x), its energy level is quite close to the valence band maximum of the Ge as schematically shown in **Figure 4.6(b)**, which indicates a negligible energy consumption for hole trapping to occur in these trap sites. As discussed in the chapter 2, the 1 atm O_2 oxidized GeO_2/Ge stack is expected to has a lot of V_O due to the GeO desorption process. Therefore, V_O in this gate stack might explain the large negative V_{FB} shift under E_{stress}. Since the V_O might be a major source of pre-existing traps in GeO_2/Ge stack, the control of which in the gate stack process is expected to improve the reliability assessment of Ge gate stacks under low E_{stress}.



(a) **(b)**

Figure 4.6(a) V_{FB} shift in 1 atm GeO_2/Ge stacks under 4 MV/cm E_{stress} with both polarities. The large negative shift of the V_{FB} represents the large amount of hole trapping. **(b)** The

calculated energy level for V_O in the GeO_2/Ge gate stack,[22] where GeO_x is the transition region. Note that, regardless the dominant hole traps, certain amount of electron trap might also exists in the GeO_2/Ge, which only observed under positive E_{stress} with time longer than 300 sec (slightly positive V_{FB} shift).

4.1.3 Control of pre-existing traps by gate stack process

It has also been clarified in the chapter 2 that the V_O formation (GeO desorption, equally) might be suppressed by HPO or M-GeO_2. Therefore, in this section, the impact of HPO and M-GeO_2 on the pre-existing hole traps are examined.

The V_{FB} shift of GeO_2/Ge stacks with various annealing P_{O2} is examined under 4 MV/cm as shown in **Figure 4.7(a)** and **(b)** for positive and negative E_{stress}, respectively. It is found that by increasing the P_{O2}, the larger negative V_{FB} shift is reduced comparing to 1 atm oxidized GeO_2/Ge gate stacks for both positive and negative E_{stress}, which is in agreement with the expectation from V_O consideration. It is noted that, since the total amount of the pre-existing hole traps is limited in these HPO-GeO_2/Ge stacks, the V_{FB} shifts saturate over long stress time. Thus, it can be concluded that the suppression of V_O during gate stack process by HPO might be a useful approach to reduce the pre-existing hole trap density in the gate stack.

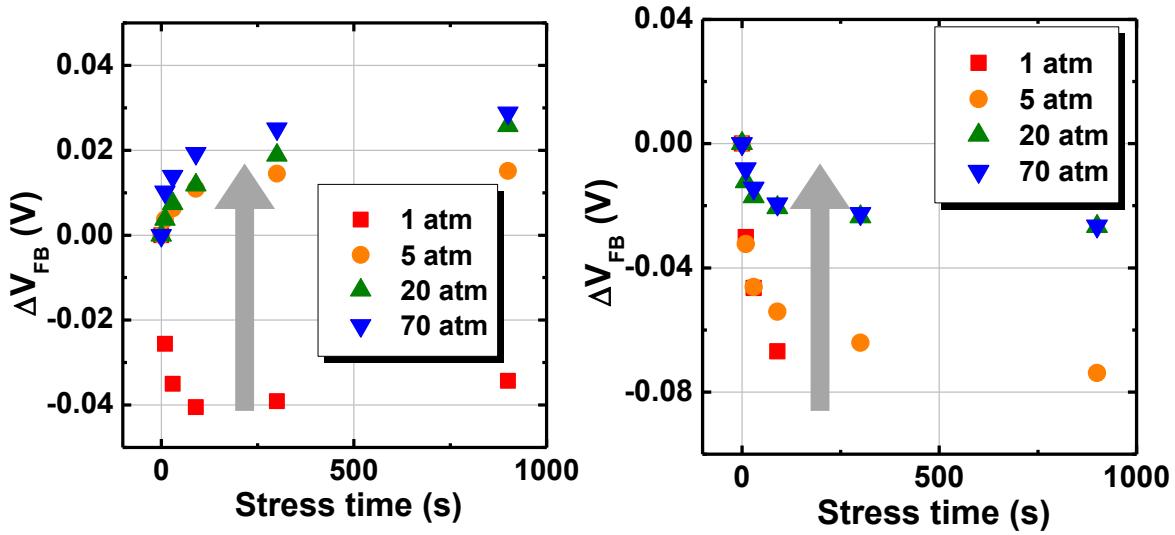


Figure 4.7 V_{FB} shift in GeO_2/Ge stacks with various process P_{O2} (1 to 70 atm) as a function of time under **(a)** positive and **(b)** negative E_{stress}. The large negative V_{FB} shifts are reduced in both polarities by increase P_{O2}, which might be explained by less V_O formation during the gate stack process.

It has also been proposed in chapter 2 that M-GeO_2 is another effective method to suppress the V_O formation in the gate stack. So, low field E_{stress} (4 MV/cm) is carried out on the M-GeO_2/Ge stacks as well. The effects of various kinds of M doping (Al, Sc and Y) are also compared with that of GeO_2/Ge stack. Note that the M-GeO_2/Ge stack is annealed in N_2 ambient, thus there is no HPO effect. Their impact on the pre-existing trap densities are estimated from the saturated V_{FB} shift by equation 4.1 and listed on the following **Table 4.1** together with that of pure GeO_2. Y and Sc doping have strong effect on reducing the pre-existing traps, which is also in agreement with the suppression of GeO desorption and V_O formation as discussed in chapter 2.

Table 4.1 Trap densities of GeO_2 and M-GeO_2/Ge stacks estimated from the saturated V_{FB} shift under 4 MV/cm E_{stress}

Dielectric	1 atm GeO_2	70 atm GeO_2	Al-GeO_2	Sc-GeO_2	Y-GeO_2
N_t (cm^{-2})	~10^{12}	~2.5×10^{11}	~4.5×10^{11}	~3.0×10^{11}	~2.5×10^{11}

In the final part of this section, I would like to discuss a little about the definition of pre-existing traps. It is simply assumed in the previous discussion that under 4 MV/cm E_{stress} the trapping of carriers mainly occurs at the pre-existing traps formed during gate stack process, while the newly generated traps are negligible. (The criterion on the E_{stress} for no trap generation is usually 4 to 8 MV/cm for the SiO_2/Si stack.[8-10]) However, this assumption is yet to be confirmed that 4 MV/cm E_{stress} is really low enough or not to neglect the trap generation in GeO_2/Ge stack. The circularly trapping-detrapping behaviors are investigated on a (6 nm) HPO-GeO_2/Ge stack, with 900 sec of positive E_{stress} for trapping follower by 10 sec of negative E_{stress} in a same magnitude for detrapping circularly as shown in **Figure 4.8**. The magnitude of E_{stress} here is 2 and 4 MV/cm. Under the negative E_{stress} carrier trapping occurs which results in obvious V_{FB} shift and it is recovered by detrapping under 10 sec positive E_{stress}. It is notable that when the second and the third runs of negative E_{stress} are applied, the magnitude of V_{FB} shift saturated at a same value as the first stress (for both 2 and 4 MV/cm). Similar repeatability can also be observed under and negative-trapping/positive-detrapping experiment. Such repeatability indicates that the total trap sites in the dielectric might not be obviously changed by the low field E_{stress} below 4 MV/cm, while only those pre-existing traps are filled by the carriers and then depleted.

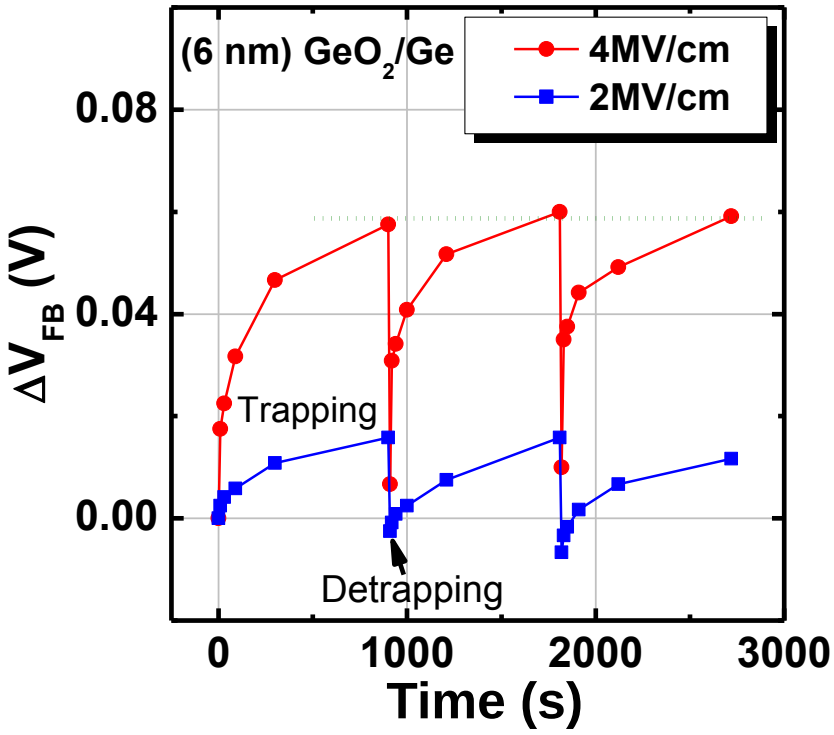


Figure 4.8 V_{FB} shift under circularly trapping-detrapping process by 900 sec of positive E_{stress} and 10 sec of negative E_{stress}. It is found that the trapping is highly repeatable under both 2 and 4 MV/cm, which indicate that the trap generation can be neglected in these stress condition.

In summary, it is found that the pre-existing hole trap is a critical concern for the GeO_2/Ge gate stacks, which might be related to the V_O formation during gate stack process. By the reduction of V_O through controlling the process condition like HPO or M-GeO_2, the pre-existing hole traps can be reduces, and the reliability of Ge gate stacks can be improvement for low field E_{stress}.

4.3 Dielectric degradation under high electric field

4.3.1 Trap creation in GeO_2 based oxides under high field

It is concerned that the promising initial properties of Ge gate stack (including a low pre-existing trap density) might be degraded under the elevated E_{stress}. In fact, the trap generation occurs due to the bond breaking and ion displacement in the gate dielectric, which results in significantly larger V_{FB} shift, and finally, breakdown of the gate dielectric.[18, 20, 23-25] To examine the trap generation behaviors in HPO-GeO_2/Ge and M-GeO_2/Ge stacks, E_{stress} with higher intensities (6.5 and 9 MV/cm) was applied, and V_{FB} shift was extracted from *C-V* characteristic before and after stress. The densities of newly generated traps under high intensity E_{stress} were also derived by equation 4.1 (note that in the results, the pre-existing trap density is subtracted from the total trap density).

Since HPO-GeO_2/Ge stacks show quite low pre-existing trap densities for both electron and hole, its property under high E_{stress} is also examined. **Figure 4.9** shows the newly generated electron trap density in the GeO_2/Ge gate stacks as a function of process P_{O2}. Note that the trap density is estimated from the V_{FB} shift with 90 sec E_{stress} by equation 4.1. Though HPO-GeO_2/Ge slightly reduces the trap generation under high E_{stress} comparing to 1 atm P_{O2} processed gate stack, the trap generation is unfortunately still not satisfying (reduced by less than half comparing to 1 atm P_{O2} oxidized GeO_2). The weak dependence of the trap generation on the P_{O2} indicates that other approaches might be needed to improve the reliability robustness of the Ge gate stacks under high E_{stress}

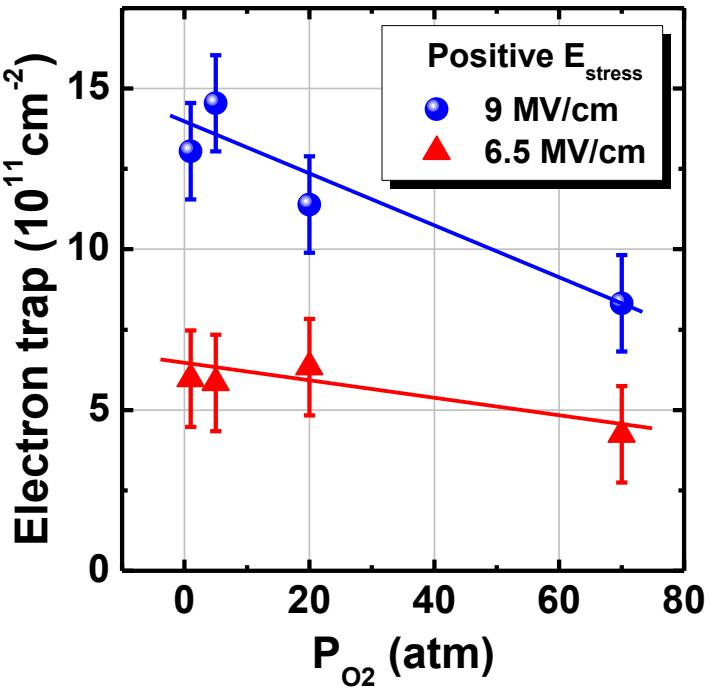


Figure 4.9 The newly generated electron trap density in GeO_2/Ge stacks under positive E_{stress} as a function of P_{O2} in the gate stack process. HPO can not sufficiently control the trap generation under high E_{stress} regardless of very promising properties in the initial and under low E_{stress} field.

Y-GeO_2 might have a different impact on the trap generation, because Y-GeO_2 not only suppresses the V_O formation, but also changed the GeO_2 network. The trap generation in Y-GeO_2/Ge stacks is also investigated under high field E_{stress} (6.5 and 9 MV/cm). **Figure 4.10** shows the newly generated electron trap densities in the Y-GeO_2/Ge stacks as a function of Y percentage under positive E_{stress}. Again, the trap density is estimated from the V_{FB} shift with 90 sec E_{stress} by equation 4.1. It is notable that with small amount of Y doping, the trap generation is drastically reduced (1/4 of the value of GeO_2/Ge). However, further increase the Y percentage will enhance the trap generation again, which might be attributed to the over constraint and immiscibility as well since the dielectric might be mechanically stressed and less uniform for with high Y percentage.[26, 27]

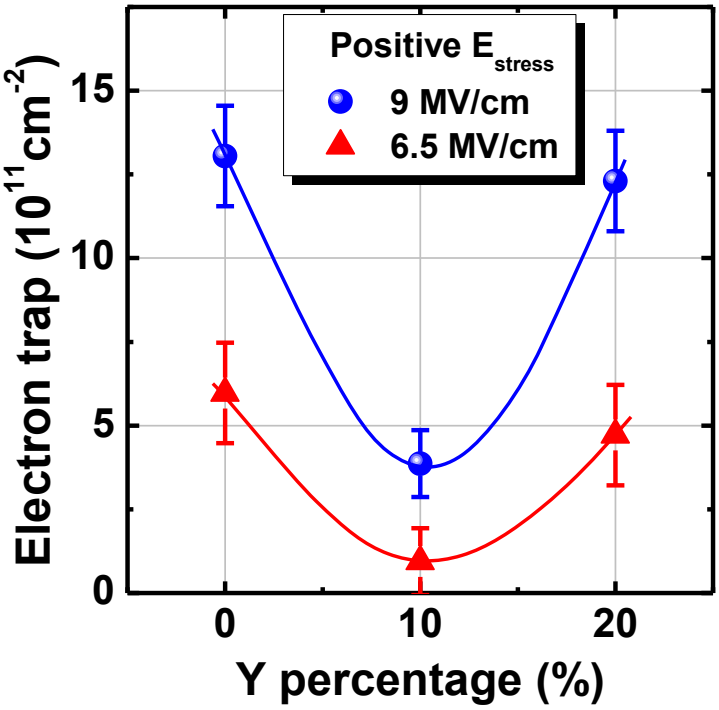
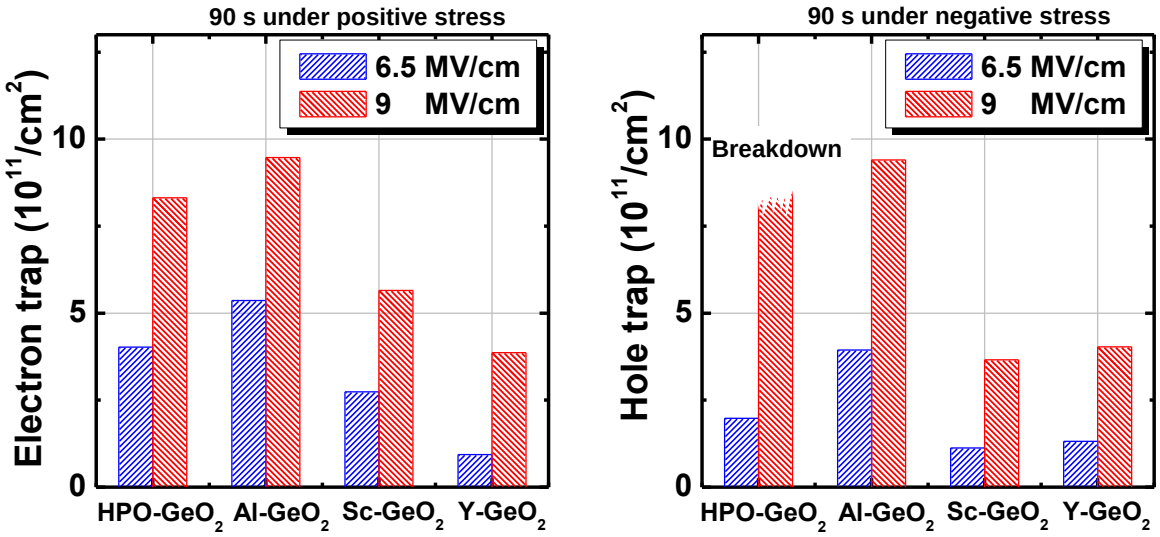


Figure 4.10 The newly generated electron trap density in Y-GeO_2/Ge stacks as a function of Y percentage under positive E_{stress}. Small amount of Y doping can drastically suppress the trap generation while high Y percentage degrades it again.

Figure 4.11 summarizes the trap generation under both positive and negative E_{stress} for HPO-GeO_2 and M-GeO_2/Ge stacks.[28] Note that the stress time was fixed at 90 sec for all the gate stacks. Traps are generated drastically in HPO-GeO_2/Ge stack regardless of its good initial characteristics and dielectric breakdown occurs immediately in HPO-GeO_2/Ge under 9 MV/cm negative E_{stress}. It is noted that only Y-GeO_2/Ge and Sc-GeO_2/Ge stacks significantly reduce the trap generation under both positive and negative E_{stress} comparing to that of HPO-GeO_2/Ge. On the other hand, Al-GeO_2/Ge stack does not suppress the trap generation.



(a) **(b)**

Figure 4.11(a) Electron trap generation calculated from the V_{FB} shift in HPO-GeO_2/Ge and M-GeO_2/Ge stacks under positive high E_{stress} (6.5 and 9 MV/cm). Note that the stress time is fixed at 90 sec for a fair comparison. **(b)** Electron trap generation in HPO-GeO_2/Ge and M-GeO_2/Ge stacks under negative E_{stress} calculated through the same way, while breakdown occurs rapidly in HPO-GeO_2/Ge stack under 9 MV/cm.[28]

The generated traps might also enhance the trap-assisted tunneling through the gate oxides, which results in the SILC after high E_{stress}.[4, 5] To investigate the SILC in HPO-GeO_2/Ge and M-GeO_2/Ge stacks, *I-V* characteristics before and after stress were compared. **Figure 4.12** shows the J_G of HPO-GeO_2/Ge and M-GeO_2/Ge stacks with different stress time under 9 MV/cm positive E_{stress}.[28] Though HPO-GeO_2/Ge stack shows the low initial J_G, it increases J_G a lot after the stress due to the SILC. Y-GeO_2 and Sc-GeO_2 show less SILC than HPO-GeO_2 and Al-GeO_2. The smaller SILC is a strong indication that Y-GeO_2 and Sc-GeO_2 stacks suppress the trap generation, which is in agreement with the less trap generation derived from the V_{FB} shift as shown in figure. 4.11. The low trap generation rate and the prominent initial properties favor Y-GeO_2/Ge and Sc-GeO_2/Ge gate stacks for long time device application.

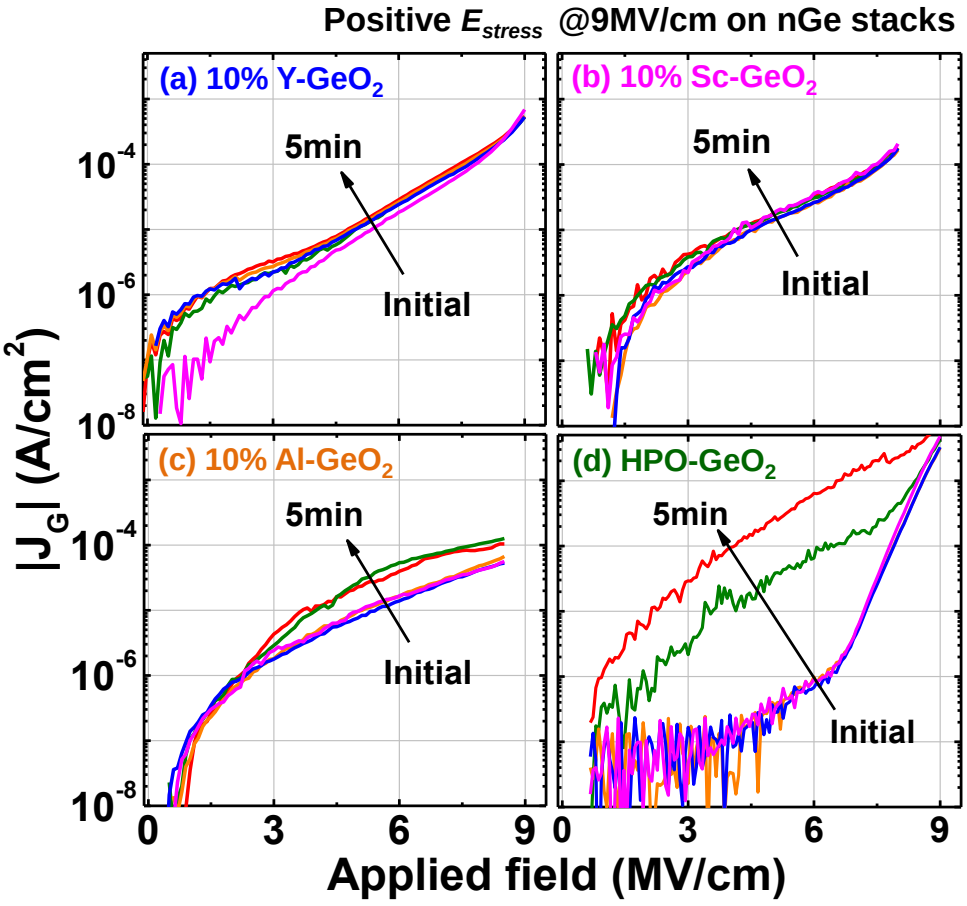


Figure 4.12 J_G in **(a)** Y-GeO_2/Ge, **(b)** Sc-GeO_2/Ge, **(c)** Al-GeO_2/Ge and **(d)** HPO-GeO_2/Ge stacks with different stress time at 9 MV/cm positive E_{stress}. Though HPO-GeO_2 shows low initial J_G, it increases a lot due to SILC. Y-GeO_2 and Sc-GeO_2 are stronger against SILC than HPO-GeO2 and Al-GeO_2. Note that the applied field in J_G measurement is also defined by V_{OX}/EOT.[28]

4.3.2 Interface degradation under high field

The interface degradation is one of the critical issues in the device reliability since it results in the reduction of G_m.[3] Under high E_{stress} field where traps are generated, it is concerned that the D_{it} might also be increased, which result into interface degradation. The D_{it} at HPO-GeO_2 and Y-GeO_2/Ge stacks are investigated by high-low-frequency-capacitance method before and after E_{stress}. **Figure 4.13** shows the

change of D_{it} at V_{FB} (E_i-0.2 eV or E_i+0.17 eV for the p-Ge or n-Ge, respectively) as a function of time under 9 MV/cm E_{stress} with both polarities. The D_{it} increase in HPO-GeO_2/Ge stacks is much larger than that of Y-GeO_2/Ge stacks regardless of their similarly low initial D_{it}. Thus, it is suggested that the Y doping is also effective for the reliability of the interface as well.

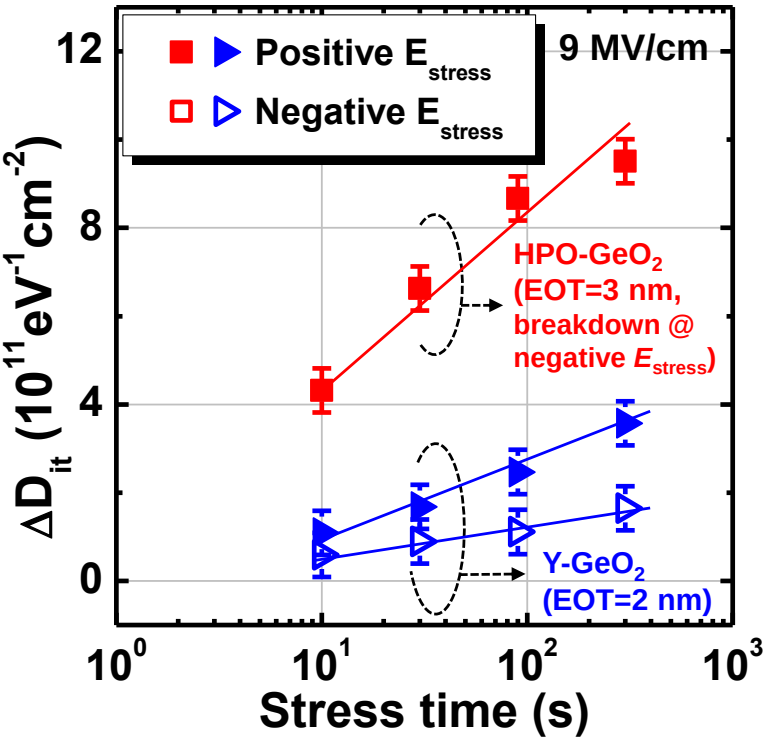


Figure 4.13 D_{it} at V_{FB} (E_i-0.2 eV or E_i+0.17 eV for the p-Ge or n-Ge, respectively) increase in HPO-GeO_2 and Y-GeO_2/Ge stacks as a function of time under positive or negative 9 MV/cm E_{stress}. Y-GeO_2 can suppress the D_{it} generation compared to that of HPO-GeO_2.

Though it has been assumed in the beginning of this chapter that trap generations in the investigated stacks are compared and analyzed based on thermochemical model, one might concern that, for the D_{it} increase, the definition of E_{stress} (V_{OX}/EOT) for different gate stacks is still a fare comparison condition or not. So, here, I would like to compare the D_{it} increase in different gate stacks by fixing the same E_{stress} or V_{OX}. **Figure 4.14** shows the D_{it}

at V_{FB} increase after 90 sec stress for HPO-GeO_2 and Y-GeO_2/Ge stacks as a function of **(a)** E_{stress} and **(b)** V_{OX}. Note that they are actually the same experimental data, which is just re-plotted versus different X-axis. It is noticed that for both plots, the advantage of Y-GeO_2 over that of HPO-GeO_2 can be confirmed. Therefore, it can be concluded that the better strength of Y-GeO_2 over HPO-GeO_2 against D_{it} degradation is valid from both field and voltage viewpoint.

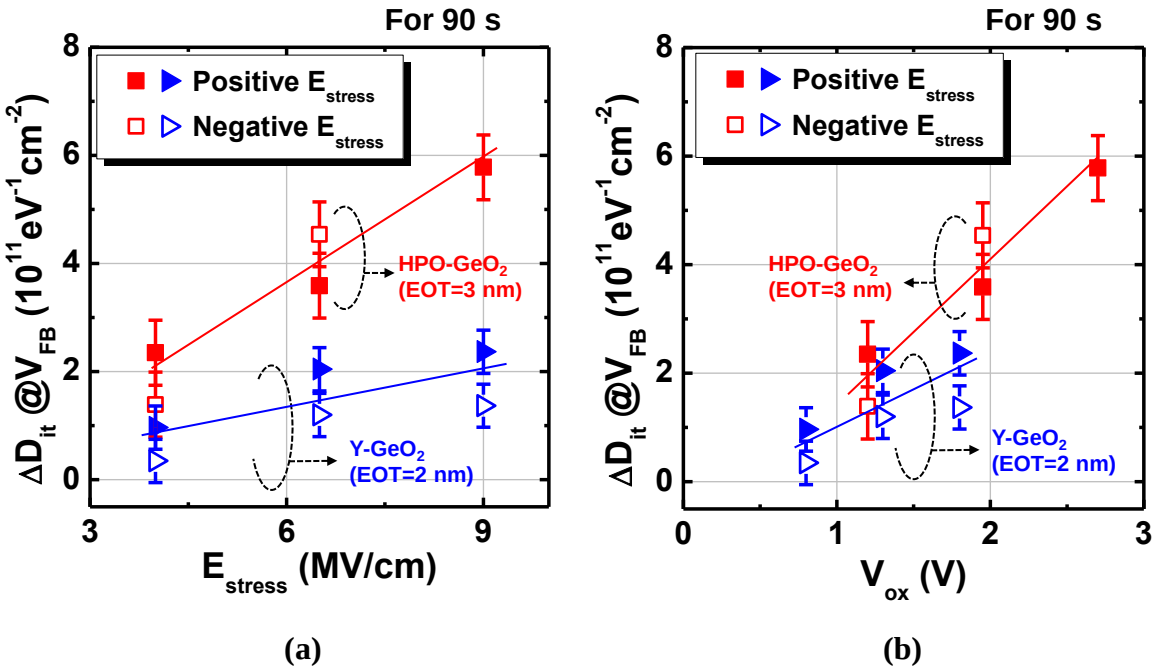


Figure 4.14 D_{it} at V_{FB} increase after 90 sec stress for HPO-GeO_2 and Y-GeO_2/Ge stacks as a function of **(a)** E_{stress} and **(b)** V_{OX}. The V_{FB} here is E_i-0.2 eV or E_i+0.17 eV for the p-Ge or n-Ge, respectively. Regardless of the X-axis, the smaller D_{it} generation in Y-GeO_2/Ge stack can be confirmed in the viewpoint of both E_{stress} and V_{OX}.

4.3.3 Guideline for controlling dielectric degradation

The thermochemical model has been quite successful in describing the reliability degradation of gate oxides with different k-values.[18, 20] From the thermochemical viewpoint, it is reasonable to expect that the trap generation is tightly related to the local bond breaking and consequent ion displacement by the local electric field in the oxides. To

understand the thermochemical model for trap generation in GeO_2, let us imagine an extreme situation, under which the trap generation continuously happens in the oxide until all the possible bonds are broken and ions are free to move under electric field (not a real situation because normally the dielectric will break down with many defects). In fact, under such an imaginary situation, the network of an oxide is dissociated into separated species again, which is similar to the thermal desorption and water etching as discussed in chapter 2. Therefore, in the thermochemical model, the trap generation process is the dissociation of an oxide network (partially dissociate), and the network rigidity becomes helpful again here to discuss the different dielectric degradation behaviors in different dielectrics. So here, I would employ the simple terms of the rigidity again for the dielectric degradation mechanism. Under a given E_{stress}, the rigidity are critical parameters for the bond breaking and ion displacement, respectively.[20] By assuming the ΔH_0 in equation 4.2 to be $-\alpha(N_{av}\times\gamma)$, the equation 4.2 can be written as follows,

$$r = r_0 \exp\left(-\frac{\alpha(N_{av}\times\gamma) - \mu \cdot E_{loc}}{k_B T}\right) \tag{4.3}$$

It can be inferred from this equation that, under a fixed E_{stress} condition, when the N_{av} of the dielectrics is increased, the trap generation rate would be reduced as well (assuming the γ and μ is not largely changed by higher N_{av}). Therefore, the higher N_{av} dielectrics can offer a smaller trap generation rate.

From a more microscopic viewpoint, GeO_2 has a weaker Ge-O single bond than SiO_2 counterpart,[29] which makes Ge-O bond highly susceptible to bond breaking under the same E_{stress}. Note that it stands true even a smaller external field was applied on GeO_2 because the higher k-value of GeO_2 (5.6) than that of SiO_2 (3.9) can enhance the E_{loc}. Since the N_{av} of GeO_2 is as low as 2.67, ion displacement and collapse of GeO_2 network readily occur when Ge-O bonds are broken as schematically shown in **Figure 4.15**.[28] On the other hand, a small amount of Y or Sc doping is expected to enhance the rigidity of the flexible GeO_2

network and suppress the trap generation, which is understandable from the MRN model as discussed in chapter 2.[30, 31] Small amount of Y or Sc doping exists as M^{3+} cation in GeO_2 network and forms many M-O bonds (7 and 6 for Y^{3+} and Sc^{3+}, respectively) with the nearest O^{2-} anions due to their large cation radii.[30, 31] Thus, the N_{av} necessarily increased to about 3 in Y-GeO_2 or Sc-GeO_2 (at 10% of Y or Sc) by the introduction of Y-O or Sc-O bonds. The suppression of ion displacement and network collapse are expected with the increase of N_{av} in the network,[20] therefore, the trap generation is reduced in Y-GeO_2 or Sc-GeO_2.

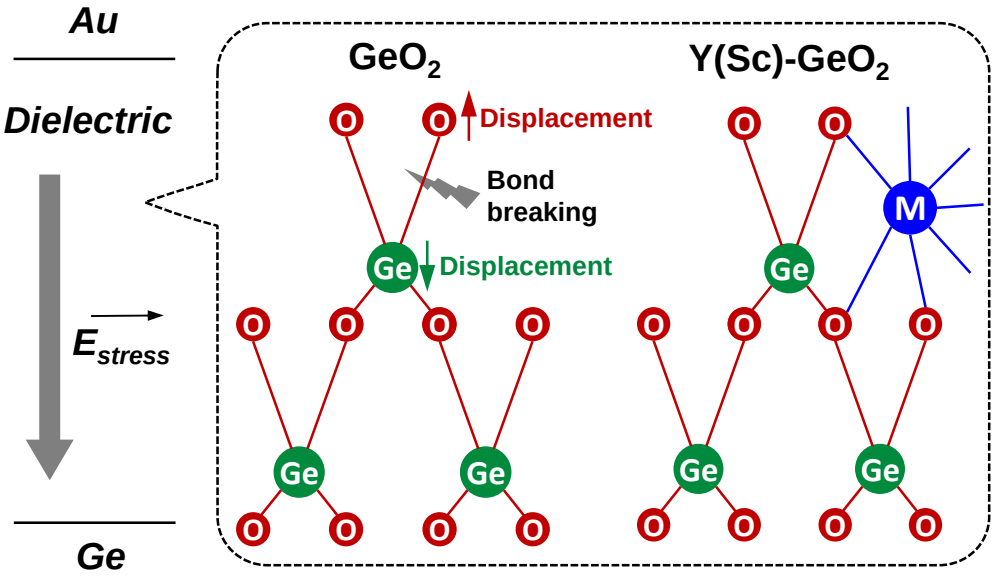


Figure 4.15 Schematic of GeO_2 network modification by Y or Sc doping (2-dimensional representation) and their influence on the ion displacement. The M-O bond number per cation is high for the doped M^{3+} in Y-GeO_2 and Sc-GeO_2,[30, 31] result in the higher N_{av} of the network. Under high E_{stress}, the local bond breaking and consequent ion displacement occur in GeO_2, while appropriate amount of additional M-O bonds enhance the rigidity of the network and suppress ion displacement.[28]

It is notable that, regardless of the prominent properties of 10% Y-GeO_2 and Sc-GeO_2, the rigidity enhancement effect is strongly dependent on both the concentration and the

species of doping. Excessive Y or Sc concentration in M-GeO_2/Ge stacks yields too high N_{av} value, which might lead to the over constrained network[26] and the immiscibility.[27] Contrary to the more rigid Y-GeO_2 and Sc-GeO_2 network, Al-GeO_2 has no observable influence on the trap generation. It is also understandable from the network viewpoint that, unlike Y or Sc, Al doping substitutes the Ge position in Ge-O_4 tetrahedron unit.[32] Thus, the strengthening effect from Al-O bonds is restricted locally in a single tetrahedron unit without changing the whole network properties. Some other cation like Hf^{4+} or La^{3+} easily forms M-Ge bonds at M-GeO_2/Ge interface as discussed in the chapter 2, which deteriorate even the initial interface properties of the gate stacks.

Since the rigidity enhancement effect of M-GeO_2 is also represented by the thermal stability against GeO desorption and water resistance as described in chapter 2, the fact that Y-GeO_2/Ge and Sc-GeO_2/Ge stacks have better thermal stability and lower water etching rate than GeO_2/Ge and Al-GeO_2/Ge stacks further supports the MRN model for explaining the reliability improvement. Thus, it can be concluded that the rigidity enhancement of GeO_2 by a proper amount of large cation doping is a striking strategy to improve the reliability of GeO_2.

To summarize the works in this section, the reliability assessment was carried out on HPO-GeO_2/Ge and M-GeO_2/Ge stacks. It is found that the initial Ge gate stack properties did not necessarily mean the high reliability robustness. Though both HPO-GeO_2/Ge and M-GeO_2/Ge stacks show promising initial electrical properties, the HPO-GeO_2/Ge stack suffers from significant V_{FB} shift, SILC increase and D_{it} degradation under high E_{stress} due to the trap generation in the gate oxides. Large cations like Y^{3+} or Sc^{3+} doping enhance the rigidity of GeO_2 network, which drastically reduced the trap generation under high E_{stress}. Thus, Y-GeO_2/Ge and Sc-GeO_2/Ge stacks show the prominent initial characteristics as well as remarkable reliability robustness.

4.4 Demonstration of reliability improvements in Ge gate stacks

Two important guidelines on the Ge gate stack reliability are established in the previous discussion. That is (1) the process condition should be well controlled to reduce the pre-existing hole traps and (2) the rigidity in the network of the dielectric should be enhanced to suppress the interface degradation and trap generation under high E_{stress} field. Both concept (1) and (2) are experimentally demonstrated by HPO-GeO_2 and Y-GeO_2, respectively. It is natural to consider what will be yield when both methods are combined together.

In this section, a (4 nm) Y-GeO_2/Ge gate stack is annealed in HPO at 500^{o}C conditions (HPO-Y-GeO_2/Ge) and the obtained gate stack is examined for reliability under both low and high E_{stress} field. It should be noted that very promising initial *C-V* curves are also obtainable in HPO-Y-GeO_2 on both n-Ge and p-Ge as shown in **Figure 4.16(a)** and **(b)** respectively. The thickness of the dielectric is not increased by the HPO annealing due to the strong oxidation barrier effect of Y-GeO_2 as discussed in chapter 2.

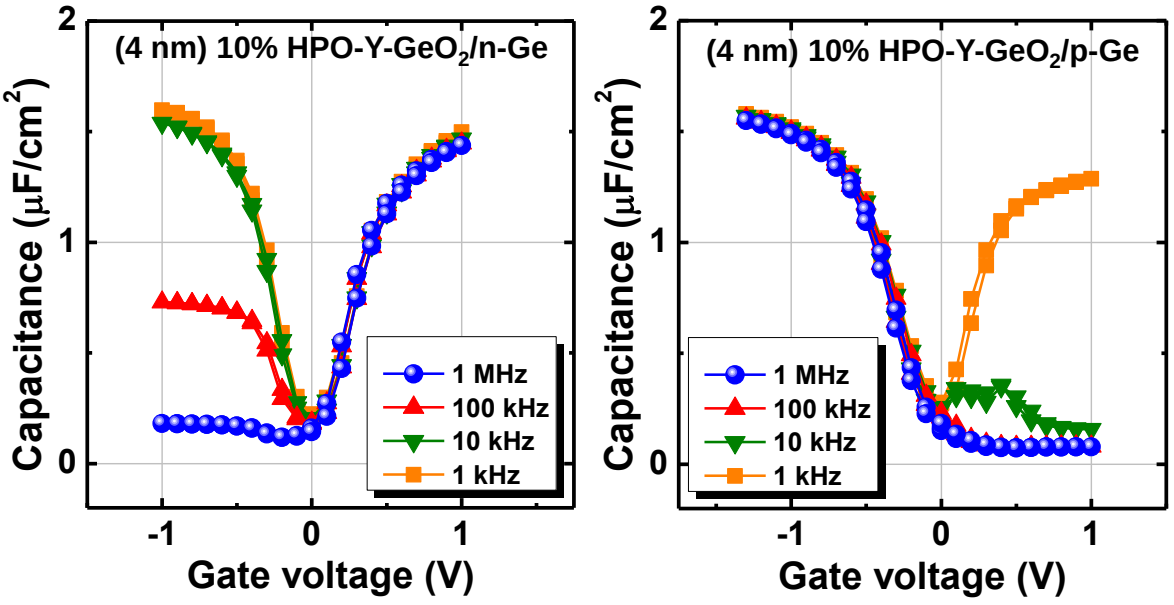


Figure 4.16 (a) Bidirectional *C-V* curves of an Au/10% HPO-Y-GeO_2/n-Ge MOSCAPs measured at RT. **(b)** Bidirectional *C-V* curves of Au/10% HPO-Y-GeO_2/p-Ge MOSCAPs.

Note that the thickness of HPO-Y-GeO_2 is 4 nm, which is the not changed by HPO annealing from the as deposited Y-GeO_2.

The V_{FB} shift of a HPO-Y-GeO_2/Ge stack as a function time under different E_{stress} is extracted from the *C-V* curves as shown in **Figure 4.17(a) and (b)** for positive and negative E_{stress}, respectively. It is found that the V_{FB} shift under low E_{stress} (4 MV/cm) is less than 10 mV even with long stress time, which indicates very low pre-existing both electron and hole trap density (below 10^{11} cm^{-2}). Under the high E_{stress} field (6.5 and 9 MV/cm), the trap generation in HPO-Y-GeO_2 is even smaller than that of the Y-GeO_2/Ge stacks (figure 4.11). The small V_{FB} shift in HPO-Y-GeO_2 indicates that very low pre-existing trap density and small trap generation can be obtained simultaneously in HPO-Y-GeO_2/Ge stack.

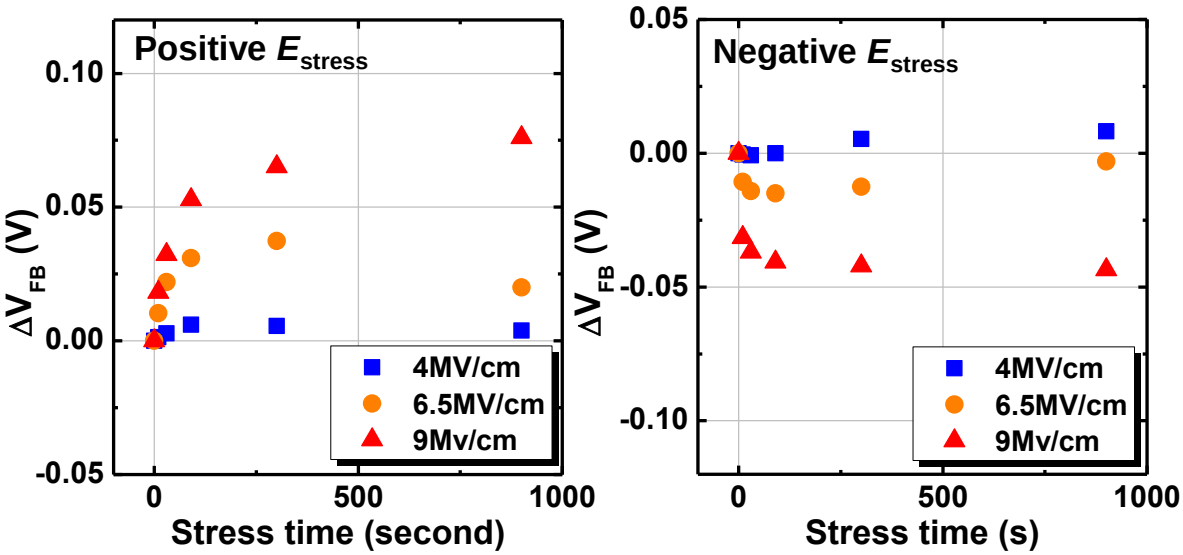


Figure 4.17 V_{FB} shift in HPO-Y-GeO_2/Ge stack as a function of stress time at various stress condition (4, 6.5 and 9 MV/cm of **(a)** positive and **(b)** negative E_{stress}). It is worth noting that the V_{FB} shift in this gate stack is the smallest among all the gates stacks discussed in this chapter.

The prominent reliability of HPO-Y-GeO_2 is also reflected from the SILC as shown in **Figure 4.18** for **(a)** positive and **(b)** negative E_{stress}, respectively. The HPO-Y-GeO_2/Ge gate stack shows both very low initial J_G and a negligible SILC after long stress time. The low initial J_G indicates a low pre-existing traps and the negligible SILC reflects a small trap generation. Both are in agreement with the observation from V_{FB} shift.

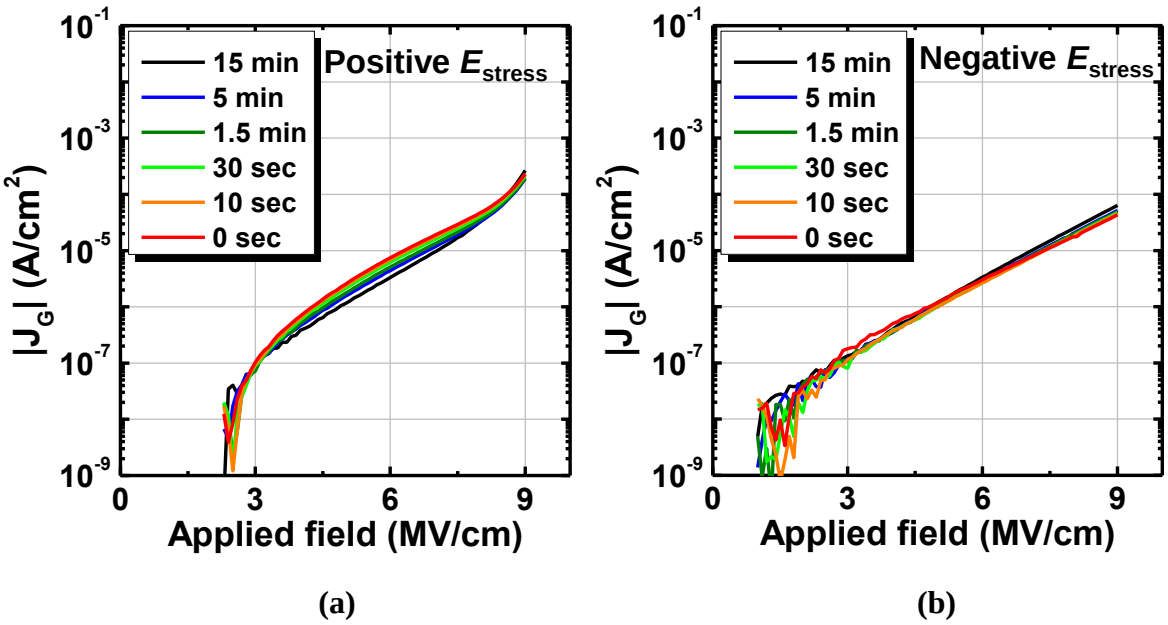


Figure 4.18 J_G (absolute value) in HPO-Y-GeO_2/Ge gate stack with different stress time at 9 MV/cm. The low initial J_G reflects that HPO-Y-GeO_2/Ge is an initially ideal gate dielectric. While the negligible SILC in this gate stack indicates its remarkably strong ability against trap generation.

The interface degradation of the HPO-Y-GeO_2/Ge gate stacks under E_{stress} is also examined. **Figure 4.19** shows the D_{it} increase at V_{FB} (E_i+0.17 eV and E_i-0.2 eV for n-Ge and p-Ge, respectively) as a function of time under both **(a)** positive and **(b)** negative E_{stress}. The E_{stress} here is 4, 6.5 and 9MV/cm and the thickness of HPO-Y-GeO_2 is 4 nm. The increase of D_{it} in HPO-Y-GeO_2/Ge gate stack is also negligible for both polarities, which is the also the smallest value among all the stacks discussed in the chapter. Thus it is confirmed that, by combining HPO and Y doping, the advantage of both can be acquired in

a same HPO-Y-GeO_2/Ge stack. And this gate stack is probably the most reliability GeO_2 based gated stack ever reported.

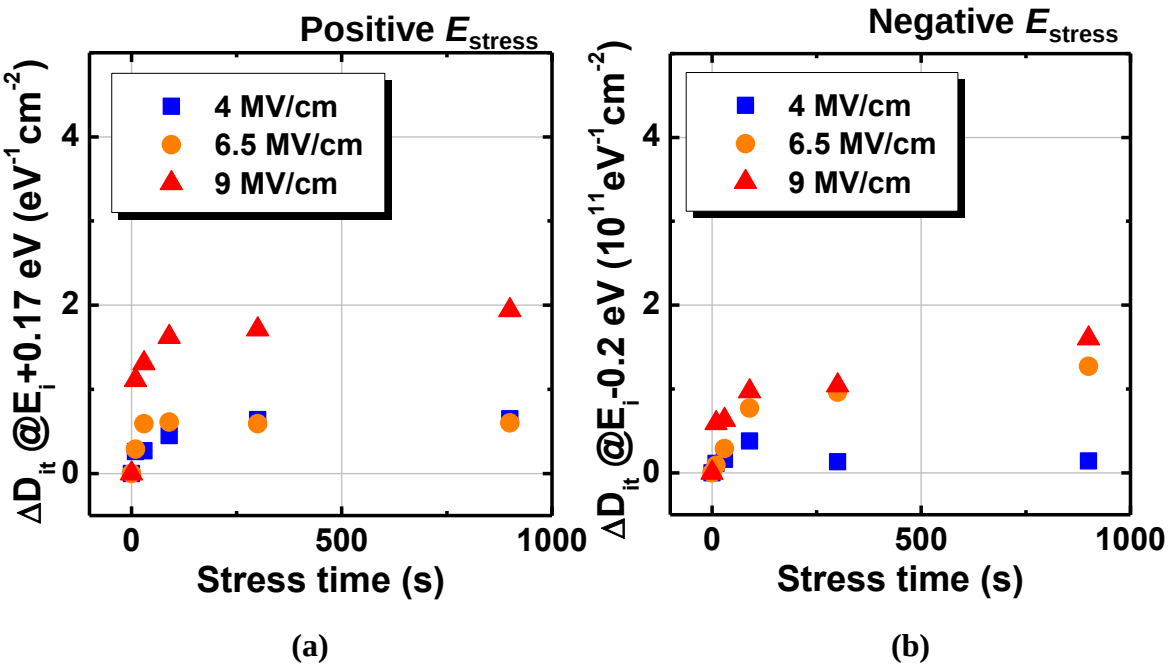


Figure 4.19 D_{it} change in HPO-Y-GeO_2/Ge stack as a function of stress time at various stress condition (4, 6.5 and 9 MV/cm of both polarities). The HPO-Y-GeO_2/Ge is also the strongest gated stack against interface degradation among all the stacks reported in this work.

4.5 Reliability assessment for sub-nm EOT Ge gate stack

In the discussion of previous sections, I have focused on the pre-existing trap and newly generation traps in GeO_2 and M-GeO_2/Ge gates stack, and found that Y or Sc-GeO_2 can improve the reliability in terms of both pre-existing traps and trap generation. In a sub-nm EOT gate stack, the GeO_2 based dielectrics are used only as an ultra-thin IL and real high-*k* dielectrics should be deposited on it. So in this section, by fixing the prominent Y-GeO_2 as IL, the reliability of sub-nm EOT stacks was investigated with $YScO_3$ as high-*k*. Again, HfO_2/Y-GeO_2/Ge stacks were also characterized as a comparison.

Beside the different interface properties in $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge stacks, it has also been found that the *C-V* hysteresis of these stacks is different, which might be related to the border or bulk traps in the gate stacks.[21, 33] **Figure 4.20** shows the *C-V* hysteresis of HfO_2/Y-GeO_2/Ge and $YScO_3$/Y-GeO_2/Ge stacks as a function of Y-GeO_2 IL thickness measured at room temperature. The results from the previous reports are also shown as comparison.[34, 35] It is found that $YScO_3$/Y-GeO_2/Ge stacks have obviously smaller hysteresis than that of HfO_2 counterpart (also smaller than the ref. 34, 35) at a given IL thickness, which indicates that the border or bulk trap densities are also lower in $YScO_3$/Y-GeO_2/Ge stacks in addition to its low D_{it}.

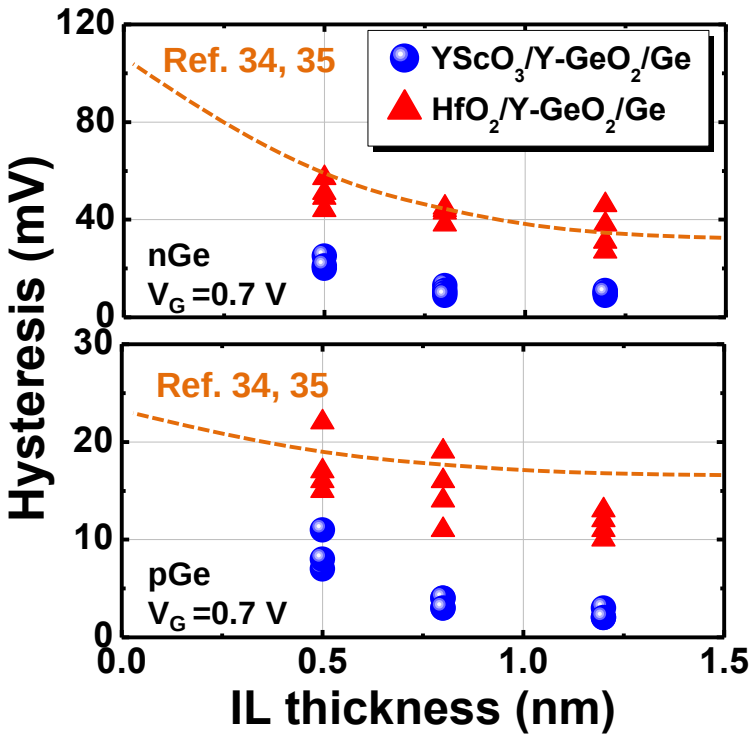


Figure 4.20 Hysteresis of the *C-V* curves in HfO_2/Y-GeO_2/Ge and $YScO_3$/Y-GeO_2/Ge stacks as a function of Y-GeO_2 IL thickness. The references show the hysteresis of the Ge gate capacitances with GeO_x as IL. [34, 35]

According to different hysteresis, the different trapping behaviors in $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge stacks are also expected. **Figure 4.21** shows the V_{FB} shift in HfO_2/Y-GeO_2/Ge and $YScO_3$/Y-GeO_2/Ge stacks as a function of time under high negative E_{stress} (V_G=1.5 and 2 V, E_{stress}=10 and 15 MV/cm), where the EOT was controlled to be 0.8 nm for both stacks. $YScO_3$/Y-GeO_2/Ge shows obviously smaller V_{FB} shift than HfO_2/Y-GeO_2/Ge stack, which reflects a lower trap density. The different trap densities might also be related to the different bond configurations described in section 2.4 of chapter 2.

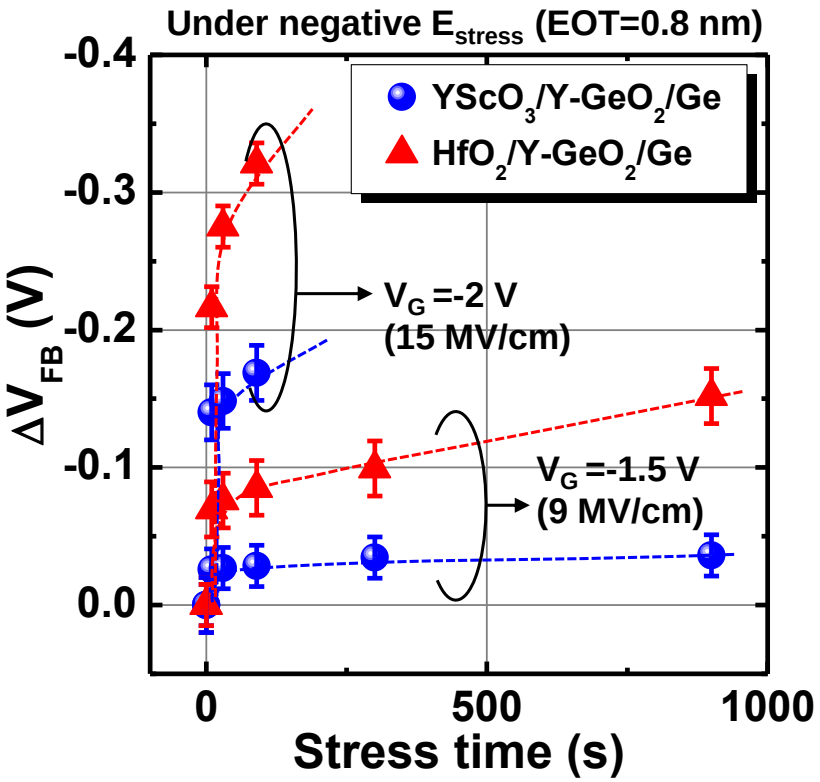


Figure 4.21 V_{FB} shift in HfO_2/Y-GeO_2/Ge and $YScO_3$/Y-GeO_2/Ge stacks (EOT=0.8 nm) as a function of time under high negative V_G (V_G=1.5 and 2 V, E_{stress}=10 and 15 MV/cm). The $YScO_3$/Y-GeO_2/Ge stacks show less V_{FB} shift than the HfO_2 counterpart at a fixed V_G and EOT.

The interface properties of $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge stacks are also examined as a function of stress time by high-low-frequency-capacitance method.

Figure 4.22 shows the D_{it} at E_i-0.2 eV of $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge gate stacks as a function of time under 9 MV/cm negative E_{stress}. The D_{it} of Y-GeO_2/Ge stack is also shown for comparison. $YScO_3$/Y-GeO_2/Ge stack has not only the similar initial D_{it} as that of Y-GeO_2/Ge stack, but also the similar D_{it} increment as a function of stress time. It is understandable that, with $YScO_3$ as high-k, the bond type or coordination numbers in the IL is not changed, thus, the reliability against D_{it} increase is also similar with Y-GeO_2/Ge interface. While, unexpectedly, HfO_2/Y-GeO_2/Ge stack shows both higher initial D_{it} and larger amount of D_{it} increase as a function of time under E_{stress}. It implies that some bond breaking at the interface might be enhanced by the initially existed defects.

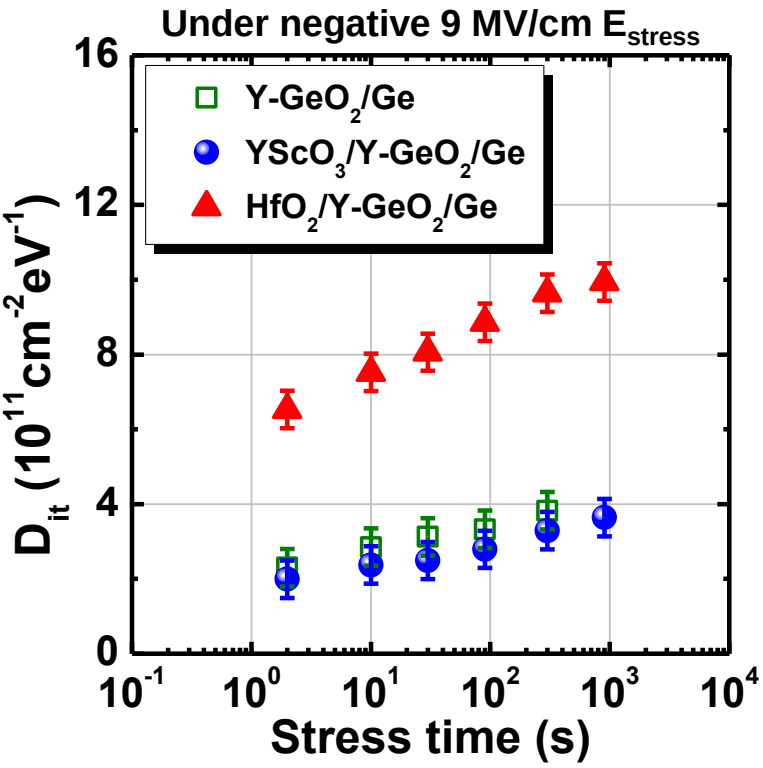


Figure 4.22 D_{it} at E_i-0.2 eV of $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge gate stacks as a function of time under 9 MV/cm negative E_{stress}. The D_{it} at Y-GeO_2/Ge stack is also shown for comparison.

The contrast between $YScO_3$ and HfO_2 in terms of reliability assessment further emphasizes the importance of high-*k* selection for device application, which is not only a vital parameter for initial interface property and EOT scalability, but also an important factor for reliability of long term device application.

In the final part of this section, the breakdown of $YScO_3$/Y-GeO_2/Ge (EOT 0.8 nm) and HfO_2/Y-GeO_2/Ge (EOT 0.8 nm) are roughly estimated. **Figure 4.23** shows the time to breakdown as a function of V_{OX} in $YScO_3$/Y-GeO_2/Ge (EOT 0.8 nm), HfO_2/Y-GeO_2/Ge (EOT 0.8 nm) and Y-GeO_2/Ge (EOT 2 nm) stacks. Thanks to the lower trap density, $YScO_3$/Y-GeO_2/Ge stacks can survive a much longer time than HfO_2/Y-GeO_2/Ge stacks under considerably high voltage.

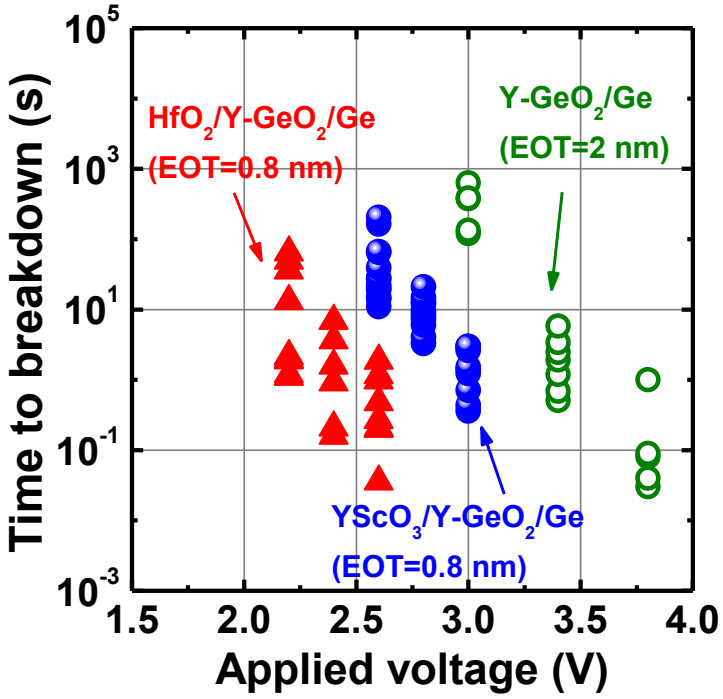


Figure 4.23 Time to breakdown as a function of E_{stress} in $YScO_3$/Y-GeO_2/Ge (EOT 0.8 nm), HfO_2/Y-GeO_2/Ge (EOT 0.8 nm) and Y-GeO_2/Ge (EOT 2 nm) stacks.

4.6 Summary

This chapter reports on the reliability assessment of Ge gate stacks with promising initial electrical properties, focusing on the pre-existing trap and trap generation under a constant E_{stress}. Initial Ge gate stack properties do not necessarily secure the high reliability robustness. It is found that the pre-existing hole traps are one of the most critical concerns in GeO_2/Ge gate stack, which might be attributed to the V_O formed during the gate stack process. The HPO-GeO_2 and M-GeO_2 can effectively reduce the V_O formation during the gate stack process, thereby reduce pre-existing hole trap density.

However, under an elevated stress field, the trap generation becomes a major concern regardless of the initial properties because Ge-O bond are highly susceptible to bond breaking and ion displacement by electric field. Small amount Y-GeO_2 or Sc-GeO_2 significantly reduces the trap generation in Ge gate stacks without the interface deterioration. This result is understandable from the increase of average coordination number (N_{av}) in the modified GeO_2 network by doping.

The reliability of sub-nm EOT $YScO_3$/Y-GeO_2/Ge and HfO_2/Y-GeO_2/Ge gate stacks are also examined. The selection of top high-k dielectric also has a significant impact on the reliability degradation. $YScO_3$/Y-GeO_2/Ge shows better long term reliability thanks to its defect free characteristics.

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Chapter 5

Conclusions and future outlook

5.1 The conclusion and achievements in this work

5.2 Future outlook

5.1 The conclusion and achievements in this work

Ge has been brought back to future again by the recent decade of researches[1-4] long after its first demonstration as MOSFET. The ultimate driving force of this Ge revival is the conflict between the technology limitations of Si and the relentless requirements on better device performance.[5,6] Ge is not the only candidate as the high mobility channel material, but it is probably the most feasible one for a symmetric c-MOS application.

The research interest on Ge MOSFET has been largely concentrated on the gate stack formation and interface passivation because the poor interface passivation was the bottle neck of the device application, especially n-MOSFET.[7] It was not until recently that researchers really understand how to prepare well passivated Ge interface by a high quality GeO_2 layer,[1-3] which becomes the starting point and premise of this work.

However, further steps are to be taken before the Ge device application becomes commercially available in a real scene. Three of these most critical challenges are discussed in this work, namely, (1) the thermal and chemical robustness of the Ge gate stack. (2) the EOT scaling of the gate stack by high-k and (3) the reliability improvement for long term application. More importantly, all of these challenges should be addressed with maintaining a promising interface passivation.

To achieve these goals, the designing of new dielectric materials are needed rather than a simple optimization of the device process, because the aforementioned challenged are dominated by the intrinsic properties of dielectric/Ge. It is proposed in this work that the structure of the dielectrics might be the most critical intrinsic parameter which determines the interface passivation, thermal stability, scalability and reliability of MOS device. It is also found that the structural parameters might be changed in a way to improve the above properties by mixing the suitable oxides.

Following this material consideration, metal oxide doped GeO_2 (M-GeO_2) was proposed to substitute GeO_2 as robust IL for Ge passivation. Drastic improvements in thermal and chemical stability were obtained with very promising interface passivation on Ge by small amount of suitable doping like Y or Sc. It is because that Ge gate stack robustness is strongly dependent on the rigidity of a dielectric network, and the improvement of which is attainable by increasing the bond number (N_{av}) through metal oxide doping.

The structural manipulation approach is also applicable on the formation of the high-*k*. A promising ternary high-*k* $YScO_3$ is proposed by mixing two medium-*k* binary components. The key point is the scandate formation of ternary oxides, in which a small cation radius Sc can enhance the density (reduce molar volume). This has lead us to the successful results, in spite of the fact that both binary oxides have medium-*k* values. $YScO_3$ is found to be a good example of desirable high-*k* material on Ge due to its interface aware character and a high permittivity about 17. Based on these understandings, EOT scaling to about 0.5 nm was demonstrated by $YScO_3$/Y-GeO_2/Ge gate stacks with promising interface properties.

Finally, the relationship between dielectric structure and reliability projection of Ge MOS device is discussed in detail. It is found that, under low E_{stress}, the pre-existing hole traps are the major concern for GeO_2/Ge based device, and the reduction of V_O by HPO can reduce the hole traps. While, under high E_{stress}, the network rigidity was found to play an important role in the reliability degradation of Ge gate stacks. Strong network material like Y-GeO_2 offers much less interface degradation and trap generation comparing to that of GeO_2. Furthermore, the advantage of $YScO_3$ over HfO_2 in terms of reliability in sub-nm EOT Ge gate stack is also observed.

The key word here concerning a desirable gate dielectric on Ge is a suitable rigidity of the network. Though the very flexible GeO_2 network offers good interface passivation, it is unsatisfying in various other points. While, by slight enhancement of the rigidity, the thermal stability, scalability and reliability can be improved without the cost of interface property.

This work offers an alternative future for Ge MOS device research. The most important philosophical point is that, the native oxide, GeO_2, is not the only (also not the best) solution for Ge passivation. And, the better properties of the newly designed materials than GeO_2/Ge convince us that the desirable materials for MOS are not given to us by luck, but are artificially controllable by knowledge.

5.2 Future outlook

This work has successfully overcome the technical requirements on the Ge MOS device process and initial properties. It has also given the first understanding on the Ge MOS device reliability control from the material viewpoint. However, for the device application in a real scene, the reliability properties of Ge MOS are still not satisfying. The further improvement of material and process are needed to reach the technical requirements on the long term reliability. This might be the last obstacle of commercial use of Ge device.

The knowledge of the Ge gate stack formation obtained in this work has demonstrated a significant impact on the MOSFET operations in a planer structure device. While for further device applications, this gate stack design could be further examined on various MOSFET structures, such as FinFET or 3D-intergrations. The application of this work on the various kind of MOSFET device structure would bring

more significance and impact from this work to the semiconductor application.

Finally, the application of this knowledge on the gate stack formation of other semiconductor materials would also be an interesting challenge. It is known that, besides Ge, other new semiconductor materials are also investigated in substitute of Si like SiGe, SiC, GeSn and group III-IV materials. Though the gate dielectrics for these semiconductors must be different with that for Ge, the knowledge obtained here might also help to select the desirable gate dielectrics for the other semiconductors. Especially the consideration on the network rigidity, which might be a universal criteria for the dielectric selection for various kinds of semiconductors.

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List of publications

A. Original papers for journal with peer review

1) **C. Lu**, C. H. Lee, T. Nishimura, and A. Toriumi, "Yttrium Scandate Thin Film as Alternative High-permittivity Dielectric for Germanium Gate Stack Formation" *Applied Physics Letters*, **107,** 072904 (2015)

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B. **Proceedings for international conferences with peer review**

1) **C. Lu**, and A. Toriumi, "Structural Coordination of Rigidity with Flexibility in Gate Dielectric Films for Sub-nm EOT Ge Gate Stack Reliability", IEEE International Electron Device Meeting (*IEDM*) (2015, To be presented in Washington)
2) **C. Lu**, C. H. Lee, T. Nishimura, and A. Toriumi, "Beyond GeO_2 on Ge: Network Modification of GeO_2 for Reliable Ge Gate Stacks", *International Conference on Solid State Devices and Materials (SSDM)*, (2015, To be presented in Sapporo)
3) **C. Lu**, C. H. Lee, T. Nishimura, and A. Toriumi, "Design and Demonstration of Reliability-aware Ge Gate Stacks", Symposium on VLSI Technology (*VLSI*) (Jun. 2015, Kyoto)
4) **C. Lu**, C. H. Lee, T. Nishimura, K. Nagashio, and A. Toriumi, "Interface Friendly High-k Dielectrics for Sub-nm EOT Gate Stacks Formation on Germanium," *45th IEEE Semiconductor Interface Specialists Conference (SISC),* (Dec. 2014, San Diego)
5) **C. Lu**, C. H. Lee, T. Nishimura, K. Nagashio, and A. Toriumi, "Impact of $YScO_3$ on Ge Gate Stack in Terms of EOT Reduction as well as Interface Control," *International Conference on Solid State Devices and Materials (SSDM),* pp. 708, (Sept. 2014, Tsukuba)
6) **C. Lu**, C. H. Lee, W. Zhang, T. Nishimura, K. Nagashio, and A. Toriumi, "Thermodynamically Controlled GeO_2 by Introducing M_2O_3 for Ultra-thin EOT Ge Gate Stacks," *MRS Spring Meeting*, (Apr. 2014, San Francisco)

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13) ***(Invited paper)*** A. Toriumi, C. H. Lee, **C. Lu**, and T. Nishimura, "High Electron Mobility n-Channel Ge MOSFETs with Sub-Nm EOT," *The 225th Electrochemical Society Meeting (ECS)*, (Oct 2014, Cancun).

14) ***(Invited paper)*** C. H. Lee, T. Nishimura, **C. Lu**, W. Zhang, K. Nagashio, and A. Toriumi, "Significant Enhancement of High-N_s Electron Mobility in Ge n-MOSFETs with Atomically Flat Ge/GeO_2 Interface," *The 225th Electrochemical Society Meeting (ECS)*, (May 2014, Orlando).

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C. Domestic conference (Japan)

1) **C. Lu**, C. H. Lee, T. Nishimura, K. Nagashio, and A. Toriumi, "Network Modification of GeO_2 by Trivalent Metal Oxide Doping," *The 61st Spring Meeting of Japan Society Applied Physics (JSAP)*, 20a-F10-10 (Mar. 2014, Sagamihara)

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