論 文 の 内 容 の 要 旨

論文題目　The Effects of Variability on Write Stability in SRAM at Low Supply Voltage
（低電圧SRAMにおける特性ばらつきの書き込み安定性への影響）

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Static random access memory (SRAM) acts as the buffer role in pyramid-like memory hierarchy to compensate the speed gap between processors and bottom-level memories. Targeting a larger capacity of SRAM arrays with higher performance and lower cost, both designers and manufacturers are driving efforts to minimize the footprint of SRAM cells. Also, both active energy and leakage power considerations make operating voltage scaling significantly compelling for SRAM. However, continued increase in variability consisting of time-zero and time-dependent variability is perceived to be a major roadblock for future operating voltage scaling. Thus, variability analysis in SRAM becomes critical for both gaining a deeper understanding of the sources of variability and for developing more robust circuits.

By adopting the intrinsic channel, silicon-on-Thin-BOX (SOTB) – in other words, fully-depleted (FD) silicon-on-insulator (SOI) – technology eliminates large time-zero variability from random dopant fluctuations (RDF) in CMOS bulk one. The immunity to RDF also helps suppress the impact of random telegraph noise (RTN). The big innovation facilitates the experimental demonstration of low-power SOTB SRAM cells operable down to sub-0.4 V regime. Considering the limited data to date, this work presents a comprehensive variability analysis on write stability in SRAM at low V_{DD} based on SOTB technology platform.

Firstly, four commonly used write stability metrics – including write static noise margin (WSNM) from write butterfly curve, I_W from write N-curve, bit-line margin (BLM) from bit-line method and combined word-line margin (CWLM) from word-line method – are compared in order to select the good candidate for write yield estimation at low V_{DD}. The core standard is that the selected one follows good normality and can correctly predict write failure. Bit-line method and word-line method are concluded as good candidates for write yield estimation at low V_{DD}. On the other hand, the non-normality of WSNM and I_W is clarified and ascribed to sub-V_{th} operation of cell transistors at low V_{DD}. HSPICE simulation results help extend our conclusions up to ±6 sigma.

Besides, a new write stability metric is proposed for write yield estimation. The extended write butterfly curve extends the voltage sweeping range of conventional write butterfly curve. Due to the clearer emergence of failure mode, the extended write noise margin (E-WSNM) shows good normality and is demonstrated as a good metric for write yield estimation. More evidence is also given to support the newly proposed one.

Lastly, a statistical model is developed to evaluate the impact of time-dependent RTN in SRAM at low V_{DD}. I_W from write N-curve is selected as the write stability metric due to its being current-based one. Based on the distribution fitting of both I_W and RTN-induced fluctuation (δI_W), the degradation due to RTN on fail bit rate (FBR) is discussed. It is found that RTN degrades V_{min} – the minimum voltage which guarantees stability of the whole capacity of SRAM arrays – over 10 % in sub-0.4 V regime, thus emphasizing the importance of RTN for low-power SRAM design.

Overall, our conclusions are not limited to SOTB technology but are applicable to other technologies such as FinFET SRAM, and give implications to SRAM design at low V_{DD}.