Operation Analysis of Steep-Subthreshold-Slope PN-Body-Tied SOI FET

（急峻サブスレッショルドスロープ PN-Body-Tied SOI FETの動作解析）

by

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Abstract

Today, increasing difficulty in suppressing power dissipation of metal-oxide-semiconductor field-effect transistors (MOSFETs) jeopardizes the continuance of improving the performance of complementary MOS (CMOS) very-large-scale integration (VLSI) circuits. Subthreshold slope (SS) requires to be reduced for suppressing power dissipation, but the SS of conventional MOSFETs has a lower boundary of 60 mV/decade at room temperature. For this reason, a variety of new steep-slope devices are studied to replace conventional MOSFETs.

The recently proposed silicon-on-insulator (SOI) MOSFET with a special PN body tie, i.e., PN-body-tied SOI FET (PNBTFET) shows an extremely steep SS with an ultralow drain voltage. Thus, PNBTFET is a promising candidate to replace the conventional MOSFETs. However, the operation mechanism of PNBTFET is not fully understood; therefore, it is difficult to design PNBTFETs optimum for low-power operation.

We pay attention to the PNPN structure with a MOS gate, i.e. MOS-gated thyristor (MGT), which is built in PNBTFET and plays a significant role in realizing a steep SS in PNBTFET. MGT has abrupt switching behavior, but its operation principle was also not clear.

We proposed a new equivalent circuit model, which consists of two cross-coupled voltage inverters, i.e., electron current inverter (ECI) and hole current inverter (HCI), into which the complex feedback system of MGT is resolved. The voltage responses of the two inverters graphically describe the behavior of the equivalent circuit model, which agrees with that of MGT.

The effects of design parameters on the equivalent circuit model and corresponding MGT are examined by 2-dimensional TCAD simulation and show good correlation. It is demonstrated that the parameter dependence of the equivalent circuit model provides a clear guide in designing MGTs with low threshold voltages and small hysteresis width. The equivalent circuit model provides intuitive understanding of the operation mechanism of MGT, and will be greatly helpful in deigning ultralow-power PNBTFETs.

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Contents

Chapter 1

Introduction

1.1 Background

Over the last half century, the electronics industry has made great advance thanks to the continuous, exponential improvement of complementary metal-oxide-semiconductor (CMOS) very-large-scale integration (VLSI) circuits. The metal-oxide-semiconductor field-effect transistor (MOSFET), which is the basic unit of CMOS circuits, has been scaled down according to Moore's law, in which the number of transistors in a chip doubles every 2 years. International Roadmap for Devices and Systems (IRDS) forecasts that the gate length for logic transistors will be scaled down to 14 nm in 2019[1]. The performance booster for long-channel MOSFETs is Dennard's scaling theory[2], where the dimensions and the supply voltage are scaled down by a constant factor of $1/\kappa$ and the doping concentration is increased by a factor of κ, resulting in reducing circuit delay by a factor of $1/\kappa$ and increasing circuit density by a factor of κ^2 with power density maintained.

Today, however, MOSFET has a problem of increasing power dissipation as the size is scaled down, so further performance improvement of CMOS VLSI circuits is a serious

challenge. To suppress power dissipation in a MOSFET, it is essential to reduce the supply voltage by the same rate as downscaling of the device dimensions and the doping concentrations according to Dennard's scaling rule. The threshold voltage should also be reduced with the supply voltage to maintain the on drain current I_{on} and the speed of CMOS circuits. Nevertheless, the off drain current I_{off} increases exponentially as the threshold voltage falls, hence the standby power dissipation increases exponentially. Therefore, there is a trade-off between the standby power dissipation and the circuit speed. IRDS stated that it is severe to reduce supply voltage when it approaches 0.6 V[1].

To overcome the trade-off between power dissipation and circuit speed, the subthreshold slope (SS) must be made smaller. SS is defined as

$$S \equiv \left(\frac{d \log_{10} I_D}{dV_G} \right)^{-1}, \tag{1.1}$$

where I_D is the drain current, and V_G the gate voltage[3, 4]. SS represents the inverse slope of $(\log_{10} I_D)$-V_G curve; therefore, small SS means steep $(\log_{10} I_D)$-V_G curve. If SS is small, it is possible to reduce the supply voltage without degrading I_{on}/I_{off} ratio.

In fact, conventional MOSFETs have a fundamental lower limit to SS of 60 mV/decade at room temperature, so there is limitation on reducing the power dissipation in a MOSFET. At a gate voltage below the threshold voltage (i.e., in the subthreshold region), minority carrier diffusion is dominant in the drain current of a MOSFET. SS in a MOSFET is given as

$$S = \ln(10) \frac{mkT}{q}, \tag{1.2}$$

where

$$m = 1 + C_D/C_{ox}, \tag{1.3}$$

is a factor greater than unity, and C_D and C_{ox} are capacitance of the depletion layer and the gate oxide layer, respectively[4]. Equation (1.2) indicates that SS of conventional MOSFETs cannot be reduced below $2.3kT/q$, or 60 mV/decade at room temperature.

To substitute conventional MOSFETs, a variety of new switching devices, such as tunnel FET (TFET)[5, 6], negative capacitance FET (NCFET)[7, 8, 9], impact ionization FET (I-MOS)[10, 11], feedback FET[12, 13], CxFET[14], Z^2-FET[15], are studied. Such devices utilize special mechanism to realize a steep SS of less than 60 mV/decade. For example, TFET uses band-to-band tunneling, NCFET uses negative capacitance in a ferroelectric insulator, and I-MOS uses impact ionization to cause avalanche breakdown. However, none of these steep-SS devices has reached the point to surpass conventional MOSFETs for various problems: TFET has low I_{on}/I_{off} owing to high tunnel resistance; I-MOS requires high drain voltage to induce impact ionization.

1.2 Objective of This Work

In this thesis, the author focuses on the newly proposed steep-SS device, i.e., PN-body tied silicon-on-insulator (SOI) FET (PNBTFET), which shows a supersteep SS of less than 6 mV/decade even at an ultralow drain voltage of 0.1 V[16, 17, 18, 19].

The objective of this work is to analyze the operation mechanism of PNBTFET for designing PNBTFETs with optimum characteristics for low-power operation. PNBTFET has many design parameters owing to the additional PN body tie structure, but the effects of the design parameters on PNBTFET characteristics are not clear. To analyze PNBTFET, we concentrate on a partial structure in PNBTFET, i.e., MOS-gated thyristor (MGT), and propose a new equivalent circuit model of MGT, which provides an insight into MGT and PNBTFET operation by simplifying the complicated feedback system of MGT.

1.3 Chapter Organization

This thesis consists of 5 chapters. Following chapters are organized as follows.

- Chapter 2 reviews the previous study on PNBTFET, and focuses on MGT, which is the key to analyzing the operation of PNBTFET.

- Chapter 3 describes our modeling approach that analyzes the operation mechanism of PNBTFET. The behavior of the proposed model is discussed using TCAD simulation and simple analytical equations.

- Chapter 4 compares the simulation results of MGT and the equivalent circuit model described in Chapter 3. The effects of design parameters and the thermal stability are examined and discussed. These results provide a clear guide in designing MGTs with optimum characteristics for low-power PNBTFETs.

- Chapter 5 summarizes the thesis achievements.

References

[1] International Roadmap for Devices and Systems 2016 Edition.

[2] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, IEEE J. Solid-State Circuits **9** [5], 256 (1974).

[3] S. M. Sze and M. K. Lee, *Semiconductor Devices — Physics and Technology* (John Wiley & Sones Inc., New York, 2012) 3rd Edition.

[4] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 2009) 2nd Edition.

[5] A. M. Ionescu and H. Riel, Nature **479**, 329 (2011).

[6] A. C. Seabaugh and Q. Zhang, Proc. IEEE **98**, 2095 (2010).

[7] S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008).

[8] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, IEDM Tech. Dig., 2011, p. 255.

[9] M. Kobayashi, and T. Hiramoto, AIP Advances **6**, 025113 (2016).

[10] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, IEDM Tech. Dig., 2002, p. 289.

[11] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, IEEE Trans. Electron Devices **52**, 69 (2005).

[12] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T. J. King Liu, IEDM Tech. Dig., 2008, p. 1.

[13] Y. Jeon, M. Kim, Y. Kim, and S. Kim, ACS Nano **8**, 3781 (2014).

[14] D. Hisamoto, S. Saito, A. Shima, H. Yoshimoto, and K. Torii, IEEE Silicon Nanoelectronics Workshop (SNW), 2012, p. 1.

[15] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, Proc. Tech. Program of 2012 VLSI Technology, 2012, p. 1.

[16] J. Ida, T. Mori, Y. Kuramoto, T. Horii, T. Yoshida, K. Takeda, H. Kasai, M. Okihara, and Y. Arai, IEDM Tech. Dig., 2015, p. 624.

[17] T. Yoshida, J. Ida, T. Horii, M. Okihara, and Y. Arai, Proc. IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S), 2016, p. 1.

[18] T. Horii, J. Ida, T. Yoshida, M. Okihara, and Y. Arai, Proc. of IEEE Silicon Nanoelectronics Workshop (SNW), 2016, p. 148.

[19] T. Yoshida, J. Ida, S. Inoue, S. Uchikura, A. Hashimoto, K. Hayashi, T. Iwasaki, M. Kamako, and T. Horii, IEEE Electron Devices Technology and Manufacturing Conf. (EDTM) Proc. Tech. Pap., 2017, p. 75.

Chapter 2

PN-Body-Tied SOI FET and MOS-Gated Thyristor

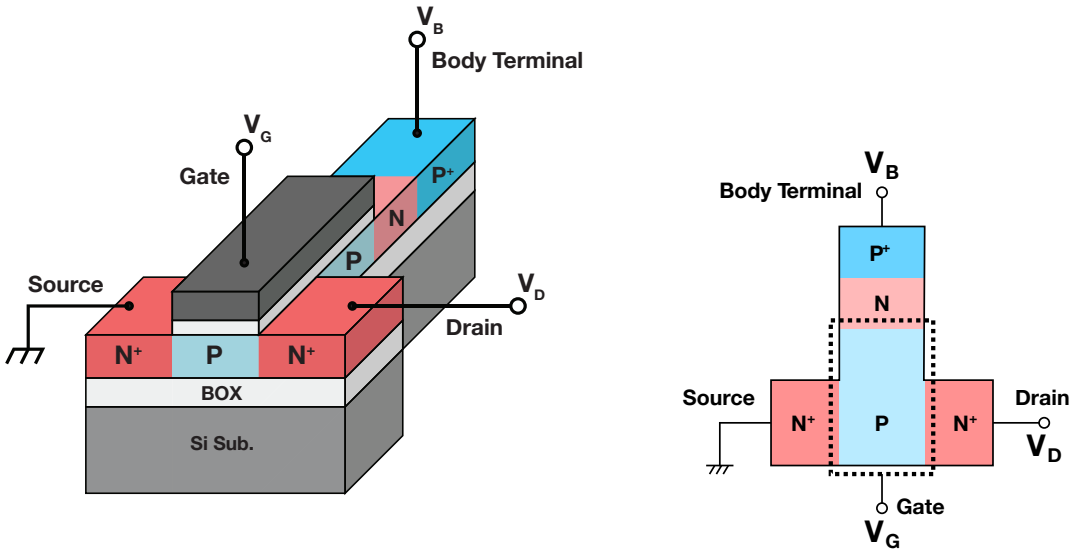
2.1 Introduction

In Chapter 2, the previous work on the PN-body-tied silicon-on-insulator (SOI) FET (PNBTFET) conducted by Ida's group is reviewed. PNBTFET is a steep-SS device which operates at an ultralow drain voltage. Moreover, the partial structure in PNBTFET, i.e., MOS-gated thyritor (MGT) is explored. MGT is important because it is the cause of a supersteep SS in PNBTFET.

2.2 PN-Body-Tied SOI FET

PNBTFET is a new steep-SS device proposed by Ida's group in 2015[1]. An extremely steep SS less than 6 mV/decade at a very low drain voltage of 0.1 V is confirmed both in the simulation[1] and experiment[2]. For this reason, PNBTFET is a promising candidate to replace conventional MOSFETs.

2.2.1 Structure and Electrical Characteristics



(a) (b)

Figure 2.1: Schematic (a) bird's-eye view and (b) plain view of PNBTFET. PNBTFET is an SOI MOSFET whose floating P-type body is connected to the body terminal via a PNP diode. The source is grounded, and the drain and the body terminal are applied constant positive voltage.

Figure 2.1 shows the structure of PNBTFET. PNBTFET is fabricated on an SOI substrate, and has a gate, source, and drain as well as conventional SOI MOSFETs. The entire device is insulated from the silicon substrate by the buried oxide (BOX) layer. In addition, PNBTFET has a special body tie structure with a N region and P^+ region, which is connected to the body terminal. Thus, PNBTFET has a 3-dimensional structure.

PNBTFET requires the source to be grounded, and a positive drain voltage V_A and a positive body terminal voltage V_B are applied. PNBTFET turns on when the gate voltage V_G is sufficiently high, and turns off when V_G is sufficiently low. The difference between MOSFET and PNBTFET is that PNBTFET requires the additional body terminal voltage (V_B).

As shown in Fig. 2.2, PNBTFET shows an abrupt SS of less than 6 mV/decade even at $V_D = 0.05$ V[1]. I_D increases abruptly at a certain V_G value around 0.3 V, and the abrupt

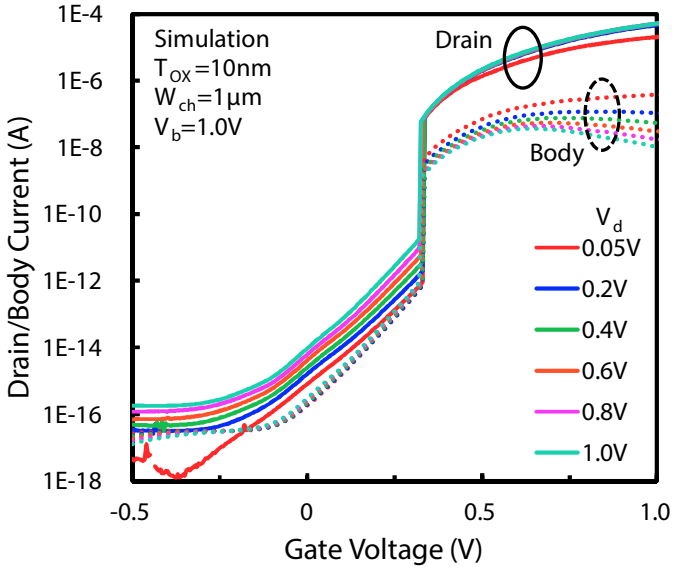


Figure 2.2: Simulated I_D-V_G characteristics at various V_D values[1]. The body terminal current I_B vs. V_G is also shown. I_D and I_B surge at a certain V_G value around 0.3 V.

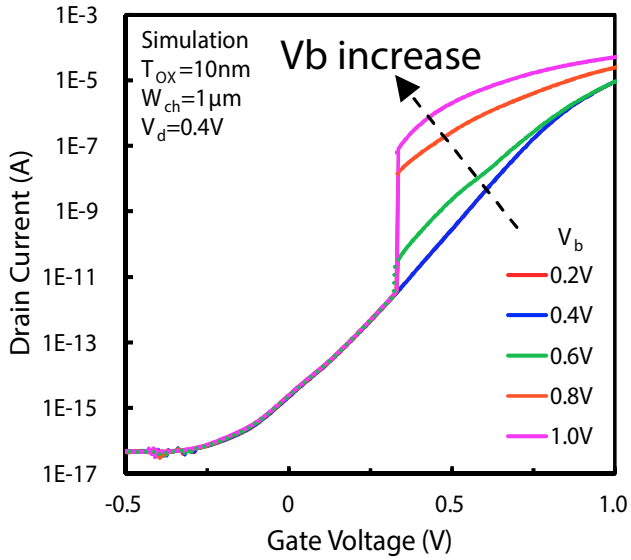


Figure 2.3: Simulated I_D-V_G characteristics at various V_B values[1]. A super-steep SS occurs at V_B higher than 0.6 V.

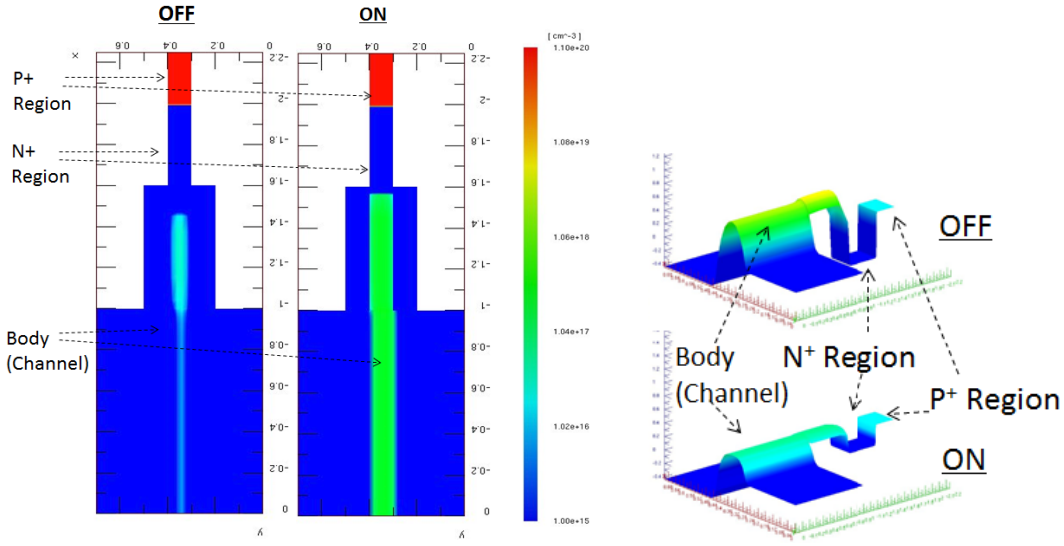
SS occurs over 4 decades. At the same V_G, the body terminal current I_B also increases abruptly. Note that the I_B in Fig. 2.2 is around 10^2 times smaller than I_D.

Figure 2.3 shows the simulated I_D-V_G characteristics at various V_B values. The abrupt SS occurs at V_B of higher than 0.6 V, and the increment of I_B increases with V_B.

2.2.2 Role of Floating-Body Effect on PN-Body-Tied SOI FET

PNBTFET realizes a steep SS by injecting holes into the floating P-type body[1, 3]. Hole current flows through the PNP transistor in the body tie into the P region, and holes accumulate in the P region. Figure 2.4(a) shows the hole densities in a PNBTFET at the off and on state, and indicates that the hole injection is active when PNBTFET is on. By this hole injection, the P region potential rises at the on state, as confirmed in Fig. 2.4(b), and the drain current increases. In other words, the steep SS in PNBTFET is realized by the floating-body effect[4], in which majority carriers are injected into the floating body to increase drain current. It should be noted that the floating-body effect generally occurs in a partially-depleted SOI (PD-SOI) substrate, whose depletion layer width of channel is thinner than the SOI layer so that the substrate has a neutral region under the depletion layer[5]. In this work, we deal with PNBTFETs fabricated on PD-SOI substrates.

There are already steep-SS devices that take advantage of the floating-body effect. However, some devices such as I-MOS[6, 7] and SOI MOSFET with special bias[8, 9, 10] require a drain voltage higher than 1 V to induce impact ionization. Other devices such as CxFETs[11] use bipolar transistor action to cause the floating-body effect, but the drain current decreases exponentially as the drain voltage falls owing to the different doping types between the source and the drain. On the other hand, PNBTFET operates at a very low drain voltage because it does not use impact ionization. Moreover, in PNBTFET, the drain current and the current to induce the floating-body effect (i.e., the body terminal current) are separated, so the drain current is linear to the drain voltage as well as the drain current in conventional MOSFETs.



(a) (b)

Figure 2.4: (a) Hole densities and (b) internal potentials in PNBTFET at the off and on state[1]. When the PNBTFET turns on, holes accumulates in the P region to raise its potential.

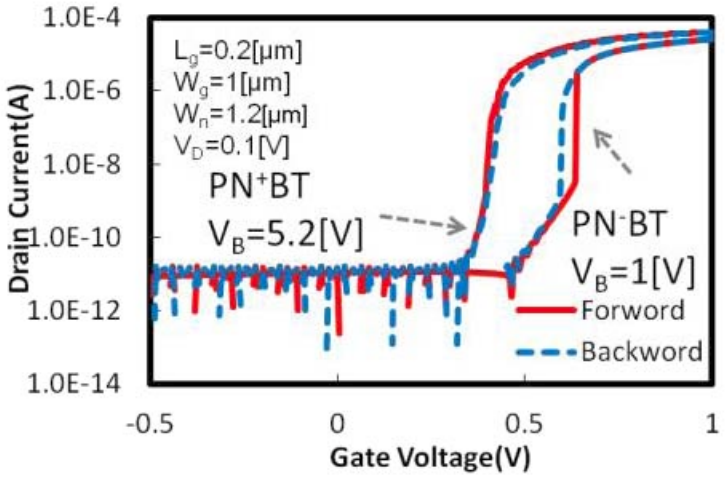


Figure 2.5: Double-sweep measurement of two different PNBTFETs[2]. The PN$^-$BTFET turns on and off at different gate voltages; PNBTFET has hysteresis.

2.2.3 Problems of PN-Body-Tied SOI FET

Despite the attractive features, PNBTFET has some problems: hysteresis and additional standby power dissipation.

In PNBTFET, the turn-on gate voltage V_{on} and turn-off gate voltage V_{off} are different, as shown in Fig. 2.5[2]; PNBTFET has hysteresis in the I_D-V_G curve. V_{on} and V_{off} should be low, and the hysteresis width should be small so that the CMOS circuits work properly.

The body terminal current I_B will cause additional power dissipation in complementary PNBTFET circuits. In a complementary PNBTFET inverter circuit shown in Fig. 2.6, I_B flows from the body terminal to the source when V_G is higher than V_{on}. The off-state complementary PNBTFET in series cannot block this I_B in the on-state PNBTFET. As a result, I_B in either PNBTFETs flows at any moment, and causes additional standby power dissipation. In the simulation shown in Fig. 2.2, the on-state I_B is much greater than the off-state I_D, so the standby power dissipation by the on-state I_B is dominant. To achieve ultralow-power PNBTFETs, the on-state I_B and V_B must be reduced.

2.3 MOS-Gated Thyristor

In PNBTFET, between the source and body terminal is a P^+NPN^+ structure whose P region is topped with a MOS gate, i.e., MOS-gated thyristor (MGT)[12, 13], which plays a significant role in realizing an abrupt SS in PNBTFET[1].

2.3.1 Structure of MOS-Gated Thyristor

As shown in Fig. 2.7, MGT has a P^+NPN^+ structure and a MOS gate on the P region. Whereas the gate of general thyristors is directly connected to the P region[14], the gate of MGT is connected to the P region via a MOS capacitor. The gate, cathode, and anode

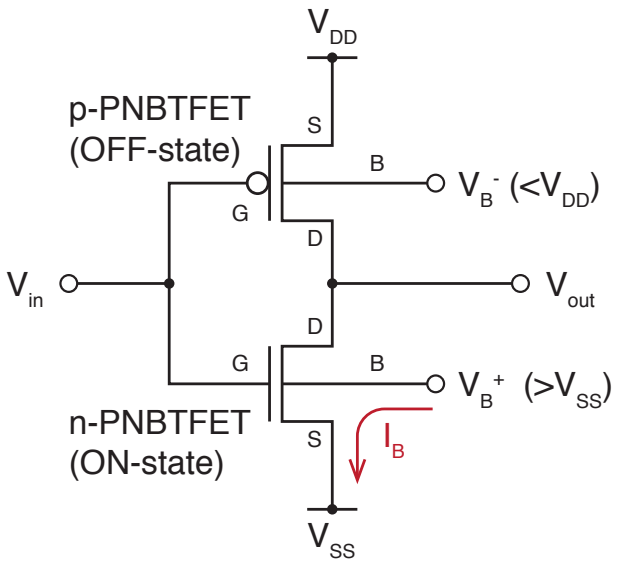


Figure 2.6: Complementary PNBTFET inverter circuit. When the input gate voltage V_{in} is high, the MGT inherent in the n-PNBTFET is on, and I_B continues to flow even when the drain voltage is low. The on-state I_B cannot be blocked by the off-state p-PNBTFET.

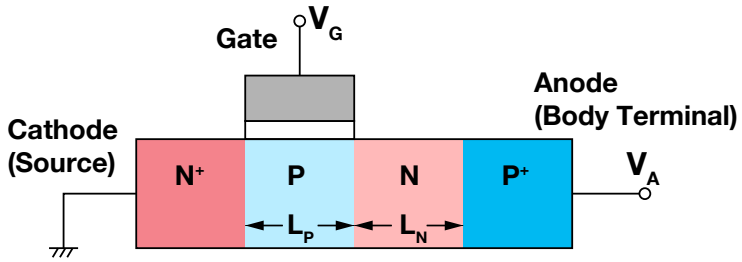
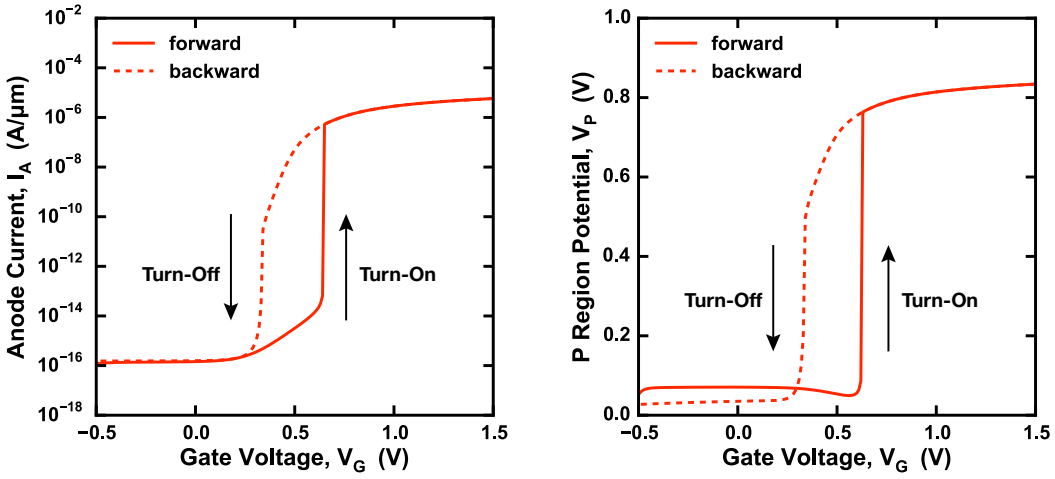


Figure 2.7: Schematic cross-section of MGT, which has a P^+NPN^+ structure with a MOS gate. The gate, cathode, and anode in MGT correspond to the gate, source, and body terminal in PNBTFET. The cathode is grounded, and positive constant anode voltage V_A is applied to the anode. Anode current I_A, P region potential V_P, and N region potential V_N are modulated by gate voltage V_G.



(a) (b)

Figure 2.8: (a) I_A-V_G and (b) V_P-V_G characteristics in the whole MGT simulation. V_G rises in the forward sweep and falls in the backward sweep. I_A and V_P rise abruptly when MGT turns on at $V_G = 0.65\,\mathrm{V}$, and fall abruptly when it turns off at $V_G = 0.34\,\mathrm{V}$. SOI layer thickness $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, gate oxide thickness $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, L_P 2.0 μm, $L_N = 0.5\,\mu\mathrm{m}$, $N_P = 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$.

in MGT correspond to the gate, source, and body terminal in PNBTFET. The cathode is connected to the ground, and the anode is applied positive constant anode voltage V_A. The anode current I_A, P region potential V_P, and N region potential V_N are controlled by V_G.

2.3.2 TCAD Simulation of MOS-Gated Thyristor

Figure 2.8 shows an example of simulated characteristics of MGT with the 2-dimensional structure shown in Fig.2.7, which we simulated on Synopsis Sentaurus Device[15]. When the MGT switches from the off state to the on state at $V_G = 0.65\,\mathrm{V}$, the I_A suddenly increases by 10^8 times, and holes accumulate in the P region to raise V_P abruptly. The MGT can also turn off at $V_G = 0.34\,\mathrm{V}$ to lower I_A and V_P abruptly. It is noted that V_{on} and V_{off} in the MGT are different; MGT also has hysteresis.

It is difficult to determine the design parameters of MGT so that it works propoerly.

Figure 2.9 shows examples of unsuitable V_P-V_G characteristics of MGTs. The MGT in Fig. 2.9(a) cannot turn off by lowering V_G once it turns on. On the other hand, the MGT in Fig. 2.9(b) does not turn off. To design MGT with proper behavior, it is essential to reveal how the design parameters affect the MGT characteristics.

2.3.3 Role of MOS-Gated Thyristor in PN-Body-Tied SOI FET

It is considered that abrupt V_P modulation also occurs in the inherent MGT in PNBTFET. Now, PNBTFET can be seen as a combination of an SOI MOSFET and an MGT, as shown in Fig. 2.10. The P region in PNBTFET is shared by the MOSFET and the MGT, so abrupt V_P modulation in the MGT affects the threshold voltage of MOSFET; thus, the floating-body effect occurs suddenly when the inherent MGT turns on, so the drain current of the MOSFET increases abruptly, hence the abrupt SS.

Now, it is assumed that when PNBTFET turns on abruptly, V_P rises by ΔV_P. At this time, the drain current is multiplied by a factor of α, which is given as

$$\alpha = \exp\left[\frac{q(m-1)\Delta V_P}{mkT}\right]. \tag{2.1}$$

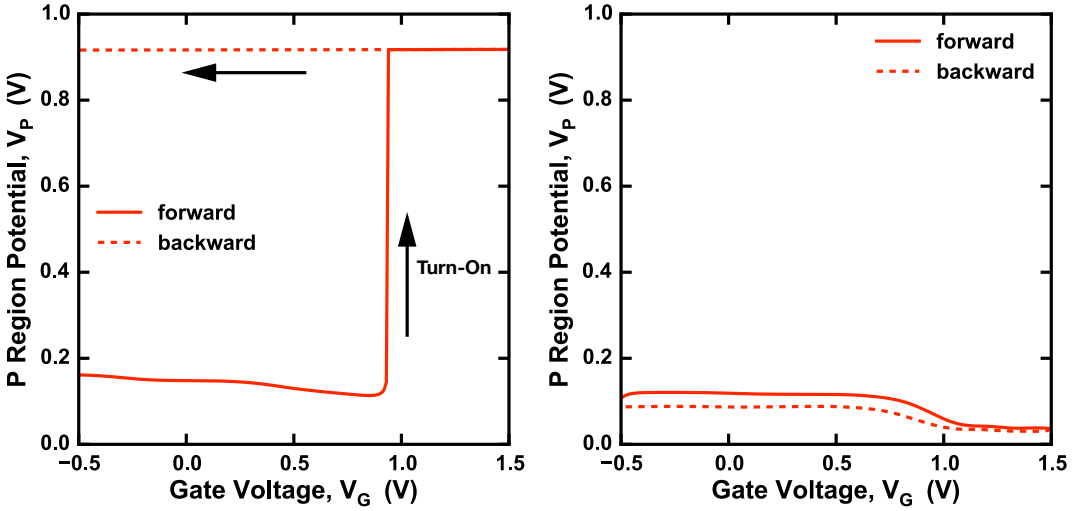
Since m is greater than unity [Eq. (1.3)], the range of α is

$$1 < \alpha < \exp\left(\frac{q\Delta V_P}{kT}\right). \tag{2.2}$$

α increases with a factor m, but there is an upper boundary.

It is considered that PNBTFET turns on and off according with the switching action of the inherent MGT, and the hysteresis in I_D-V_G curve of PNBTFETs stems from the hysteresis in I_A-V_G curve of the inherent MGT. Therefore, it is important to reduce the hysteresis width of MGT in order to reduce that of PNBTFET.

In addition, the on-state I_A and V_A in MGT should be reduced to suppress constant



(a) (b)

Figure 2.9: Examples of unsuitable V_P-V_G characteristics of MGTs. (a) $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, $L_P = 0.1\,\mu\mathrm{m}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$. The MGT does not turn off once it turns on. (b) $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, L_P $2.0\,\mu\mathrm{m}$, $L_N = 5.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$. The MGT does not turn on.

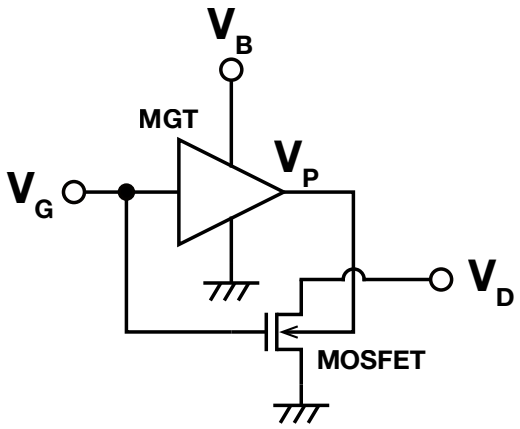


Figure 2.10: Equivalent circuit of PNBTFET, where an SOI MOSFET and an MGT share the P region and the gate. V_G modulates V_P in MGT abruptly, which, in turn, alters the drain current abruptly, hence the abrupt SS.

standby power dissipation in PNBTFET caused by the on-state I_B.

2.3.4 Conventional Equivalent Circuit Model

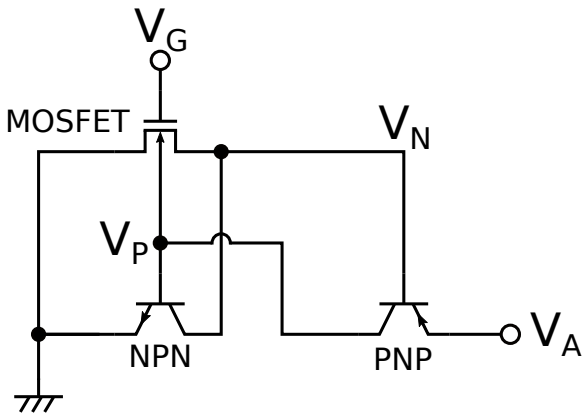


Figure 2.11: Conventional equivalent circuit of MGT, where bipolar transistors and a MOSFET are combined to form a current-based feedback loop[1].

The operation mechanism of MGT is approximately explained in Ref. [1] on the basis of the equivalent circuit shown in Fig. 2.11. A MOSFET and an NPN and PNP bipolar transistors are included in the P^+NPN^+ structure with a MOS gate of MGT. When the MOSFET turns on, the current starts to be amplified by the feedback system as follows:

1. Electrons flowing into the N region increase, so that the electron density in the N region increases to lower V_N.

2. Drop in V_N increases the current in the PNP transistor.

3. Holes flowing into the P region increase, so that the hole density in the P region increases to raise V_P.

4. Rise in V_P increases the currents in the NPN transistor and MOSFET.

In this "current-based" feedback loop, the current turns on when

$$\left(\frac{dI_e}{dI_h}\right)_{\mathrm{NPN+MOSFET}} \left(\frac{dI_h}{dI_e}\right)_{\mathrm{PNP}} > 1, \tag{2.3}$$

where I_e is the electron current, I_h is the hole current, $(dI_e/dI_h)_{\mathrm{NPN+MOSFET}}$ is the differential current gain of the combination of the NPN transistor and MOSFET, and $(dI_h/dI_e)_{\mathrm{PNP}}$ is the differential current gain of the PNP transistor. However, it is difficult to design MGT with optimum current gains at desired V_G in order to control V_{on} and V_{off} owing to the complicated interrelationship between the bipolar transistors and unipolar MOSFET.

To solve this problem, we have reported on a new equivalent circuit model of MGT, which provides intuitive understanding into the MGT operation and a clear guide in optimizing PNBTFET. The new equivalent circuit model will be discussed later in Chapter 3.

2.4 Summary

PNBTFET shows an abrupt SS at very low drain voltage by injecting holes from the body terminal into the P region and inducing the floating-body effect. PNBTFET can be seen as an SOI MOSFET merged with MGT, whose abrupt switching causes an abrupt SS in PNBTFET. Therefore, it is important to analyze the opration of MGT for determining method to design low-power PNBTFETs.

References

[1] J. Ida, T. Mori, Y. Kuramoto, T. Horii, T. Yoshida, K. Takeda, H. Kasai, M. Okihara, and Y. Arai, IEDM Tech. Dig., 2015, p. 624.

[2] T. Yoshida, J. Ida, T. Horii, M. Okihara, and Y. Arai, Proc. IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S), 2016, p. 1.

[3] T. Yoshida, J. Ida, S. Inoue, S. Uchikawa, A. Hashimoto, K. Hayashi, T. Iwasaki, M. Kamako, and T. Horii, IEEE Electron Devices Technology and Manufacturing Conf. Proc. Tech. Pap. (EDTM), 2017, p. 75.

[4] M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada, K. Kato, and H. Tango, IEEE Tans. Electron Devices **36**, 493 (1989).

[5] S. M. Sze and M. K. Lee, *Semiconductor Devices — Physics and Technology* (John Wiley & Sones Inc., New York, 2012) 3rd Edition.

[6] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, IEDM Tech. Dig., 2002, p. 289.

[7] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, IEEE Trans. Electron Devices **52**, 69 (2005).

[8] J. G. Fossum, R. Sundaresan, and M. Matloubian, IEEE Electron Device Lett. 8, 544 (1987).

[9] J. G. Fossum and Z. Lu, Proc. IEEE Int. SOI Conf., 2011, p. 1.

[10] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J. G. Fossum, L. Altimime, and M. Jurczak, IEDM Tech. Dig., 2010, p. 407.

[11] D. Hisamoto, S. Saito, A. Shima, H. Yoshimoto, and K. Torii, IEEE Silicon Nanoelectronics Workshop (SNW), 2012, p. 1.

[12] V. A. K. Temple, IEEE Trans. Electron Devices **33**, 1609 (1986).

[13] A. Q. Huang, Solid-State Electronics **42**, 1855 (1998).

[14] B. J. Baliga, *Fundamentals of Power Semiconductor Devices* (Springer, New York, 2008) p. 625.

[15] Synopsis, Sentaurus Device User Guide Version I-2013.12 (2013).

Chapter 3

Voltage-Based Equivalent Circuit Model of MOS-Gated Thyristor

3.1 Introduction

In Chapter 3, our new equivalent circuit model of MGT is proposed. The equivalent circuit model graphically explains the mechanism of the switching behavior in MGT by decomposing the complex feedback system into a simple cross-coupling of two voltage inverters. 2-dimensional TCAD models are simulated to confirm the behavior of the equivalent circuit model. In addition, the voltage response of the equivalent circuit model is discussed with a simple analytical model, which is helpful for discussing the simulation results of the equivalent circuit model.

3.2 Concept of Voltage-Based Equivalent Circuit Model

We proposed a voltage-based equivalent circuit model of MGT shown in Fig. 3.1. The equivalent circuit model is composed of two voltage inverters, i.e., the electron current

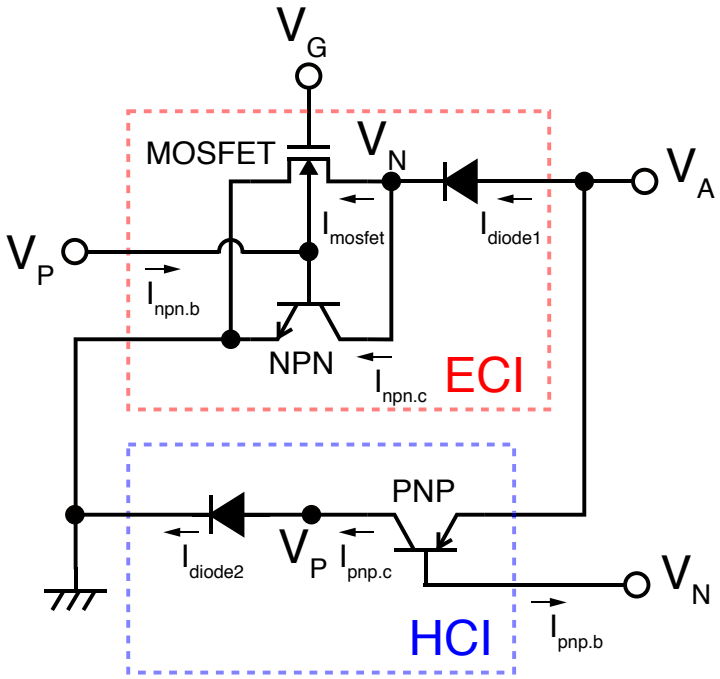


Figure 3.1: Voltage-based equivalent circuit model of MGT consists of two cross-coupled voltage inverters, i.e., ECI and HCI. ECI has input V_G and V_P and output V_N. HCI has input V_N and output V_P. The output of each inverter is fed to the input of the other to shape a voltage-based feedback loop.

inverter (ECI) and hole current inverter (HCI). The bases and emitters of the bipolar transistors in the conventional equivalent circuit model are replaced with PN junction diodes in the voltage-based equivalent circuit model. MGT includes a MOSFET and NPN bipolar transistor, so the gate voltage V_G and the P region potential V_P modulate the current in MGT; thus, V_G and V_P affect the density of the electrons in the N region and the N region potential V_N. ECI imitates this voltage response, in which input V_G and V_P affect output V_N. Similarly, MGT includes a PNP bipolar transistor, so V_N modulates the current in MGT and affects V_P by altering the density of the holes in the P region. HCI imitates this voltage response, in which input V_N affect output V_P.

In the equivalent circuit model, ECI and HCI are cross-coupled; ECI output V_N is fed to HCI output V_N, and HCI output V_P is fed to ECI input V_P. Thus, V_P values in ECI and

HCI are identical, so are V_N values. Thus, this cross-coupling shapes a "voltage-based" feedback loop; V_P affects V_N in ECI, which, in turn, affects V_P in HCI.

3.3 TCAD Simulation of Voltage-Based Equivalent Circuit Model

3.3.1 TCAD Simulation Models

To observe the behavior of the equivalent circuit model, we conducted 2-dimensional TCAD simulation on a commercial TCAD simulator of Synopsis Sentaurus Device[1]. The input-output characteristics (i.e., transfer curves) of ECI and HCI are simulated independently using TCAD models shown in Fig. 3.2. The ECI TCAD model in Fig. 3.2(a) is designed to function as an ECI circuit. The ECI TCAD model has the same structure as the corresponding MGT TCAD model (Fig. 2.7) except the N region length (L'_N), which is extended so that holes injected from the anode completely recombine in the N region and do not reach the P region. This eliminates the effect of a PNP transistor and realizes the ECI function. On the other hand, the HCI TCAD model in Fig. 3.2(b) is designed to function as an HCI circuit. The HCI TCAD model has the same structure as the corresponding MGT model except that the MOS gate is removed and the P region length (L'_P) is extended to eliminate the effect of an NPN transistor; thus, the HCI function is realized.

In the simulation of these TCAD models, the cathode is grounded, and the constant anode voltage V_A is applied. In the ECI TCAD model, the characteristics of the output V_N versus the input V_P at various V_G values are simulated. In the HCI TCAD model, the characteristics of the output V_P versus the input V_N are simulated.

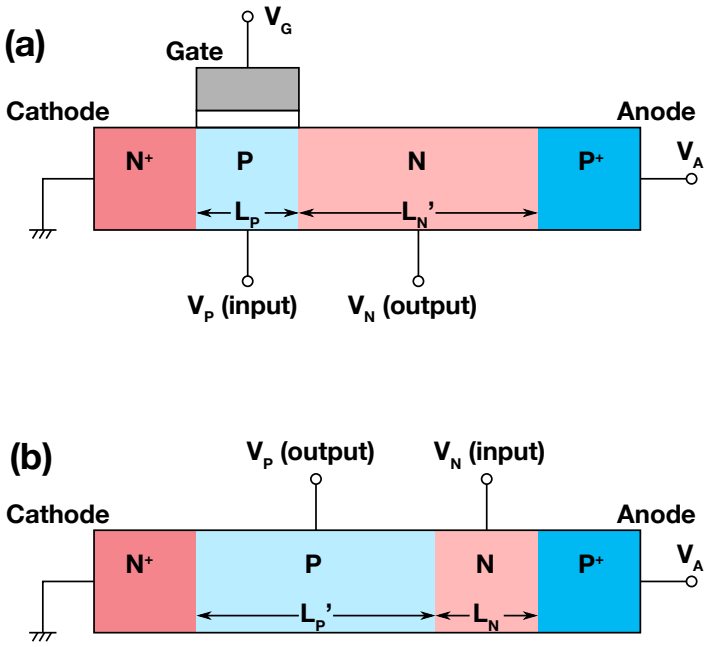


Figure 3.2: Schematic cross section of the two-dimensional TCAD models of (a) ECI and (b) HCI. The ECI TCAD model has N region length extended to eliminate the PNP bipolar action. The HCI TCAD model has P region length extended to eliminate the NPN bipolar action, and the MOS gate is removed. In all of the ECI and HCI TCAD simulations in this thesis, both L'_N and L'_P are fixed at 10 µm.

3.3.2 Switching Mechanism of Voltage-Based Equivalent Circuit Model

Now, the input-output characteristics (i.e., transfer curves) of ECI and HCI at various V_G values are simulated and plotted on the V_P-V_N diagram as shown in Fig. 3.3. ECI curve is modulated by V_G. As ECI and HCI are cross-coupled, the operating point (V_P, V_N) of the equivalent circuit model settles at one of the stable points located at the intersections of the ECI and HCI transfer curves, which are indicated by circles in Fig. 3.3. Stable points may move, appear or disappear as ECI transfer curve is modulated by V_G.

The behavior of the simulated transfer curves provides an explanation for the switching process of MGT. Now, it is assumed that V_G increases from 0.0 to 0.7 V. When V_G is 0.0 V [Fig. 3.3(a)], the ECI and HCI transfer curves cross at one point on the left top.

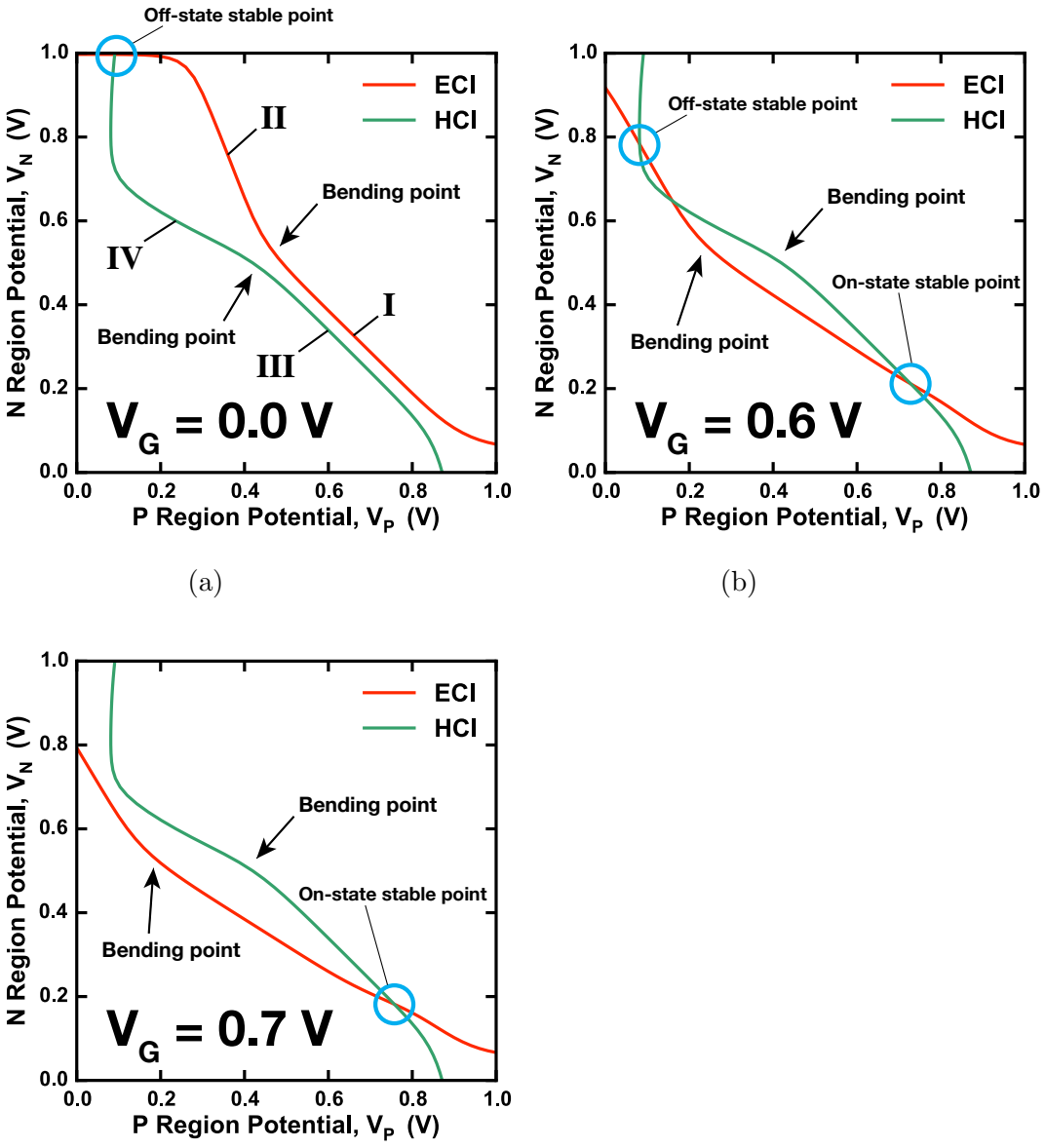


Figure 3.3: Simulated transfer curves of ECI and HCI at three different V_G values. V_G modulates the ECI transfer curve, affecting the stable points indicated by circles. (a) At $V_G = 0.0\,\mathrm{V}$, only the off-state stable point exists on the left top. (b) At $V_G = 0.6\,\mathrm{V}$, both the off-state and the on-state stable points exists; the model is bistable. (c) At $V_G = 0.7\,\mathrm{V}$, only the on-state stable point exists on the right bottom. These ECI and HCI correspond to the whole MGT simulation shown in Fig. 2.8. The ECI transfer curve has bends at V_N of around 0.5 V, and the HCI transfer curve at V_P of around 0.5 V. $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, $L_P = 2.0\,\mu\mathrm{m}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_P = 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$.

This is the off-state stable point, at which the operating point settles; V_P is low, and V_N is high. Thus, the equivalent circuit model is in the off state at $V_G = 0.0\,\mathrm{V}$ When V_G increases to 0.6 V [Fig. 3.3(b)], the on-state stable point has appeared on the right bottom; the equivalent circuit model is bistable[1]. However, the operating point remains on the off-state stable point unless the off-state stable point disappears; the equivalent circuit model is still off at $V_G = 0.6\,\mathrm{V}$. When V_G increases to 0.7 V [Fig. 3.3(c)], the ECI and HCI transfer curves cross at one point on the right bottom; the off-state stable point has disappeared. The operating point is forced to move instantly to the on-state stable point. As a consequence, V_P rises and V_N falls abruptly; the equivalent circuit model turns on. Thus, the turn-on process in MGT is explained by the equivalent circuit model.

Similarly, the turn-off process can be explained. It is assumed that V_G decreases from 0.7 to 0.0 V. At first, the operating point is on the on-state stable point at $V_G = 0.7\,\mathrm{V}$ [Fig. 3.3(c)] and remains there at $V_G = 0.6\,\mathrm{V}$ [Fig. 3.3(b)]. When V_G decreases to 0.0 V, the on-state stable point has disappeared. The operaint point is forced to move instantly to the off-state stable point; the equivalent circuit model turns off.

If the equivalent circuit model can be bistable at once at an intermediate V_G, the V_G at which the off-state stable point disappears when V_G is rising and the V_G at which the on-state stable point disappears when V_G is falling are different. This leads to the hysteresis, as shown in Fig. 2.8, whose width is equal to the V_G extent in which the equivalent circuit model possesses the two stable points.

The equivalent circuit model also provides intuitive understanding to the malfunctioning MGTs shown in Fig. 2.9. Figures 3.4(a) and 3.4(b) show the simulated transfer curves of the equivalent circuit models that respectively correspond to the MGTs in Figs. 2.9(a) and 2.9(b). In Fig. 3.4(a), there are two stable points even at $V_G = -0.5\,\mathrm{V}$. Therefore, after the off-state stable point disappears by raising V_G, the equivalent circuit model cannot

[1]Note that the intermediate sintersection seen in Fig. 3.3(b) is not a stable point. The loop gain for V_P is lower than unity on the left side of the intermediate intersection, and higher than unity on the right side. Consequently, the operating point with even a small gap from the intermediate intersection will move away from it.

turn off because the on-state stable point does not extinguish by lowering V_G. In Fig. 3.4(b), there is only one stable point on the left at any V_G value, so V_P remains low; the equivalent circuit model does not turn on. Thus, the equivalent circuit model also explains the mechanism of improper behavior of MGT.

Figure 3.5 shows the V_P-V_G characteristics in the equivalent circuit model simulation in Fig. 3.3 derived from the stable points at various V_G values. This can be compared with the V_P-V_G characteristics in whole MGT simulations as shown in Fig 2.8.

3.4 Analytical Model of Voltage-Based Equivalent Circuit Model

In this section, simple analytical model of ECI and HCI is discussed. Currents in ECI and HCI are labeled in Fig. 3.1 as follows: I_{diode1} is the PN diode current in ECI, I_{mosfet} is the current in the MOSFET, $I_{\mathrm{npn.c}}$ and $I_{\mathrm{npn.b}}$ are the collector and base currents in the NPN transistor in ECI, respectively, I_{diode2} is the PN diode current in HCI, and $I_{\mathrm{pnp.c}}$ and $I_{\mathrm{pnp.b}}$ are the collector and base currents in the PNP transistor in HCI, respectively.

In ECI, the currents are given as

$$I_{\mathrm{diode1}} = I_{\mathrm{diode1.dif0}}\left[e^{q(V_A-V_N)/kT}-1\right] + I_{\mathrm{diode1.gr0}}\left[e^{q(V_A-V_N)/2kT}-1\right], \quad (3.1)$$

$$I_{\mathrm{npn.b}} = I_{\mathrm{npn.b.dif0}}\left(e^{qV_P/kT}-1\right) + I_{\mathrm{npn.b.gr0}}\left(e^{qV_P/2kT}-1\right), \quad (3.2)$$

$$I_{\mathrm{npn.c}} = \beta_{\mathrm{npn}} I_{\mathrm{npn.b.dif0}}\left(e^{qV_P/kT}-1\right), \quad (3.3)$$

$$I_{\mathrm{mosfet}} = I_{\mathrm{mosfet0}} e^{q(V_G-V_{th}+(m-1)V_P)/mkT}, \quad (3.4)$$

where β_{npn} is the current gain of the NPN transistor in ECI, and V_{th} is the threshold volatage of the MOSFET. The first terms of Eqs. (3.1) and (3.2) are diffusion current, and the second terms are generation-recombination current. In a PN junction diode current, diffusion current is dominant at a high voltage, and generation-recombination current is

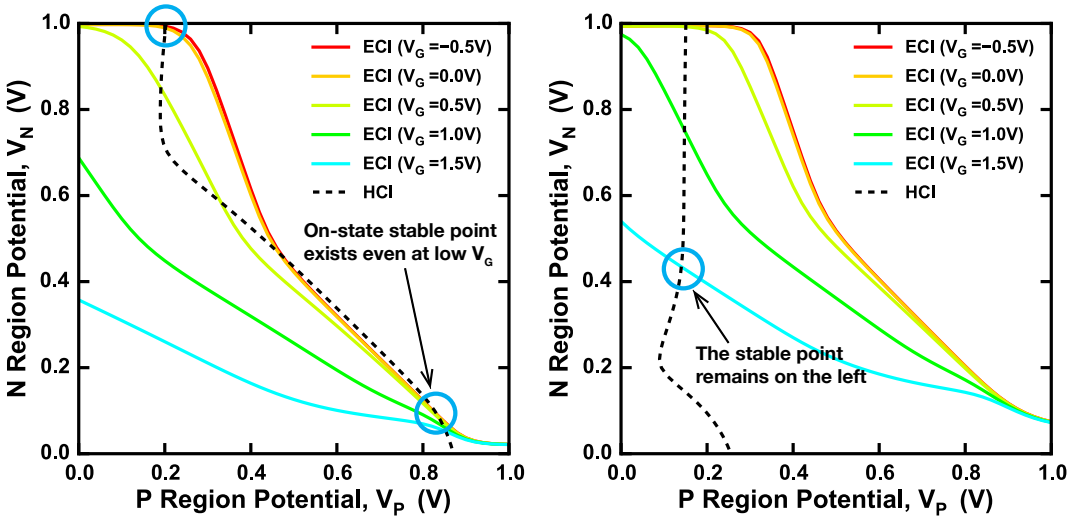


Figure 3.4: Simulated transfer curves of the equivalent circuit models that correspond to the MGTs in in Fig. 2.9. (a) $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, $L_P = 0.1\,\mu\mathrm{m}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$. (b) $T_{\mathrm{SOI}} = 200\,\mathrm{nm}$, $T_{\mathrm{OX}} = 10\,\mathrm{nm}$, L_P $2.0\,\mu\mathrm{m}$, $L_N = 5.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, $V_A = 1.0\,\mathrm{V}$.

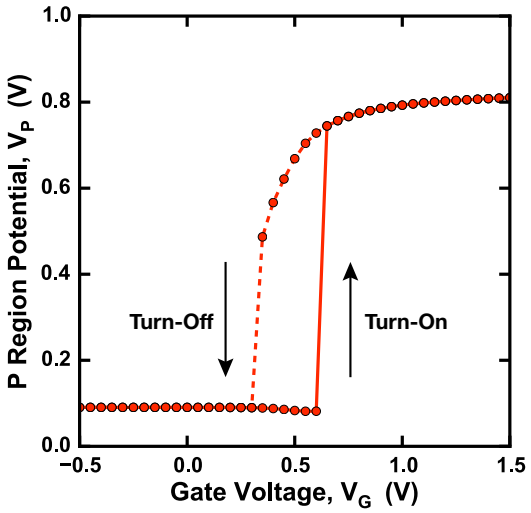


Figure 3.5: V_P-V_G characteristics derived from the stable points of the equivalent circuit model simulation in Fig. 3.3. $V_{on} = 0.65\,\mathrm{V}$ and $V_{off} = 0.30\,\mathrm{V}$.

dominant at a low voltage[2].

Now, it is assumed that V_G is so low that I_{mosfet} is zero, and I_{diode1} is equal to $I_{\mathrm{npn.c}}$. When $(V_A - V_N), V_P \gg kT/q$, $(V_A - V_N)$ in ECI can be approximated as

$$V_A - V_N = V_P + \frac{kT}{q} \ln\left(\frac{\beta_{\mathrm{npn}} I_{\mathrm{npn.b.dif0}}}{I_{\mathrm{diode1.dif0}}}\right) \quad \text{for high } (V_A - V_N), \tag{3.5}$$

$$V_A - V_N = 2V_P + \frac{2kT}{q} \ln\left(\frac{\beta_{\mathrm{npn}} I_{\mathrm{npn.b.dif0}}}{I_{\mathrm{diode1.gr0}}}\right) \quad \text{for low } (V_A - V_N). \tag{3.6}$$

Equations (3.5) and (3.6) respectively correspond to the straight parts of the simulated ECI transfer curve labeled I and II in Fig. 3.3(a). There is a bend in the simulated ECI transfer curve, as shown in Fig. 3.3. A bending point of ECI transfer curve is located approximately at

$$V_N = V_A - \frac{2kT}{q} \ln\left(\frac{I_{\mathrm{diode1.gr0}}}{I_{\mathrm{diode1.dif0}}}\right), \tag{3.7}$$

so it moves upward in the V_P-V_N graph as the generation-recombination current decreases.

On the other hand, in the case where V_G is sufficiently high so that the MOSFET current I_{mosfet} is dominant in ECI and I_{diode1} is equal to I_{mosfet}, $(V_A - V_N)$ is approximated as

$$V_A - V_N = \frac{[V_G - V_{th} + (m-1)V_P]}{m} + \frac{kT}{q} \ln\left(\frac{I_{\mathrm{mosfet0}}}{I_{\mathrm{diode1.dif0}}}\right) \quad \text{for high } (V_A - V_N), \tag{3.8}$$

$$V_A - V_N = \frac{2[V_G - V_{th} + (m-1)V_P]}{m} + \frac{2kT}{q} \ln\left(\frac{I_{\mathrm{mosfet0}}}{I_{\mathrm{diode1.gr0}}}\right) \quad \text{for low } (V_A - V_N). \tag{3.9}$$

Equations (3.8) and (3.9) means that the sensitivity of the ECI transfer curve to V_G dependes only on a factor m, which is greater than unity [Eq. (1.3)], and that the ECI transfer curve becomes sensitive to V_G as m approaches unity.

The currents in HCI are given as

$$I_{\text{diode2}} = I_{\text{diode2.dif0}}\left(e^{qV_P/kT}-1\right)+I_{\text{diode2.gr0}}\left(e^{qV_P/2kT}-1\right), \quad (3.10)$$

$$I_{\text{pnp.b}} = I_{\text{pnp.b.dif0}}\left[e^{q(V_A-V_N)/kT}-1\right]+I_{\text{pnp.b.gr0}}\left[e^{q(V_A-V_N)/2kT}-1\right], \quad (3.11)$$

$$I_{\text{pnp.c}} = \beta_{\text{pnp}} I_{\text{pnp.b.dif0}}\left[e^{q(V_A-V_N)/kT}-1\right], \quad (3.12)$$

where β_{pnp} is the current gain of the PNP transistor in HCI. When $(V_A-V_N), V_P \gg kT/q$, V_P in HCI can be approximated as

$$V_P = (V_A-V_N)+\frac{kT}{q}\ln\left(\frac{\beta_{\text{pnp}} I_{\text{pnp.b.dif0}}}{I_{\text{diode2.dif0}}}\right) \quad \text{for high } V_P, \quad (3.13)$$

$$V_P = 2(V_A-V_N)+\frac{2kT}{q}\ln\left(\frac{\beta_{\text{pnp}} I_{\text{pnp.b.dif0}}}{I_{\text{diode2.gr0}}}\right) \quad \text{for low } V_P. \quad (3.14)$$

Equations (3.13) and (3.14) respectively correspond to the straight parts of the simulated HCI transfer curve labeled III and IV in Fig. 3.3(a). A bending point in HCI transfer curve is located approximately at

$$V_P = \frac{2kT}{q}\ln\left(\frac{I_{\text{diode2.gr0}}}{I_{\text{diode2.dif0}}}\right), \quad (3.15)$$

so it moves to the left in the V_P-V_N graph as the generation-recombination current decreases.

3.5 Summary

Our new modeling approach, i.e., the voltage-based equivalent circuit model simplifies the complex feedback system of MGT by decomposing it into a cross-coupling of voltage inverters ECI and HCI. The simulated transfer curves of ECI and HCI provide intuitive understanding into the switching mechanism of MGT. In addition, the transfer curves of ECI and HCI are approximately expressed by simple analytical equations, which provide

good explanations for the parameter dependence of MGT characteristics, as shown later in Chapter 4.

References

[1] Synopsis, Sentaurus Device User Guide Version I-2013.12 (2013).

[2] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 2009) 2nd Edition.

Chapter 4

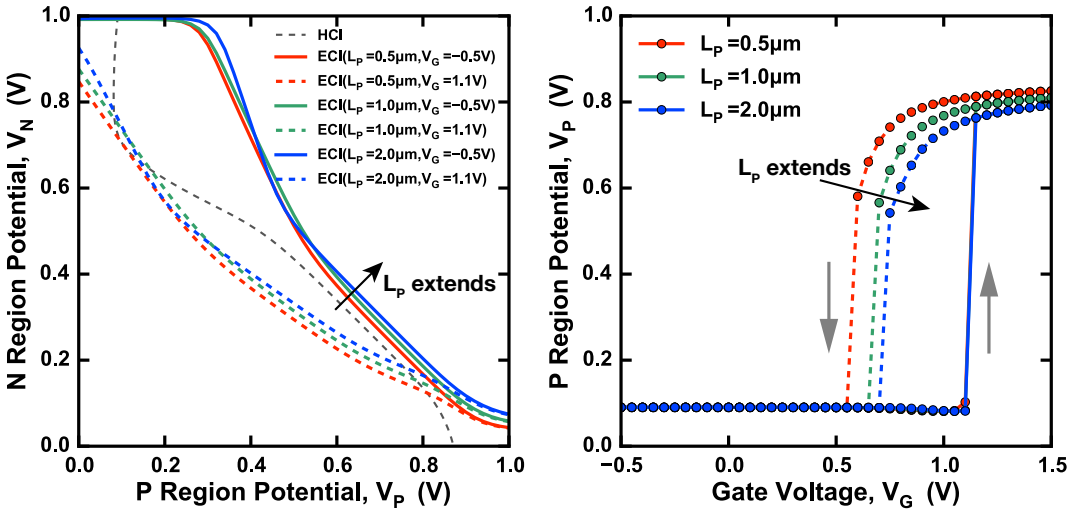
Comparison of MOS-Gated Thyristor & Proposed Model

4.1 Introduction

In Chapter 4, simulation results of MGT and the voltage-based equivalent circuit model are compared and discussed. The effects of various parameters on MGT and the equivalent circuit model are examined by 2-dimensional TCAD simulations on Synopsis Sentaurus Device[1]. There are two types of simulations in this chapter:

- The transfer curves of ECI and HCI TCAD models (Fig. 3.2) are simulated, and V_P-V_G characteristics in the equivalent circuit model are derived from the stable points, which are located at the intersections of the transfer curves, as shown in Fig. 3.5.

- V_P-V_G characteristics of whole MGT TCAD model (Fig. 2.7) are directly simulated, as shown in Fig. 2.8.



(a) (b)

Figure 4.1: (a) Simulated transfer curves and (b) V_P-V_G characteristics of the equivalent circuit model at various L_P values. V_P-V_G characteristics are calculated from the stable points in the V_P-V_N graph for each V_G. $V_A = 1.0\,\mathrm{V}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

4.2 Parameter Dependence of MOS-Gated Thyristor & Proposed Model

To realize proper threshold voltages (V_{on} and V_{off}) in the voltage-based equivalent circuit model, it is essential to determine how the design parameters affect ECI and HCI transfer curves. The effects of the P region length L_P, N region length L_N, P region acceptor concentration N_P, N region donor concentration N_N, anode voltage V_A, and minority carrier lifetimes on the equivalent circuit model and MGT are examined and compared.

4.2.1 Dependence on P Region Length

First of all, the effect of L_P on the equivalent circuit model is examined. Varying L_P affects the MOSFET and NPN transistor in ECI, and, therefore, the ECI transfer curves. Figure 4.1 shows simulated transfer curves at various L_P values from 0.5 to 2.0 μm. As

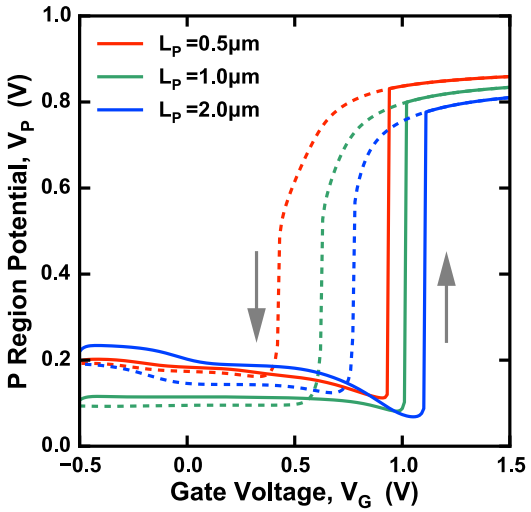
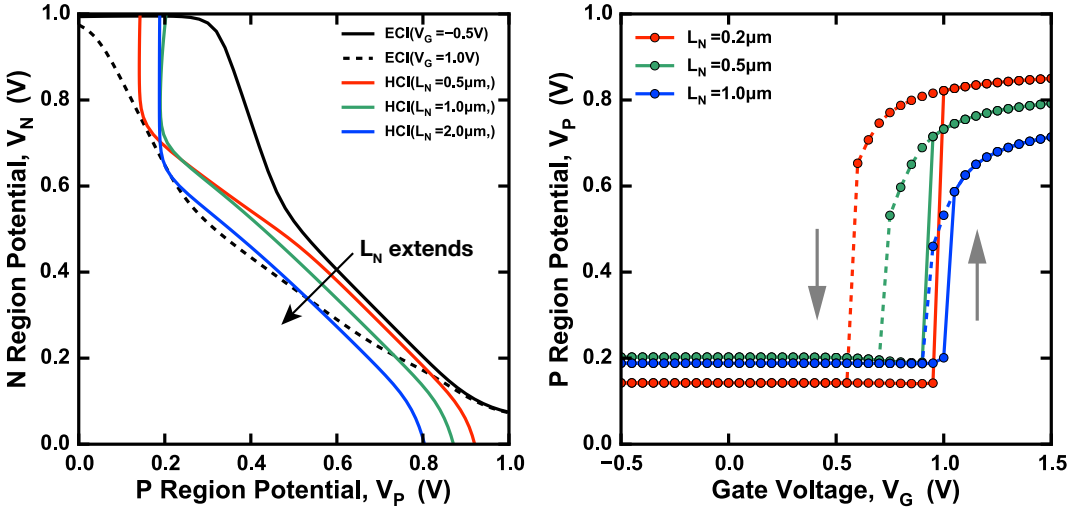


Figure 4.2: V_P-V_G characteristics at various L_P values in whole MGT simulation. $V_A = 1.0\,\mathrm{V}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

L_P extends, the cuurent gain of the NPN transistor reduces, so that the threshold voltage of ECI rises and the ECI transfer curve shifts upward. This tendency of the ECI transfer curve is supported by Eqs. (3.5) and (3.6). As a result, when V_G is decreasing, the ECI transfer curve at a high V_P detaches from the HCI curve at a higher V_G; V_{off} rises as L_P extends. It is confirmed that as L_P extends from 0.5 to 2.0 µm, V_{off} rises from 0.55 to 0.70 V with V_{on} kept 1.10 V, and the hysteresis width decreases from 0.55 to 0.40 V.

Figure 4.2 shows the effect of L_P on the simulated V_P-V_G characteristics of MGT. This MGT corresponds to the equivalent circuit model in the simulation shown in Fig. 4.1. That is, this MGT has the same L_P and N_P values as the ECI TCAD model and the same L_N and N_N values as the HCI TCAD model. It is confirmed that as L_P in MGT extends from 0.5 to 2.0 µm, V_{off} rises from 0.42 to 0.77 V, V_{on} rises from 0.94 to 1.11 V, and the hysteresis width decreases 0.52 to 0.34 V.

Thus, extending L_P raises V_{off} and reduces the hysteresis width, as seen in both the equivalent circuit model and MGT. While the equivalent circuit model and MGT show



(a) (b)

Figure 4.3: (a) Simulated transfer curves and (b) V_P-V_G characteristics of the equivalent circuit model at various L_N values. $V_A = 1.0\,\mathrm{V}$, $L_P = 2.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

good correlation in the tendency of V_{off} and the hysteresis width versus varying L_P, the tendency of V_{on} are different. We consider that this difference stems from the extended regions in the equivalent circuit TCAD models, and there is room for improving TCAD models to realize the ECI and HCI functions.

4.2.2 Dependence on N Region Length

The effect of L_N on the equivalent circuit model is examined. Varying L_N affects the PNP transistor in HCI, and, therefore, the HCI transfer curves. Figure 4.3 shows simulated transfer curves at various L_N values from 0.2 to 1.0 μm. As L_N extends, the current gain of the PNP transistor reduces, so that the threshold voltage of HCI rises and the HCI transfer curve shifts downward. This tendency coincides with Eqs. (3.13) and (3.14). As a result, the HCI transfer curve at a high V_P shifts away from the ECI curve, so that V_{off} rises. In addition, as the HCI transfer curve shifts downward by extending L_N, the ECI and HCI transfer curves cross with almost parallel positional relationship when the

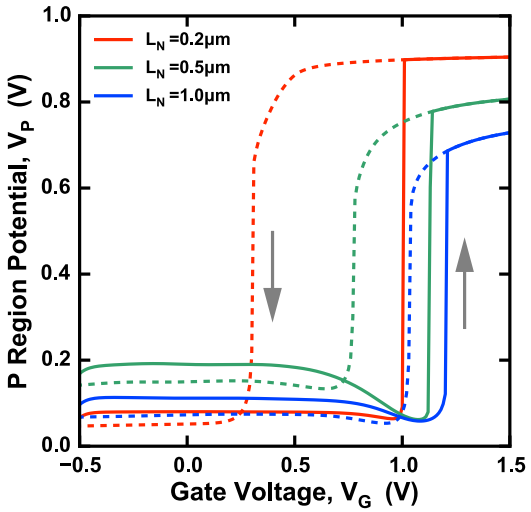


Figure 4.4: V_P-V_G characteristics at various L_N values in whole MGT simulation. V_A = 1.0 V, L_P = 2.0 µm, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

equivalent circuit model is bistable, so the hysteresis width decreases. It is confirmed that as L_N extends from 0.5 to 2.0 µm, V_{off} rises from 0.55 to 0.90 V, and the hysteresis width decreases from 0.40 to 0.10 V.

Similar tendency is confirmed in the MGT characteristics, as shown in Fig. 4.4. It is confirmed that as L_N in MGT extends from 0.2 to 1.0 µm, V_{off} rises from 0.30 to 1.03 V, V_{on} rises from 1.00 to 1.21 V, and the hysteresis width decreases 0.73 to 0.18 V.

Thus, extending L_N raises V_{off} and reduces the hysteresis width, as seen in both the equivalent circuit model and MGT.

4.2.3 Dependence on P Region Acceptor Concentration

The effect of N_P on the transfer curves is examined. Figure 4.5(a) shows the simulated transfer curves at various N_P values from 2×10^{18} to $7 \times 10^{17}\,\mathrm{cm}^{-3}$. As N_P decreases, the threshold voltage of the inherent MOSFET is lowered so that ECI transfer curve starts

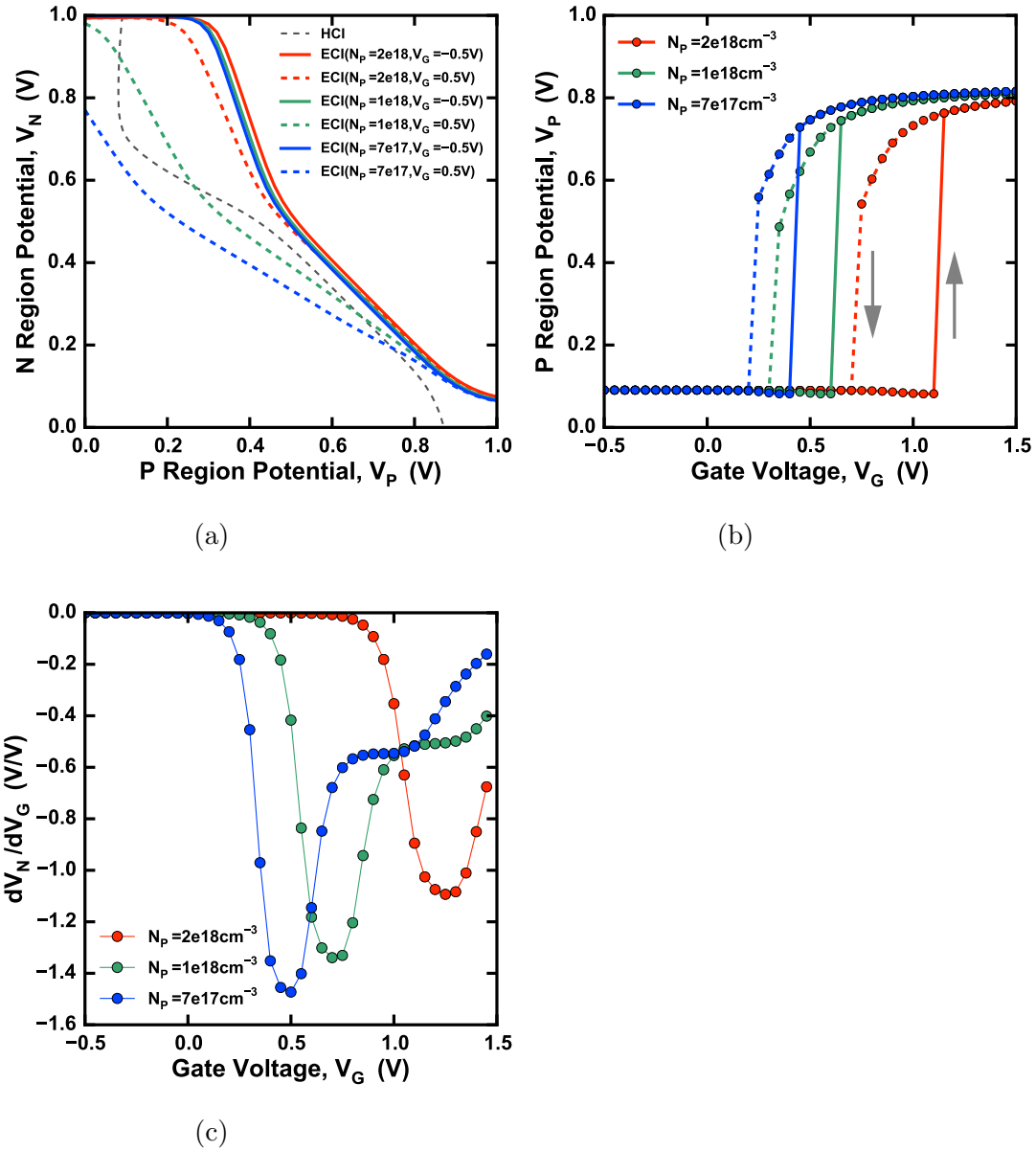


Figure 4.5: (a) Simulated transfer curves, (b) V_P-V_G characteristics, and (c) ($\mathrm{d}V_N/\mathrm{d}V_G$)-$V_G$ characteristics at $V_P = 0\,\mathrm{V}$ of the equivalent circuit model at various N_P values. $V_A = 1.0\,\mathrm{V}$, $L_P = 2.0\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

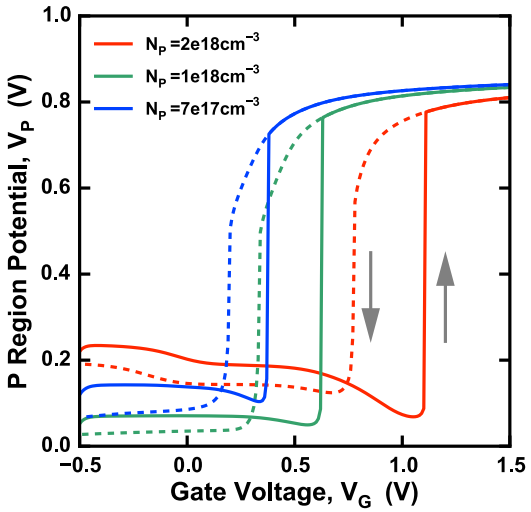
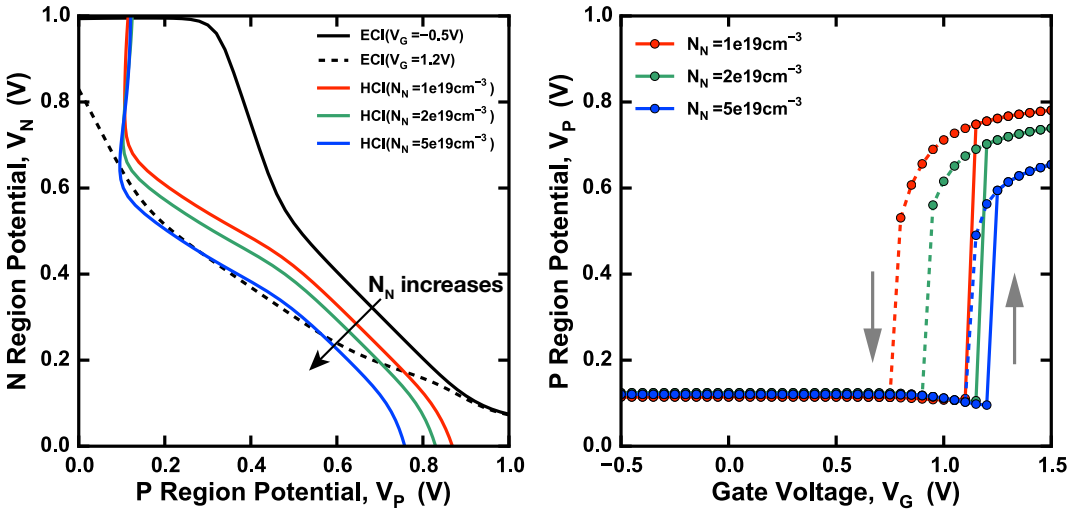


Figure 4.6: V_P-V_G characteristics at various N_P values in whole MGT simulation. V_A = 1.0 V, L_P = 2.0 µm, L_N = 0.5 µm, N_N = 10^{20} cm^{-3}.

to be modulated at lower V_G. As a result, both V_{on} and V_{off} of the equivalent circuit model are lowered from 1.10 to 0.40 V and from 0.70 to 0.20 V, respectively [Fig. 4.5(b)]. Moreover, Eqs. (3.8) and (3.9) imply that ECI transfer curve becomes more sensitive to V_G when a factor m of the MOSFET in ECI [Eq. (1.3)] approaches unity by decreasing N_P. This is confirmed in the (dV_N/dV_G)-V_G graph shown in Fig. 4.5(c). By increasing the sensitivity, the hysteresis width is reduced from 0.40 to 0.20 V [Fig. 4.5(b)].

On the other hand, Fig. 4.6 shows the simulated V_P-V_G characteristic of MGT corresponding to the equicalent circuit model in Fig. 4.5, at various N_P values from 2×10^{18} to 7×10^{17} cm^{-3}. It is confirmed that by decreasing N_P in MGT from 2×10^{18} to 7×10^{17} cm^{-3}, V_{on} and V_{off} are lowered from 1.11 to 0.38 V and from 0.77 to 0.19 V, respectively, and the hysteresis width is reduced from 0.34 to 0.19 V.

Thus, it is demonstrated that the effect of N_P on the threshold voltages and the hysteresis widths of the equivalent circuit model correlates with that of corresponding MGT.



(a) (b)

Figure 4.7: (a) Simulated transfer curves and (b) V_P-V_G characteristics of the equivalent circuit model at various N_N values. $V_A = 1.0\,\mathrm{V}$, $L_P = 2.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 2.0\,\mu\mathrm{m}$.

4.2.4 Dependence on N Region Donor Concentration

The effect of N_N on the equivalent circuit model is also examined. Similar to the L_N dependence, increasing N_N degrades the current gain of the PNP bipolar transistor in HCI and shifts the HCI transfer curve downward. Consequently, V_{off} rises and the hysteresis width reduces as N_N decreases. It is confirmed that by increasing N_N from 1×10^{19} to $5 \times 10^{19}\,\mathrm{cm}^{-3}$, V_{off} rises from 0.75 to 1.10 V, and the hysteresis width is reduced from 0.35 to 0.10 V.

Figure 4.8 shows the simulated V_P-V_G characteristics at various N_N values in MGT. It is confirmed that by increasing N_N in MGT from 1×10^{19} to $5 \times 10^{19}\,\mathrm{cm}^{-3}$, V_{off} rises from 0.80 to 1.19 V, and the hysteresis width is reduced from 0.47 to 0.23 V.

Thus, increasing N_N raises V_{off} and reduces the hysteresis width, as seen in both the equivalent circuit model and MGT.

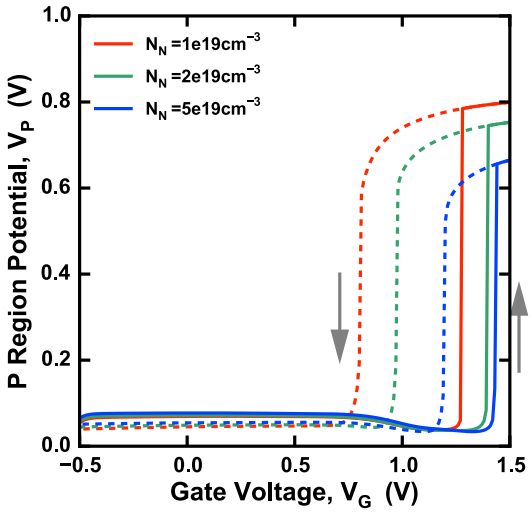


Figure 4.8: V_P-V_G characteristics at various N_N values in whole MGT simulation. V_A = 1.0 V, L_P = 2.0 µm, $N_P = 2 \times 10^{18}$ cm^{-3}, L_N = 2.0 µm.

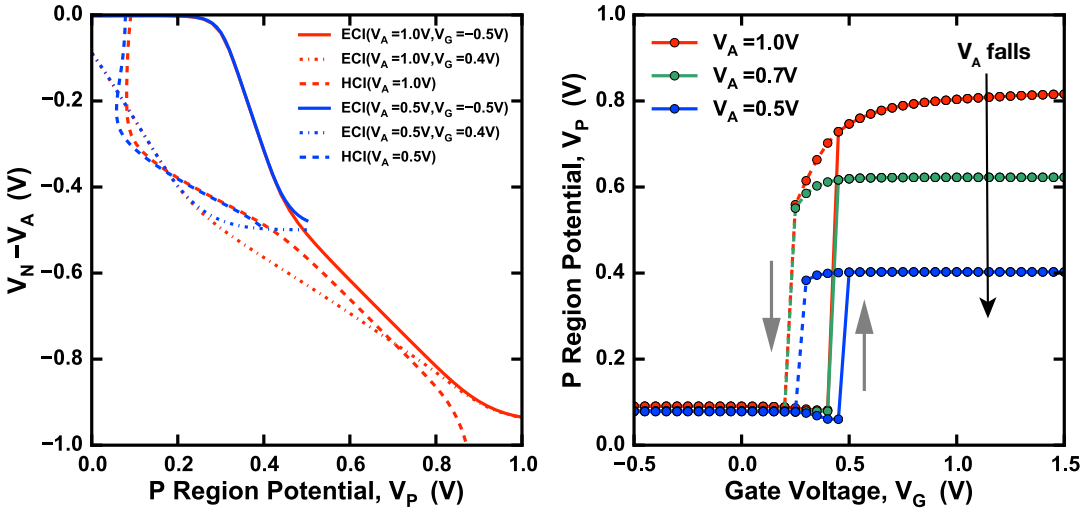
4.2.5 Dependence on Anode Voltage

The effect of V_A on the equivalent circuit model is also examined. Equations (3.5), (3.6), (3.13), and (3.14) imply that V_A does not affect transfer curves. This is demonstrated in the simulated transfer curves at V_A values shown in Fig. 4.9(a). The positional relationship between the transfer curves is maintained, hence V_{on} and V_{off} of the equivalent circuit model hardly change [Fig. 4.9(b)].

Figure 4.10(a) shows the simulated V_P-V_G characteristics in MGT at various V_G values from 0.5 to 1.0 V. It is confirmed that V_{on} and V_{off} of MGT do not shift as well.

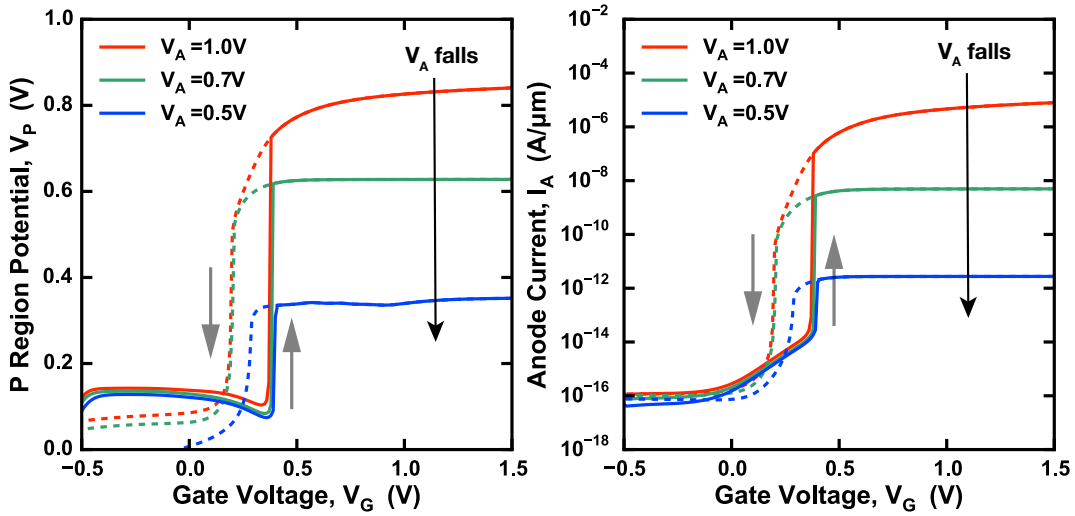
Since $(V_A - V_N)$ and V_P are close to V_A at the on state, the on-sate current in MGT decreases exponentially as V_A decreases, as inferred from Eqs. (3.1) and (3.10). This tendency is confirmed in MGT [Fig. 4.10(b)].

The current in MGT corresponds to the body current I_B in PNBTFET, so the on-state I_B can be suppressed by lowering the body terminal voltage V_B; the constant standby power



(a) (b)

Figure 4.9: (a) Simulated transfer curves and (b) V_P-V_G characteristics of the equivalent circuit model at various V_A values. $L_P = 2.0\,\mu\text{m}$, $N_P = 7 \times 10^{17}\,\text{cm}^{-3}$, $L_N = 0.5\,\mu\text{m}$, $N_N = 10^{20}\,\text{cm}^{-3}$.



(a) (b)

Figure 4.10: (a) V_P-V_G and (b) I_A-V_G characteristics at various V_A values in whole MGT simulation. $L_P = 2.0\,\mu\text{m}$, $N_P = 7 \times 10^{17}\,\text{cm}^{-3}$, $L_N = 0.5\,\mu\text{m}$, $N_N = 10^{20}\,\text{cm}^{-3}$.

dissipation in PNBTFET can be greatly reduced. In MGT in Fig. 4.10, the on-state power dissipation is reduced by about 10^{-7} times by lowering V_A from 1.0 to 0.5 V.

However, there is trade-off that the V_P variation (ΔV_P) decreases with V_A, so that the height of the abrupt SS and the average SS reduces. In PNBTFET, lowering V_B degrades ΔV_P and a multiplier α in Eq. (2.1). Consequently, rise in drain current at switching degrades, as seen in Fig. 2.3. In the MGT in Fig. 4.10, m is around 1.8, and rise in V_P (ΔV_P) is 0.51 V at $V_A = 0.7$ V, and 0.22 V at $V_A = 0.5$ V. If this MGT is applied to PNBTFET, α is estimated to be over 5×10^4 at $V_A = 0.7$ V, and over 10^2 at $V_A = 0.5$ V; an abrupt SS in PNBTFET will occur over 4 decades at $V_A = 0.7$ V, and over 2 decades at $V_A = 0.5$ V.

4.2.6 Dependence on Minority Carrier Lifetimes

The hysteresis width is equal to the V_G extent in which the equivalent circuit model is bistable, and is sensitively affected by subtle change in the positional relationship between the ECI and HCI transfer curves. It is inferred that if the ECI and HCI transfer curves are straight so that the ECI and HCI transfer curves respectively have only I and III regions [labeled in Fig. 3.3(a)], the hysteresis width will be small because the transfer curves will cross with almost parallel relationship. In order to realize this situation, generation-recombination current should be suppressed. Generation-recombination current in a PN junction diode is given as

$$I_{\mathrm{gr}} = I_{\mathrm{gr0}} \left[\exp\left(\frac{qV}{2kT} \right) - 1 \right], \tag{4.1}$$

with

$$I_{\mathrm{gr0}} = \frac{Aqn_i W_d}{\tau_n + \tau_p}, \tag{4.2}$$

where A is the cross-sectional area of the diode, W_d is the depletion layer width, and τ_n and τ_p are the electron lifetime in P region and the hole lifetime in N region, respectively[2]. Therefore, minority carrier lifetimes τ_n and τ_p should be extended to straighten the transfer

curves.

Figure 4.11(a) shows the simulated transfer curves at $V_G = -0.5\,\mathrm{V}$ at various minority carrier lifetimes. In the parameter 1, the electron lifetimes in the anode P^+ region (τ_{n1}) and in the inner P region (τ_{n2}) are 3×10^{-13} and $3 \times 10^{-10}\,\mathrm{s}$, respectively, and the hole lifetimes in the cathode N^+ region (τ_{p1}) and in the inner N region (τ_{p2}) are 3×10^{-11} and $3 \times 10^{-10}\,\mathrm{s}$, respectively. The minority carrier lifetimes in the parameter 2 are 10 times larger than those in the parameter 1, and those in parameter 3 are 100 times larger than those in the parameter 1. It is confirmed that as lifetimes extend, the bending point in the ECI transfer curve shifts to lower V_N, and one in the HCI transfer curve shifts to lower V_P, as predicted. However, the hysteresis width in the equivalent circuit model does not reduce, and V_{on} and V_{off} fall, as shown in Fig. 4.11(b). In fact, minority carrier lifetimes affect not only generation-recombination current but also bipolar transistor current; as lifetimes extends, the current gains of NPN and PNP transistor are enhanced, so the ECI transfer curve shifts downward and the HCI transfer curve shifts upward. As a result, the transfer curves approach each other, and the threshold voltages are lowered. The cause of increase in the hysteresis width is considered that the ECI transfer curve is relatively insensitive to V_G at low V_G. ECI transfer curves tend to be modulated slowly when it starts to be modulated by V_G, as confirmed in the transfer curves shown in Figs. 4.11(c) and 4.11(d). The transfer curves in the parameter 1 have two stable points at high V_G, so the V_G extent in which the equivalent circuit model is bistable is narrow [Fig. 4.11(c)]. On the other hand, the transfer curves in the parameter 3 have two stable points when the ECI transfer curve has just started to be modulated at low V_G [Fig. 4.11(d)].

Figure 4.12 shows simulated V_P-V_G characteristics at various minority carrier lifetimes in whole MGT simulation. The minority carrier lifetimes in the MGT correspond to those in the equivalent circuit model in Fig. 4.11. It is also confirmed in MGT that as lifetimes extend, the threshold voltages fall and the hysteresis width increases. However, the MGT in the parameter 3 does not turn off one it turns on as opposed to the corresponding

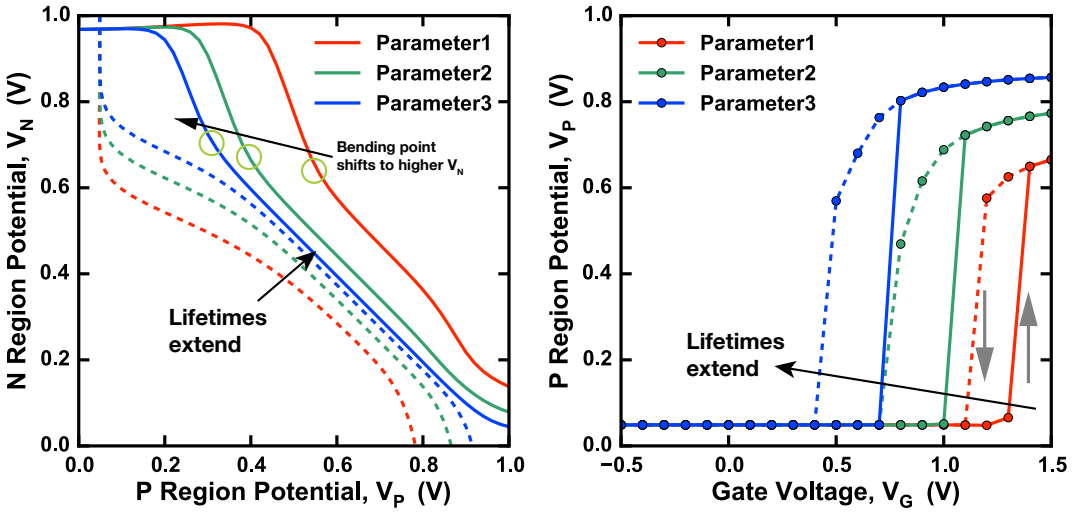


Figure 4.11: (a) Simulated transfer curves at $V_G = -0.5\,\mathrm{V}$ and (b) V_P-V_G characteristics at various minority carrier lifetimes. In the parameter 1, τ_{n1}, τ_{n2}, τ_{p1}, and τ_{p2} are 3×10^{-13}, 3×10^{-10}, 3×10^{-11}, and $3 \times 10^{-10}\,\mathrm{s}$, respectively. The lifetimes in the parameter 2 are 10 times larger than those in the parameter 1, and those in parameter 3 are 100 times larger. (c) and (d) are the simulated transfer curves at various V_G values in the parameter 1 and 3, respectively. $V_A = 1.0\,\mathrm{V}$, $L_P = 2.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

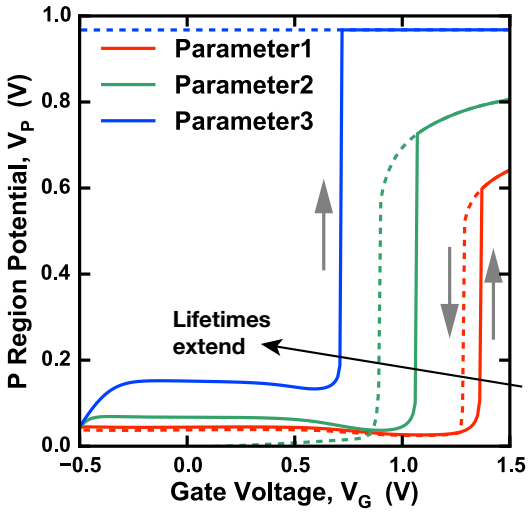


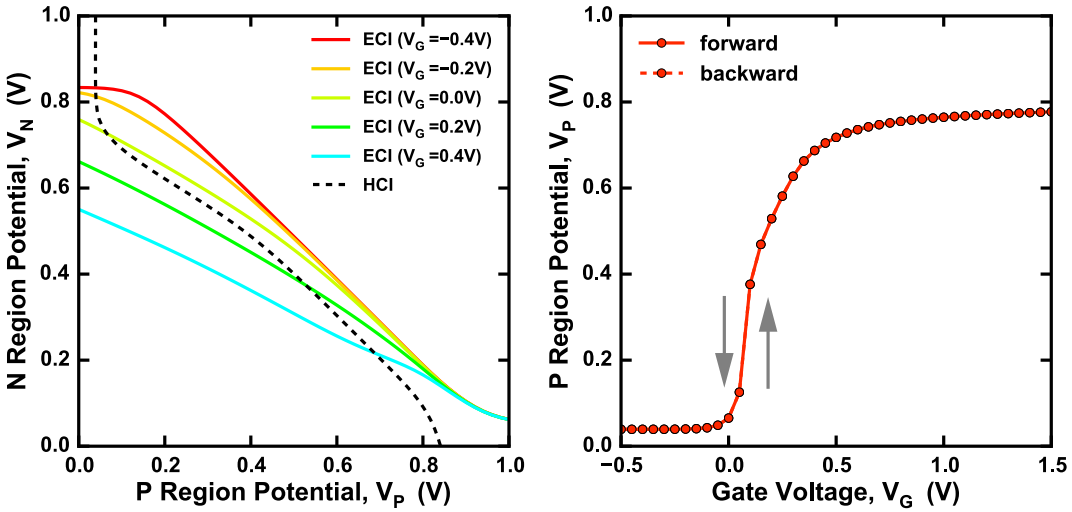
Figure 4.12: V_P-V_G characteristics at various minority carrier lifetimes in whole MGT simulation. In the parameter 1, τ_{n1}, τ_{n2}, τ_{p1}, and τ_{p2} are 3×10^{-13}, 3×10^{-10}, 3×10^{-11}, and 3×10^{-10} s, respectively. The lifetimes in the parameter 2 are 10 times larger than those in the parameter 1, and those in parameter 3 are 100 times larger. $V_A = 1.0\,\mathrm{V}$, $L_P = 2.0\,\mu\mathrm{m}$, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 0.5\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

equivalent circuit model in Fig. 4.11, and this is considered to be caused by the inaccuracy of the TCAD models for the equivalent circuit model.

Minority carrier lifetimes affect the current gain of bipolar transistors, so it is necessary to regulate other design parameters as well as lifetimes.

4.3 Optimizing MOS-Gated Thyristor

We have shown the effects of L_P, L_N, N_P, N_N, V_A, and minority carrier lifetimes on the characteristics of MGT and the equivalent circuit model. The effects of design parameters on MGT and the equivalent circuit model show good correlation, so the characteristic of MGT can be deduced from the behavior of ECI and HCI transfer curves. When the design parameters of ECI (L_P, N_P) and HCI (L_N, N_N) are applied to those of MGT, the MGT



(a) (b)

Figure 4.13: (a) Simulated transfer curves and (b) V_P-V_G characteristics of the optimized equivalent circuit model. $V_A = 1.0\,\mathrm{V}$, $L_P = 4.0\,\mu\mathrm{m}$, $N_P = 5 \times 10^{17}\,\mathrm{cm}^{-3}$, $L_N = 4.0\,\mu\mathrm{m}$, $N_N = 10^{20}\,\mathrm{cm}^{-3}$, τ_{n1}, τ_{n2}, τ_{p1}, and τ_{p2} are 3×10^{-11}, 3×10^{-8}, 3×10^{-9}, and $3 \times 10^{-8}\,\mathrm{s}$, respectively.

shows characteristics similar to the characteristics of the equivalent circuit model.

MGT is required to have low threshold voltages and small hysteresis width so that PNBTFET operates at an ultralow supply voltage. We consider that the hysteresis width can be reduced by increasing minority carrier lifetimes while adjusting the positions of the transfer curves by changing dimensions and concentrations.

An example of optimized transfer curves of ECI and HCI is shown in Fig. 4.13. The minority carrier lifetimes are same as the parameter 3 (cf. Subsection 4.2.6); τ_{n1}, τ_{n2}, τ_{p1}, and τ_{p2} are 3×10^{-11}, 3×10^{-8}, 3×10^{-9}, and $3 \times 10^{-8}\,\mathrm{s}$, respectively. The transfer curves are straightened by extending lifetimes and adjusted so that the equivalent circuit model turns on and off at low V_G [Fig. 4.13(a)]. The equivalent circuit model keeps on having one stable point thanks to the straightened transfer curves, so it does not have a hysteresis window as shown in Fig. 4.13(b).

Now, the design parameters of the optimized equivalent circuit model are applied to

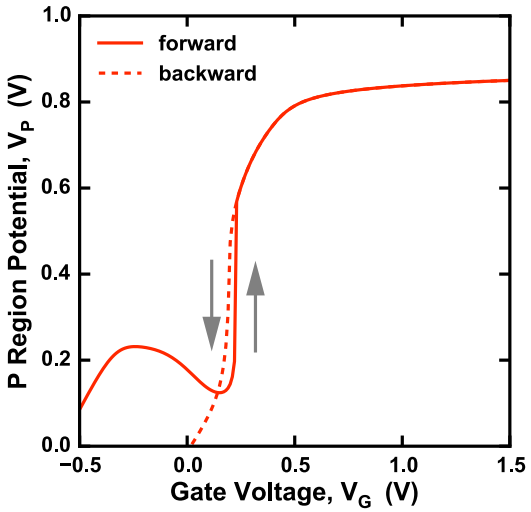


Figure 4.14: V_P-V_G characteristics of the optimized MGT. The design parameters in the MGT are same as those of the optimized equivalent circuit model in Fig. 4.13.

MGT. Figure 4.14 shows the simulated V_P-V_G characteristic of the optimized MGT. The MGT turns on and off around $V_G = 0.2\,\mathrm{V}$ with negligible hysteresis width. Thus, it is demonstrated that MGT with low threshold voltages and small hysteresis is designed by utilizing the equivalent circuit model.

4.4 Thermal Stability of MOS-Gated Thyristor

For MOSFETs, the thermal stability of the threshold voltage is an important topic[3, 4, 5]. In this work, the temperature dependence of the equivalent circuit model and MGT is investigated by TCAD simulations.

Figure 4.15 shows the simulated V_P-V_G characteristics at three different temperatures in whole MGT simulation. It is confirmed that as temperature rises, V_{on} and V_{off} approach each other with the average threshold voltage maintained, and the hysteresis width reduces. Note that the temperature dependence of PNBTFET is different from

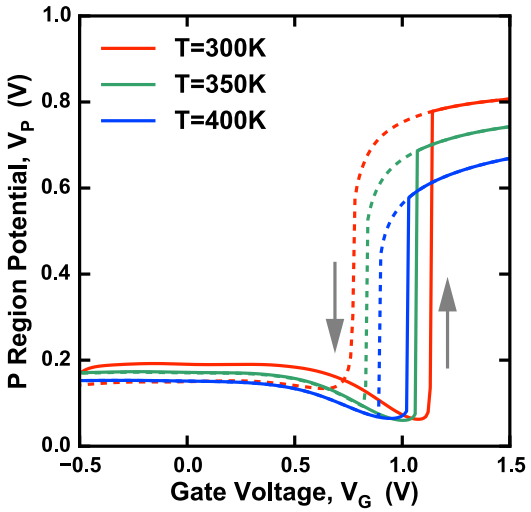
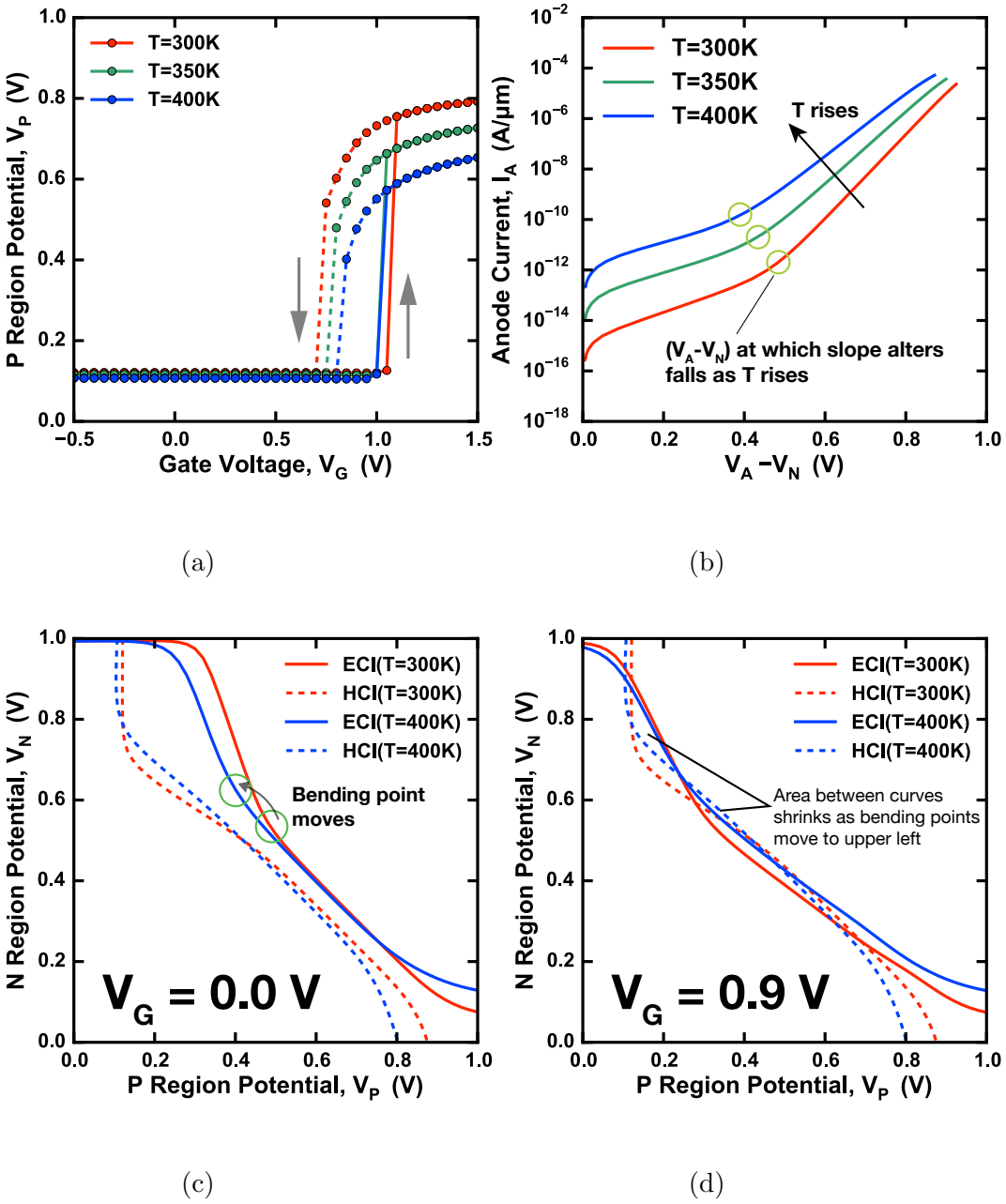


Figure 4.15: V_P-V_G characteristic at various temperatures in whole MGT simulation. V_A = 1.0 V, L_P = 2.0 µm, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, L_N = 0.5 µm, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

that of a conventional MOSFET, in which the threshold voltage falls as temperature rises[3].

The mechanism underlying the temperature dependence of MGT can be explained by the equivalent circuit model. Figure 4.16(a) shows the simulated V_P-V_G characteristics at three different temperatures in the equivalent circuit model. The threshold voltages approach the center of the hysteresis window also in the equivalent circuit model. Figure 4.16(b) shows the anode current versus the voltage applied to the PN junction between the anode and N region ($V_A - V_N$) in the ECI TCAD model. It is confirmed that the $V_A - V_N$ at which the dominant current, which is desribed as Eq. (3.1), switches between diffusion current and generation-recombination current falls as temperature rises. As a result, the bending point of the ECI tansfer curve shifts to lower V_N value, as shown in Fig. 4.16(c). Similarly, the bending point of the HCI transfer curve shifts to lower V_P value. Consequently, when the ECI and HCI transfer curves cross, the area between the two transfer curves becomes smaller as temperature rises [Fig. 4.16(d)], hence the hysteresis



(a) (b)

(c) (d)

Figure 4.16: (a) Simulated V_P-V_G characteristics and (b) anode current I_A versus $(V_A - V_N)$ in the equivalent circuit model at various temperatures. (c) Simulated transfer curves at $V_G = 0.0$ and (d) at 0.9 V. $V_A = 1.0$ V, $L_P = 2.0\,\mu$m, $N_P = 2 \times 10^{18}\,\mathrm{cm}^{-3}$, $L_N = 0.5\,\mu$m, $N_N = 10^{20}\,\mathrm{cm}^{-3}$.

width reduces. In addition, it is confirmed that the average threshold voltage of MGT and the equivalent circuit model is insensitive to temperature as opposed to MOSFETs. It is considered that the both sides of the PN junction current in MGT exponentially increases with temperature, and V_P and V_N are balanced by these currents.

4.5 Summary

The effects of design parameters (i.e., L_P, L_N, N_P, N_N, V_A, and minority carrier lifetimes) on MGT and the equivalent circuit model are examined by TCAD simulation, and the tendencies of the parameter dependence have remarkable similarities between MGT and the equivalent circuit model. Moreover, it is demonstrated that the parameter dependence is conveniently used in designing optimum MGT, which has low V_{on} and V_{off} with negligible hysteresis width.

The equivalent circuit model also explains the mechanism of the thermal stability of MGT, in which the average of the threshold voltages of MGT hardly changes but the hysteresis width reduces as temperature rises.

References

[1] Synopsis, Sentaurus Device User Guide Version I-2013.12 (2013).

[2] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 2009) 2nd Edition.

[3] G. Groeseneken, J. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, IEEE Electron Device Lett. **11**, 329 (1990).

[4] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, IEEE J. Solid-State Circuits **36**, 1559 (2001).

[5] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, IEEE Trans. Electron Devices **57**, 620 (2010).

Chapter 5

Conclusions

In this thesis, we aimed to analyze the operation mechanism of PNBTFET, which shows an abrupt SS at an ultralow supply voltage, and focused on the MGT structure inherent in PNBTFET because MGT plays a significant role in realizing an abrupt SS in PNBTFET.

In Chapter 3, we proposed a new equivalent circuit model of MGT, which decomposes the feedback system in MGT into a simple cross-coupling of two voltage inverters, i.e., ECI and HCI. ECI and HCI are simulated by using TCAD models, which are based on MGT structure, and it is confirmed that the behavior of ECI and HCI transfer curves provides good explanations for the abrupt switching behavior and the hysteresis of MGT. Moreover, the analytical model for ECI and HCI provides an insight into the behavior of the transfer curves.

In Chapter 4, it is demonstrated that the effects of design parameters on MGT correlate with those on the equivalent circuit model. The parameter dependence can be conveniently used in determining design parameters of MGT and PNBTFET. The threshold voltages V_{on} and V_{off} can be regulated by altering design parameters in MGT, and the on-state body current in PNBTFET can be exponentially reduced by lowering the body terminal voltage. Thus, the equivalent circuit model provides a clear guide in designing MGT

with optimum threshold voltages. The equivalent circuit model will make it possible to design ultralow-power PNBTFETs by integrating the optimized MGTs into PNBTFETs. However, the TCAD models of ECI and HCI, which respectively have extended N and P regions, does not exactly predict the threshold voltages of MGT, as seen in the L_P dependence. Therefore, further study on how to improve the TCAD models of ECI and HCI is needed.

List of Publication and Presentations

Publication

[1] Daiki Ueda, Kiyoshi Takeuchi, Masaharu Kobayashi, and Toshiro Hiramoto, "Optimizing MOS-gated thyristor using voltage-based equivalent circuit model for designing steep-subthreshold-slope PN-body-tied silicon-on-insulator FET," Japanese Journal of Applied Physics (to be published).

Presentations at International Conferences

[1] Daiki Ueda, Kiyoshi Takeuchi, Masaharu Kobayashi, and Toshiro Hiramoto, "Carrier-Separated Equivalent Circuit Modeling for Steep Subthreshold Slope PN-Body Tied SOI FET," IEEE Silicon Nanoelectronics Workshop (SNW), Kyoto, June 2017, p.13.

[2] Daiki Ueda, Kiyoshi Takeuchi, Masaharu Kobayashi, and Toshiro Hiramoto, "Optimizing MOS-Gated Thyristor using Voltage-Based Equivalent Circuit Model for Designing Steep Subthreshold Slope PN-Body Tied SOI FET," International Conference on Solid State Devices and Materials (SSDM), Sendai, September 2017,

p.243.

Presentations at Domestic Conferences

[1] 植田大貴，竹内潔，小林正治，平本俊郎，“急峻サブスレッショルドスロープ PN-Body Tied SOI FET の最適化に向けた MOS-Gated Thyristor の電圧ベース等価回路モデル”，第 78 回応用物理学会秋季学術講演会，福岡，2017 年 9 月.

[2] 植田大貴，竹内潔，小林正治，平本俊郎，“MOS-Gated Thyristor の電圧ベース等価回路モデルを用いた急峻スロープ PN-Body Tied SOI FET のパラメータ依存性の検討”，第 65 回応用物理学会春季学術講演会，東京，2018 年 3 月発表予定.