Master's Degree Dissertation

Design, Fabrication and Measurement of Electrically-Pumped Wavelength-Scale Metal-Clad Semiconductor Laser with Potential for Waveguide Coupling

（導波路結合を可能にする電流励起波長スケール金属クラッド半導体レーザの設計、作製と評価）

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Abstract

Wavelength-scale metal-clad semiconductor lasers have been of considerable interest as potentially ideal light sources for on-chip optical interconnects and photonic integrated circuits. Eligible device should provide continuous-wave electrically-pumped lasing under room-temperature with integration to waveguides, which gives advancement in terms of energy efficiency, modulation response, as well as high integration density from modern fabrication techniques.

This thesis aims at contributing to research on electrically-pumped wavelength-scale metal-clad semiconductor lasers with potential for waveguide-coupling, from both device design and fabrication perspectives. We present design of novel waveguide-coupling schemes with comprehensive numerical computation including both electromagnetic analysis and thermodynamic analysis, and an extensive investigation in fabrication techniques for wavelength-scale metal-clad semiconductor lasers to achieve continuous-wave electrically-pumped room-temperature lasing.

For device design, we propose a wavelength-scale silver-clad InP/InGaAs cavity coupled to silicon-on-insulator (SOI) waveguide with thin InP lower-cladding layer for improved heat dissipation under typical working conditions. We present design of an integrated feedback stub for external tuning of the Q-factor for such waveguide-coupled lasers without sacrificing its figure-of-merit or heat-management performance, and we demonstrate more than 5-fold Q-factor improvement of the cavity through finite-dimension time-domain (FDTD) simulation results. In addition, we provide theoretical analysis of the Q-factor-tuning mechanism with coupled-mode theory, and the modeling results agree well with those obtained from FDTD simulations.

In the case of device fabrication and measurement, we present extensive investigation of the complete fabrication process of silver-clad InP/InGaAs cavities on InP substrate packaged with gold electrodes eligible for electrically-pumped operation. We demonstrate several improvements in the fabrication process including semiconductor side-wall verticality and silver quality, and provide detailed discussions on possible future improvements. We present I-V measurement and electroluminescence measurement results of selected devices after fabrication. In particular, cavity enhancement in room-temperature of a silver-clad InP/InGaAs circular light emitter of volume 0.52 λ^3 is achieved under continuous wave electrically-pumping.

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Chapter 1

Background: What Leads us to Metal-Clad Semiconductor Lasers

1.1 Introduction

This chapter elaborates the motivation of studying design and fabrication of wavelength-scale metal-clad semiconductor lasers with potential of being coupled to waveguide in integrated photonic circuits.

Before we get into the technical problem, in section 1.2, we briefly explain the research motivation from a more philosophical understanding of the problem we face, so as to clarify what benefits this project intends to bring to the world, from a personal perspective of academic research in electrical engineering.

Then, in section 1.3, we would go into the details of the problem, and lead the audience into the role that metal-clad semiconductor laser tries to fit in. After that, in section 1.4, we would provide a brief review of previous research of such metal-clad semiconductor lasers, covering several different works and comparing their results in term of solving the problem discussed in section 1.3.

1.2 Research Motivation: A Personal Understanding

Electrical engineering sets off to tackle problems that could be solved using novel electrical devices. Different from engineering research in the industry, engineering research in academics would target on research projects that may lead to products that come to the market decades ahead of time, and seek for solutions of a problem at higher dimension, or say, would benefit mankind in a longer term. In my opinion, such problems drop into three main categories, to realize novel functionality that is previously unavailable, to develop new technology so as to reduce cost or save energy replacing existing solutions to a given problem, or to demonstrate applications of a new discovery in physics that may potentially raise new problem or develop new technology.

The information and telecommunication industry has been growing rapidly during the past decades and has brought huge change in human's everyday life. It becomes an essential part of almost any urban lifestyle, revolutionizing in every aspect from components of novel electronic devices to computation powers of huge data centers. Human desire

increases inevitably, calling for faster communication and service of larger scale, thus providing a potential market for such solutions. Among them, low-energy on-chip light source for optical interconnects and telecommunication applications is one of a research problem that attracts major attention. This is a problem that drops in the second category, that is, developing new technology so as to reduce cost or save energy replacing existing solutions to a given problem. I am personally interested in problems in this category, because it demonstrates wisdom applied to live life in better quality with lower consumption of nature resources, in the long term. A concept as simple as to “live more with less”. This is, in my opinion, the only category that saves mankind from dying of unstoppable desire and losing humanity. Though not usually cared for nowadays, I still feel strongly obligated to clarify this motivation, and therefore this has become a short explanation of why low-energy on-chip light source for optical interconnects and telecommunication applications is worth researching on.

1.3 Global Energy Consumption and Low-Energy On-Chip Light Source

In this section, I would like to explain briefly why low-energy on-chip light source for optical interconnects and telecommunication applications falls in the second category, and what problem in energy it is truly served for.

1.3.1 Increasing Demand in Energy-Efficient Communication

The data traffic in long distance and short distance are growing rapidly in recent decades, especially after the development of internet. Total internet traffic in 2016 is estimated at ~280 Tb/s, while in 2012 inside a data center the capacity would be estimated for larger than 1Pb/s. As an example, one graphics processor chip has a peak data rate on and off the chip of 1.4 Tb/s, which shows how heavy the interconnect traffic at shorter distances deeper inside information processing machines could be [1, 2].

As to handle such traffic to communicate information, at longer or shorter distance, energy is consumed. In 2012, it was estimated that information processing and computing including data centers, personal computers and networks consume 4.6 % of world electricity production, and the growth rate of consumption exceeds the growth rate in electricity generation capacity. In other words, the energy consumption will be larger than we could afford with current growth rate. Thus, we would need to reduce the total energy consumption.

Operation	Energy per bit
Wireless data	10 – 30μJ
Internet: access	40 – 80nJ
Internet: routing	20nJ
Internet: optical WDM links	3nJ
Reading DRAM	5pJ
Communicating off chip	1 – 20 pJ
Data link multiplexing and timing circuits	~ 2 pJ
Communicating across chip	600 fJ
Floating point operation	100fJ
Energy in DRAM cell	10fJ
Switching CMOS gate	~50aJ – 3fJ
1 electron at 1V, or 1 photon @1eV	0.16aJ (160zJ)

Table I Energies for communications and computations [1]. WDM- wavelength division multiplexing, DRAM – dynamic random-access memory, CMOS- complementary metal-oxide-semiconductor transistor. Refer to [1] for detailed notes and references of each data.

To reduce the total energy consumption with a growing data rate, the only solution would be to reduce the energy per bit in communication and processing. That is to say, if we can communicate more efficiently, we can communicate in higher capacity with lower consumption of total energy. Table I shows the approximate energies per bit in various processing and communication operations using electrical circuits [1].

1.3.2 Low-Energy On-Chip Light Source

From various previous studies, it is shown that the energy consumption of current electrical interconnects can typically range from picojoules-per-bit to much higher values. The energy efficiency of electrical circuits has a lower limit, since that one has to inevitably charge the line or other electromagnetic medium to the signal voltage.

This is where optics comes to play a competitive role. In optics, one only has to charge or discharge the optoelectronic detector or any equivalent device, and the detection of light is a quantum-mechanical process of absorbing photons, instead of a classical process of measuring the voltage of the light beam. That is to say, the photodetector counts photons, instead of measuring voltage. Also, optics allows higher densities of information to flow (higher bandwidth), which has already been adopted in longer distance communications. With wavelength division multiplexing (WDM) or space division multiplexing (SDM), the information transmission capacity is further expanded.

With such potential in revolutionary reduction in energy consumption, optical interconnect has attracted much attention in research during the past decades. The key challenge of

outperforming electrical interconnect would be to realize the lower energy-per-bit as promised. In other words, we should make optoelectronic device that consumes lower energy than the energy required to charge an equivalent length of electrical line.

One of the key component in optical interconnection links is an optical output device that can (1) operate at low energy but deliver the power efficiently, and (2) emit power in a form that can be efficiently delivered to the photodetector at the other end of the link, preferably to emit light into a single spatial mode.

Lasers and light-emitting diodes (LEDs) in wavelength-scale naturally become competitive choices in realizing the required standards for optical output device.

As for lasers, semiconductor lasers today are perfect candidates as they have high gain per unit length. The energy per bit of a laser less than 50 fJ/bit is required for competing with the current electrical interconnects [1]. This could be realized by using advanced structures such as photonic crystal, nano-ring structures and so on [3].

As for LEDs, despite their typical optical inefficiency from emitting into large numbers of spatial modes, it comes into attention in this case due to its advantage in small dimensions. LED with subwavelength volumes can emit into only one spatial mode (or two, including polarization), which is required in low-energy high-efficiency optical communication. Small LEDs also attract much recent attention due to the Purcell enhancement related [4, 5], as in smaller dimension there proves to be enhancement of the spontaneous rate emission into the modes with strong optical concentration. Examples include nanoLEDs with antenna enhancement [6], nanoLEDs coupled to InP waveguides [7] and so on.

1.4 Wavelength-Scale Metal-Clad Semiconductor Lasers

In search for an ideal low-energy on-chip light source, we would look into the light emitter in terms of integration density, speed and energy efficiency. Although hybrid III-V/Si lasers using either hybrid growth or wafer bonding techniques have been demonstrated [8], and largely improved confinement in small footprint has been demonstrated using novel designs of ring structures [9] or photonic crystal structures [10, 11], the device footprints are still relatively large and power consumptions are still larger than required.

Another powerful approach, however, has also been under active research during the past decade. That is to use a metal-cladding layer outside the semiconductor laser cavity for improving the device performance for devices of small footprint at wavelength scale. Such wavelength-scale metal-clad semiconductor lasers are promising because of their high integration density, fast modulation, and ease for electrical-pumped operation [12-14].

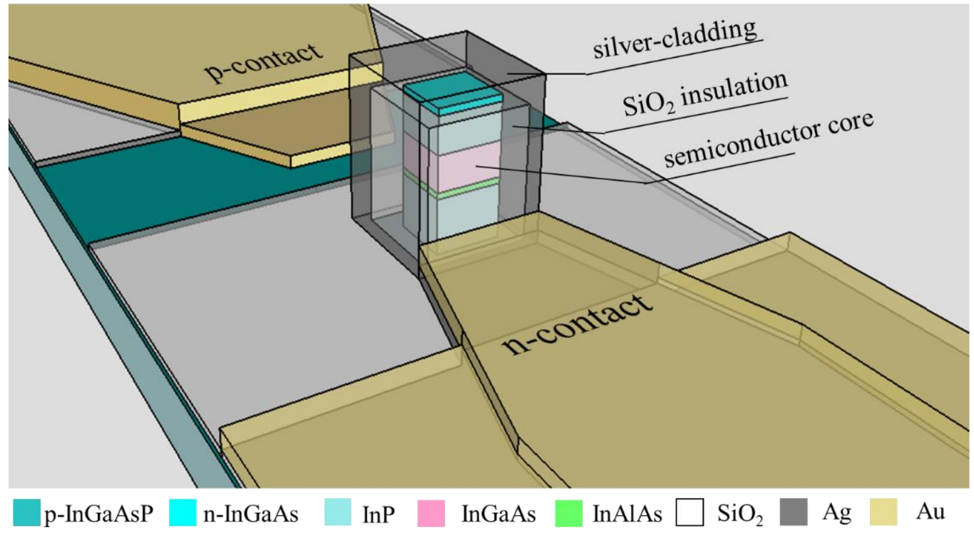


Figure 1.1 Schematic of a typical wavelength-scale metal-clad semiconductor laser compatible for electrically-pumped operation. In this schematic, the semiconductor core is formed by InP/InGaAs/InP stack, and the insulation layer is formed by SiO_2, with a metal-cladding coated by silver.

Figure 1.1 shows a schematic of a typical wavelength-scale metal-clad semiconductor lasers compatible for electrically-pumped operation. Various types of metal-clad semiconductor lasers have been demonstrated experimentally by using cylindrical [15-22], narrow waveguide [23], rectangular [24, 25], and capsule-shaped [26, 27] geometries.

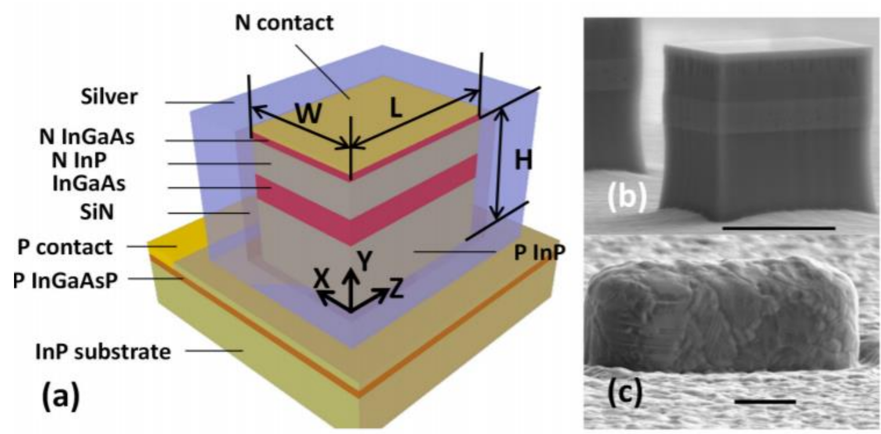


Figure 1.2 Structures of electrically-pumped wavelength-scale metal-clad semiconductor laser[24]. (a) Layer compositions of the silver-clad InP/InGaAs rectangular semiconductor cavity. (b) Scanning electron microscope (SEM) image of the semiconductor core, (c) SEM image of the cavity after coating with SiN and silver. Scale bars in (b) and (c) are both 1 um.

Electrically-pumped wavelength-scale metal-clad semiconductor laser was firstly demonstrated for room-temperature continuous-wave operation in 2013, reported by K.Ding *et al* [24]. As shown in Fig 1.2, this laser cavity has a cavity volume of $0.67\lambda^3$ (λ =

1591 nm) including the SiN insulation layer. The linewidth is measured as 0.5 nm at RT, giving a Q-value of 3182 and a turn-on threshold around 1.1 mA.

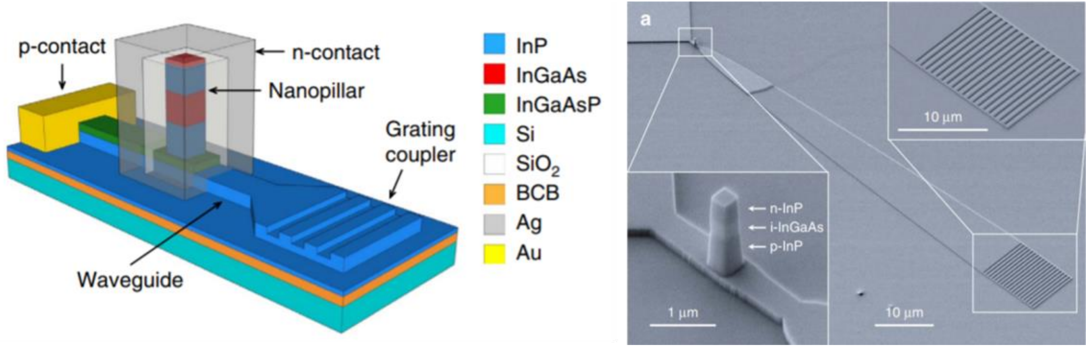


Figure 1.3 Design of the metal-clad nanopillar LED on silicon substrate coupled to InP-waveguide. The left graph shows schematic representation of the design, while the right shows the SEM image of the fabricated device before metallization with enlarged view of the nanopillar on top of the waveguide and the grating coupler connected downstream [28].

More recently, metal-clad nanopillar LED on a silicon substrate coupled to an InP-membrane waveguide has been demonstrated, showing the potential of metal-clad nanoLEDs for efficient low-power interconnects operating at Gb/s data rates [28]. As shown in Fig 1.3, this device is composed of layers stack from top to bottom as: n-InGaAs(100nm) /n-InP(350nm) /InGaAs(350nm) /p-InP(600nm) /p-InGaAsP(200nm) /InP(250 nm) /SiO_2 /BCB /SiO_2 /Si. It is reported to give nW measured output powers at ~100 µA current injection levels, at room temperature.

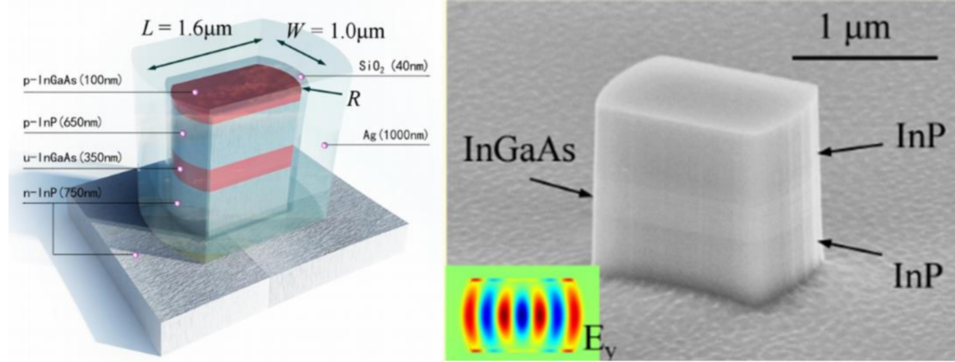


Figure 1.4 Design of the metal-clad InP/InGaAs semiconductor laser with capsule-shaped cavity. The left graph shows schematic representation of the cavity layer compositions and shaping design, while the right shows the SEM image of the fabricated semiconductor core before metal deposition, with inset showing electric field profile of the TE-like mode as of a top-view cross-section inside the active layer [29].

Apart from common rectangular and square cavities, active research in our group has recently proved some special properties in wavelength-scale metal-clad semiconductor laser with capsule-shaped cavity. As shown in Fig 1.4, this device is composed of a cavity

with capsule-shape introduced to reduce scattering loss and improve TE-mode competence. With pulsed-mode optical pumping at room temperature, this cavity shows spectrum with two peaks at 1535 nm and 1522 nm respectively, and its threshold power of TE-mode lasing is estimated to be 230 μW [29].

From previous efforts, research of wavelength-scale metal-clad semiconductor light emitters have made much progress during the past years. In order to achieve its best application so as to tackle the problem described in section 1.3, serious improvement is needed in terms of (1) efficient coupling of the laser with Si-based or InP-based waveguide for integrated fabrication and compatibility with downstream photonic circuits, (2) electrically-pumped operation of the wavelength-scale metal-clad semiconductor laser under room temperature with lower current threshold and higher efficiency.

In this thesis work, research of wavelength-scale metal-clad semiconductor light emitter is presented. We present our endeavor in (1) theoretical and comprehensive simulation work in designing a novel waveguide-coupling scheme with integrated feedback stub for wavelength-scale metal-clad semiconductor laser, and (2) fabrication and measurement of electrically-pumped wavelength-scale silver-clad InP/InGaAs laser under room-temperature. These two aspects serve to investigate possible improvements mentioned in the above paragraph accordingly, aiming for realization of truly energy-efficient on-chip light source coupled to waveguide for optical interconnects.

1.5 Thesis Outline

This thesis is organized in six chapters as described below.

Chapter 1 gives an introduction to the motivation of this research work, from a general perspective of what problem we face, to details of background research in previous works in this field of wavelength-scale metal-clad semiconductor lasers. It also introduces the scope we work on and the potential applications it may bring in to solve the problem.

Chapter 2 explains the design of metal-clad semiconductor laser cavity in this work. Comprehensive analysis including both electromagnetic and thermodynamic simulation of the cavity structure is presented and discussed, in search for a cavity with improved optical performance as well as thermal management.

Chapter 3 presents the design of metal-clad semiconductor laser cavity coupled to a silicon-on-insulation (SOI) waveguide. Novel design of a feedback stub on one end of the waveguide is proposed and discussed with finite-dimension time-domain (FDTD) simulation which gives detailed analysis of its optical performance. Theoretical explanation using coupled-mode theory is presented and compared with the simulation results.

Chapter 4 describes the fabrication of metal-clad semiconductor laser cavity. Detailed procedures are presented step by step for the fabrication of silver-clad InP/InGaAs laser cavity with various dimensions and shapes integrated with electrodes ready for electrically-

pumped operation, with discussions on fabrication quality and possible future improvements.

Chapter 5 presents the characterization of selected fabricated devices, including the electrical property measurement and optical property measurement. Room-temperature electrically-pumped lasing is observed in selected laser cavities, proving the advancement in device design as well as the improvement in fabrication quality.

Chapter 6 summarizes the main conclusions of the research presented in this thesis and provides an outlook on related future works.

Chapter 2

Design of Metal-Clad Semiconductor Lasers: Cavity Structures and Thermal Properties

2.1 Introduction

Many of the works mentioned in Chapter 1 of metal-clad semiconductor lasers have demonstrated high quality performance with low energy, but only under low temperature. However, as candidates of light source in integrated photonic circuits, it is inevitable to investigate the possibility of room-temperature operation for these lasers. Thermal considerations thus become an essential part in device design, as the device self-heating may be severe for these lasers due to small device size and high local current density. To improve this situation, the relationship of the thermal properties with the cavity structure needs to be studied in detail. In this chapter, we explain the design of metal-clad semiconductor laser cavities and conduct thermodynamic simulations for improving the cavity design with better heat dissipation.

In section 2.2, the structure of wavelength-scale metal-clad semiconductor laser cavity is explained, including its key components and the factors to be taken into consideration for an optimized cavity design. We present a silver-clad InP/InGaAs cavity with an advanced capsule-shape that could be coupled to silicon-on-insulator (SOI) waveguide.

Then, in section 2.3, we investigate the thermal properties of the silver-clad InP/InGaAs cavity with relation to cavity layer components. Thermodynamic analysis is carried out to study the temperature distribution and self-heating with different InP p-cladding layer thickness.

2.2 Cavity Structure

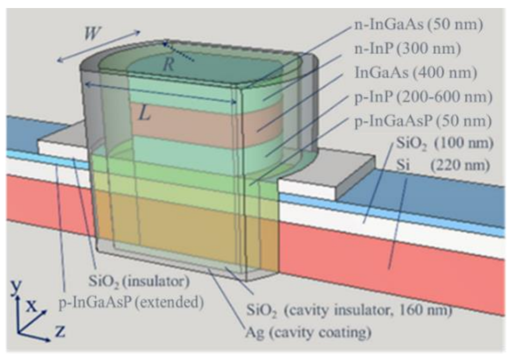


Figure 2.1 Design of a wavelength-scale silver-clad InP/InGaAs semiconductor laser cavity in capsule-shape.

As shown in Fig. 2.1, the laser cavity active layer is formed by InGaAs, with InP cladding on top and bottom serving as cladding. This design has been adopted from previous works in our laboratory, with serious efforts of optimizing each component [30]. Details of the cavity structure are explained as below.

Cavity Dimension The cavity dimension is set as in wavelength-scale, which means around 1.55 μm as of the desired working wavelength for InGaAs, aiming at applications in telecommunication fields. We set the cavity length L to be 1.1 μm and the cavity width W to be 0.84 μm. The cavity is basically rectangular in shape, forming a Fabry-Perot cavity through the horizontal direction along the longer side of the cavity. In addition, the cavity has a curvature of R/L = 1.4 (R is radius of curvature) at both ends of the sidewall to form a capsule-like shape. Such capsule-shaped cavity is proved to reduce corner scattering and improve the optical confinement as compared to strictly rectangular cavities of the same dimensions [26, 27].

Active Layer The active layer is formed by InGaAs, with its thickness designed as 400 nm. This value is expected to provide enough confinement and Q factor of the cavity, while not being too high to bring difficulty in device fabrication.

Cladding Layers Above and below the active layer, there are two InP cladding layers which provides optical confinement in the vertical direction for the cavity. Regarding their layer thickness, the same trade-off between optical property and fabrication feasibility exists. We consider them to be at least 300 nm thick from results of optical simulations. For the lower InP cladding layer, it appears that the thickness also affects the coupling of cavity to the waveguide beneath, if there is any, since the light is expected to be coupled evanescently. For this layer, higher thickness provides better optical confinement and cavity Q factor, but gives worse coupling efficiency to the waveguide. Apart from optical properties, we later find out that this layer thickness also affects the thermal property of the cavity significantly, thus, we would keep the value as a range of 200 nm – 600 nm for the time being, and leave the discussion of this parameter in section 2.3.

Contact Layers The cavity is designed to work under electrically-pumped operation. The active layer and two adjacent InP cladding layers form a p-i-n junction ready for electroluminescence. There should be contact layers next to the InP layers, providing proper current injection. The n-contact layer is formed by n-InGaAs with a doping of 2e19 cm^-3. The p-contact layer is formed by p-InGaAsP with a doping of 2e19 cm^-3. In this case, the device is chosen to be n-top, since the electron injection from silver to n-InGaAs is easier without any barrier, while hole injection from metal into p-InGaAs has a large barrier of nearly 1 eV. As a result, the upper InP is n-doped, with a 50-nm n-InGaAs layer on top, and the lower InP is p-doped, with a 50-nm p-InGaAsP at the bottom.

Insulation Layer Since the cavity will be later covered in metal-cladding, there ought to be an insulation layer surrounding the III-V core (but not on top or bottom), separating it from the metal-cladding to avoid heavy optical loss from metal absorption. The insulation layer can be formed with various materials, such as SiN or SiO_2. The choice of this insulation material depends on both optical and thermodynamic performance, as well as the ease of fabrication given the facilities available. The thickness of the insulation layer is also a critical parameter for the cavity performance. For smaller cavity of ~300 nm in diameter, the insulation layer is preferred to be gently thicker, about 175 nm, for higher quality factor [31]. However, for larger cavity, a thinner insulation layer reduces the cavity radiation loss into the substrate [31]. As SiO_2 has very low thermal conductivity, higher thickness may also bring in additional heat dissipation challenges. Thus, we use SiO_2 of about 70-100 nm in our design and fabrication.

Metal Clad A metal shield is covered all over the cavity, giving the name of "metal-clad" semiconductor cavity. Noble metal such as silver or gold would be preferred to act as a mirror-like structure, which is proved to bring strong optical confinement with relatively low loss, and to give better heat dissipation for the semiconductor structure in small size [15]. Silver is usually chosen, as it as it has lower loss under room temperature compared to gold or aluminum [30]. We also choose silver in our case, and it naturally acts as the cathode electrode adjacent to the n-InGaAs contact layer. In addition, very thin titanium is usually added as an adhesive layer underneath silver as silver may have poor adhesion to SiO_2 in real fabrication situation. The anode electrode, on the other hand, is chosen to be a gold layer, placed at some distance to the cavity and connected to the p-InGaAsP layer that is exposed through etching from the substrate. Since it would have not so much effect on the optical performance of the cavity itself, it is not included in this cavity model.

In the schematic shown in Fig 2.1, the cavity is seated on top of a silicon-on-insulator (SOI) waveguide at the bottom, which is proposed as a possible coupling scheme for downstream integration. SOI waveguide is chosen as it is compatible with the silicon technology and can be fabricated with standard techniques and low cost. In this design, the waveguide has a Si thickness of 220 nm, with a thin SiO_2 of 100 nm on top and a thick SiO_2 substrate at the bottom. Details of the integration with waveguide will be covered in Chapter 3.

2.3 Cavity Layer Composition and Thermal Analysis

The heating issue plays an important role for the room-temperature operation of the electrically-pumped metal-clad semiconductor laser given its small foot print in micrometer scale. The major heating sources in the device are explained as below [32].

Joule Heating This is the heating due to resistance in the semiconductor layers, and can be interpreted from its definition $Q = I^2R$. In this structure, larger Joule heating will be generated mainly by the lower InP cladding layer and the bottom p-contact layer. However, Joule heating only contributes to a small part of the self-heating generally.

Junction and Heterojunction Heating The junction and heterojunction heating is the heat generated by the voltage change at the layer junctions. Junction heating is the heat generated between the undoped layer and adjacent doped layers, at the top and bottom of active layer in this case. Heterojunction heating is the heat generated between the doped semiconductor layers. Though heterojunction heating is estimated to be higher than Joule heating, they can be easily dissipated through the contact layers to the metal electrodes.

Surface Recombination Heating This heating source plays a more important role in small lasers than larger lasers, as the surface-to-volume ratio is higher. Surface recombination heating can be simulated with the electronic simulation model considering carrier density, surface recombination velocity, gain region area and quasi-Fermi level.

Auger Recombination Heating Auger recombination is another major heat source in small lasers, which is related to the carrier density, gain region volume, and quasi Fermi level. From previous studies, Auger recombination contributes largely to the self-heating issue with small lasers, and it is generated in the middle of the semiconductor layers which could be hard to dissipate [32].

Layer Material	Thickness (nm)	Refractive index *n*	Doping (cm^-3)
n-InGaAs	50	3.53	2 e19
n-InP	300	3.17	1 e18
InGaAs	400	3.53	Undoped
p-InP	200-600	3.17	5 e18
p-InGaAsP	50	3.4	2 e19
SiO_2/Ag	160/100	1.45/-	N/A

Table II List of layer materials and their doping concentration used for thermal analysis [33]. The refractive index of each layer is also shown for reference.

In order to improve the cavity design with better heat dissipation aimed for room-temperature operation, we look into the thermal properties of this cavity to investigate its temperature distribution and self-heating with relation to cladding layer thickness. A commercial simulator, Sentaurus TCAD by Synopsys, is used for conducting thermodynamic simulations. The model is built according to layer constructions shown in Table II [30, 33].

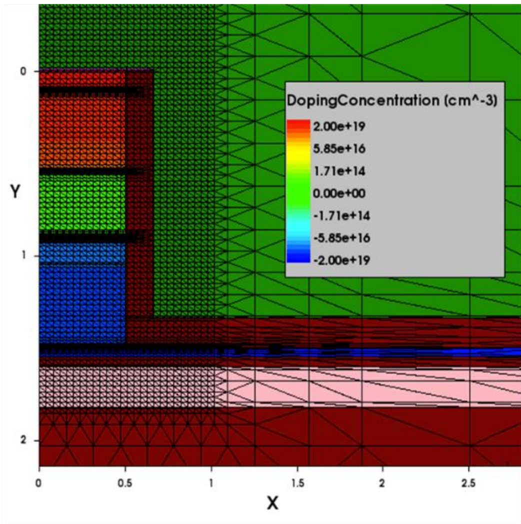


Figure 2.2 Constructed 2D structure with cylindrical symmetry in Sentaurus TCAD. Different color indicates p- and n- doping in the compositions. Black lines show the non-universal mesh for conducting simulation. The units for x- and y- axis are both um. The lower substrate is InP, and the upper green background is assumed to be silver.

For simplicity, we approximate the structure to be a symmetrical cylindrical cavity occupying the same footprint as the capsule-shaped one, and conduct 2D simulation in the cylindrical coordinate, as shown in Fig 2.2. The black lines are the non-universal mesh defined for simulation, and the color indicates the doping concentration in the 2D map. The mesh is set to be denser near the junctions for giving accurate calculation while keeping the simulation time rather feasible. We also include the silicon-on-insulator substrate at the bottom of the cavity, since the substrate also plays an important role in heat trapping, which should be taken into consideration for the device design. To analyze the self-heating effect, we include three main categories of heat sources: (1) Joule heating, (2) junction and heterojunction heating, and (3) non-radiative recombination heating [30, 33]. The thermal conductivities of critical materials are listed in Table III.

Materials	Thermal Conductivity ($W \cdot m^{-1} \cdot K^{-1}$)
Ag	429
InGaAsP	9.3
InP	68
InGaAs	5.0
SiO_2	1.1
Si	155

Table III Thermal conductivity of different materials used in thermal simulations. It can be seen that SiO_2 has extremely low thermal conductivity, which makes it hard for heat dissipation in this structure, while silver provides great thermal conductivity as a metal.

In order to have a general idea of the heating issue inside the cavity, we look into the heat localization inside the device by studying the temperature distribution at its cross-section at a typical operating current.

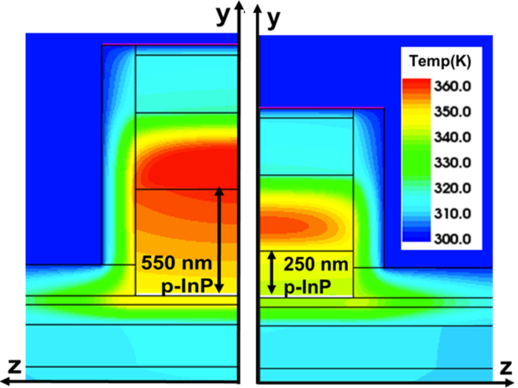


Figure 2.3 Temperature distribution inside the cavity under I = 2mA. The graph on the left shows a cavity with p-InP thickness of 550 nm and the graph on the right shows a cavity with p-InP thickness of 250 nm. The color map shows severe heat localization at the active layer and its surrounding, and more at lower regions as compared to upper regions.

Figure 2.3 depicts the temperature distribution at the device cross-section under an operation current of $I = 2$ mA. The left shows a device with thick (550 nm) p-InP cladding, and the right shows one with thin (250 nm) p-InP cladding, while other factors are kept as the same. One could tell that in each case, the active layer has the highest temperature, while lower p-InP cladding also has higher temperature than the upper n-InP cladding. This is probably due to that the upper cladding has an easy heat dissipation path from the silver cladding at top, while the lower cladding is surrounded by insulation layers densely, without direct heat dissipation path. For the model with p-InP thickness lower as 250 nm, however, we see that self-heating effect inside this cladding layer is significantly suppressed.

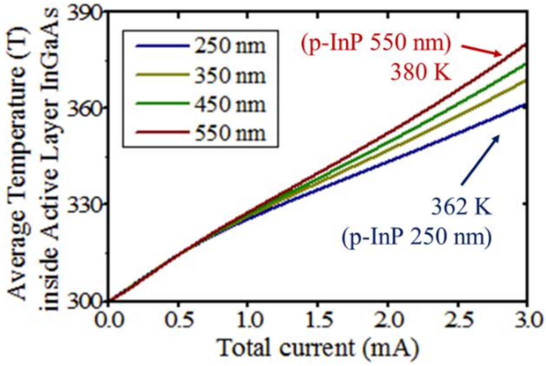


Figure 2.4 Average temperature inside the device active layer InGaAs with increasing current, for cavities with different p-InP cladding thickness ranging from 250 nm to 550 nm.

We then move on to study the relationship of p-InP thickness with the overall device temperature. We calculate the average temperature inside active layer with increasing current, for devices with different p-InP thickness ranging from 550 nm to 250 nm. It can be seen that the relationship of the temperature with p-InP thickness is obvious, while the temperature inside active layer rises much quicker for a device with thicker p-InP cladding layer than that with thinner p-InP cladding layer. The cavity of 250 nm p-InP gives almost 20K temperature reduction at I = 3 mA compared to that of 550 nm p-InP thickness. The result proves that lower p-InP thickness gives advantage in device's thermal management and reduces the self-heating issue. Such improvement is critical for realizing room-temperature electrically-pumped operation of wavelength-scale metal-clad semiconductor laser.

However, a lower p-InP thickness may give worse optical confinement on the other hand, as the light could easily leak out to the device substrate, especially when the contrast of dielectric constant in InP (3.14) and InGaAs (3.53) is not sharply large. Further optimization of the cavity design in order to keep the improvement in thermal performance while not undermining the optical confinement is covered in Chapter 3.

2.4 Summary

In this chapter, the design of a wavelength-scale silver-clad InP/InGaAs cavity with advanced capsule-shape is presented and explained in detail. The thermal properties of this cavity sitting on top of SOI waveguide is studied.

It can be seen that the self-heating issue of small-size metal-clad semiconductor cavity is related to the p-InP layer thickness at the bottom of active layer, mainly due to the non-radiative process happened inside and at the junctions. By reducing the p-InP layer thickness to as low as 250 nm, one could mitigate the heat-trapping inside the cavity and reduce the active layer temperature as a result. In this way, the cavity structure is optimized for possible operating in room temperature.

Chapter 3

Design of Metal-Clad Semiconductor Lasers: Integration with Waveguides

3.1 Introduction

In the previous chapter, we discuss the structure of the metal-clad semiconductor laser cavity and several factors affecting its performance in both optical and thermodynamic aspects. However, related optical confinement problems may arise when the we set the low p-InP layer thickness to be thinner as suggested by thermal considerations.

In order to solve this problem, we keep the optimized device cavity structure proposed in chapter 2, but look into the waveguide coupling scheme in search for a solution of both improved optical and thermal performance. There are two main considerations:

(1) For the design of cavity itself, optical confinement and thermal trapping are correlated as a trade-off, as a thicker InP gives better optical confinement but a thinner InP gives better heat dissipation, thus one would go into dead-end if limited to optimization of the cavity layer structure.

(2) For the application of our ultimate goal as searching for energy-efficient on-chip light source, the integration with waveguide is anyway inevitable to be taken into consideration for cavity design, since the proposed laser is aimed for emitting light to be coupled for downstream applications in integrated photonic circuits.

As a result, we look into design of the cavity with integration to waveguides, in search for a solution to save us out of the dilemma and solve both problems. In this chapter, we investigate integration of the metal-clad III-V semiconductor laser to a common silicon-on-insulator (SOI) waveguide, as proposed in chapter 2.

In section 3.2 to 3.4, we present our design of a special integrated feedback stub in the silver-clad InP/InGaAs laser coupled SOI waveguide, which serves as a powerful tool offering external tuning of the cavity quality factor (Q factor). We provide the result of finite-dimension time-domain (FDTD) simulation to confirm the effect of Q-factor tuning. We show step by step that with this integrated feedback stub, one could compensate the optical loss related to low InP thickness, without sacrificing the heat dissipation merits from the previous cavity design.

After that, in section 3.5, we provide theoretical analysis based on coupled-mode theory to explain this Q-factor-tuning mechanism quantitatively, and we compare the theoretical analysis result with those obtained from FDTD simulation.

3.2 Problem with Coupling Cavity to Waveguide

For integrated photonic circuits, there has been the debates over III-V/Si hybrid system with III-V-only system regarding active devices integrated with passive components. III-V-only system certainly gives advantages in the fabrication realm for research purpose, since the wafer can be grown directly using Metal-Organic Chemical Vapour Deposition (MOCVD) and do not need further manipulation such as alignment or bonding. However, III-V/Si hybrid system still remain a popular choice, as it can potentially make use of the supreme optical property of III-V materials for high quality active devices as well as the fundamental fabrication techniques in Si industry [34, 35]. Common methods of III-V/Si hybrid fabrication are either bottom-up (such as hybrid epitaxial growth of III-V on Si) or top-down (such as III-V layer and Si layer bonding).

In our design, we propose to couple the cavity evanescently to a silicon-on-insulator waveguide at the bottom for its simplicity in design and practicality in applications.

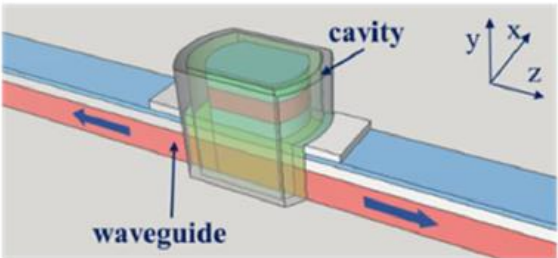


Figure 3.1 Schematic of a typical metal-clad semiconductor cavity coupled to waveguide with two-end output.

Figure 3.1 shows the schematic of the cavity structure optimized from chapter 2 coupled to SOI waveguide. We study the cavity quality and the coupling situation of this structure with 3D finishte-dimension time-domatin (FDTD) simulation using a commercial software by *Lumerical Solutions, Inc*.

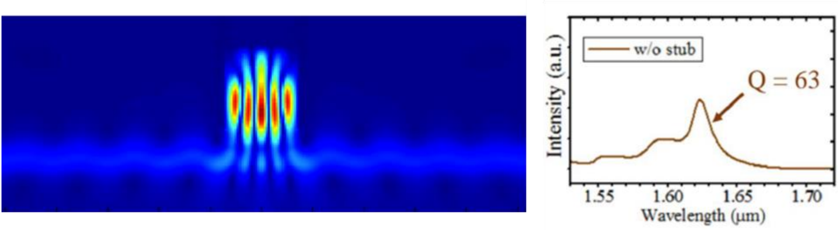


Figure 3.2 Left: The electric field intensity distribution of the resonant mode of this cavity coupled to SOI waveguide, obtained from FDTD simulation with a point-source excitation

inside the cavity. It can be seen that much light is leaked from both ends of the waveguide. Right: Simulated spectrum of light collected from the cavity of this coupled structure, under the same point-source excitation, showing a resonant mode with very low quality-factor, $Q = 63$.

The results are shown in Fig 3.2. From the electric field intensity distribution, it can be seen that both ends of the waveguide serve as an outlet of the light, and due to weak overlapping of the fields as well as scattering loss at the structure corners, the quality factor of the cavity is very low. The low InP thickness also contributes to the poor confinement, as light tends to be radiated out on their way to the waveguide. From the spectrum emitted from the cavity coupled to SOI waveguide, one could tell that this design has very poor optical quality and would not be feasible for an efficient on-chip light emitter.

Aiming for more efficient coupling scheme, we look into possibilities in advanced waveguide design.

3. 3 Coupling with Straight Integrated Feedback Stub

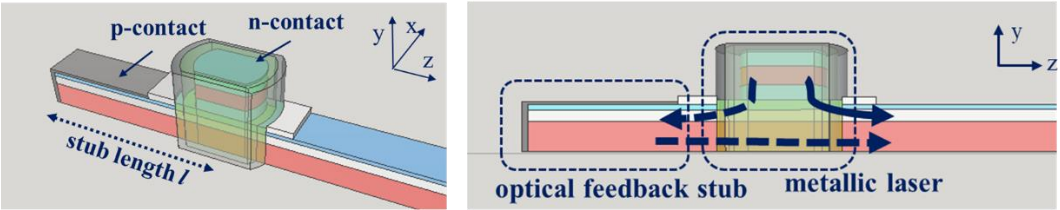
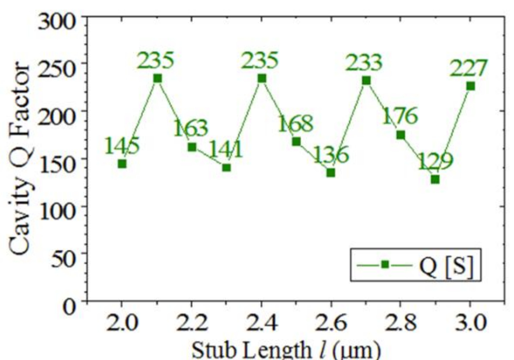


Figure 3.3 Left: Proposed coupling scheme with a straight integrated feedback stub. Right: Side view of the structure, with arrows showing the tentative light paths through the metal-clad laser (metallic laser) and the optical feedback stub.

To explore possible structures, we truncate one end of the waveguide with a mirror, and construct a laser integrated to waveguide with single-end output. In this structure, one-end of the silicon waveguide is truncated and coated with silver to serve as a mirror, forming a stub-like structure with certain distance to the cavity. The distance from this mirror to the cavity edge is defined as the stub length *l*.

We construct this structure using 3D FDTD simulation and investigate the Q factor in the cavity with the same method as in section 3.2. It seems that there could be constructive or destructive interference of the light from the stub and from the cavity, when they interfere at the edge of the cavity. As a result, the overall quality factor of the cavity may be affected by the stub length l. Thus, we study the cavity Q factor with relation to varying stub length *l*.



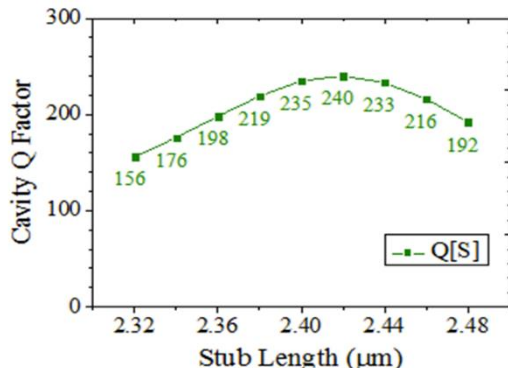


Figure 3.4 The Q factor of the cavity obtained from 3D FDTD simulation, as a function of varying stub length *l*. The left plot shows the periodic change of Q factor as *l* changes from 2.0 μm to 3.0 μm at steps of 0.1 μm, while the right plot shows the result at finer resolution as l changes from 2.32 μm to 2.48 μm at steps of 0.02 μm, and the peak value of Q factor in this local case is 240. [S] stands for straight waveguide, as it will be compared to different structures in the following sections.

Figure 3.4 shows the result of the changing of Q factor as a function of stub length *l*. The left is the relationship as l changes from around 1.4 μm to 2.5 μm. One can see that as the distance changes, the quality factor of the cavity gets affected periodically, which agrees well with our intuitive expectation. To look further into the effect, we conduct the simulation with finer step of stub length, as shown on the right of Fig 3.4. It can be seen that the quality factor rises up to $Q = 240$ at a stub length of 2.42 μm in this case, which is much larger than the double-end output waveguide case with $Q = 63$.

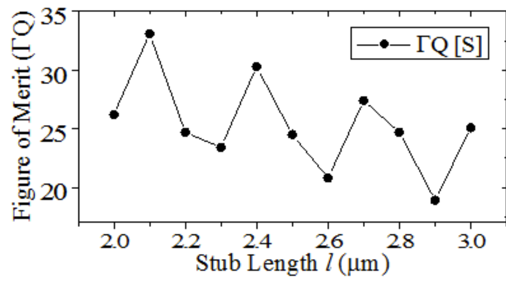


Figure 3.5 Figure of merit (ΓQ) of the cavity coupled to waveguide with integrated feedback stub of changing length *l*.

Apart from cavity quality factor, we are actually more interested in its effect on the lasing threshold of the cavity. We would like to see whether the overall lasing threshold can be reduced from improvement of the cavity Q factor. In this case, the lasing threshold is determined by ΓQ, where Γ is the confinement factor of the mode inside the entire structure. We include the computation of Γ in our simulation, and plot ΓQ as the figure-of-merit along with the cavity Q factor, as of changing stub length *l*. The result is shown in Fig 3.5. One could see that the figure of merit changes accordingly as well, and it drops only very moderately with slightly a longer stub length.

This proves that the integrated feedback stub serves as a powerful tool in improving the overall optical performance of the device from optimized waveguide design. It improves the overall optical performance for the given cavity, with more efficient manipulation of the light with less radiative loss. Moreover, the improvement is made in the waveguide part, and does not affect the previously optimized thermal properties from the cavity structure.

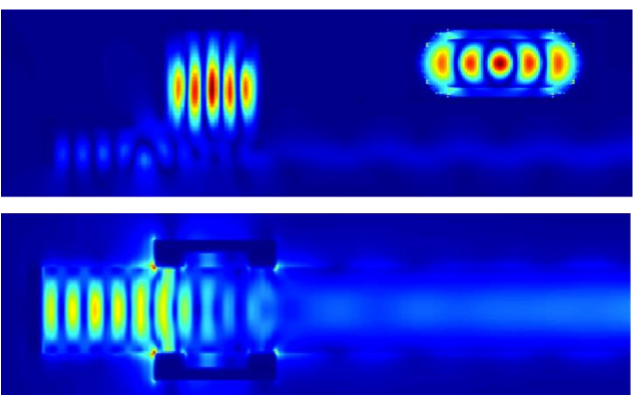


Figure 3.6 Electric field intensity of *y-z* plane at $x = 0$ (top), *x-z* plane at center of waveguide core (below) and *x-z* plane at center of active layer (inset) at the resonant wavelength 1630 µm, with a straight feedback stub of length $l = 2.42$ µm.

To have a better understanding of the optical performance of this integrated structure, we look into the electric field intensity of the resonant mode in several critical cross-sections, as shown in Fig 3.6. One could see that the resonant mode inside the cavity is nicely confined, and there is also similar light confinement in the feedback stub. However, it can also be seen that there exists certain scattering loss, especially as the stub geometry is in a scale comparable with of the wavelength-scale-sized cavity, probably owing to the sharp corners of the stub shape.

We then look into possibilities to further improve the waveguide structure with this integrated feedback stub. Following the same philosophy of designing capsule-shaped cavity as an improvement of the rectangular ones, we propose to tune the shape of the feedback stub and investigate its potential pros and cons.

3. 4 Coupling with Curved Integrated Feedback Stub

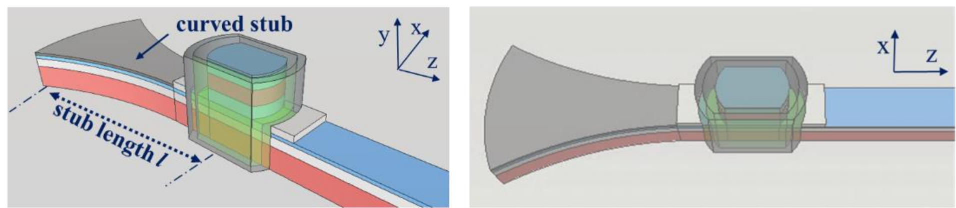


Figure 3.7 Schematics of the cavity coupled to a curved integrated feedback stub. Left shows a perspective view of the stub, while the right gives a top-view of the *x-z* plane, showing the expanded edges of the stub into a Gaussian-beam-like shape.

We would like to find an improved shape of the feedback stub. In order to do so, we simulated the electric field distribution of the metal-clad III-V cavity coupled to an infinite silicon-on-insulator plate and studied the shape of such vertically guided wave front. We expand the sidewalls to match with such shape, which actually resembles a Gaussian-beam profile. The structure of the metal-clad cavity coupled to waveguide with such a curved integrated feedback stub is shown in Fig 3.7. The stub length *l* is defined in a similar manner, from the end of the feedback stub mirror to the cavity. Again, we use 3D FDTD to study the Q factor and figure of merit of this structure, with changing stub length *l*.

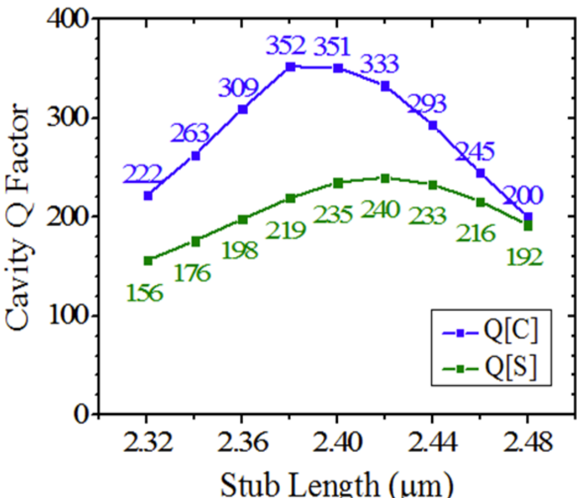


Figure 3.8 Cavity Q factor with the feedback stub of changing stub length *l*, from 2.32 μm to 2.48 μm at step of 0.02 um. The blue line plots Q[C] as of a curved stub, while the green line plots Q[S] as of the previous results we obtained from a straight stub.

As shown in the plots in Fig. 3.8, the results show clearly significant improvement in cavity quality factor of a feedback stub with tuned shape compared to that of the straight one. At stub length l = 2.38 μm, the overall cavity Q factor reaches a local peak of Q = 352 at resonant wavelength of 1630 nm. The shift of the locally optimized stub length *l* from 2.42 μm to 2.38 μm can be intuitively understood as a change of effective reflective index of the waveguide in the stub from the expanded curved shape.

To confirm the improved optical property with a curved integrated feedback stub of tuned shape, we look into the electric field intensity distribution inside the center of waveguide of both a curved structure and straight structure, as shown in Fig 3.9 below.

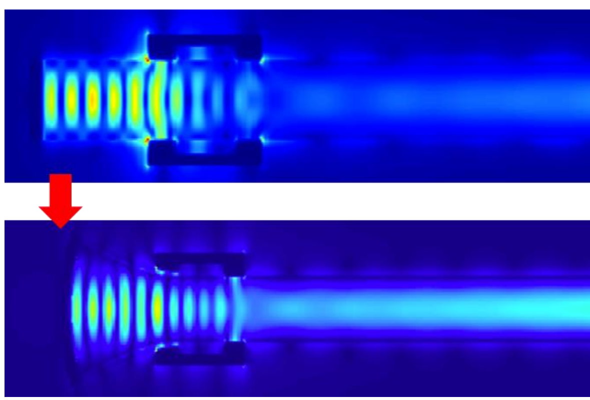


Figure 3.9 Electric field intensity of *x-z* plane at center of waveguide core at the resonant wavelength 1630 um, with a straight feedback stub of length $l = 2.42$ µm (top) and with a curved feedback stub of length $l = 2.38$ µm (bottom).

From the figure, one could see that the loss at the sharp corners that appear in straight feedback stub is largely reduced in the curved structure, which is consistent with the higher Q factor obtained from curved structure.

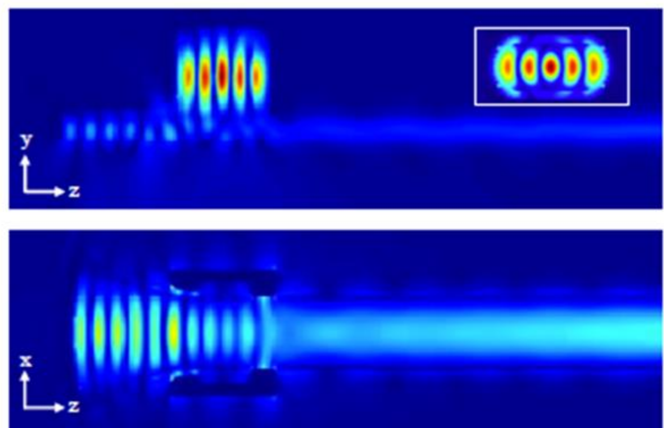


Figure 3.10 Electric field intensity of *y-z* plane at $x = 0$ (top), *x-z* plane at center of waveguide core (below) and *x-z* plane at center of active layer (inset) at the resonant wavelength 1630 um, with a curved feedback stub of length $l = 2.38$ µm.

Figure 3.10 shows the electric field intensity of the cavity coupled to waveguide with curved integrated feedback stub with $l = 2.38$ µm obtained from 3D FDTD simulation. One could see that the cavity mode is well confined, while the coupling to waveguide gives improved results.

To see a more straight-forward comparison of the improvements, we plot the optical spectrum of the cavity with curved feedback stub of $l = 2.38$ µm, compared with that in the same cavity with a straight feedback stub at $l = 2.42$ µm, as well as without feedback stub but only SOI waveguide with double-end output. The spectrum is collected from FDTD simulation in the same method as described before, from a point-source excitation inside

the cavity. The results are shown in Fig 3.11. Schematics of the corresponding coupling schemes are also listed on the right side for comparison.

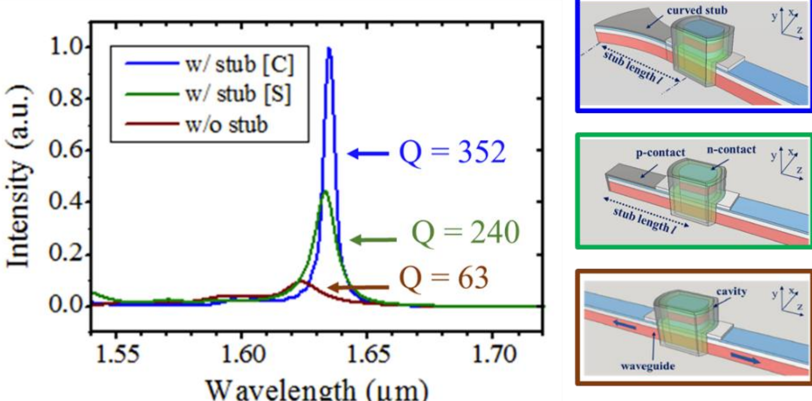


Figure 3.11 Optical spectrum of the cavity with a curved feedback stub at l = 2.38 um (blue) which gives Q = 352, compared to that of the same cavity with a straight feedback stub at d = 2.42 μm (green) which gives Q = 240, and without feedback stub but only SOI waveguide (brown) which gives Q = 63. Schematics of the corresponding structures are listed at the right.

It is worth noticing that in addition to nearly 5-fold higher Q factor and lower threshold, the feedback stub section is broadened to 2.47 μm^2 in this design, which could be used for practical p-type electrical contact with reduced contact resistance and improved overall heat dissipation, since it is coated in metal. This is also an improvement compared to previously-demonstrated designs, where the electrodes are not taken into consideration during numerical investigation [36-38], or large-area electrical contact on the bottom InP substrate is proposed, which might be challenging for device fabrication [39, 40].

3. 5 Understanding the Integrated Feedback Stub with Coupled-Mode Theory

From the previous investigations, we propose the design of a capsule-shaped metal-clad InP/InGaAs laser cavity coupled to a curved integrated optical feedback stub, as shown in Fig. 3.12.

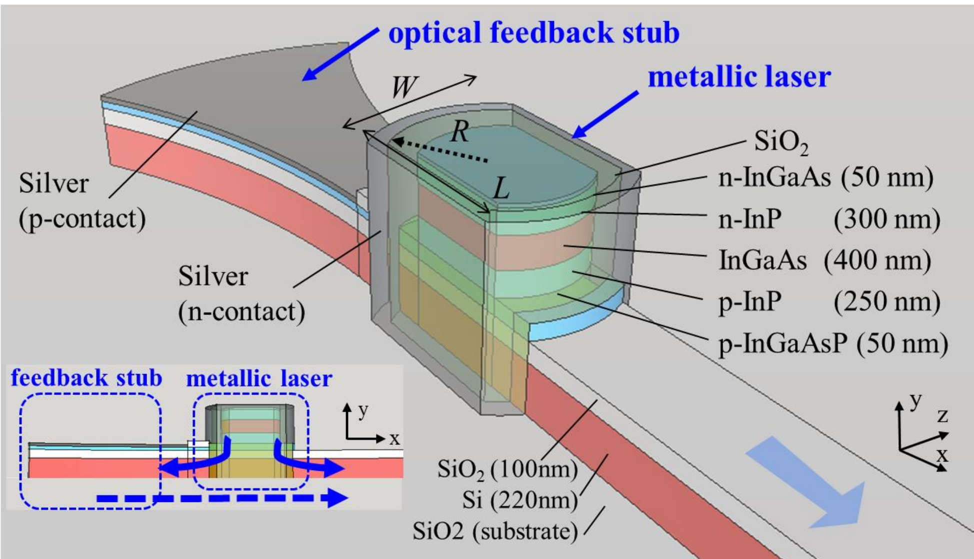


Figure 3.12 Perspective view of the of proposed wavelength-scale silver-clad InP/InGaAs laser coupled to SOI waveguide with curved integrated feedback stub. Inset shows a side view from *x-y* plane which explains the interaction between the metal-clad cavity (marked as metallic laser) and the feedback stub.

As mentioned before, we can intuitively understand this model by the idea of engineering the optical phase of the reflected wave from the stub from tuning the stub distance carefully, and reduce the light coupled directly from the cavity to the waveguide through destructive interference.

In order to understand the mechanism of such improvements in optical performance quantitively from a theoretical perspective, we look into the mode-coupling theory for a given coupled-cavity system.

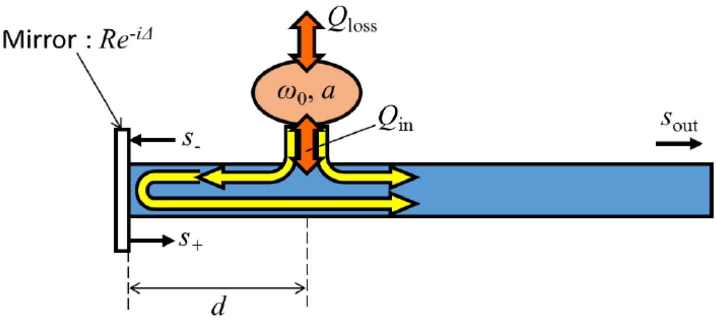


Figure 3.13 Diagraph of a typical system that consists of cavity and the optical feedback stub. The orange oval represents the cavity, and thee blue rectangle represents the waveguide. Yellow arrows partially show the light flowing in the system.

We adopt a general coupled-cavity system as shown in Fig 3.13. It consists of a cavity coupled to a waveguide terminated by a perfect mirror on one end, where ω_0 is the resonant

frequency of the cavity, Q_{loss} is the quality factor that represents the excess cavity loss due to absorption and/or scattering, and Q_{in} is the one that accounts for the optical coupling between the cavity and waveguide. s_+ and s_- represent complex electrical amplitudes of the incoming and outgoing wave at the edge of the stub, R and Δ are reflectance and phase-shift at the mirror, and d is the distance from the cavity to the end of stub.

One should notice that here, the stub distance d is used instead of the length l. d is defined as the distance from the edge of cavity to the end of stub, while l is the length from cavity center to the end of stub. In our case, $d = l - 0.55$ µm. For the theoretical analysis, the distance d is used since it is more intuitively relevant in the coupling mechanism, though l is a more general parameter and is independent of cavity size.

If we define $a(t)$ as the electric amplitude of the resonant mode inside the cavity, its time evolution can be described based on the coupled mode theory as [41, 42]

$$\frac{da(t)}{dt} = \left(i\omega_0 - \frac{\omega_0}{2Q_{\text{loss}}} - \frac{\omega_0}{2Q_{\text{in}}}\right)a(t) + \sqrt{\frac{\omega_0}{2Q_{\text{in}}}}e^{-i\theta}s_+\left(t - \frac{d}{v}\right), \tag{1}$$

where v is the light velocity inside the stub. Incoming and outgoing wave s_+ and s_- can be expressed as follows:

$$s_+(t) = Re^{-i\Delta}s_-(t)\ , \tag{2}$$

$$s_-(t) = -\sqrt{\frac{\omega_0}{2Q_{\text{in}}}}e^{i\theta}a\left(t - \frac{d}{v}\right). \tag{3}$$

By inserting Eqs. (1) and (2) to Eq. (3), we obtain

$$\begin{aligned}\frac{da(t)}{dt} = &\left(i\omega_0 - \frac{\omega_0}{2Q_{\text{loss}}} - \frac{\omega_0}{2Q_{\text{in}}}\right)a(t) \\ &- Re^{-i\Delta}\frac{\omega_0}{2Q_{\text{in}}}a\left(t - \frac{2d}{v}\right).\end{aligned} \tag{4}$$

Now, let us write $a(t)$ as

$$a(t) \equiv a_0 \exp\left(-\frac{\omega_{\text{sys}}}{2Q_{\text{sys}}}t + i\omega_{\text{sys}}t\right), \tag{5}$$

where ω_{sys} and Q_{sys} are the resonant frequency and quality factor of the total system that we want to derive. Then, $a\left(t - {}^{2d}/_{v}\right)$ in Eq. (4) can be expressed as

$$a\left(t - \frac{2d}{v}\right) = \exp\left[\frac{\omega_{\text{sys}}}{Q_{\text{sys}}}\frac{d}{v} - i\omega_{\text{sys}}\left(\frac{2d}{v}\right)\right]a(t)\ . \tag{6}$$

As a result, we can solve Eq. (4) with ω_{sys} and Q_{sys} expressed as

$$\omega_{\text{sys}} = \omega_0 \left[1 + \frac{R}{2Q_{\text{in}}} \exp\left(\frac{\omega_{\text{sys}}}{Q_{\text{sys}}}\frac{d}{v}\right) \sin\left(\frac{2\omega_{\text{sys}} d}{v} + \Delta\right) \right], \tag{7}$$

$$\frac{1}{Q_{\text{sys}}} = \frac{\omega_0}{\omega_{\text{sys}}} \left[\frac{1}{Q_{\text{loss}}} + \frac{1 + R\cos\left(2\frac{\omega_{\text{sys}}}{c} d + \Delta\right) \exp\left(\frac{\omega_{\text{sys}} d}{Q_{\text{sys}} v}\right)}{Q_{\text{in}}} \right]. \tag{8}$$

When $Q_{\text{in}} \gg 1$ ($> R$) and stub is sufficiently short, $\omega_{\text{sys}} \approx \omega_0$ in Eq. (7), so that Eq. (8) can be approximated as

$$\frac{1}{Q_{\text{sys}}} = \frac{1}{Q_{\text{loss}}} + \frac{1 + R\cos(2\beta d + \Delta) \exp\left(\frac{\beta d}{Q_{\text{sys}}}\right)}{Q_{\text{in}}}, \tag{9}$$

where phase constant β is defined as $\beta = {}^{\omega_{\text{sys}}}/_{v}$.

From Eq. (9), we can understand that Q_{sys} changes periodically by tuning the stub distance *d*. This is due to the fact that the backward travelling wave reflected by the mirror interferes with the forward wave and influence the *Q* factor of the total system.

We apply this theory to the simulation results we obtain in section 3.3 and section 3.4, and plot the relationship of Q factor and figure of merit with distance d from theoretical analysis, as shown in Fig 3.14.

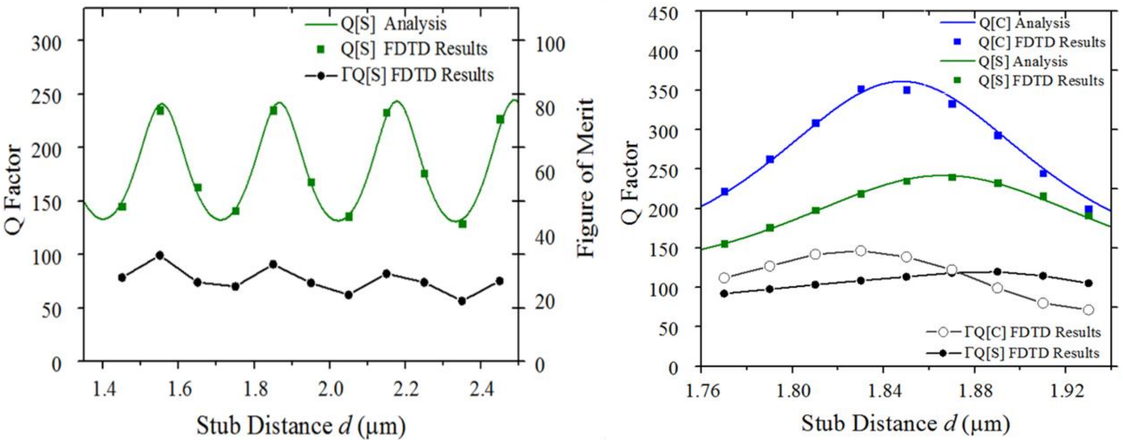


Figure 3.14 Relationship of Q factor (green for straight feedback stub and blue for curved feedback stub) with changing stub distance d, obtained from the coupled mode theory (lines) compared to that from FDTD simulation results (dots). The figure-of-merits obtained from FDTD simulation results are also plotted accordingly. Again, [S] stands for straight stub, and [C] stands for curved stub.

For the case of straight integrated feedback stub, as shown in the left of Fig. 3.14, the Q_{in} and Q_{loss} are derived to be 650 and 235 respectively. From the graph, we could see that excellent agreement is observed between the theory and simulation, both showing that the Q factor oscillates periodically with *d* as a result of interference and coupling.

For the case of curved integrated feedback stub, as shown in the right side of Fig. 3.14, the

Q_{in} and Q_{loss} are 600 and 650, respectively. Such results imply reduced scattering loss and increased coupling efficiency of the curved integrated feedback stub compared to the straight case, which agrees well with the intuition of such design, as well as the simulation results we obtained.

3. 6 Summary

In this chapter, we study the design of the cavity with integration to waveguides, in search for a structure that gives improved optical performance without disturbing the merits of heat dissipation we obtained with the low p-InP thickness structure discussed in Chapter 2.

We present our design of the silver-clad InP/InGaAs laser coupled to SOI waveguide with an integrated feedback stub formed at the non-output end of the waveguide, and investigate the relationship of cavity Q factor as well as figure of merit with relation to the feedback stub length and shape.

Periodic change of the cavity quality factor with relation the length is proved, and an optimized shape and length of the stub is obtained to effectively to tune the Q factor of the resonant mode inside the cavity. 5-fold improvement of the overall Q factor is obtained with a curved integrated feedback stub, confirmed through optical analysis using FDTD simulation.

In addition, theoretical explanation of the Q-factor tuning mechanism adopting coupled-mode theory is presented, and the computation results agree well with the simulation data obtained from FDTD simulation.

As a result, an advanced structure of silver-clad InP/InGaAs laser cavity of capsule shape coupled to SOI waveguide with a curved integrated feedback stub is proposed to give significantly improved optical quality while keeping the advanced heat dissipation properties from the cavity structure.

It is also worth notice that the concept of integrated feedback stub is rather general and not limited to this specific case, and can be applicable to a variety of other waveguide-coupled metal-clad small lasers.

Chapter 4

Fabrication of Metal-Clad Semiconductor Lasers

4.1 Introduction

As one could tell from the device structural design, the fabrication of metal-clad semiconductor lasers consists of a number of steps covering a fabrication process time of over 80 hours in total, and usually takes more than two weeks of continuous work for one complete batch. The fabrication process involves almost all aspects of modern nano- and micro- scale fabrication technology, including and not limited to wafer handling, multi-layer e-beam lithography, III-V semiconductor etching and cleansing with both dry-etching and wet-etching methods, plasma-enhanced chemical vapor deposition, multi-layer e-beam evaporation with lift-off processes and so on. As for devices designed for electrically-pumped operation and coupled to waveguide, the handling of electrodes, contact layers as well as the underneath waveguide geometry add even more complexity and additional steps in the fabrication flow.

The overall performance of the proposed metal-clad semiconductor lasers largely depends on the fabrication quality, and it is non-trivial to optimize each step in the fabrication process for the realization of such devices in application [30, 43]. Before proceeding to advanced structures with waveguide and feedback stubs, we start from the fabrication of wavelength-scale silver-clad InP/InGaAs cavities, of various shapes, on InP substrate with gold electrodes aimed for electrically-pumped room-temperature lasing aiming for room-temperature electroluminescence.

In this chapter, a complete fabrication flow including all relevant steps with detailed discussions on possible improvements in each step is presented. In section 4.2, we provide an introduction of the overall arrangement of device design of one fabrication batch. From section 4.3 to 4.4, extensive descriptions of the fabrication details and some characterization results of the fabrication quality with discussions on their effect and potential improvements are provided. Section 4.4 is divided into 23 steps in consequence, explaining the fabrication process of a batch of cavities on one sample. In addition, a flow chart of the fabrication process is included in Appendix A. In section 4.5, we give a brief review with general comments on the fabrication process instead of a summary. Potential improvements and some unsolved mysteries are also listed.

4.2 Overall Arrangement of the Fabrication Batch

In each batch of fabrication, a group of cavities are fabricated and compared. It is very important to design wisely the cavity geometries for the experiment groups. As the pattern will be written in one wafer and go through exactly the same fabrication process, it provides a naturally controlled group of cavities to study only the effect of cavity shapes on their performance.

In this work, a series of 84 cavities are fabricated in each batch. There are 3 cavities for each design, and 28 different geometrical designs in total. The cavities are placed in 21 columns and 4 rows, and certain space is designed in between cavities for placing the electrodes in electrical pumping. The whole pattern occupies a space of around 6 mm length and 4 mm width on a wafer sample of about 1 cm by 1 cm size, which is easy to handle in various clean-room fabrication facilities. A list of the fabricated device designs is shown at Appendix B.

4. 3 Wafer Preparation and Cleansing

InP-based wafer is utilized for fabrication. The epitaxial wafer is pre-ordered from a company and the layer composition is shown in Table IV. In particular, there is an InAlAs layer added next to the active layer which acts as an electron blocking layer to reduce the lasing threshold, suggested by previous thermoelectrical studies [30, 44].

Layer Number	Layer Thickness	Composition	Doping (cm^-3)
0	-	InP Substrate	Fe-Doped
1	200 nm	p-1.4um InGaAsP	> 5 x 10e18
2	690 nm	p-InP	> 1 x 10e18
3	100 nm	p-InP	1 x 10e18
4	12 nm	p-InAlAs	1 x 10e18
5	400 nm	U-InGaAs	Undoped
6	200 nm	n-InP	1 x 10e18
7	250 nm	n-InP	5 x 10e18
8	50 nm	n-InP	>5 x 10e18
9	50 nm	n-InGaAs	2 x 10e19

Table IV Layer composition of the InP-based III-V wafer utilized in fabrication process.

The wafer is usually stored in a vacuum chamber in clean room to keep its quality. Before using, the wafer can be taken out and cut to desired size. Standard organic cleansing is recommended to generally clean the surface.

4.4 Fabrication Technology: Procedures and Discussions

4.4.1 PECVD of SiO_2 as hard mask

A layer of SiO_2 is deposited to the epitaxial wafer surface. The thickness is usually a few hundreds of nanometers, and it is not very critical. For example, we deposited 430 nm and 350 nm for two of our wafers. The SiO_2 is deposited using plasma-enhanced chemical vapor deposition (PECVD).

This step was performed before cutting the wafer into smaller pieces, thus performed to the whole sheet of wafer at one time. There might be some non-uniformity of the deposited SiO_2 thickness near the edges of the wafer, but since this layer of SiO_2 serves as the hard mask and will be removed, it is not especially critical. The potential drawback might be non-uniformity when spin-coating resist gel in the following step, causing some non-uniformity of the pattern development time after e-beam lithography.

4.4.2 E-Beam Lithography (I): The Cavity

We perform the first E-beam lithography for defining the cavity structure for future etching. Since this is the first layer we write, it is very important to also define all markers for future alignments. Apart from markers surrounding each cavity, additional corner markers are placed. Some special markers are also included for exposure leading to corner markers. Waveguides, square and circular arrays are also included for checking the conditions in future steps such as development and etching.

Organic cleansing of the wafer is performed before spin-coating. Then OAP, a gel precursor, and ZEP520A, a positive e-beam resist gel, are spin-coated onto the SiO_2-covered wafer.

E-beam lithography is carried out using RAITH SEM and E-Beam Lithography. In this step of E-beam lithography, the aperture is set to be the smallest possible, which is 10 μm, and the step size is also set to as small as 6 nm. The dosage is tuned to be different for cavities and markers of different sizes so as to get the best development results.

The development is done using ZED-N50 followed by IPA rinsing. The development time is very critical. Based on previous experience, we use 1 min at first and check the results under an optical microscope. If it is not developed thoroughly, we add time section of 20 s and check the results. If one is not sure about the development according to new conditions and changed dosage, it is recommended to start from shorter time, e.g. 20 s or 40 s, and add on additional sections gradually after checking each time.

4.4.3 Cr Deposition and Lift-off

After E-beam lithography, the pattern of cavities and markers is developed, and these areas have SiO_2 exposed out as ZEP520A is a positive resist gel.

We perform deposition of Chromium afterwards. The deposition is done using e-beam evaporation, and it is quite vertical as we keep the sample non-rotated in the chamber. The Cr thickness is designed to be around 30 nm. This thickness has been optimized roughly. If it is too thick like over 50 nm, the following lift-off step would be hard. If it is too thin like thinner than 25 nm, the pattern edges may also be not sharp enough for serving as high-resolution hard mask for future etching steps.

After Cr Deposition, we perform a process called lift-off. This is to use organic solution to react with the un-developed e-beam resist gel ZEP520A, so as to lift away the Cr on those areas together with the gel, leaving only Cr on the patterned area sticking to SiO_2.

The solution used is ZDMAC, which can wash away ZEP520A effectively. Heating the beaker to 90 °C on a hot plate can improve the effectiveness of lift-off. The reaction last for over 2 min, sometimes for about 5 min or even 10 min to make sure the lift-off is completed. This step needs to be very carefully conducted inside the organic process hood, as ZDMAC is harmful if inhaled or absorbed through skin, and may produce vapors of mists that can cause eye, skin or respiratory tract irritation. The heating of ZDMAC may be skipped if room-temperature process is enough for successful lift-off. Then the sample will go through acetone and IPA cleansing.

4.4.4 Dry Etching of SiO_2

Reactive-ion etching (RIE) is performed afterwards to etch the SiO_2 in areas where it is exposed, i.e. not covered by Cr from the previous lift-off step. In this way, we expose the top layer of InP epitaxial wafer to air at regions without the pattern. The regions of patterning, the cavities and markers, are protected by Cr and SiO_2 layers on top of the wafer.

We use Samco RIE etcher for the SiO_2 etching, using CHF_3 and Ar as the source. The conditions are summarized in Table V below.

RF Power	Gas Source	Gas Flow	Pressure	Tray	Reference Etch Rate
80 W	CHF_3/Ar	20/10 sccm	2 Pa	Quartz	22 nm/ min

Table V Samco RIE SiO_2 etching conditions.

Standard 10 min O_2 cleansing procedures are carried out before and after reaction with the sample, aiming to keep the chamber as clean as possible. To minimize the dirt left after dry etching, it is also important to keep the sample clean before putting in the reaction chamber. The SiO_2 etching rate in this recipe is about 22 nm/ min, thus it takes about 16 min to etch the 350 nm SiO_2 mask, and about 22 min to etch the 430 nm SiO_2 mask. We add about 2 min of additional cleansing, using CHF_3/Ar/O_2, so as to improve the surface conditions. The table VI below shows the condition of additional cleansing.

Step	RF Power	Gas Source	Gas Flow	Pressure	Tray	Reference Etch Rate

(1) SiO_2 etching	80 W	CHF3/Ar	20/10 sccm	2 Pa	Quartz	~ 22 nm/min
(2) SiO_2 additional cleansing	100 W	$CHF_3/Ar/O_2$	20/10/5 sccm	2 Pa	Quartz	~ 21.5 nm/min

Table VI Samco RIE etching protocol for (1) SiO_2 etching; (2) post-SiO_2-etching additional cleansing conditions.

After dry-etching, we conduct hydrogen chloride surface cleansing to remove the oxide residues left. Diluted hydrogen chloride acid (H_2O : HCl 100:6) is utilized. The sample is soaked in the solution for 2 min and rinsed in water twice. Then it is dried on top of 140 °C hot plate surface for 2 min.

4.4.5 Dry etching of III-V cavity

Following the previous steps, a Cr/SiO_2 hard mask of cavities are formed. Thus, we would move on to one of the most critical steps of this fabrication procedure, dry-etching of the III-V cavity.

Oxford ICP-RIE is used for dry etching of the III-V cavity, using CH_4 and H_2 as source. The conditions are summarized as Table VII below.

HF Power	ICP Power	Pressure	Gas flow	Step time	Steps of a cycle
120 W	100 W	15 mTorr	CH_4 15 sccm	60 s	4 - 8
			H_2 45 sccm		

Table VII Oxford ICP-RIE etching condition of InP/InGaAs/InP structure [30].

This recipe has been developed and tuned by C. Yu [30]. Huge efforts have been paid so as to improve the verticality of the cavity, so as to maximize the optical confinement performance. There are also several additional points to note in performing this step:

(1) O_2 cleansing of the empty chamber is performed before and after the sample etching and cleansing.

(2) Sufficient rest of about 10 min is recommended for after every about 4 or 5 cycles, so as to cool down the chamber temperature.

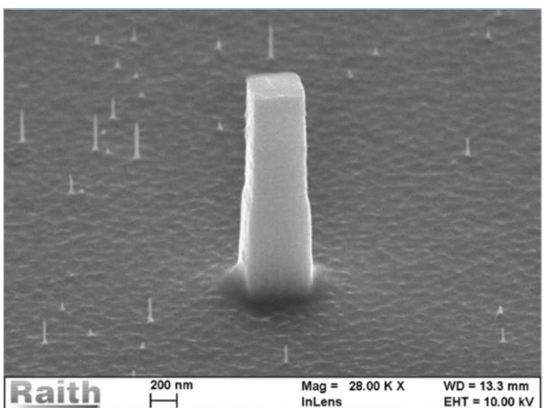
(3) For wafer with InAlAs layer, the etching recipe has to be changed when etching through the InAlAs layer. This special recipe is as Table VIII below.

HF Power	ICP Power	Pressure	Gas flow	Step time	Steps of a cycle
80 W	0 W	15 mTorr	CH_4: 15 sccm	5 min	depends
			H_2: 45 sccm		

Table VIII Oxford ICP-RIE etching conditions for etching through InAlAs layer.

(4) It is very important to keep track of the cavity height in etching procedures so as to fabricate a pillar with desired height. Knowing the height is also important for changing etching recipes to go over InAlAs layer. As the etching conditions may be different in each time, we would take out the cavity several times and check the height using DekTak Data Analyzer. As the cavity size is too small, the heights of the waveguide markers on the sample are measured as a reference since they undergo exactly the same etching procedures.

However, taking out and putting in the sample several times may also affect the etching result for the side wall smoothness as well as verticality. It is recommended to minimize the number of times for taking sample out and in. Figure 4.1 compares the SEM of an etched cavity with InAlAs layer (left) to that of a cavity without InAlAs layer but with similar dimension (right). It can be seen that the side wall condition degrades significantly at regions after the InAlAs layer.



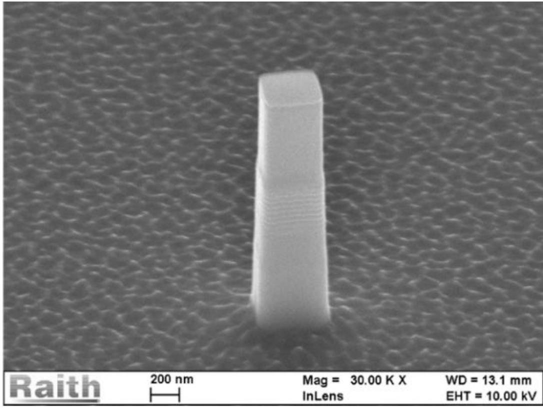


Figure 4.1 SEM of the InP/InGaAs/InP cavity core with (left) and without (right) InAlAs layer. The cavities are designed with a 350-nm side length, and it can be seen that the left cavity with InAlAs layer has less cavity verticality from the etching, probably due to frequent etching mode change and increased handling procedures of the sample in and out of the chamber.

4.4.6 Buffered HF Cleaning

After etching of the pillar, we should note that the Cr and SiO_2 mask is still on top of the cavities. We use buffered HF solution to remove these masks.

For larger cavities, sometimes the Cr layer on top of SiO_2 is not successfully removed, and may stay at the cavity top, as compared in Fig 4.2. At the right side is a circular cavity with

diameter around 2 μm with Cr layer sticking at the top, this is probably due to the relatively large size of the cavity. It may cause problem in the future if the Cr layer cannot be removed.

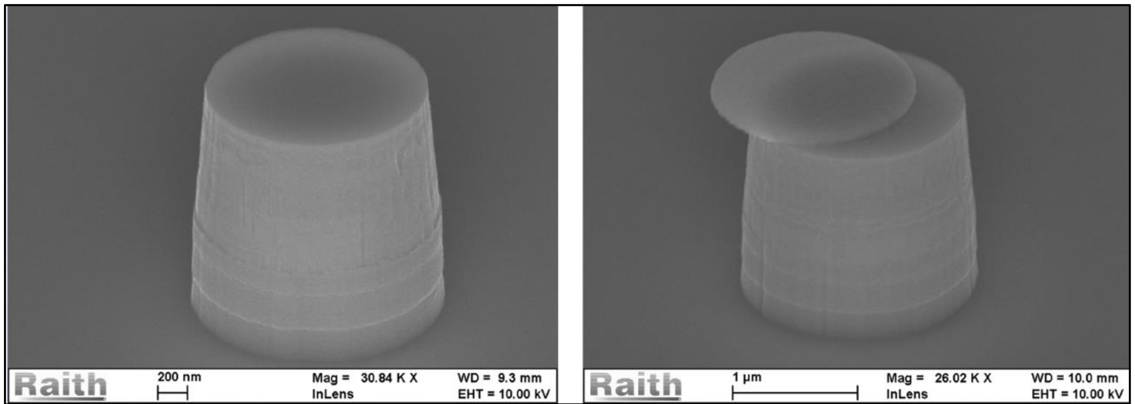


Figure 4.2 SEM of two circular InP/InGaAs/InP cavity core with Cr layer successfully removed (left) and sticking at top (right), respectively, after the buffered HF cleansing step.

4.4.7 E-Beam Lithography (II): The Insulation Frame

We perform the second e-beam lithography after the pillar etching. This is to define an "insulation frame" for the cavities. The pattern is a framework that divide the future electrode pad of all cavities, shown in Fig 4.3. At these regions, we plan to use dry-etching to remove the InP substrate and wet-etching to wash away the p-contact layer in the frame, like the moat surrounding the Imperial Palace. In future steps, we would deposit SiO_2 all over the surface, filling up this frame as additional insulation to avoid short-circuit in electrode formation.

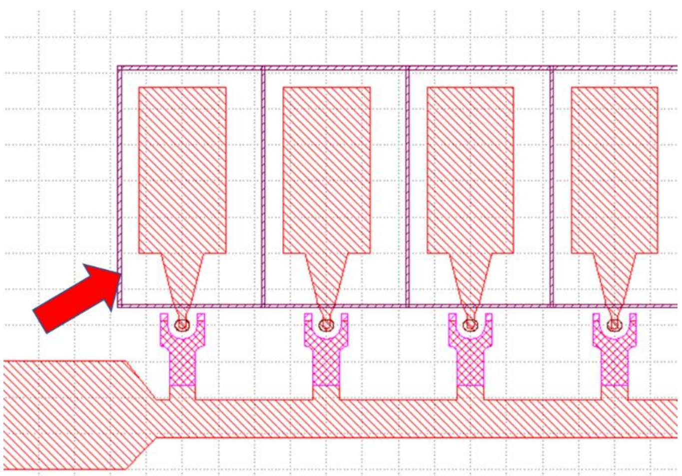


Figure 4.3 Part of the GDS design graph including multiple layers of the device E-beam lithography pattern. The rectangular framework pointed by the red arrow shows the patterning layer this time, which is only the insulation grid framework, and does not include the electrode pads and other structures in red or pink.

Bi-layer e-beam resist is formed using spin-coating this time, the first layer being LOR7B, and second ZEP520A. The spin-coating and future development parameters of the bi-layer

resist are shown in Table IV below. It is recommended to check the bi-layer resist has successfully formed and well-covered the sample, using NMD solution, which can react with the LOR7B in the inner layer. As long as no LOR7B is reacted or removed, one can ensure that ZEP520A has covered LOR7B all over the surface and the bi-layer resist is well formed. We generally soak the spin-coated samples in NMD for 1 min, rinse twice using water, and check the result using optical microscope.

	Layer Formation		Developing (after EBL)	
Material	Peak Spin-Coating Speed	Post-coating Baking Time (Baking temperature: 180 °C)	Developer	Developing Time
LOR7B	1400 rpm	2 min	NMD	12 s
ZEP520A	2500 rpm	3 min	ZED-N50	2 min

Table IX LOR7B/ZEP520A bi-layer resist spin-coating and developing conditions.

Since the frame has only straight patterns and no extra precise details in shape, we use a rather rough set-up with aperture of 60 μm. The width of the frame is about 5 μm, and the dosage is set to 70 $\mu C/cm^2$.

Three-point alignment is performed to align the pattern of frame to the previous layer utilizing the markers.

4.4.8 Dry Etching of the Insulation Frame

Dry-etching using Oxford ICP-RIE is performed to remove the InP at the insulation frame. The recipe is generally the same as the general pillar etching conditions.

Since the epitaxial wafer layer composition is known, one should be able to calculate the remaining InP thickness after pillar etching, and estimate the etching time and required cycles based on given InP thickness. Since that the left InP thickness is not very high, we use the previous estimated rate to calculate the time and perform the etching straight away without taking the sample out and in. The final etched depth of the frame can be checked using DekTak, similar as before.

4.4.9 Wet Etching of the Insulation Frame

To remove the active layer in the frame, wet etching is used. To control the process and avoid over-digging of the active layer, it is critical to control the etching time during wet-etching and avoid too much shaking.

H2O2/H2SO4 solution is prepared for the reaction. The sample is soaked inside for about 2 min without shaking, and then rinsed twice in water.

After wet etching, one should use ZDMAC and NMD solution to remove the residues of bi-layer E-beam resist gel formed on top. For removing ZEP520A residues, soaking in

ZDMAC for 5 min – 20 min is generally used, with heating to 90 °C using hot plate under the beaker if needed, followed by rinsing with acetone and IPA. For removing LOR7B residues, soaking in NMD solution for over 5 min is generally used, followed by rinsing twice with water.

4.4.10 Surface Cleansing and Surface Passivation Before Insulation Layer Deposition

Since the InP/InGaAs/InP pillar is fabricated for electrically-pumped optical emission, and the pillar is down to wavelength-scale of size around 1um, the surface-to-volume ratio is increasingly large which also makes the surface condition of the pillar very critical for overall lasing efficiency.

There are two main factors affecting the overall performance. One is the surface roughness made during ICP/RIE dry etching steps in section 4.4.5. Rough sidewalls will definitely decrease the quality factor of the Fabry-Perot laser cavity. Another factor is related with the electronically active states at the surface due to unsaturated surface bonds. As a result, the injected carriers recombine faster, giving increased threshold current and low efficiency of light emission due to predominance of nonradiative recombination [45]. Therefore, surface passivation aiming at removing the dangling bonds (unsaturated surface bonds) is performed so as to improve the cavity quality.

To deal with these two factors, we perform a multi-step surface cleansing procedure followed by surface passivation steps, referring to some previous works by K. Ding [46] and A. Higuera-Rodriguez *et. al* [45]. Hydrogen peroxide, phosphoric acid and ammonium sulfide are used. The steps are explained below.

(1) H_2O_2 and H_3PO_4 cleansing

Diluted hydrogen peroxide solution (H_2O:H_2O_2 100:2) and diluted phosphoric acid solution (H_2O:H_3PO_4 100:6) are prepared in two separate beakers. Several beakers containing water are also prepared for rinsing. In each cleansing cycle, the sample is soaked in H_2O_2 solution for 12s, then rinsed in water and dried by N_2 pistol, then soaked in H_3PO_4 solution for 30s, then rinsed in water and dried by N_2 pistol. The sample goes through about 3 to 6 cycles in total. Not enough number of cycles may leave the surface not clean enough, but too many cycles will also undercut the device a little. One can use SEM to check the cavity structure after certain number of cycles to make sure it is sufficient.

It is also worth noticing that this cleansing step is performed in dark environment, as recommended by K. Ding [46]. It is said that if done under room light, there would be bumps on the surface, while smooth surface can be obtained during if conducted in dark. This might be related to photo-assisted electric-chemical reaction at the surface related to the photo-generated current in the InP/InGaAs/InP p-i-n junction under illumination [46]. A comparison of results of the cleansing done in room light and in dark is shown in Fig 4.4 [46].

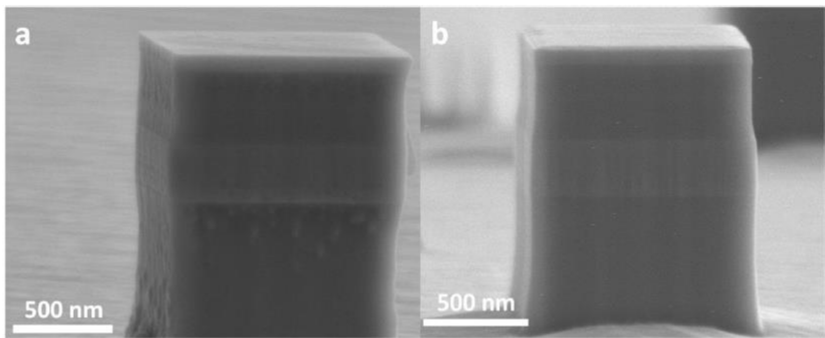


Figure 4.4 SEM of an InP/InGaAs/InP pillar after cleaning (a) under room light compared with that after cleaning (b) in dark. The sample cleaned in dark shows improved surface condition [46].

(2) $(NH_4)_2S$ cleansing

The sample is then submerged in diluted ammonium sulfide solution (H_2O : $(NH_4)_2S$ (from bottle, already diluted (need confirmation)) 100:40) for 10 minutes without shaking, and then rinsed in water twice and dried using 120 °C hot plate for 1 min. In [45], the sample is submerged in diluted ammonium sulfide, not rinsed by water and dried with N_2 pistol immediately. We did not compare the difference in these two protocols, and one may try either for their own interests.

It is worth noticing that this step is recommended to be immediately followed by the next step, PECVD deposition of insulation layer, so as to maximize the surface passivation result. In our case, the experiment facilities are physically in some distance thus some damage might be made during the transition of the sample form one building to another, thus the surface treatment result has the potential to be improved.

4.4.11 PECVD of SiO_2

The insulation layer is deposited to the structure surface, covering all over the cavities, markers, as well as the etched insulation frame. The deposition is done by plasma-enhanced chemical vapor deposition (PECVD) again. The thickness of SiO_2 is preferred to be about 70 nm – 100 nm, based on the results of comprehensive simulation relating to both heat dissipation and cavity quality factor.

Apart from SiO_2, SiN can also serve as good insulation material in this step. We also tried SiN with about 70 nm in some samples, and it provides no worse situation as SiO_2.

4.4.12 Contact Open for N-Contact

From the previous step, the whole structure is covered by insulation layer. As we would like to conduct electrically-pumped operation of the laser, thus proper electrodes have to be placed to the p-i-n junction. In this case, the top n-InGaAs layer is designed as the n-

contact layer, thus should have direct contact with the silver cladding which serves as the electrical conducting layer for current injection.

This contact open step is aimed for removing the SiO_2 on top of the cavities, thus exposing the n-contact layer for future silver deposition. The method is to cover the cavity structures by photoresist gel and use Samco RIE dry etching to etch downward so as to just remove the SiO_2 on top of the cavities.

Photoresist AZ5200NH is spin-coated to the sample with 3000 rpm, and SEM image of a typical circular cavity top after this step is shown in the left of Fig 4.5. Afterwards, etching is conducted with (1) O_2 ashing of the photoresist gel, and (2) SiO_2 etching protocols. Details of the conditions are summarized in Table X below.

Figure 4.5 The left is an SEM showing a cavity top covered by photoresist AZ5200NH spin-coated at 3000 rpm [30]. The right two pictures are the sample under optical microscope showing different stages of the dry-etching process for contact opening. One could see that the circular cavity top-views show different color due to the exposed height.

Step	RF Power	Gas Source	Gas Flow	Pressure	Tray	Reference Etch Rate
(1) O_2 ashing for photoresist	100 W	O_2/CHF_3	20/2 sccm	30 Pa	Quartz	-
(2) SiO_2 etching	80 W	CHF3/Ar	20/10 scccm	2 Pa	Quartz	~ 22 nm/min

Table X Samco RIE SiO_2 etching conditions for (1) O_2 ashing of the photoresist gel, and (2) SiO_2 etching.

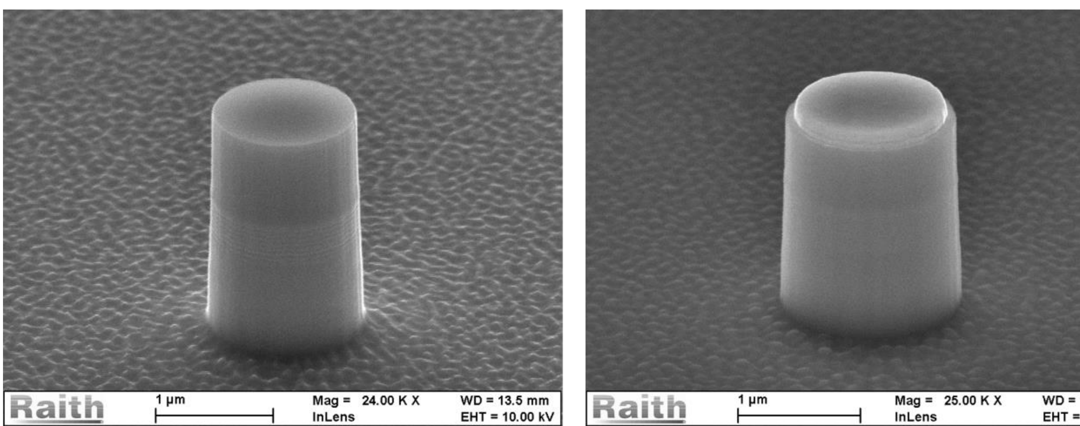


Figure 4.5 SEM of the same InP/InGaAs/InP cavity before insulation layer deposition (left) and after insulation layer deposition and contact open (right). This is a circular cavity designed with a diameter of 1.2 µm.

4.4.13 E-Beam Lithography (III): Bi-layer Resist Mask for Silver Deposition

After contact opening, we would like to coat silver all over the cavity as the metal-cladding layer, which also serves as the n-contact electrode. The silver should cover cavity structure only, thus we need to create a mask for only exposing the cavity surroundings for future e-beam evaporation of silver.

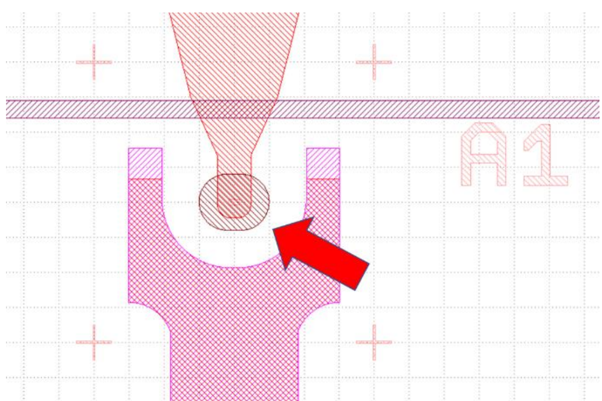


Figure 4.6 Part of the GDS design graph including multiple layers of the device E-beam lithography pattern. The red arrow indicates the rounded-rectangular-shaped pattern for the silver deposition opening window.

The mask is designed as shown in Fig 4.6. A window of approximately 16 µm in width and 20 µm in length is made surrounding each cavity, given that silver has to be deposited from a tilted degree in different directions so as cover the cavity thoroughly. The deposition will be conducted from an angle of about 30° to 45°, thus the window size can be estimated with certain space left around.

LOR7B and ZEP520A bi-layer resist layers are formed as the same in section 4.4.7. Considering the resolution accuracy required and also the time consumption, we used the

aperture size of 30 μm. Three-point alignment is used once again as the same in section 4.4.7. Step size is set as 80 nm, and dosage is set to about 70 $\mu C/cm^2$ or 80 $\mu C/cm^2$.

The development has to be very well-controlled to avoid the window to be expanded too much in the lower layer. We use ZED-N50 for ZEP520A development for about 20 min first, followed by NMD for LOR7B reaction for about 15s. Note that one should shake only very much gently and slightly while submerging the sample in NMD to control the reaction area, and it might be okay to even not shake though we did not have time to verify this. Minor undercut might occur, as shown in Fig. 4.7 [30], which would do no harm for future lift-off after silver deposition.

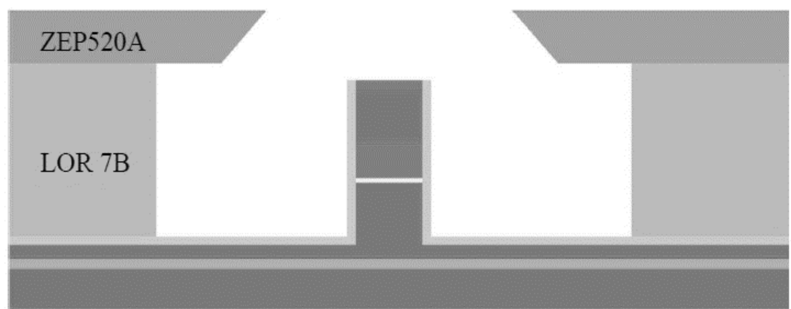


Figure 4.7 Schematic graph showing minor undercut of LOR7B during the bi-layer opening window for silver deposition [30].

4.4.14 Surface Cleansing Before Silver Deposition

Diluted hydrogen chloride (H_2O : HCl 100:12) is used for surface cleansing before silver deposition. This is the same as mentioned in section 4.4.4, to remove the oxide residues from previous O_2 plasma in RIE. The conditions and procedures are almost the same. This step is put as a separate section as it is recommended to be done right before metal deposition so as to make a clean contact between metal and n-contact surface. It may be easily overlooked, however should be done carefully for the best possible device quality.

4.4.15 Multi-Step Silver Deposition, Lift-off and RTA

Silver deposition is one of the most time-consuming step in this fabrication process. To thoroughly cover the cavity using a vertically-emitted e-beam evaporation facility, we divide the process into four separate deposition processes [30] as described in Table XI.

Step	Sample Orientation	Tilted Angle	Deposition material	Deposition Speed	Deposition Thickness
Deposition (Pre-1)	+45°	0°	Ti	0.05 nm/s	10 nm
			Au	0.05 nm/s	10 nm

Deposition (1)	+ 45°	+ 60°, -60°, + 60°, -60°	Ag	1 nm/s	100 nm, 100 nm, 250 nm, 250 nm
Deposition (2)	-45°	+ 60°, -60°, + 60°, -60°	Ag	1 nm/s	200 nm, 150 nm, 300 nm, 250 nm
Lift-off (I)					
Deposition (3)	+45°	+ 55°, -50°, + 55°, -50°	Ag	1 nm/s	150 nm, 200 nm, 200 nm, 300 nm
Deposition (4)	-45°	+ 50°, -50°, + 55°, -50°	Ag	1 nm/s	200 nm, 150 nm, 250 nm, 200 nm
Lift-off (II)					

Table XI Multi-step e-beam evaporation and lift-off process for silver deposition.

Thin layers of titanium and gold are deposited prior to the silver deposition so as to improve the adhesion of silver layer to the surface. In the coming four depositions, the sample orientations, tilted degrees, and the deposition thickness of each step can be varied slightly according to one's judgement. The goal after all is to have the cavity covered by silver with the best possible quality and as even as possible. This step can be much improved if better deposition facility could be available.

Lift-off of the bi-layer resist gel is performed twice, each time following two depositions, due to the thickness limit for successful lift-off. The lift-off procedure is similar to that in section 5.5, but with different conditions, as described here:

(1) ZDMAC is used for removing the remaining ZEP520A. One should soak the sample in a beaker containing ZDMAC heated up to 90 °C on a hot plate, shaking heavily for about 10 min and make sure the unwanted silver is thoroughly removed together with the ZEP520A gel. Again, this step needs to be very carefully conducted inside the organic process hood, as ZDMAC is harmful if inhaled or absorbed through skin, and may produce vapors of mists that can cause eye, skin or respiratory tract irritation. As previously mentioned, the heating of ZDMAC may be skipped if room-temperature process is enough for successful lift-off. However, unfortunately the silver layer is relatively thick, and the lift-off may be challenging. Afterwards, one should also rinse the sample carefully using acetone and IPA, and dry the surface using N_2 pistol.

(2) After this, to remove the remaining LOR7B on surface, one should soak the sample in NMD for around 5 min, shake if needed, and rinse twice in water. The sample can be dried from 120 °C hot plate surface for about 2 min.

The deposition result can be observed under optical microscope. One may also inspect using SEM, if needed.

After silver deposition, we perform rapid thermal annealing (RTA) to increase the grain size of silver, aiming at reducing the plasmonic loss of this metal-cladding over the cavity [30]. RTA is performed at 400 °C for 2 min. The comparison of a typical cavity surface before and after RTA is shown in fig 4.8. It can be seen that the grain size is increased, which would give better optical performance for the cavity. Minor dislocation of the silver-cladding happened during RTA, probably due to relatively weak adhesion at the corners especially under high temperature.

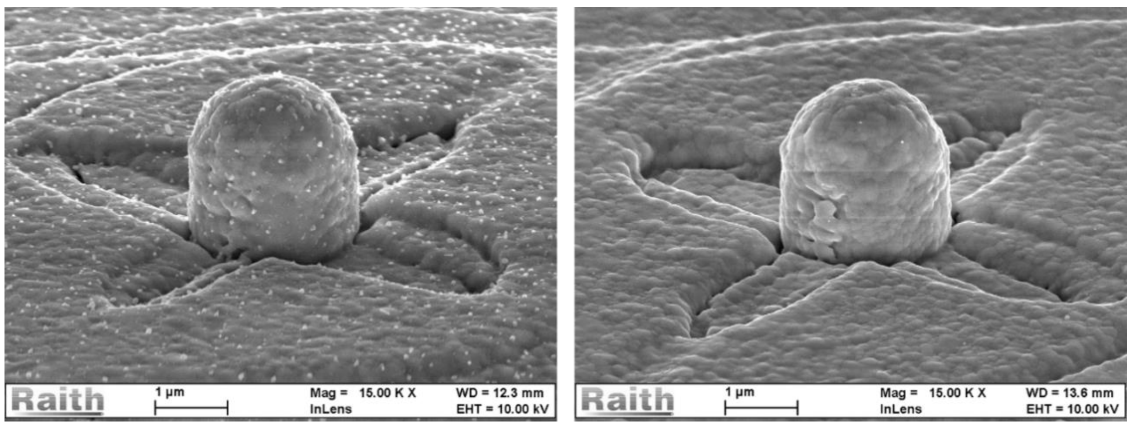


Figure 4.8 SEM of the same InP/InGaAs/InP cavity with silver cladding before (left) and after (right) RTA treatment. This is a cavity consisting of square cross-section semiconductor core with side length of 350 nm.

4.4.16 E-Beam Lithography (IV): Bi-Layer Resist Mask for Gold Protection Layer Deposition Before P-Contact Opening

Ideally the sample would be ready for p-contact opening in the next step, and it is required to cover the cavity structures thoroughly before going through the etching of p-contact. However, the cavity height is relatively high after previous steps, with semiconductor pillar height of about 1 μm and silver of about 1 μm. Thus, the common bi-layer resist we use is not enough to cover the cavities over their top. This was tried and checked by NMD solution using the same method as mentioned in section 4.4.7, as it can be seen that NMD solution flowed inside easily and reacted with LOR7B, which proved that the cavities were not successfully covered and the bi-layer resist formed was not high enough for protection process.

To solve this problem, we decided to deposit a layer of gold to protect the cavity before put it into further etching process. The gold protection layer has to deposited only over the cavities, connecting to the n-contact, and it should never get in touch with the p-contact area. In order to do so, we need to go through similar process as in section 4.4.13, using e-beam lithography to write the window for areas surrounding the cavity. The writing

parameters and patterns are the same as in 4.4.13. It takes only around 10 min for our RAITH E-beam writer to finish this patterning.

The development conditions are also similar to that in section 4.4.13. We used ZED-N50 for 2 min 30 s development, followed by twice IPA rinsing, and then NMD reaction for 12 s to 13 s, followed by twice water rinsing, and then used optical microscope to check the results. The sample is dried on 120 °C hot plate for 1 min.

4.4.17 Gold Protection Layer Deposition and Lift-off Before P-Contact Opening

The deposition of the gold protection layer is similar to silver deposition, but simplified a little since the metal quality is less critical and required thickness is lower. Thus, one round of deposition for Ti and Au respectively could be enough. Titanium, again is used prior to gold deposition for better adhesion. The conditions are set in Table XII below, and the following lift-off process is the same as used in section 4.4.15.

Step	Sample Orientation	Tilted Angle	Deposition material	Deposition Speed	Deposition Thickness
Deposition (1)	+ 45° or +60°	+50°, -50°	Ti	0.05 nm/s	40 nm, 40 nm
Deposition (2)	+ 45° or +60°	+ 50°, -50°	Au	0.2 nm/s	250 nm, 250 nm
Lift-off					

Table XII E-beam evaporation and lift-off process for gold protection layer.

Figure 4.9 shows an optical microscopy image of the wafer with cavities covered in gold protection. It can be seen that the gold protection covers the cavity well and overlaps largely with the silver-cladding of the cavity.

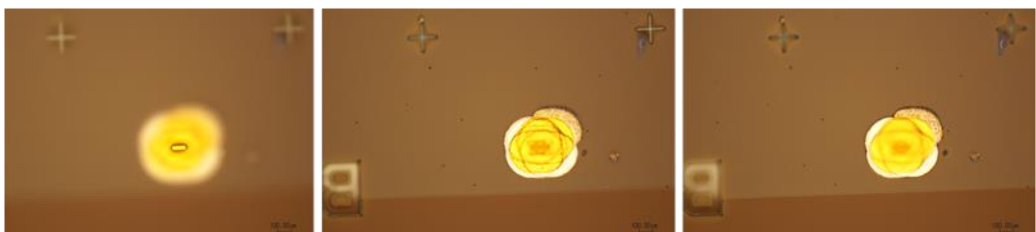


Figure 4.9 Optical microscope image of the cavity covered in gold protection. The bright area is the silver-cladding covering the semiconductor cavity, and the yellowish (gold) area is the gold protection layer. Three images are taken at different focus length, so as to show the layering over the cavity from top to bottom.

4.4.18 E-Beam Lithography (V): Defining Areas of P-Contact Opening

E-beam lithography is performed one more time to write the pattern of p-contact opening areas, as shown in Fig 4.10.

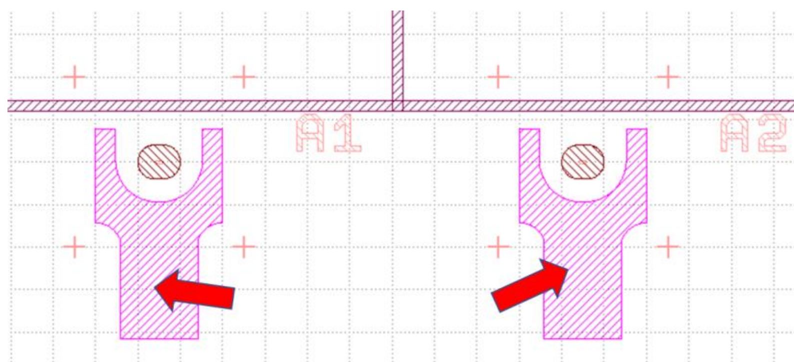


Figure 4.10 Part of the GDS design graph including multiple layers of the device E-beam lithography pattern. As indicated by the red arrows, the pink areas are patterned this time, defining the space where we will later etch the InP substrate for exposing underneath p-contact layer. In this graph, the pattern layer for p-contact gold electrode deposition is now shown so as to avoid confusion.

One should be extremely careful to leave enough space between the p-contact and the cavity coating window to avoid possible short-circuit. However, too large the distance may also increase the resistance in optical-pumping. Thus, we designed the mask to leave around 10-µm distance in between.

The spin-coating conditions, and writing parameters, are generally the same as in section 4.4.13 E-Beam Lithography (III) and section 4.4.16 E-Beam Lithography (IV).

For development and reaction to open the pattern window, ZED-N50 development of 2 min 30 s followed by IPA rinsing twice is used for ZEP520A development, and NMD reaction for about 12 s followed by water rinsing twice is used for LOR7B reaction. If one is not sure about the development and reaction time, it is always recommended to use shorter time and add additional time sections after checking under optical microscope.

Typical optical microscopy images of the contact area under optical microscope after ZEP520A development and after LOR7B reaction, respectively, are shown as in Fig 4.11. It is advised to gently dry the sample after the reaction using hot plate, for around 30s – 1 min at about 120 °C.

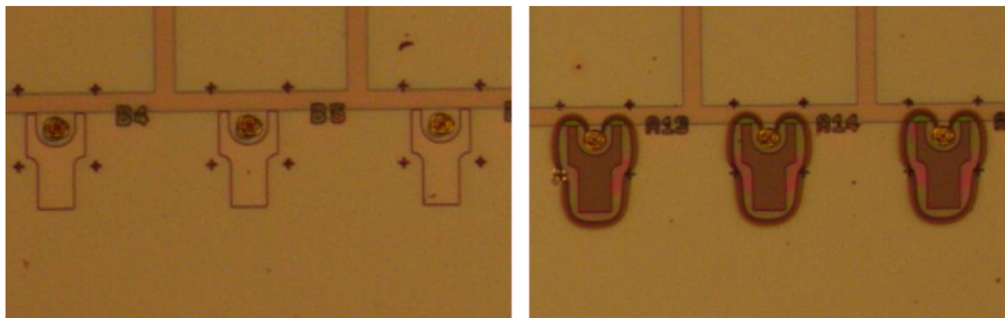


Figure 4.11 Optical microscope images of the p-contact opening area after ZEP520A development (left) and after LOR7B reaction (right), respectively.

4.4.19 Dry Etching of SiO_2 for P-Contact Opening

We would like to first etch away the thin SiO_2 coating at areas designed for p-contact electrodes. Samco RIE is used. The reaction time is calculated for SiO_2 thickness measured during PECVD deposition in section 4.4.11. The conditions are the same as standard SiO_2 etching previously used in section 4.4.4.

The points to note are similar as in previous processes related to Samco RIE. Separate hydrochloride cleansing which is usually done after RIE of SiO_2 is skipped this time. This is because the next step, etching of remaining InP covering the p-contact, is done by wet etching using several acid solutions.

4.4.20 Wet Etching of InP for P-Contact Opening

To clean the contact surface and remove the InP for p-contact opening, we use wet etching with a combination of phosphoric acid solution and hydrogen chloride solution (H_3PO_4 : HCl 3:1). The sample is submerged in such solution for about 2 min, and rinsed by water twice, then dried by N_2 pistol. The result can be checked by optical microscope, as shown in Fig 4.12.

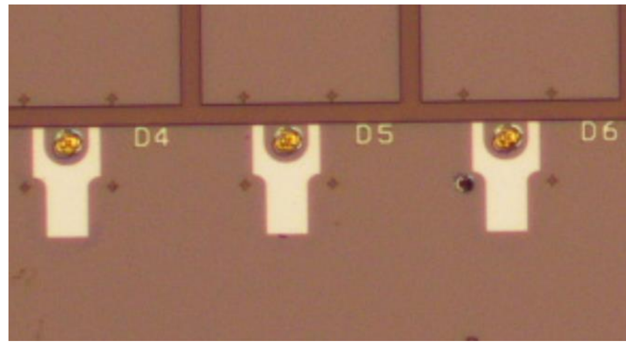


Figure 4.12 Optical microscope image of the p-contact opening area after dry-etching of SiO_2 and wet-etching of InP. The bright areas indicate where the bi-layer resist has been fully developed and reacted, and the SiO_2/InP layers above p-contact layer has been removed at those areas.

After wet etching, one should use ZDMAC and NMD solution to remove the residues of bi-layer E-beam resist residues. The conditions are similar to that in section 4.4.9. Afterwards, one could check the results using SEM, as shown in Fig 4.13 below.

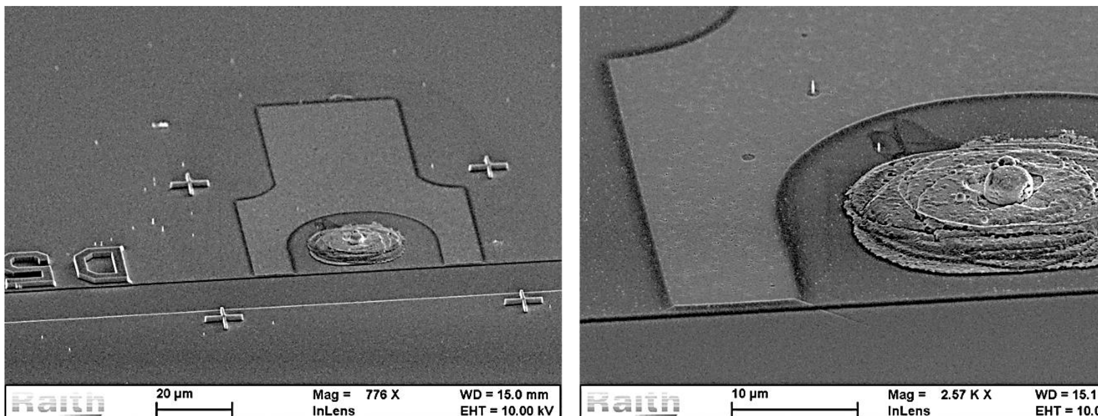
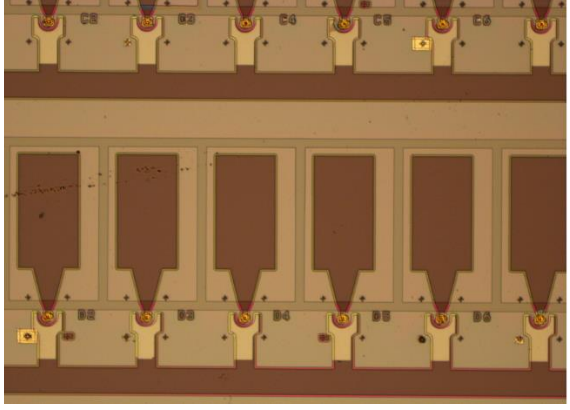


Figure 4.13 SEM images of the cavity after p-contact opening, shown at different scale. This is a circular cavity with diameter designed to be 1.7 µm. From the zoomed-in view, one could distinguish clearly the layering of the silver n-contact covered by gold protection layer, and the etched opening for p-contact layer. The actual distance of these two areas are estimated to be about 5 µm, which would be safe for avoiding short-circuit.

4.4.21 E-Beam Lithography (VI): Bi-Layer Resist Mask for Contact Electrodes Gold Deposition

Another round of e-beam lithography is performed to define the bi-layer resist mask for gold deposition on both p-contact and n-contact electrodes. The patterns and conditions are generally the same as in section 4.4.18 since we would like to reproduce the same window for metal deposition. The development is also similar, using ZED-N50 for 2 min 30 s and NMD for 12 s. Still, it is recommended to keep in mind that conditions may be different, and development and reaction time may need to change accordingly. Thus, we recommend to carefully check the results using optical microscopy for precise timing and avoiding over-reaction. Figure 4.14 shows typical optical microscopy image of the sample after bi-layer resist development and reaction for forming the mask of contact electrode deposition.



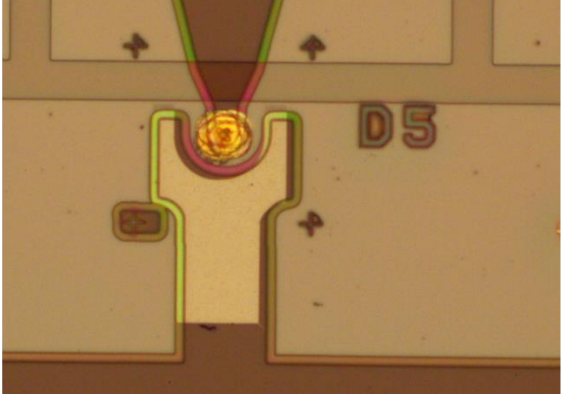


Figure 4.14 Optical microscope images of the p-contact gold electrode deposition area after development and reaction of the bi-layer resist mask, at different magnifications. The bright areas are where the p-contact layer is exposed during etching in section 4.4.19 and 4.4.20. The dark areas are the defined areas for gold deposition to form the p-contact electrodes.

4.4.22 Gold Deposition for Contact Electrodes

We perform e-beam evaporation to coat Ti/Au electrodes at the contact areas defined by bi-layer resist mask in the previous step. The conditions are set as in Table XIII below:

Step	Sample Orientation	Tilted Angle	Deposition material	Deposition Speed	Deposition Thickness
Deposition (1)	0°	0°	Ti	0.05 nm/s	60 nm
Deposition (2)	0°	0°	Au	0.2 nm/s	600 nm
Lift-off					

Table XIII E-beam evaporation and lift-off process for p-contact gold deposition.

The following lift-off is similar as in section 4.4.15 and 4.4.17. However, one should be careful as the gold layer is relatively thick, the lift-off might also be difficult this time. Optical microscope image of the finished sample after electrode deposition is shown in Fig 4.15.

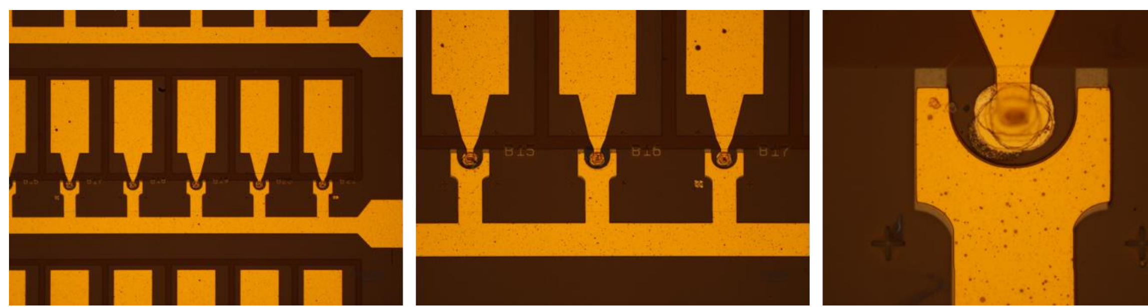


Figure 4.15 Optical microscope image after gold deposition for contact electrodes at different magnification levels.

Up to now, the sample fabrication is finished for all clean-room procedures. Clear examination of a 3D view of the fabricated devices can be examined using SEM, as shown in Fig 4.16.

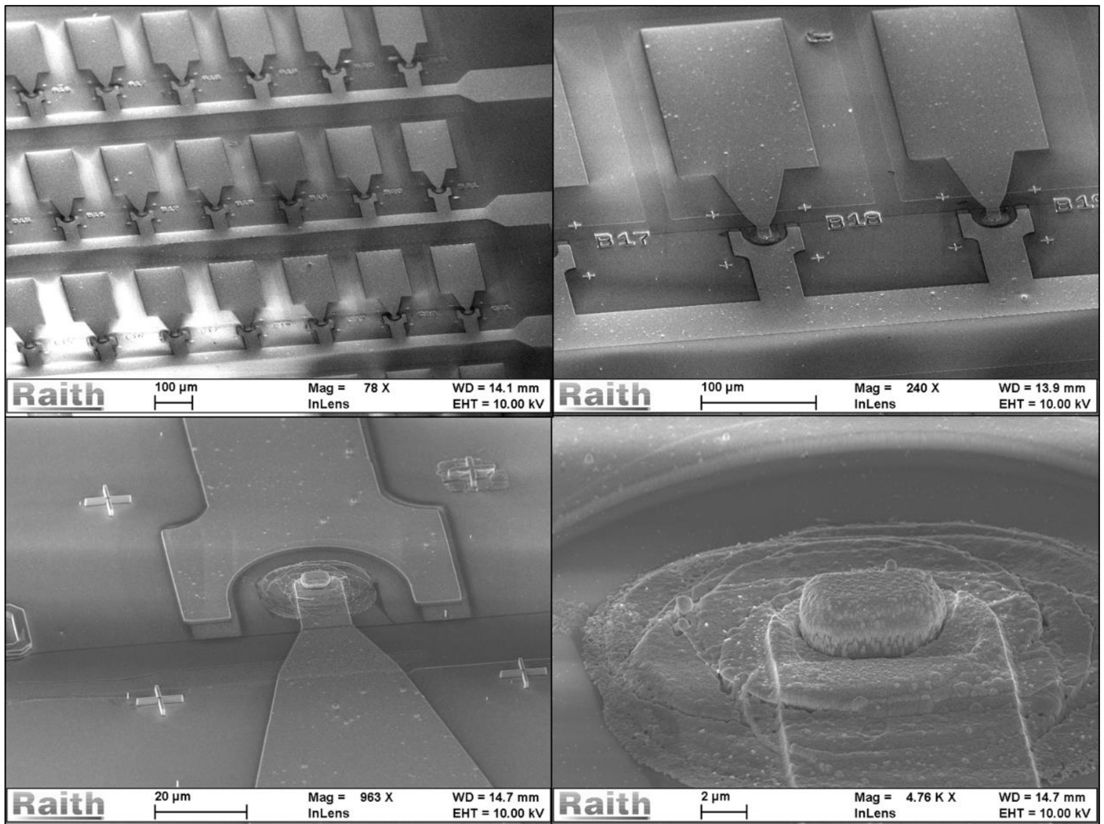


Figure 4.16 SEM of the finished devices at different magnification levels, in the order of 78x, 240x, 963x, and 4.76k x, from left-top to right-end, clockwise. The two electrode pads are well separated, with p-contact overlapping with its opening largely and the n-contact covering the cavity metal-clad thoroughly.

The next step would be device packaging and wire-bonding for electrical property and electroluminescence measurement.

4.4.23 Packaging and Wire-Bonding

The chip is mounted to a copper plate of about 5 cm by 4 cm size for testing. PCB board with several electrodes are also mounted to the copper plate, which would be suitable for current injection using electrical lines. The mounting is done using super glue.

Prior to electrically-pumped optical emission testing, wire-bonding is performed using WestBond Model 7700D Ball-Wedge Wire Bonder to connect the electrode on PCB board to the electrical pads on the sample. This step has to be done extremely carefully as high power will damage the contact layer and strike through the sample, thus create short-circuit, while too low voltage would not be enough for the bonding to be strong. We optimized the conditions as Table XIV below:

Step	Step Name (on display)	US Power	US Time	Load
Start from PCB electrode	Bond 1 of 2	400	50 ms	HIGH
Bond to chip electrode	Bond 2 of 2	50	50 ms	HIGH

Table XIV Wire-bonding conditions for bonding from PCB to sample electrode pads using WestBond Model 7700D Ball-Wedge Wire Bonder.

The power when bonding to the chip electrode end is set very weak so as to avoid damage of the device. Slight optimization of the conditions may also be needed for specific cases. The conditions depend on the deposition thickness of gold electrode as well.

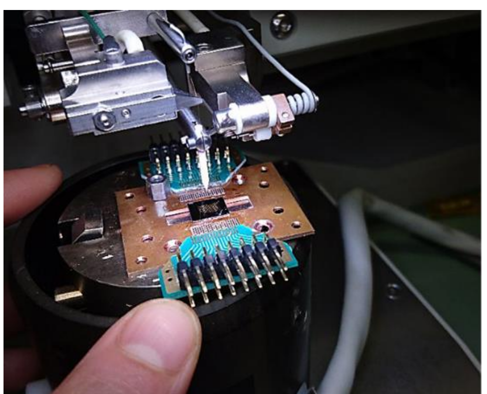


Figure 4.17 Images of the sample and PCB board mounted to copper plate and fixed on a heat stage using one screw for wire-bonding. Picture at the left shows also part of the wire-bonding machine, including the capillary tip where the copper wire passes through.

One should also be careful while handling the sample in this step, as the wire-bonding is done with the stage heated up to 120 ℃, and heavy shaking while handling the heated sample would easily break bonded wires. Figure 4.17 shows a picture of the sample fixed on the heat-stage using one screw for wire-bonding.

It is worth noticing that as the wire-bonding technique we utilized including the application of a short-time high-power ultrasonic shock to the electrodes on chip, some damage might have been introduced to the layers underneath, thus causing some device damage. In the future, it is advised to either introduce additional protection layer to the electrodes, but this might also bring in additional risks to the sample, especially for that the fabrication process already involves a large number of steps. Another alternative is to use WestBond Model 7200CR Dual Head Epoxy Die Bonder, which provides a vacuum pickup tool that can perform manual pick-up and drop-down of cooper wires. Combined with silver paste on sample, one might perform manual wire-bonding without applying additional power shock to the sample. However, the manual manipulation of such bonding might encounter much difficulty due to the ultra-small device size.

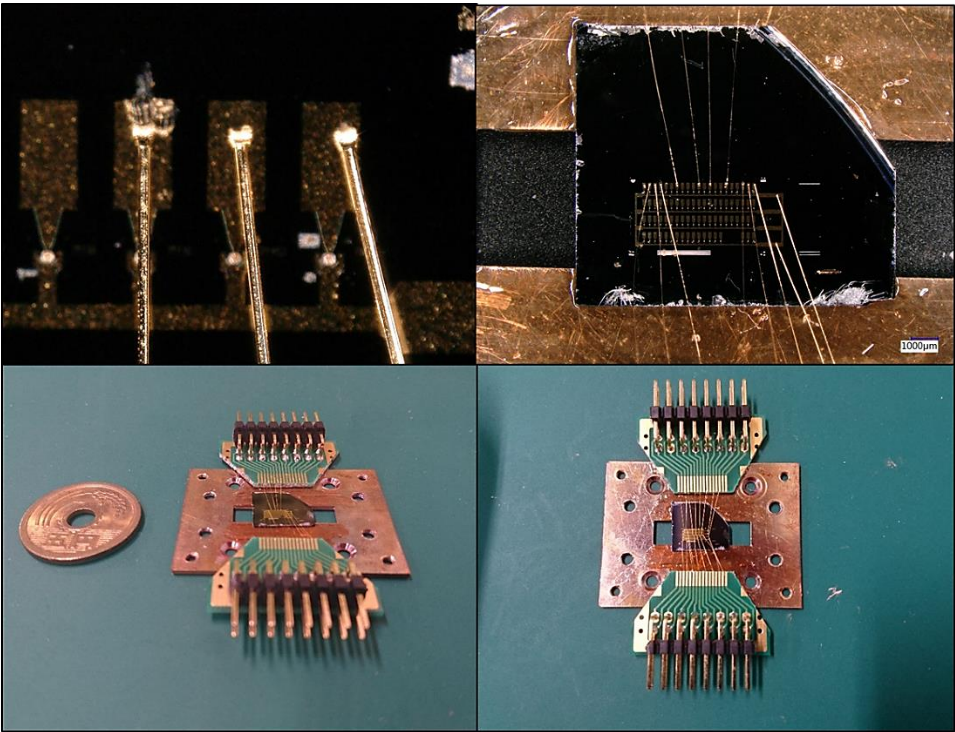


Figure 4.18 Device image after wire-bonding and packaging, from left-top to right-bottom in clockwise order: copper wire connection to p-contact, sample chip mounted to cooper plate by super-glue, sample chip dimension and thickness compared to a Japanese 5-yen coin, and overview of the finished sample chip ready for measurement.

4. 5 Comments on Fabrication Process

The fabrication process of wavelength-scale silver-clad InP/InGaAs cavities aimed for electrically-pumped lasing is presented, and critical conditions and points to note during the fabrication are discussed in great detail, thus we would avoid too much redundancy in restating them as a summary. However, here are some personal comments as a review of the fabrication process:

(1) The multi-step dry etching (section 4.4.5) is critical for verticality of the semiconductor core. It is advised to start over from the first step if one could tell from SEM that the etched pillar has poor condition (e.g. low verticality, rough surface, etc.).

(2) One should always be ultra-careful and keep in mind that the pillars are versatile due to their small size. Ultrasonic cleansing should be avoided after etching of the III-V cavity core (section 4.4.5) as it may destroy the structures easily.

(3) Generally, the surface condition of the cavity cores always needs to be taken care of before encapsulation by silver. It is always advised to keep in mind that one should keep the sample surface clean and avoid any possible dirt, and perform organic cleansing before handling the sample. Careless manipulation could easily introduce defects on surface and leads to worse conditions in following steps. In particular, the surface cleansing steps and

surface passivation steps (section 4.4.10) is the last treatment of the III-V core before insulation layer, and we believe that it plays an important role in improving the performance.

(4) The III-V wafer is very fragile, and is more brittle than Si wafer. One should always handle the sample with great care and avoid excess force when using tweezers.

In addition, certain improvements could also be made in future fabrication:

(1) Improved design of the markers will facilitate easier three-point alignment in multi-layer e-beam lithography. We carried out six e-beam lithography on the same sample, with markers on various locations of the first layer of the mask. However, the largest marker (leading marker) is designed only at the left-bottom corner of the wafer, and it becomes hard to locate after a few exposures. Additional leading markers are advised to be incorporated at other corners to make better three-point alignment.

(2) The contact open for n-contact (section 4.4.12) is a technique that is hard to standardize and needs to be learned from experience, thus limited details are provided in this section. In future works, it is advisory to note down carefully the gradual change of the device surface through the etching cycles for one's reference in developing a standardized n-contact open process.

(3) The difficulty in wire-bonding is related to the design of copper plate as the packaging and the device mounting. In the future, improved design of packaging could largely alleviate the risk in wire-bonding of damaging the device. For example, more space could be added as buffers in the arrangement of cavity arrays, and the electrode pads could also be designed with better placement to avoid crossing of wires and possible short-circuits. It is also better to reduce the gapping space in between the PCB board and the sample chip mounted on the copper plate, so that the bonding wire does not need to risk the long-distance dangling in space.

Chapter 5

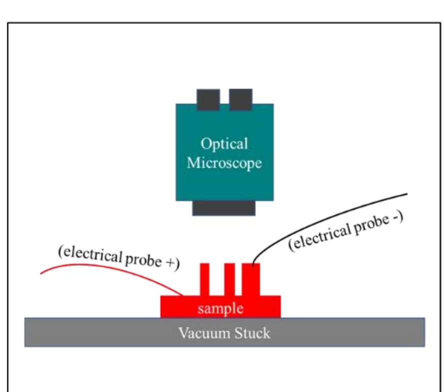
Measurement Results and Discussions

5.1 Introduction

In this chapter, we present and discuss the experimental measurements of the fabricated devices. There are 84 laser cavities designed and fabricated on one sample chip, as explained in detail in section 4.2. We performed measurement of both the electrical properties and optical properties of some selected devices.

In Section 5.2, we will discuss the electrical properties of the selected devices. In section 5.3, we will discuss the electrically-pumped optical performance of the selected devices. In particular, unambiguous room temperature electrically-pumped lasing of a circular cavity of diameter 1.5 um is observed and characterized. This cavity has an estimated volume of $0.6\lambda^3$, which marks much improved fabrication techniques with advanced design, and it is comparable to the world record of the smallest room temperature electrically-pumped metal-clad semiconductor laser [24].

5.2 Electrical Properties of the Cavities: I-V Measurement



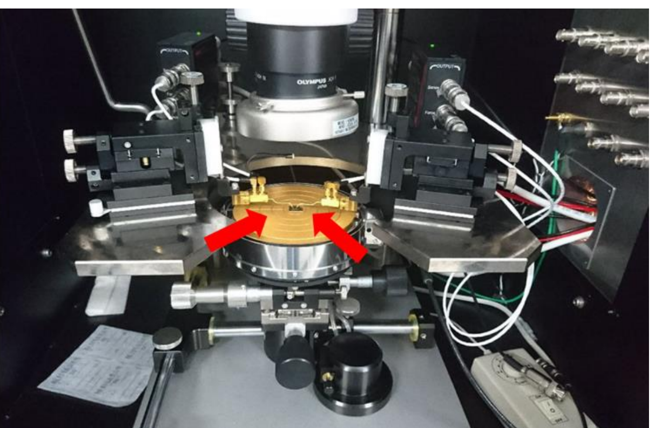


Figure 5.1 Measurement experiment set-up for I-V Measurement. A schematic representation is shown at the left, and a photo is shown at the right. On the photo, angles indicate the anode (left) and cathode (right) of the probe needles for applying voltage to the electrodes on cavity directly.

We use Keithley 4200-SCS Semiconductor Parameter Analyzer to measure the electrical properties of the cavities. The set-up is shown as in Fig. 5.1. The device is placed on the chuck and fixed with vacuum channels from the chuck. As marked in the figure, the anode

and cathode probe needles are carefully manually adjusted to directly touch the p-electrode and n-electrode fabricated on the chip respectively. One should be extremely careful at this step to avoid crushing the electrode coating on the sample surface.

In order to perform DC I-V measurement, we applied forward-biased voltage to the p-i-n junction using KITE software installed to the computer. Usually, a voltage sweep of range 0 – 3V, 0 – 4V, and 0-5 V are applied, chosen and judged according to cavity sizes for a fair comparison in terms of current density.

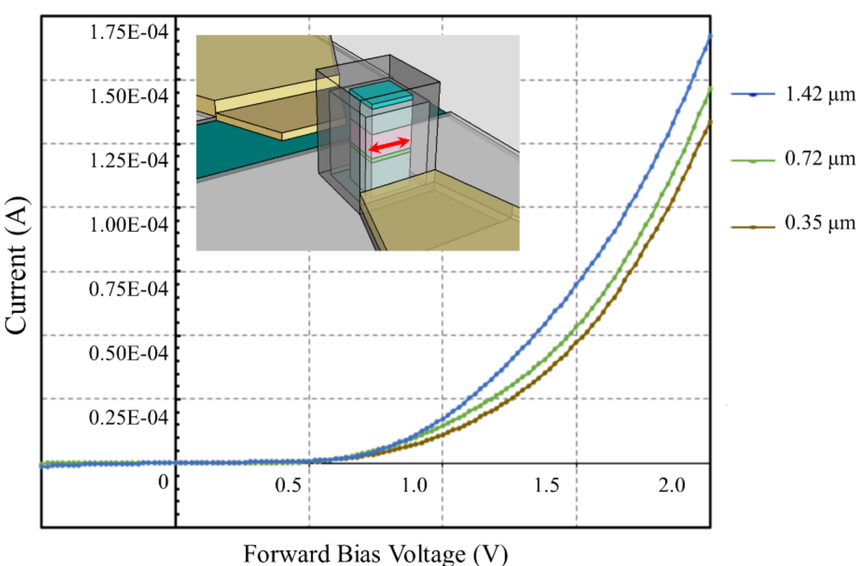


Figure 5.2 I-V measurement results of wavelength-scale metal-clad semiconductor laser cavities with square cross-section, as side length of the device semiconductor core ranges from 0.35 μm to 1.42 μm. Inset shows schematic of the device, and the red arrow indicates the device side length of the III-V semiconductor core.

Figure 5.2 shows the measured I-V curves of square cavities with side length 0.35 μm, 0.72 μm and 1.42 μm, respectively. One could see that the threshold voltage is generally consistent as around 1.0 V, and smaller device shows larger overall resistance. The overall resistance can be seen as the semiconductor core resistance, bottom contact resistance and other circuitry resistance connected in series. Ideal fabrication quality should give the same bottom contact resistance and circuitry resistance for different devices on the same chip, and making the semiconductor core resistance the dominant factor of overall resistance. Given that for a resistive material, $R = \rho \cdot l/A$, where R is the resistance, ρ is the electrical resistivity of the material, l is the length and A is the cross-sectional area. The reverse dependency relationship of overall resistance on device cross-sectional area is consistent with our expectation, showing that the fabrication quality of the electrodes of the devices are generally consistent and it plays a minor role in overall device resistance.

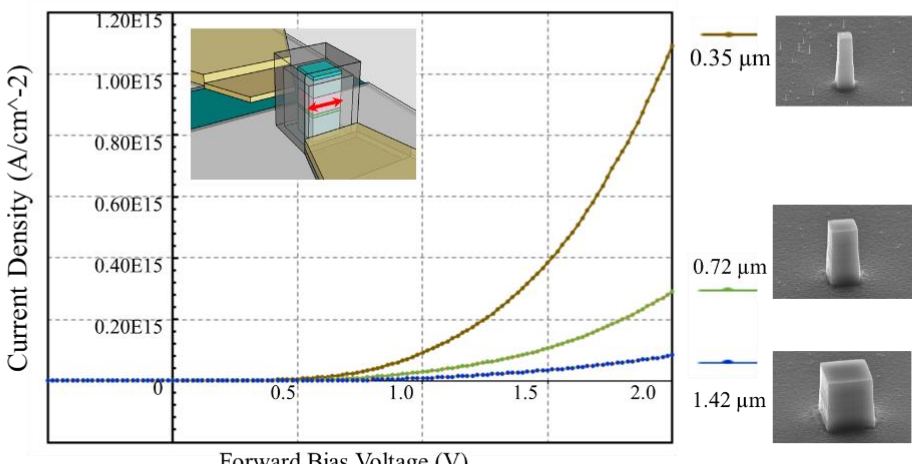


Figure 5.3 J-V measurement results of wavelength-scale metal-clad semiconductor laser cavities with square cross-section, as side length of the device semiconductor core ranges from 0.35 μm to 1.42 μm. Inset shows schematic of the device, and the red arrow indicates the device side length of the III-V semiconductor core. SEM images of the semiconductor core of corresponding cavities are also listed on the right.

To make a fair comparison, we plot the J-V curve of the device, which is the calculated current density versus bias voltage, with the same selection of square-cross-section cavities, as shown in Fig 5.3. One could see that, assuming the same device length, the smaller cavity gives actually lower overall resistivity compared to larger ones. This may due to additional defects on the device surface or silver coating of the larger devices.

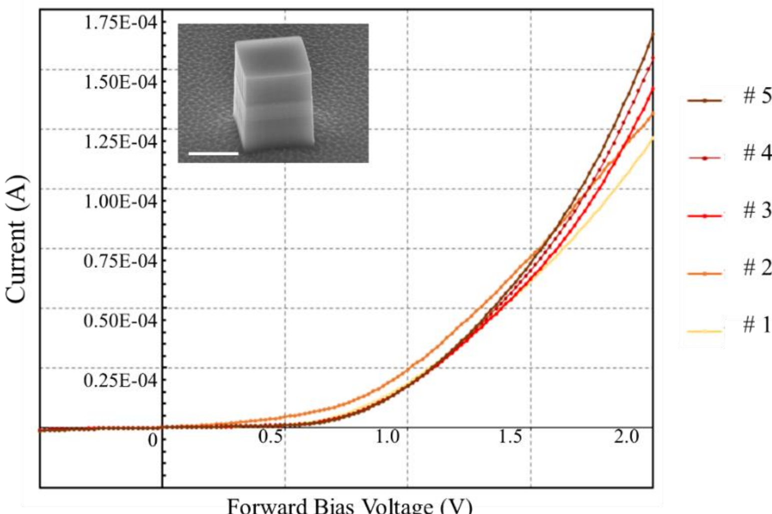


Figure 5.4 Evolution of the I-V curve of one cavity during five consecutive measurement. The colors mark different trials of the measurement, from trial # 1 to trial #5. This is a cavity with square cross-section of side length 1.42 μm, and an SEM of its semiconductor core is shown in the inset. The scale bar is 1 μm.

It is worth noticing that the I-V curve of one device will change slightly during the first few trials when one performs the measurement. Figure 5.4 shows the evolution of I-V curve of the same device (as of a square cavity with side length 1.42 um) during five consecutive measurements. The resistance reduces gradually in future measurement compared with the starting ones, and later stables down as the last entry. This is suspected to be related to the silver quality and heating effect. During the I-V measurement, the device generates some heat, thus creating an annealing-like effect on the silver cladding of the cavities. Thus, the future measurements give better I-V qualities for the same diode, and the results tend to stay stable after a few times of trials, typically about five or six times.

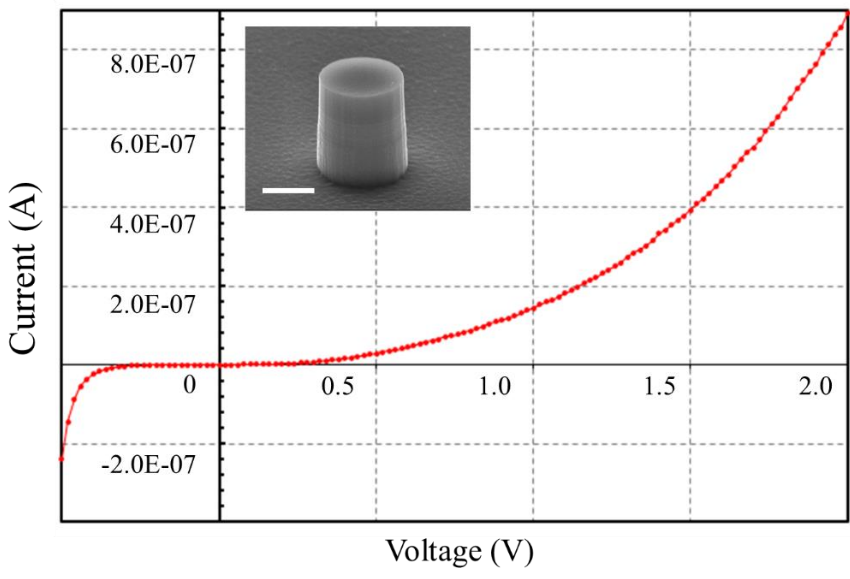


Figure 5.5 I-V measurement result of a device showing large reverse current, marking possible defects. This is a cavity with circular cross-section of diameter 1.4 μm, and an SEM of its semiconductor core is shown in the inset. The scale bar is 1 μm. The data correspond to cavity #C17 at Appendix B.

It is worth notice that we prefer to perform the I-V measurement before wire-bonding of the devices, as one can tell from Fig 5.1. This is because that the ultrasonic shock applied during wire bonding could very easily strike through the device and destroy the junction. Figure 5.5 shows the I-V curve measurement of a circular cavity after wire-bonding. There exists clearly very large reverse current when a negative voltage is applied, and we suspect this is caused by the wire-bonding step. The exact reason of the break-down, whether it is due to the wire-bonding, and potential alternatives to improve the device tolerance still need to be studied.

After measurement of the I-V characteristics, we move on to perform electroluminescence measurement of the selected devices that have satisfactory electrical properties.

5. 3 Optical Properties of the Cavities: Electroluminescence Measurement

Prior to electroluminescence measurement, it is required to perform wire-bonding of the selected cavities, as discussed in section 4.4.23.

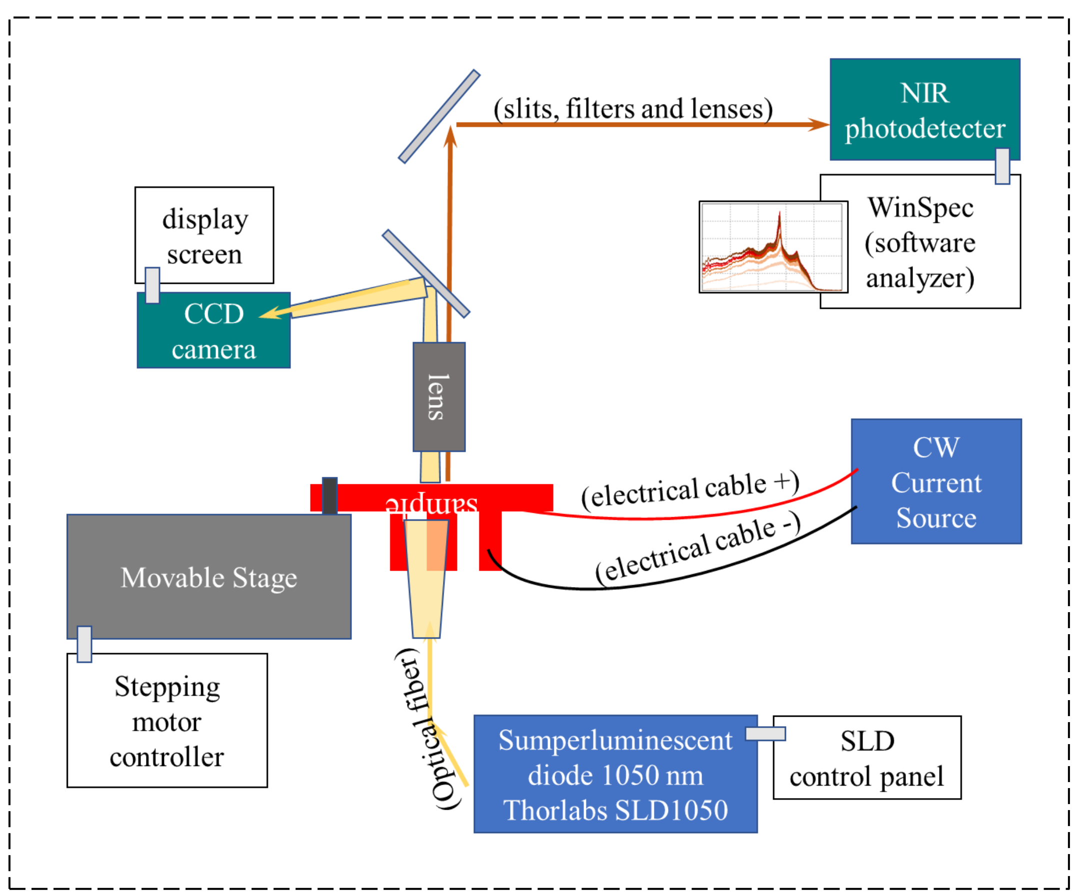


Figure 5.6 Schematic of the experiment set-up for electroluminescent measurement.

The experiment set-up of the electroluminescence measurement is shown in Fig 5.6 and Fig 5.7. The copper plate mounted with the sample is fixed on a movable stage connected to external stepping motor controller that could control the stage location in *x, y, z* directions with precision down to micrometer scale. The sample is placed with cavities facing downwards and InP substrate flipped on top, such that one could collect the emitted light from above, through the InP substrate. The light is collected through 50x NIR lens, and after several mirrors, lenses and filters it would pass a slit with adjustable aperture and be collected by a Princeton Instruments Acton SP2500 NIR Monochromator/Spectrographs. The spectrum is analyzed using Princeton Instruments WinSpec Spectroscopy Software.

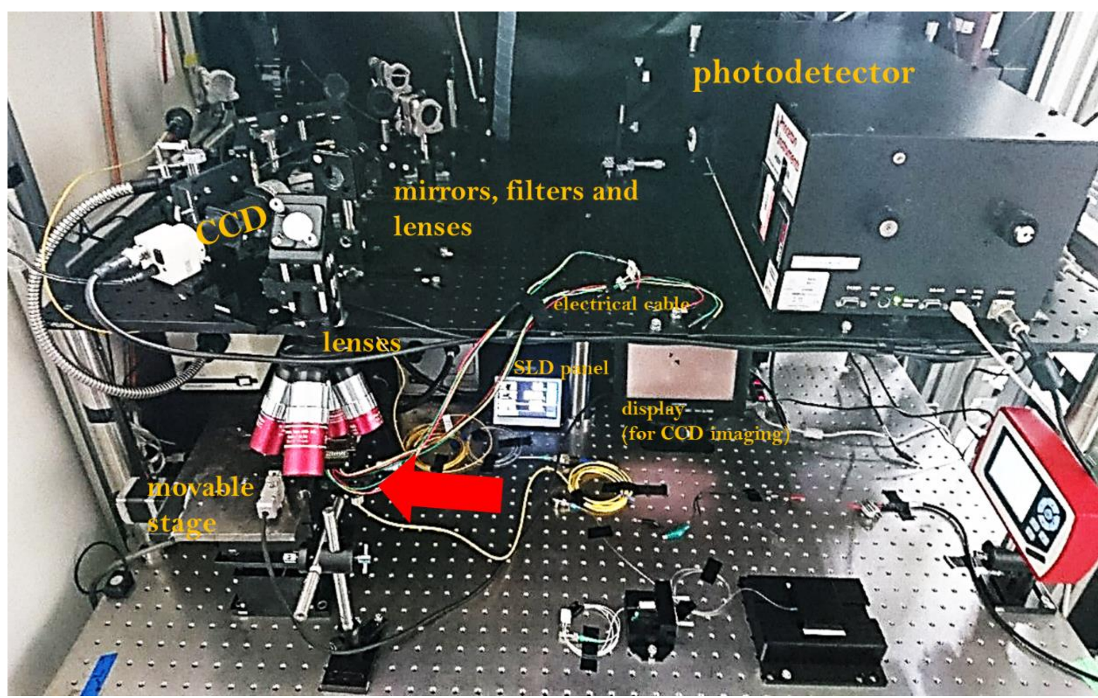


Figure 5.7 Experiment set-up of the electroluminescent measurement. Red arrow in the figure indicates location of the sample. Critical components in the set-up are marked out in yellow.

To locate the tested cavity from the sample and identify the cavity from the 21 x 4 cavity arrays, we use Thorlabs SLD1050, a superluminescent diode at 1050 nm, to illuminate the sample through a fiber cable from beneath. A CCD camera is used to collect the light that goes through the sample and reflected by a mirror, after carefully adjusting the focus, one could get a clear image from the camera. Shading of electrode pads and bonded wires on the sample will be visible from the camera imaging, as shown in Fig 5.8. One could manually adjust the movable stage using the stepping motor controller so as to locate each cavity.

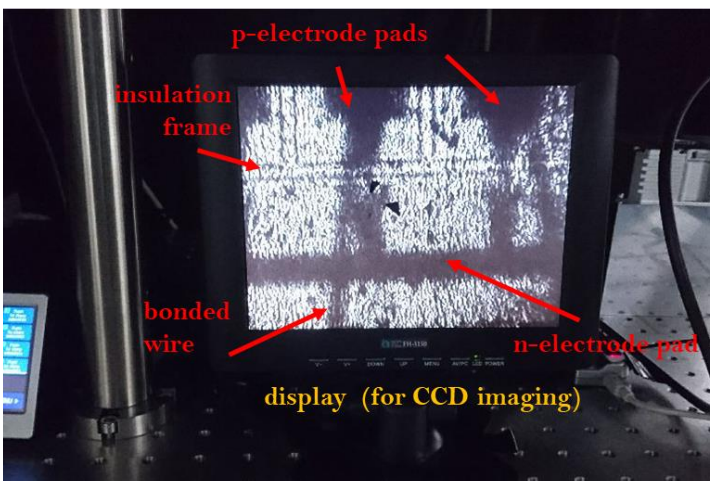


Figure 5.8 Understanding the display from CCD imaging to locate the cavity. Red markers explain the components in the imaged shadings. Black triangles are tapes sticked on the screen earlier to mark the actual focus region, which is pointing to a cavity from this photo.

This set-up is compatible with an additional cooling system using Cryostat. Details are provided in [30]. In this thesis, only room-temperature measurement results are presented and discussed, thus we would omit redundancy of the low-temperature measurement results of some devices performed and discussed in [30].

Current injection of the sample is performed with current source using electrical cables. Room temperature continuous-wave electrical pumped operation of the devices are measured and characterized. Here we present the measured electroluminescent spectrum of four different devices from the same sample.

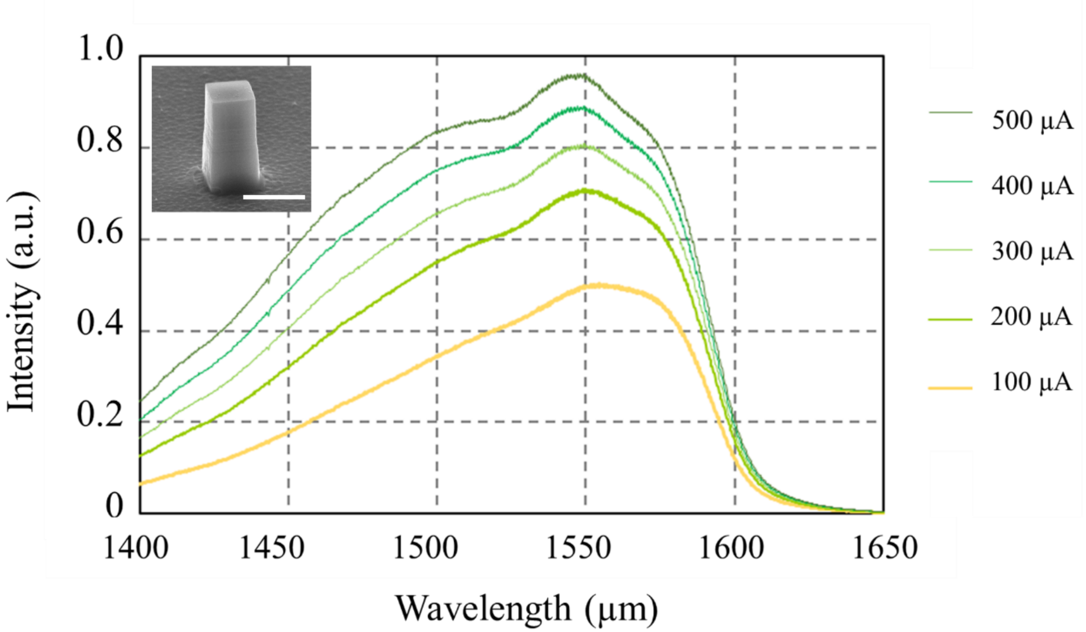


Figure 5.9 Spectrum under RT CW operation of a metal-clad semiconductor cavity with volume size $0.51\lambda^3$ with varying injection current. Inset shows an SEM image of the semiconductor core of this cavity before deposition of the insulation layer and metal-cladding. The scale bar is 1 μm. The data correspond to cavity #A10 at Appendix B.

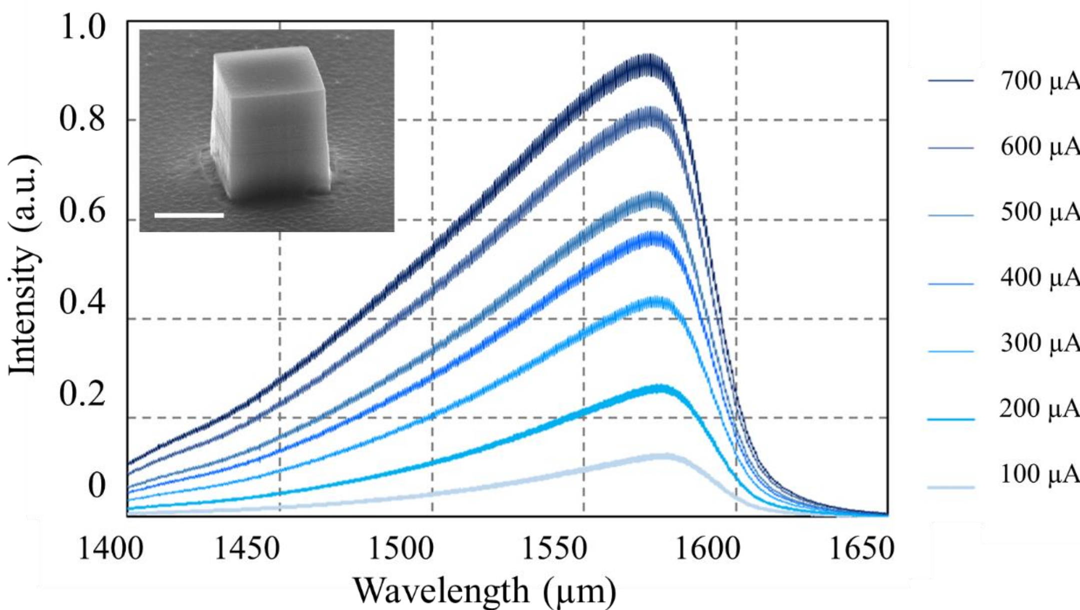


Figure 5.10 Spectrum under RT CW operation of a metal-clad semiconductor cavity with volume size 1.15 λ^3 with varying injection current. Inset shows an SEM image of the semiconductor core of this cavity before deposition of the insulation layer and metal-cladding. The scale bar is 1 μm. The data correspond to cavity #A16 at Appendix B.

Figure 5.9 shows the room-temperature (RT) continuous wave (CW) electroluminescent spectrum of a wavelength-scale silver-clad InP/InGaAs cavity with square cross-section of side length 0.71 μm and estimated cavity volume of $0.51\lambda^3$ under increasing pumping current. Broadband emission is observed under current injection, and the peak is estimated to be at 1550 nm. Figure 5.10 shows the spectrum of another cavity with square cross-section, but of slightly larger side length 1.42 μm and estimated cavity volume of 1.15 λ^3. Again, broadband emission is observed under RT, CW current injection, and the peak is estimated to be at around 1570 nm.

Lasing is not observed from these two cavities, and we suspect the reason could be low cavity Q factor due to large scattering loss at the corners of the cavities. These devices still have the potential to give better optical performance under low temperature, however the experiments are not carried out at this stage.

We move on with the same set-up to measure some cavities with circular cross sections. From previous analysis of FDTD simulation, circular cavities of the same geometry usually provide higher cavity Q factor compared to other shapes, due to better confinement of the modes, namely whispering-gallery mode, inside the active layer. Though the circular design may make it harder for waveguide coupling, it remains valuable to study their electroluminescent properties. The results are advisory on examining the fabrication qualities from improvements reported in chapter 4, as the standard circular shape cavity brings in little additional factors affecting the performance, and can be compared with the results of many previous works reported in literature.

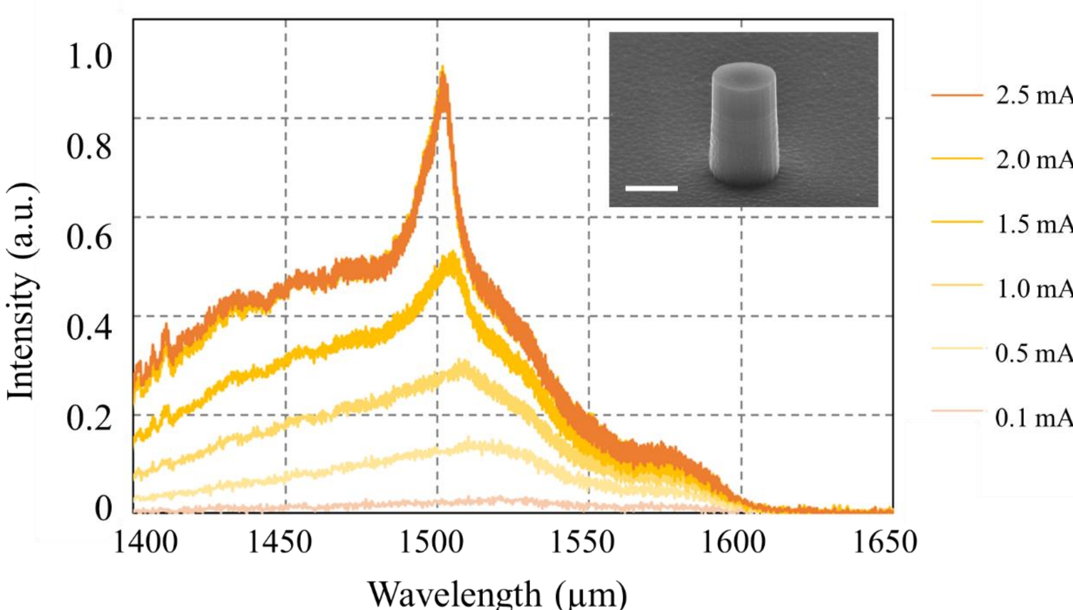


Figure 5.11 Spectrum under RT CW operation of a metal-clad semiconductor cavity of circular cross-section and diameter 1 µm, with varying injection current. Inset shows an SEM image of the semiconductor core of this cavity before deposition of the insulation layer and metal-cladding. The scale bar is 1 um. The data correspond to cavity #C10 at Appendix B.

Figure 5.11 shows the room-temperature (RT) continuous wave (CW) electroluminescent spectrum of a wavelength-scale silver-clad InP/InGaAs cavity with circular cross-section of semiconductor core diameter 1um and estimated cavity volume of $0.23\lambda^3$ under increasing pumping current. Broadband emission is observed under low current injection, and enhanced emission at certain wavelength slowly appears with increasing current. The peak wavelength of the spectrum shifts gradually from about 1520 nm to 1500 nm with increasing current.

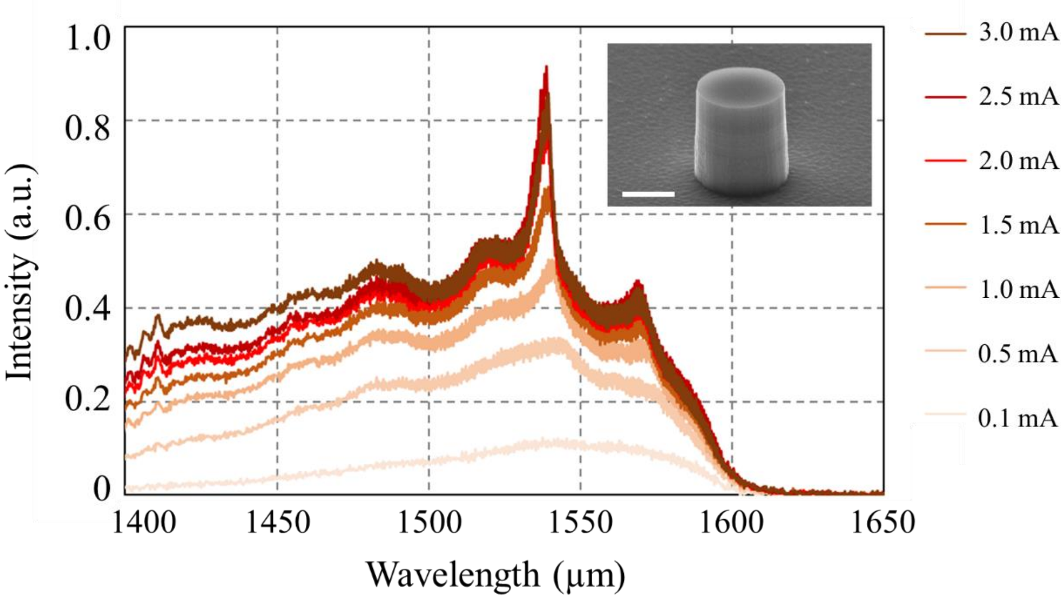
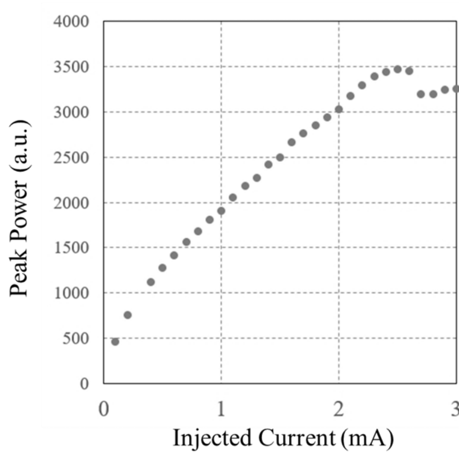


Figure 5.12 Spectrum under RT CW operation of a metal-clad semiconductor cavity of circular cross-section and diameter 1.5 µm, with varying injection current. Inset shows an SEM image of the semiconductor core of this cavity before deposition of the insulation layer and metal-cladding. The scale bar is 1 µm. The data correspond to cavity #C20 at Appendix B.

Figure 5.12 shows the operation under the same condition of a circular cavity with slightly larger diameter of 1.5 µm, and an estimated semiconductor cavity volume of about $0.52\lambda^3$. Spectrum with increasing current from 0.1 mA to 3.0 mA is plotted. The wavelength of peak intensity shifts gradually from about 1550 nm to shorter wavelength of 1540 nm with increasing current. A narrow peak is observed at higher current. We suspect room-temperature continuous-wave lasing under electrical pumping is achieved in this silver-clad InP/InGaAs semiconductor laser with circular cross section.

We plot the L-I curve of the suspected lasing mode of from this spectrum. The estimated peak power is computed by summation of the collected light power within the highest peak, which gives an estimation of the integrated intensity of the suspected lasing mode.



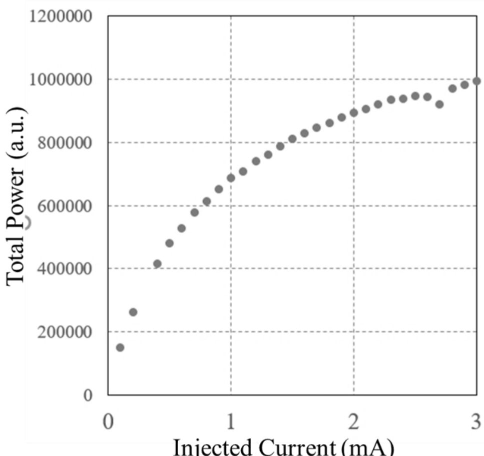


Figure 5.13 L-I curve of the circular cavity with diameter 1.5 um, computed from data presented in Fig 5.12. The data correspond to cavity #C20 at Appendix B.

The spectrum showed cavity enhancement and potential for room-temperature CW lasing of a wavelength-scale metal-clad semiconductor laser with circular cross-section. The cavity has a volume that is smaller than the record from any reported literature [24], and it marks large improvement in device design and fabricated cavity qualities, which leads to reduced scattering and absorption loss and improved cavity quality factor. The lasing threshold current might be higher than expected, and larger compared to the results obtained under low temperature [30, 44], but we did not increase the current due to concerning about temperature rise in the cavity. Quality of the cavities on the same sample chip still varies case by case, and full characterization of all fabricated cavities is not yet finished at this stage. The presented results show possibilities of achieving room-temperature lasing with lower threshold current using the optimized fabrication techniques, and possible future works will be discussed in Chapter 6.

5. 4 Summary

In this chapter, the I-V measurement and electroluminescent measurement results of selected devices with either square cross-sections or circular cross-sections are presented.

The measurement results prove high device fabrication quality and general agreement with theoretical predictions. We observe cavity enhancement of a silver-clad InP/InGaAs light emitter with a volume as small as $0.52\lambda^3$.

In addition, we would like to point out that though enhancement is observed only from one of the circular cavities, this serves as no proof of the exclusive dependency of optical property on cavity shape. The measurement of the fabricated batch of devices is not finished at this stage, and there is high potential that room-temperature operation of the cavities with similar scale but different shapes would give even improved performance.

The satisfactory results in room-temperature electroluminescent measurement proves the improvement of our fabrication quality, and it is advised that one should look into cavities of different shapes, and more importantly, their possible coupling schemes to waveguide, since it serves as a critical step in applications, as discussed and advised through Chapter 1 to Chapter 3.

Chapter 6

Conclusions and Outlook

Research on design, fabrication and experimental measurement of wavelength-scale metal-clad semiconductor lasers with potential of being coupled to waveguide in integrated photonic circuits was reported in this thesis. The main achievements can be divided in four parts:

(1) We designed a wavelength-scale silver-clad InP/InGaAs laser cavity in capsule shape with improved thermal properties to reduce self-heating, and proposed a coupling scheme for evanescent output of its emitted light to a silicon-on-insulator waveguide. Thermodynamic properties inside the laser cavity have been studied for understanding its self-heating issues. Regarding cavity design and thermal properties, possible future developments could be made by conducting thermodynamic simulation in search for alternative cavity design, and by looking for more optimized structure with less scarification of device optical properties while keeping the merits of improved heat dissipation. It may be possible through:

> - changing the insulation layer material to one with better heat conductivity (e.g. Al_2O_3 instead of SiO_2);
>
> - exploring the heat dissipation properties with different device shape by conducting 3D thermal simulations instead of using cylindrical symmetric conditions;
>
> - exploring thermal properties of metal-clad semiconductor lasers with novel designs, such as changing the laser to a ring-like profile which gives whispering-gallery mode light confinement, and depositing metal inside the ring core to serve as a heat conduction path closely in touch with the active layer for effective heat dissipation;

(2) We proposed a novel design of an integrated optical feedback stub formed at the non-output end of the cavity for the waveguide-coupled laser structure designed in (1). With optimized length and shape, the stub functions effectively to tune the Q factor of the resonant mode inside the cavity. We numerically demonstrated 5-fold improvement of the Q factor for a given cavity. We also applied coupled-mode theory to provide a quantitative analysis of the Q factor enhancement, and the results from theoretical calculation agree well with those obtained through numerical simulations. This mechanism of integrated

feedback stub could be applicable to a variety of other waveguide-coupled metal-clad lasers. Regarding this part, related future works could be:

- demonstrating the Q-factor tuning mechanism of integrated feedback stub with different waveguide-coupled small lasers, such as InP-waveguide coupled to metal-clad InP/InGaAs lasers, or SOI-waveguide coupled to wavelength-scale photonic crystal nanocavities;

- studying the effect of the integrated feedback stub on waveguide coupling efficiency. It has been shown that there may exist trade-off between the coupling efficiency and cavity Q factor through this evanescent coupling scheme. The Q-factor tuning from the integrated feedback stub may also have an effect on the coupling efficiency, which should be taken into consideration in aim for applying it to integrated photonic circuits.

- investigating fabrication techniques in realizing the proposed structure of metal-clad semiconductor cavity coupled to waveguide with integrated feedback stub, and verifying the relationship of Q factor with different stub length experimentally through electroluminescent measurement.

- proposing alternative coupling scheme for the integration of metal-clad semiconductor lasers to waveguides. For example, it may be possible to use in-plane evanescent coupling especially for the circular laser cavities, as the vertical evanescent coupling scheme may be less efficient for the whispering-gallery mode in circular cavity. However, in-plane waveguide coupling may also introduce additional complexity in fabrication in terms of wafer alignment and wafer bonding.

(3) We fabricated batches of silver-clad InP/InGaAs cavities on InP substrate with various shapes, which are eligible for measurements in demonstrating electrically-pumped light emission under room-temperature. An extensive review of the fabrication process was presented with great details, and certain improvements have been demonstrated through various fabrication steps. Regarding this part, possible improvements of fabricating these devices have been listed in section 4.5, “comments on fabrication process”, thus we would avoid redundancy in stating them in this chapter. Apart from those improvements, possible future work could also include:

- exploring future fabrication techniques of the metal-clad semiconductor laser coupled to waveguide;

- studying in details of the effectiveness in some fabrication steps by careful device characterization, such as characterization of the effect on device performance from silver quality caused by different adhesive thin layers. However, these studies may be hard to make fair comparisons for reaching convincing conclusions as one needs to limit the variables in any other step during fabrication of two separate samples.

- applying the current fabrication techniques, especially the effective surface treatment and surface passivation steps, to fabrication of other metal-related III-V nanostructures, such as the fabrication of surface-normal metallic grating modulator which is currently under active research from other members in our laboratory.

(4) We performed measurements of both electrical properties through I-V relationships and optical properties through electroluminescent experiments of some selected devices on the sample chip we fabricated in (3). Particularly, we reported cavity enhancement in electrically-pumped room temperature operation of a wavelength-scale metal-clad semiconductor light emitter with circular cross-section. The cavity has a volume that is smaller than the record of such laser from any reported literature. This experiment shows potential for room-temperature electroluminescence by metal-clad semiconductor lasers in practical applications. Possible future works in this part are:

- conducting measurements of I-V relationship and electroluminescence of the other fabricated cavities on the completed and packaged sample; comparing the results from different cavity design through the sample process and analyzing the performance with relation to cavity shapes;

- conducting electroluminescent measurement of selected devices under low temperature, e.g. that of 78 K with the aid of cryostat; studying the effect on device performance from different temperatures; explaining the experiment results using thermal simulations;

- conducting characterization of the emitted light from selected cavities, such as polarization analysis to identify the resonant mode from the cavities; comparing the measurement results with theoretical predictions and with numerical results obtained through FDTD simulations.

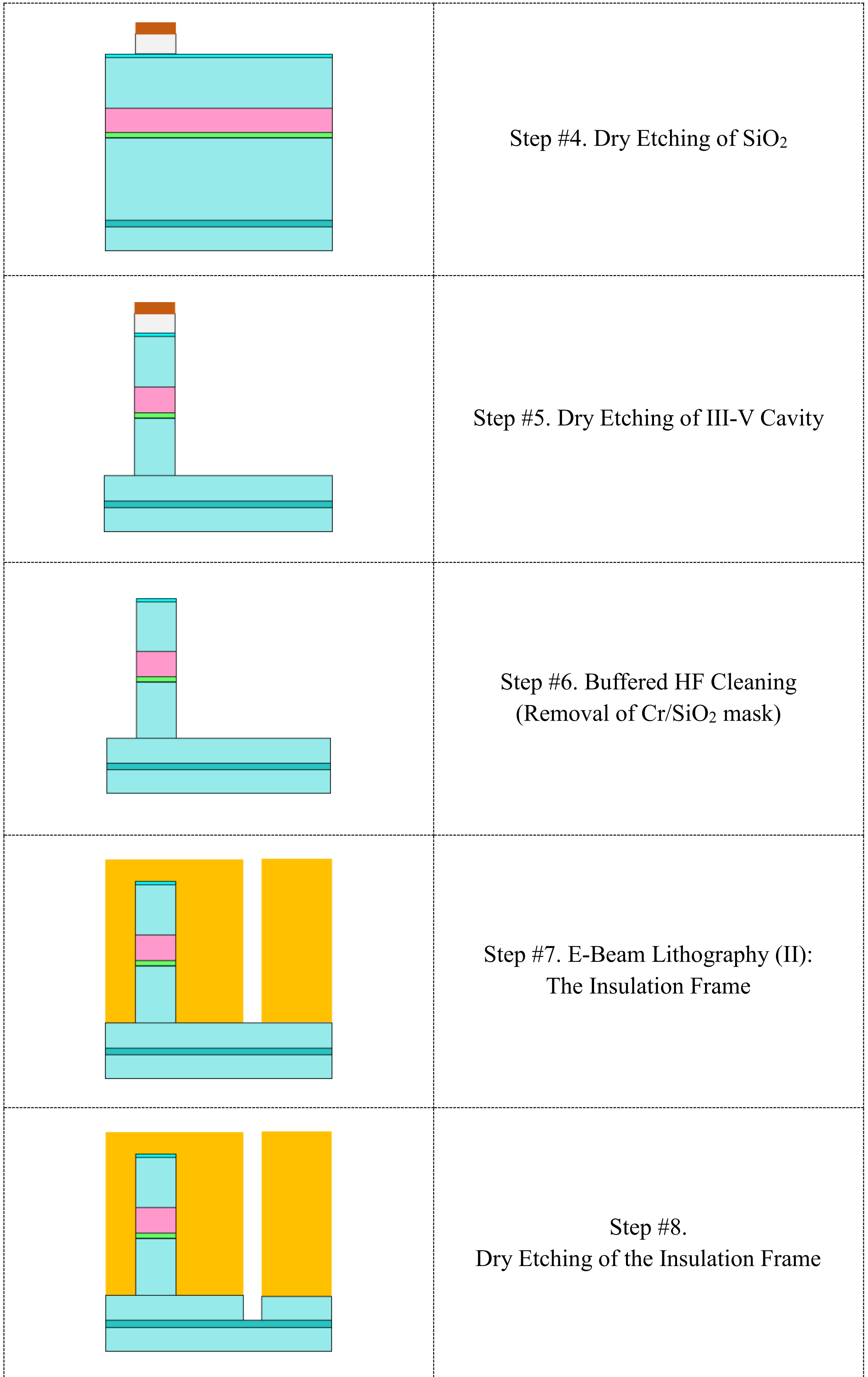
- performing photoluminescence measurement of the selected device through optical pumping, with techniques such as substrate removal; comparing the photoluminescence results and electroluminescence result of the same cavity;

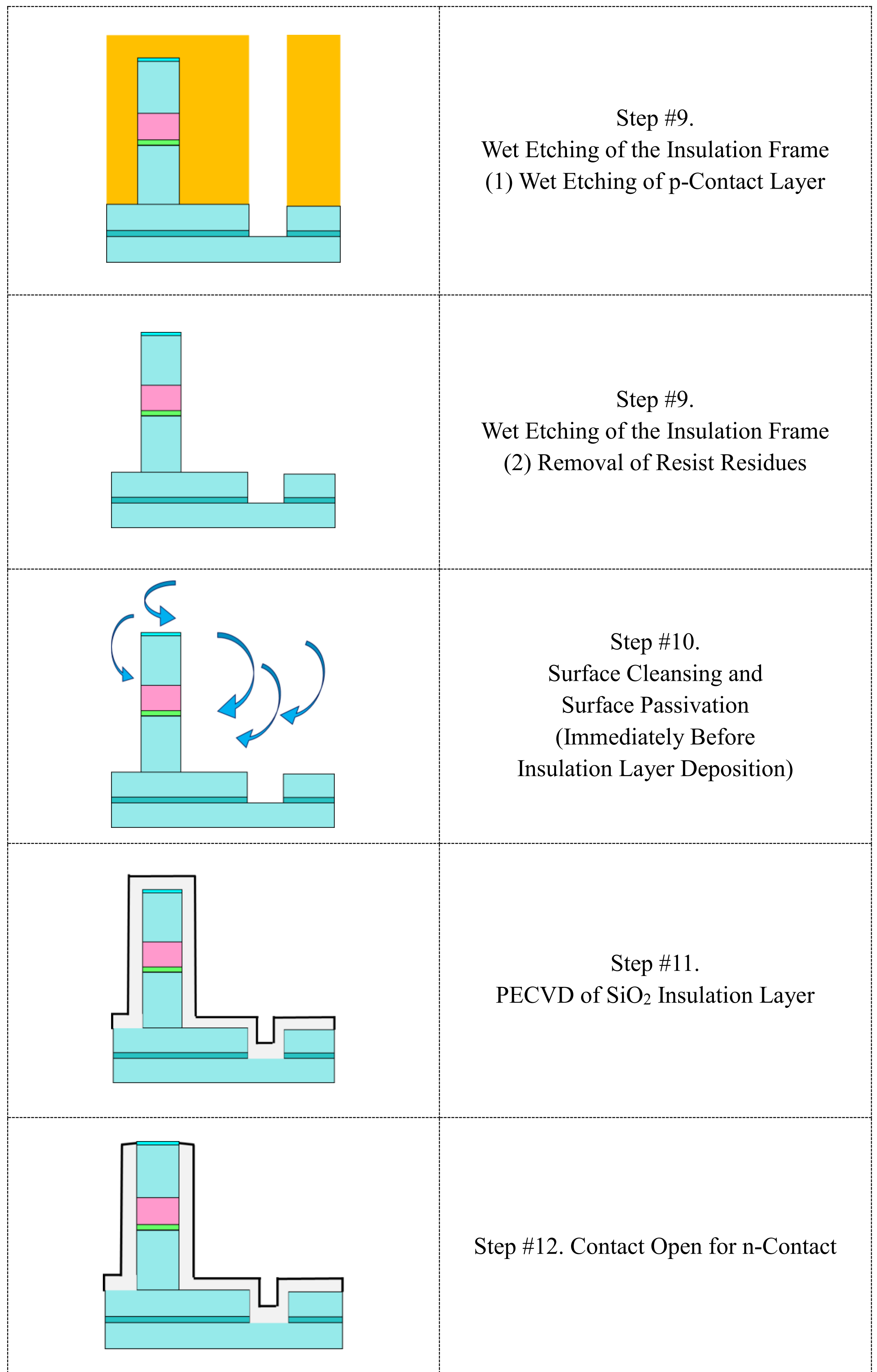
- exploring measurement set-up for devices that are coupled to waveguide; possible woks may include designing grating couplers integrated on-chip, and performing optically-pumped measurement with pumping light coupled through the same waveguide end with emitted light or from an opposite waveguide end, or electrically-pumped measurement with electroluminescent light coupled through the waveguide.

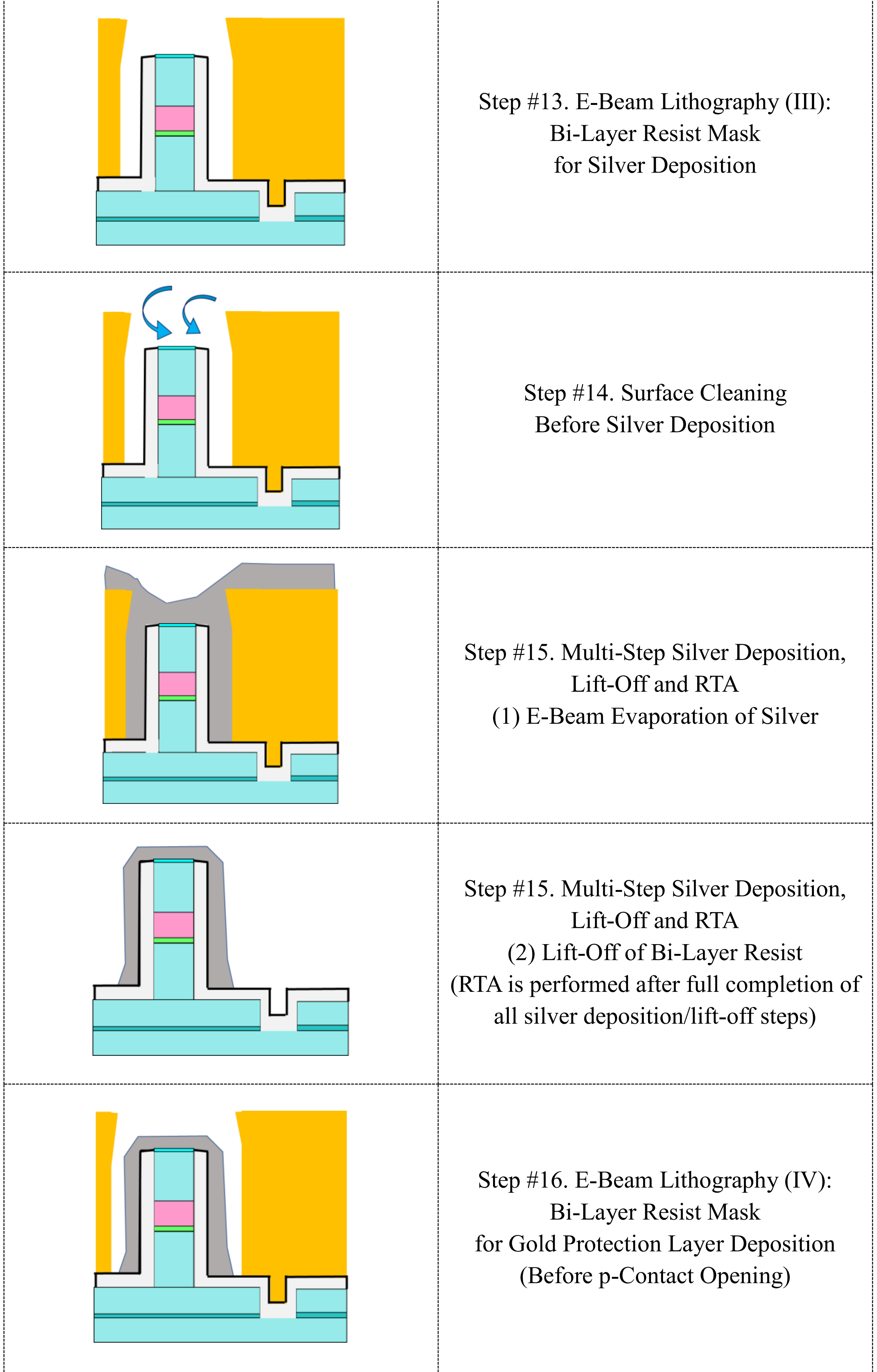
In the future, through advanced device design and further improving the fabrication techniques we developed, we hope for realizing steady room temperature metal-clad semiconductor laser with single-mode output of low threshold current and low energy consumption, which would make it possible for exciting future applications such as on-chip light sources for optical interconnects in integrated photonic circuits.

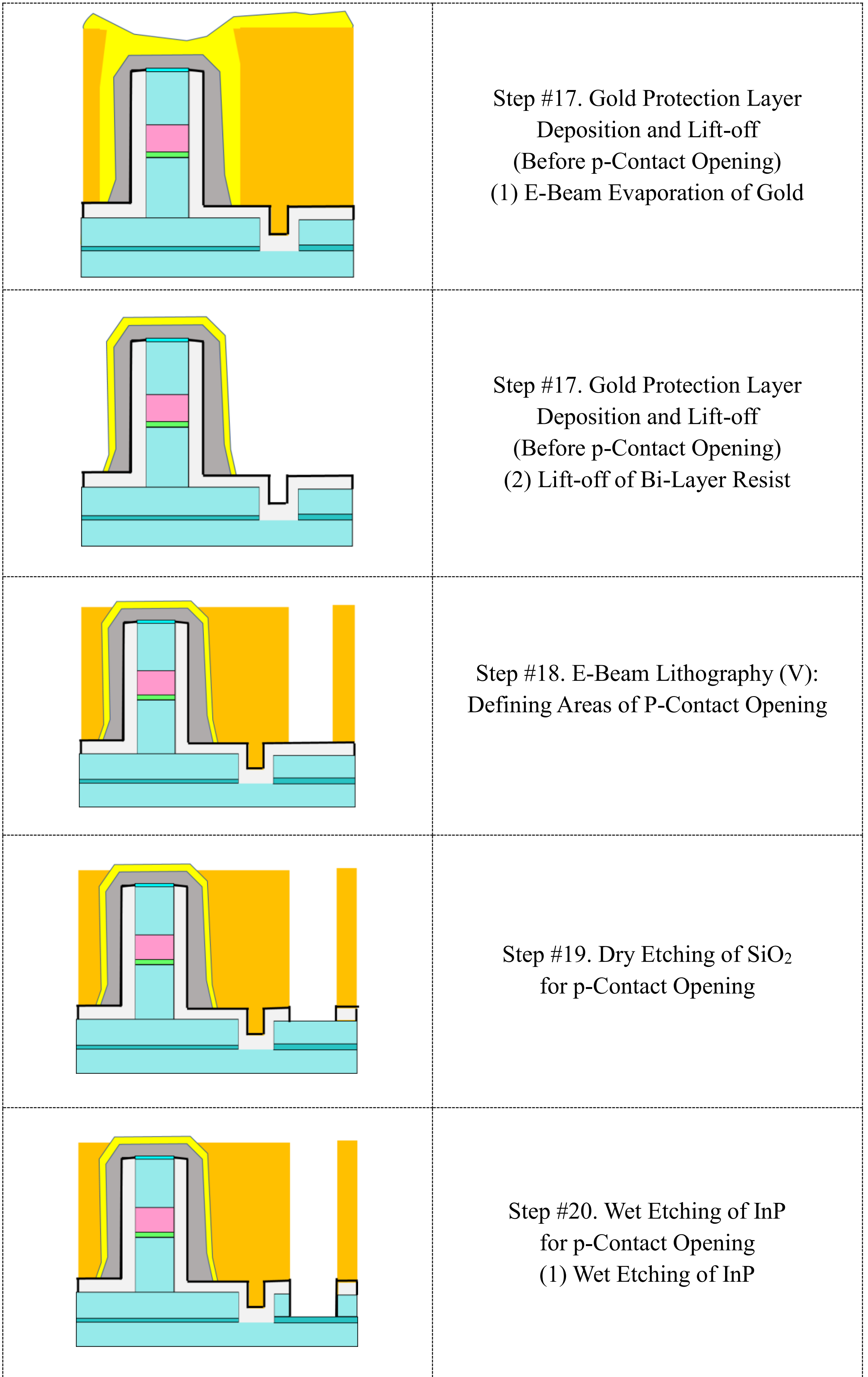
Appendix A. Fabrication Process Flow Chart

	Step #0. Wafer Preparation and Handling
	Step #1. PECVD of SiO_2 as Hard Mask
	Step #2. E-Beam Lithography (I) The Cavity
	Step #3. Cr Deposition and Lift-Off (1) E-Beam Evaporation of Cr
	Step #3. Cr Deposition and Lift-Off (2) Lift-Off

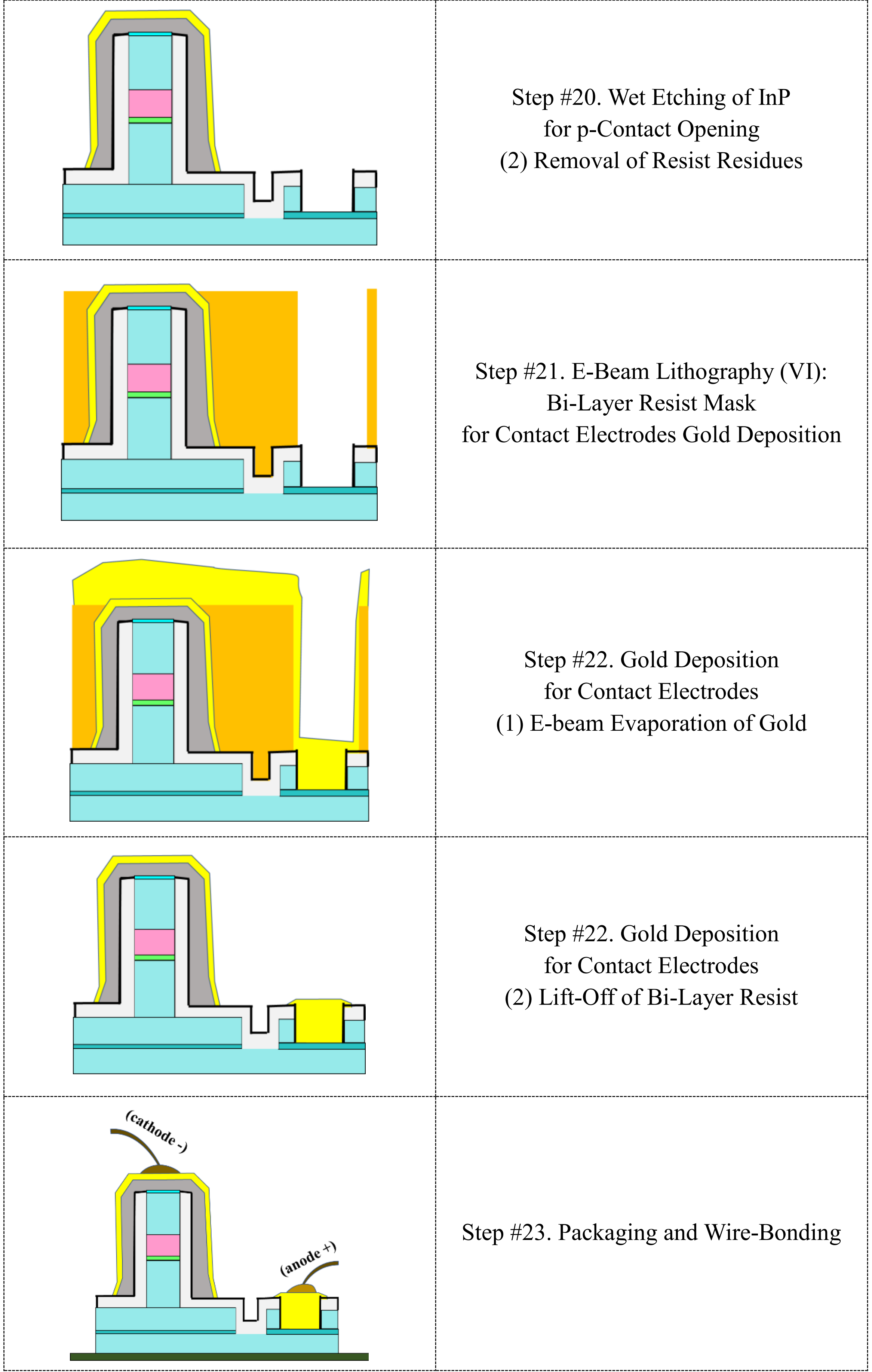

Step #4. Dry Etching of SiO2
Step #5. Dry Etching of III-V Cavity
Step #6. Buffered HF Cleaning
(Removal of Cr/SiO2 mask)
Step #7. E-Beam Lithography (II):
The Insulation Frame
Step #8.
Dry Etching of the Insulation Frame

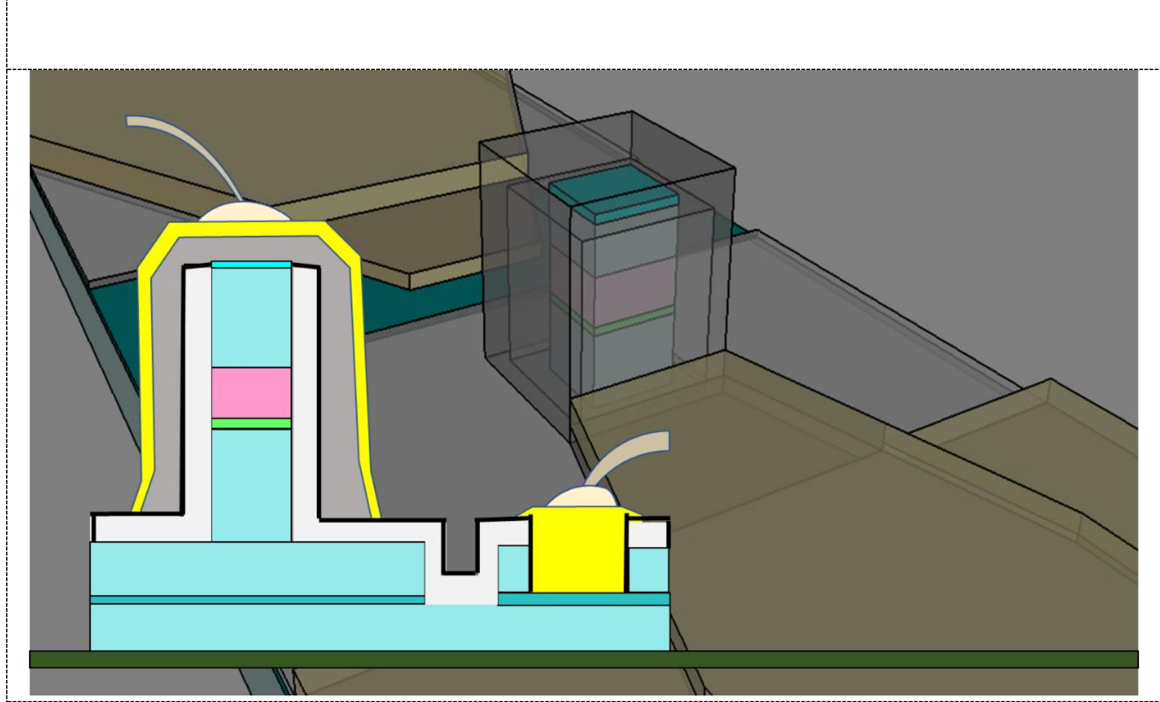

Step #9.
Wet Etching of the Insulation Frame
(1) Wet Etching of p-Contact Layer
Step #9.
Wet Etching of the Insulation Frame
(2) Removal of Resist Residues
Step #10.
Surface Cleansing and
Surface Passivation
(Immediately Before
Insulation Layer Deposition)
Step #11.
PECVD of SiO_2 Insulation Layer
Step #12. Contact Open for n-Contact


Step #13. E-Beam Lithography (III):
Bi-Layer Resist Mask
for Silver Deposition
Step #14. Surface Cleaning
Before Silver Deposition
Step #15. Multi-Step Silver Deposition,
Lift-Off and RTA
(1) E-Beam Evaporation of Silver
Step #15. Multi-Step Silver Deposition,
Lift-Off and RTA
(2) Lift-Off of Bi-Layer Resist
(RTA is performed after full completion of
all silver deposition/lift-off steps)
Step #16. E-Beam Lithography (IV):
Bi-Layer Resist Mask
for Gold Protection Layer Deposition
(Before p-Contact Opening)

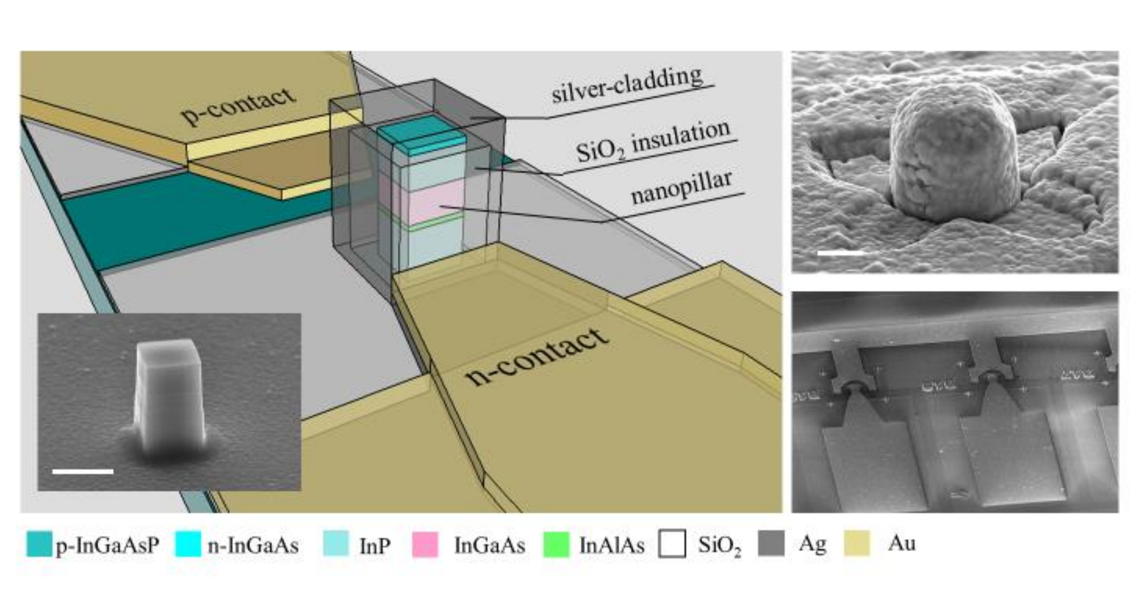


Step #17. Gold Protection Layer
Deposition and Lift-off
(Before p-Contact Opening)
(1) E-Beam Evaporation of Gold
Step #17. Gold Protection Layer
Deposition and Lift-off
(Before p-Contact Opening)
(2) Lift-off of Bi-Layer Resist
Step #18. E-Beam Lithography (V):
Defining Areas of P-Contact Opening
Step #19. Dry Etching of SiO2
for p-Contact Opening
Step #20. Wet Etching of InP
for p-Contact Opening
(1) Wet Etching of InP


Step #20. Wet Etching of InP
for p-Contact Opening
(2) Removal of Resist Residues
Step #21. E-Beam Lithography (VI):
Bi-Layer Resist Mask
for Contact Electrodes Gold Deposition
Step #22. Gold Deposition
for Contact Electrodes
(1) E-beam Evaporation of Gold
Step #22. Gold Deposition
for Contact Electrodes
(2) Lift-Off of Bi-Layer Resist
(cathode -)
(anode +)
Step #23. Packaging and Wire-Bonding



Overview of the Finished Device (forground)
Compared to the Schematic Design (at background)



Perspective Schematic of the Designed Silver-Clad InP/InGaAs Laser with Square Cross-Section for Electrically-Pumped Operation, Compared with SEMs of the Fabricated Cavity at Different Stages (Left Inset: III-V Core at Step #9, with Scale Bar showing 1 µm; Right Upper: Silver RTA at Step #15; Right Lower: After Electrode Deposition at Step #22).

Appendix B. List of Fabricated Devices

A1-A3	A4-A6	A7-A9	A10-A12	A13-A15	A16-A18	A19-A21
Capsule Shape, length ~ 3 µm	Capsule Shape, length ~ 3 µm	Square, side-length 0.35 µm	Square, side-length 0.71 µm	Square, side-length 0.89 µm	Square, side-length 1.42 µm	Square, side-length 1.77 µm
B1-B3	B4-B6	B7-A9	B10-B12	B13-B15	B16-B18	B19-B21
Rectangular, 2 µm x 1 µm	Rectangular, 3 µm x 0.7 µm	Rectangular, 4 µm x 0.5 µm	Rectangular, 5 µm x 0.4 µm	Rectangular, 6 µm x 0.34 µm	Capsule Shape, length ~ 1.1 µm	Capsule Shape, length ~ 1.6 µm
C1-C3	C4-C6	C7-C9	C10-C12	C13-C15	C16-C18	C19-C21
Capsule Shape, length ~ 3 µm	Circular, diameter 0.4 µm	Circular, diameter 0.8 µm	Circular, diameter 1 µm	Circular, diameter 1.2 µm	Circular, diameter 1.4 µm	Circular, diameter 1.5 µm
D1-D3	D4-D6	D7-D9	D10-D12	D13-D15	D16-D18	D19-D21
Circular, diameter 1.6 µm	Circular, diameter 1.7 µm	Circular, diameter 1.8 µm	Circular, diameter 2.0 µm	Circular, diameter 4.0 µm	Circular, diameter 8.0 µm	Trangular, for testing

Bibliography

[1] D. A. B. Miller, "Attojoule Optoelectronics for Low-Energy Information Processing and Communications–a Tutorial Review." *Journal of Lightwave Technology*, 2017.

[2] D. A. B. Miller, “Device requirements for optical interconnects to silicon chips,” *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, 2009.

[3] M. T. Hill, and M. C. Gather. "Advances in small lasers." *Nat. Photonics* 8.12, 908-918, 2014.

[4] C.-Y. A. Ni and S. L. Chuang, “Theory of high-speed nanolasers and nanoLEDs,” *Opt. Express*, vol. 20, no. 15, p. 16450, 2012.

[5] T. Suhr, N. Gregersen, K. Yvind, and J. Mørk, “Modulation response of nanoLEDs and nanolasers exploiting Purcell enhanced spontaneous emission.,” *Opt. Express*, vol. 18, no. 11, pp. 11230–11241, 2010.

[6] M. C. Wu, E. Yablonovitch, S. Fortuna, M. Eggleston, K. Messer, and K. Han, “Optical antenna-enhanced nano-LED for energy efficient optical interconnect”, In Energy Efficient Electronic Systems (E3S), 2015 Fourth Berkeley Symposium on (pp. 1-1). IEEE, October, 2015.

[7] M. S. Eggleston, and M. C. Wu. "Efficient coupling of an antenna-enhanced nanoLED into an integrated InP waveguide." *Nano letters* 15, no. 5: 3329-3333, 2015.

[8] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers, “III-V/silicon photonics for on-chip and intra-chip optical interconnects” *Laser & Photonics Reviews*, 4(6), pp.751-779, 2010.

[9] M. T. Hill, H. JS Dorren, T. De Vries, and X. JM Leijtens. "A fast low-power optical memory based on coupled micro-ring lasers." *Nature* 432, no. 7014: 206, 2004.

[10] H.G. Park, S.H. Kim, S.H. Kwon, Y.G. Ju, J.K. Yang, J.H. Baek, S.B. Kim, and Y.H. Lee, “Electrically driven single-cell photonic crystal laser” *Science*, 305(5689), pp.1444-1447, 2004.

[11] M. Lončar, T. Yoshie, A. Scherer, P. Gogna, and Y. Qiu, “Low-threshold photonic crystal laser”, *Applied Physics Letters*, 81(15), pp.2680-2682, 2002.

[12] Martin T. Hill, "Status and prospects for metallic and plasmonic nano-lasers [Invited]," *J. Opt. Soc. Am. B* 27, B36-B44, 2010.

[13] K. Ding and C. Z. Ning, “Metallic subwavelength-cavity semiconductor nanolasers,” *Light Sci. Appl.,* vol. 1, no. 7, p. e20, 2012.

[14] K. Ding, J. O. Diaz, D. Bimberg, and C. Z. Ning. "Modulation bandwidth and energy efficiency of metallic cavity semiconductor nanolasers with inclusion of noise effects." *Laser & Photonics Reviews* 9, no. 5: 488-497, 2015.

[15] M. T. Hill et al., “Lasing in metallic-coated nanocavities,” *Nat. Photonics*, vol. 1, no. 10, pp. 589–594, 2007.

[16] K. Yu, A. Lakhani, and M. C. Wu, “Subwavelength metal-optic semiconductor nanopatch lasers.,” *Opt. Express*, vol. 18, no. 9, pp. 8790–9, 2010.

[17] M.P. Nezhad, A. Simic, O. Bondarenko, B. Slutsky, A. Mizrahi, L. Feng, V. Lomakin, and Y. Fainman. "Room-temperature subwavelength metallo-dielectric lasers." *Nature Photonics* 4, no. 6: 395-399, 2010.

[18] J. H. Lee, M. Khajavikhan, A. Simic, Q. Gu, O. Bondarenko, B. Slutsky, M. P. Nezhad, and Y. Fainman, "Electrically pumped sub-wavelength metallo-dielectric pedestal pillar lasers," *Opt. Express* 19, 21524-21531, 2011.

[19] M. Khajavikhan et al., “Thresholdless nanoscale coaxial lasers,” *Nature*, vol. 482, no. 7384, pp. 204–207, 2012.

[20] K. Ding, L. Yin, M. T. Hill, Z. Liu, P. J. Van Veldhoven, and C. Z. Ning, “An electrical injection metallic cavity nanolaser with azimuthal polarization,” *Appl. Phys. Lett.,* vol. 102, no. 4, 2013.

[21] C. Guo, J. Xiao, Y. Yang, and Y. Huang, “Mode characteristics of subwavelength aluminum / silica-coated InAlGaAs / InP circular nanolasers,” *JOSA B* vol. 31, no. 4, pp. 865–872, 2014.

[22] J.H. Lee, M. Khajavikhan, A. Simic, Q. Gu, O. Bondarenko, B. Slutsky, M.P. Nezhad, and Y. Fainman, “Electrically pumped sub-wavelength metallo-dielectric pedestal pillar lasers”, *Optics express*, 19(22), pp.21524-21531, 2011.

[23] M. T. Hill, M. Marell, E. S. P. Leong, B. Smalbrugge, Y. Zhu, M. Sun, P. J. van Veldhoven, E. J. Geluk, F. Karouta, Y. -S. Oei, R. Nötzel, C. -Z. Ning, and M. K. Smit, "Lasing in metal-insulator-metal sub-wavelength plasmonic waveguides," *Opt. Express* 17, 11107-11112, 2009.

[24] K. Ding, M. T. Hill, Z. C. Liu, L. J. Yin, P. J. van Veldhoven, and C. Z. Ning, “Record performance of electrical injection sub-wavelength metallic-cavity semiconductor lasers at room temperature”, *Opt. Express,* vol. 21, no. 4, pp. 4728–33, 2013.

[25] C. Guo, J. Xiao, Y. Yang, Z. Zhu, Y. Huang, and S. Member, “Lasing Characteristics of Wavelength-Scale Aluminum / Silica Coated Square Cavity,” *IEEE Photonics*

Technology Letters, vol. 28, no. 2, pp. 217–220, 2016.

[26] B. Zhang, T. Okimoto, T. Tanemura, and Y. Nakano, “Proposal and numerical study on capsule-shaped nanometallic semiconductor lasers,” *Jpn. J. Appl. Phys.,* vol. 53, no. 11, 2014.

[27] B. Zhang, K. Chieda, T. Okimoto, T. Tanemura, and Y. Nakano, “Q factor improvement by capsule-shaped metallic cavity structure for subwavelength lasers,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 213, no. 4, pp. 965–969, 2016.

[28] V. Dolores-Calzadilla, B. Romeira, F. Pagliano, S. Birindelli, A. Higuera-Rodriguez, P. van Veldhoven, M. Smit, A. Fiore and D. Heiss, "Waveguide-coupled nanopillar metal-cavity light-emitting diodes on silicon", *Nature Communications,* vol. 8, p. 14323, 2017.

[29] Y. Xiao, R. Taylor, C. Yu, K. Feng, T. Tanemura, and Y. Nakano, "Room-Temperature Capsule-Shaped Wavelength-Scale Metal-Clad Laser With Enhanced Side Mode Suppression", manuscript accepted by *Applied Physics Letters*, 2017.

[30] C. Yu, *Electrically driven metallic micro cavity semiconductor lasers with thermal management*, Master’s thesis, University of Tokyo, 2017.

[31] V. M. Dolores-Calzadilla, *Metal nanocavity light sources integrated with passive waveguide components*, PhD thesis, Technische Universiteit Eindhoven, 2016.

[32] J. Shane, Q. Gu, F. Vallini, B. Wingad, J. S. T. Smalley, N. C. Frateschi, Y. Fainman, “Thermal considerations in electrically-pumped metallo-dielectric nanolasers” Proc. SPIE 8980, Physics and Simulation of Optoelectronic Devices XXII, 898027, 2014.

[33] C. Yu, B. Zhang, Y. Xiao, T. Tanemura, and Y. Nakano, "Comprehensive analysis on electrically pumped metallic cavity lasers," Compound Semiconductor Week (CSW'16), MoP-ISCS-029, Toyama, Japan, June 26-30, 2016.

[34] J. E. Bowers, "Evolution of photonic integrated circuits," 2017 75th Annual Device Research Conference (DRC), South Bend, IN, USA, 2017, pp. 1-2.

[35] D. Thomson, A. Zilkie, J.E. Bowers, T. Komljenovic, G.T. Reed, L. Vivien, D. Marris-Morini, E. Cassan, L. Virot, J.M. Fédéli, and J.M. Hartmann, “Roadmap on silicon photonics”, *Journal of Optics*, 18(7), p.073003, 2016.

[36] M. Y. Tang, S. S. Sui, Y. D. Yang, J. L. Xiao, and Y. Z. Huang, “Numerical investigation of metal-confined hybrid III–V/Si circular nanoresonator with guided emission” *Optics Communications,* 355, 306-312, 2015.

[37] M. K. Kim, A. M. Lakhani, and M. C. Wu, “Efficient waveguide-coupling of metal-clad nanolaser cavities,” *Opt. Express*, vol. 19, no. 23, pp. 23504–12, 2011.

[38] M.-K. Kim, Z. Li, K. Huang, R. Going, M.C. Wu, and H. Choo, "Engineering of metal-

clad optical nanocavity to optimize coupling with integrated waveguides," *Opt. Express* 21, 25796-25804, 2013.

[39] V. Dolores-Calzadilla, D. Heiss, A. Fiore, and M. Smit, "Metallo-dielectric nanolaser coupled to an InP- membrane waveguide," 17th Annu. Symp. IEEE Photonics Soc. Benelux Chapter, pp. 195–198, 2012.

[40] V. Dolores-Calzadilla, A. Fiore, and M. K. Smit. "Towards plasmonic lasers for optical interconnects." Transparent Optical Networks (ICTON), 2012 14th International Conference on. IEEE, 2012.

[41] C. Manolatou, M. J. Khan, S. Fan, P. R. Villeneuve, H. A. Haus and J. D. Joannopoulos, "Coupling of modes analysis of resonant channel add-drop filters," in *IEEE Journal of Quantum Electronics*, vol. 35, no. 9, pp. 1322-1331, Sep 1999.

[42] Y. Tanaka, J. Upham, T. Nagashima, T. Sugiya, T. Asano, and S. Noda, "Dynamic Control of the Q Factor in a Photonic Crystal Nanocavity," *Nature Materials,* 6.11, 862-865, 2007.

[43] K. Ding, and C. Z. Ning, "Fabrication challenges of electrical injection metallic cavity semiconductor nanolasers." *Semiconductor Science and Technology* 28.12: 124002, 2013.

[44] C. Yu, Y. Xiao, R. Taylor, B. Zhang, K. Feng, T. Tanemura, and Y. Nakano "Electrically Pumped Metallic Cavity Micro Laser with InAlAs Electron Blocking Layer", The 24th Congress of the International Comission for Optics, August. 2017, Tokyo, Japan.

[45] A. Higuera-Rodriguez, B. Romeira, S. Birindelli, L. E. Black, E. Smalbrugge, P. J. van Veldhoven, W. M. M. Kessels, M. K. Smit, and A. Fiore. "Ultralow Surface Recombination Velocity in Passivated InGaAs/InP Nanopillars." *Nano Letters* 17, no. 4: 2627-2633, 2017.

[46] K. Ding, *Fabrication and Characterization of Metallic Cavity Nanolasers*, PhD dissertation, Arizona State University, 2014.

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List of Research Products

Journal Publications:

1. **K. Feng**, M. Nishimoto, C. Yu, S. Saylan, R. Taylor, T. Tanemura and Y. Nakano, "Waveguide-coupled metal-clad cavity with integrated feedback stub", *Jpn. J. Appl. Phys.* 56 082201, 2017. Manuscript online at IOPScience: http://iopscience.iop.org/article/10.7567/JJAP.56.082201

2. Y. Xiao, R. Taylor, C. Yu, **K. Feng**, T. Tanemura, and Y. Nakano, "Room-Temperature Capsule-Shaped Wavelength-Scale Metal-Clad Laser with Enhanced Side Mode Suppression", manuscript accepted by *Applied Physics Letters*, 2017.

Conferences:

1. **K. Feng**, C. Yu, M. Nishimoto, R. Taylor, T. Tanemura and Y. Nakano, "Sub-Wavelength Metallic Laser Coupled to Silicon-on-Insulator Waveguide with Integrated Optical Feedback Stub for Q Factor Enhancement" Oral Presentation, the 25th International Semiconductor Laser Conference (ISLC 2016) Sept. 2016, Kobe, Japan. Abstract online: http://ieeexplore.ieee.org/document/7765764/

2. M. Nishimoto, **K. Feng**, T. Tanemura, and Y. Nakano, "Investigation for Q factor improvement of wavelength-scale metallic cavity coupled to waveguide", The 77th Japan Society of Applied Physics (JSAP) Autumn Meeting, Sept. 2016, Niigata, Japan.

3. C. Yu, Y. Xiao, R. Taylor, B. Zhang, **K. Feng**, T. Tanemura, and Y. Nakano "Electrically Pumped Metallic Cavity Micro Laser with InAlAs Electron Blocking Layer", The 24th Congress of the International Comission for Optics, August. 2017, Tokyo, Japan.