Master Thesis

Study on Temperature Dependence of Characteristics Variability in Scaled MOSFETs

（微細 MOS トランジスタにおける特性ばらつきの温度依存性に関する研究）

by

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Abstract

With deeper electronics penetration in everyday life such as IoT devices, wide-range temperature or high temperature applications are increasingly needed, therefore understanding temperature effect on device performance is of great importance. On the other hand, with the continuous downscaling of MOSFETs towards their ultimate physical limits, its random variability is becoming insurmountable challenge, and it is also influenced by temperature. It is well known that high temperature significantly degrades MOSFET performance, but very little work has been reported so far about temperature effect on variability in MOSFETs. Therefore, the objective of this study is to investigate the impact of temperature on electrical characteristics variability in scaled MOSFETs.

Temperature dependence of characteristics variability in bulk and fully-depleted (FD) silicon-on-thin-box (SOTB) MOSFETs fabricated by 65nm technology are measured and compared. Experimental results show that variability of key device figures of merits (V_{th}, I_{on}, SS, DIBL) all reduce at high temperature in both bulk and SOTB MOSFETs.

One new finding is that SS variability is reduced at high temperature due to the negative correlation between SS and its temperature coefficient dSS/dT. Physical mechanism of this effect is explained by non-uniform electrostatics potential and current path among channel width direction based on a simple parallel model, and it is also well reproduced by 3D TCAD simulations.

Another new finding is that DIBL variability is also reduced at high temperature due to the negative correlation between DIBL and its temperature coefficient dDIBL/dT. Physical origin of this phenomenon is investigated based on the electrostatics potential variations along channel length direction (source-drain positional asymmetry). This effect is explained by extreme cases simulations combined with 3D TCAD simulation.

In conclusion, this work presents a basic physical understanding about temperature dependence of characteristics variability in scaled MOSFETs. If these effects can be exactly modeled, it will help to provide more accurate margin estimation in circuit design. We hope this work could provide helpful information for the characteristics variability prediction in a wide temperature range.

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1. Introduction

1.1 Background

During past decades, complementary metal-oxide-semiconductor (CMOS) technology scaling has been conducted to increase integration density, improve performance and reduce power consumption. With the continued downscaling of metal-oxide-semiconductor field-effect-transistor (MOSFET) devices towards their ultimate physical limits and the rapid introduction of sub-nanometer technology nodes, its random characteristics variability is becoming insurmountable challenge, and has been comprehensively studied [1-9]. It is generally known that random variations are unpredictable and are caused by random uncertainties in the fabrication process such as random dopant fluctuations (RDF), line edge roughness (LER), poly-silicon/metal gate granularity (P/MGG) and interface traps. Characteristics variability can result in failure of circuits, degradation of circuit margins and other problems, though individual device works normally. Therefore, it is important to investigate the statistical variability for its reduction and the further continuous scaling of MOSFETs.

On the other hand, it is well known temperature has significant influence on MOSFET performance, and high temperature alters or degrades device performance by reducing threshold voltage (V_{th}) and on-state drain current (I_{on}), as well as increasing subthreshold slope (SS) and off-state current (I_{off}) [10-12]. Studying the temperature effect on MOSFETs is important from three points of view: First, it is important for most commonly used room-temperature applications, as these devices can be affected by self-heating effect to at high temperature even under normal operation [13,14]. Second, with deeper electronics penetration in everyday life such as automotive, aircraft, health/medical devices [15,16], high-temperature applications are needed increasingly, therefore understanding temperature effect on device performance is of great significance. Third, in the IoT era, more and more devices will be required to operate normally in a wide temperature range. These kinds of requirements are

calling for electronic devices that can operate reliably in harsh environments, including extreme high or low temperatures.

1.2 Objective of This Thesis

The purpose of this thesis is to investigate the impact of temperature on the statistical variability in scaled MOSFETs. Temperature dependence of variability in bulk MOSFETs and fully-depleted silicon-on-thin-box (SOTB) MOSFETs fabricated by 65nm technology are measured and compared. Experimental results show that variability of key device figures of merits (threshold voltage (V_{th}), on-state current (I_{on}), subthreshold slope (SS), drain-induced-barrier-lowing (DIBL)) all reduce at high temperature. Reduced SS variability and reduced DIBL variability at high temperature are two new findings in this thesis. We investigate and explain the physical mechanism of the new findings by extreme cases study, combined 3D TCAD simulations.

1.3 Chapter Organization

Chapter 2 performs a systematic study about the impact of temperature on statistical variability in bulk and SOTB MOSFETs fabricated by 65nm technology, based on experimental measurements. We compare the variability behavior at room temperature and high temperature of four key device figures of merits: V_{th}, I_{on}, SS, and DIBL.

Chapter 3 focuses on a new finding that SS variability is reduced at high temperature. This phenomenon is explained by the non-uniform potential distribution in the channel width direction based on a simple parallel model, and it is also verified by 3D TCAD simulation.

Chapter 4 focuses on another new finding that DIBL variability is also reduced at high temperature. Physical mechanism of this new finding is explained based on source-drain potential asymmetry, combined with extreme cases simulations and 3D TCAD simulations.

Chapter 5 summaries the results and conclusions obtained in this thesis.

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2. Temperature Effect on MOSFET and its Variability

2.1 Introduction

This chapter performs a systematic study about the impact of temperature on statistical variability in bulk and SOTB MOSFETs fabricated by 65nm technology [1], based on experimental measurements. Fully depleted (FD) SOTB MOSFETs are well known for its smaller variability than conventional bulk MOSFETs due to absence of RDF thanks to the intrinsic channels. Therefore, comparing the variability in bulk and SOTB FETs could provide information about the influence of RDF.

Throughout this chapter, we compare the statistical distributions of four key device figures of merit: threshold voltage (V_{th}), on-state current (I_{on}), subthreshold slope (SS), drain-induced-barrier-lowing (DIBL), at room temperature and high temperature. First, measurement setup and parameter definition are described in section 2.2. Then, before focusing on temperature effect on MOSFETs variability, we examine and explain the measured temperature effect on a single MOSFET in section 2.3. Next, in section 2.4, we compare the measured statistical distributions at room and high temperatures. Here, two new findings are presented for the first time. First, SS variability is reduced at high temperature, which is contrary to previous simulation results in Ref [2]; Second, DIBL variability is also reduced at high temperature, which has not been reported yet. Detailed analyses about physical mechanism of the two new findings will be presented in chapter 3 and chapter 4.

In this chapter, we focus on the measurement results of n-type MOSFETs. Meanwhile, p-type MOSFETs are also measured and analyzed, and measured temperature effects on pMOSFETs behave the same trend as that in nMOSFETs. A table presents the summary of the measured temperature effects in both nMOSFETs and pMOSFETs is given in section 2.5.

2.2 Measurement Setup

1k (1024) bulk nMOSFETs and silicon-on-thin-box (SOTB) nMOSFETs fabricated with 65nm technology are measured using Device Matrix Array Test Element Group (DMA-TEG) [3]. The channel length L is 60nm while the channel width W is 120nm. Drain bias V_d is set to V_{d_lin}=50mV in the linear region and V_{d_sat} =1.2V in the saturation region. In order to investigate the temperature dependence of statistical variability, the temperature of the wafer is set to 298K (25°C, room temperature) and 393K (100°C, high temperature).

The linear I_{ds} -V_{gs} characteristics of 1k (1024) bulk and SOTB MOSFETs measured at room temperature and high temperature are shown in Figs.2.1 and 2.2. Note that we can't directly measure off-current in bulk FETs since the leakage current through unselected MOSFETs in the DMA-TEG raises up the current floor level. Therefore, we extracted the parameters using constant current method and the reference current is defined at a relatively higher level (I_0=10^{-7}×W/L) to suppress the influence of leakage current.

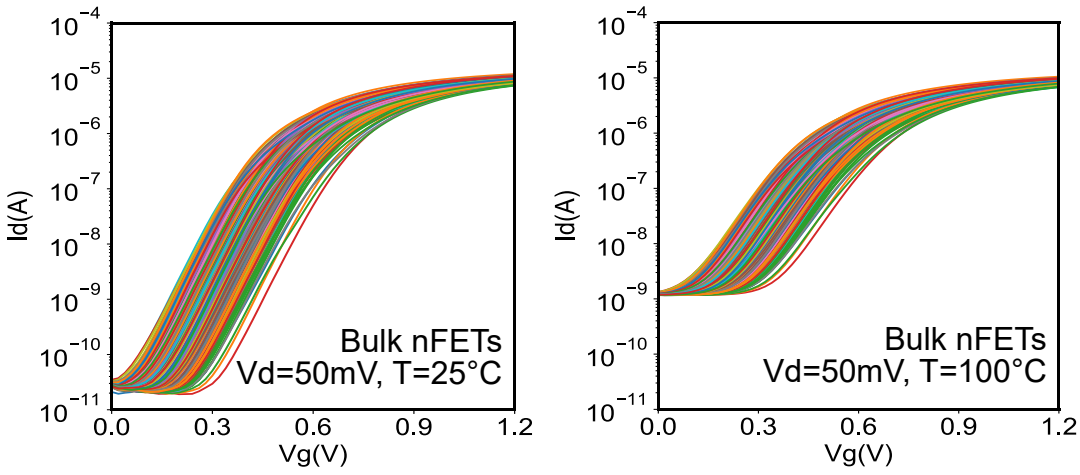

Fig.2.1 Measured I_d -V_g characteristics of 1k bulk nMOSFETs at room and high temperatures. Note that leakage current through unselected MOSFETs in the DMA-TEG raises the current floor level, especially at high temperature.

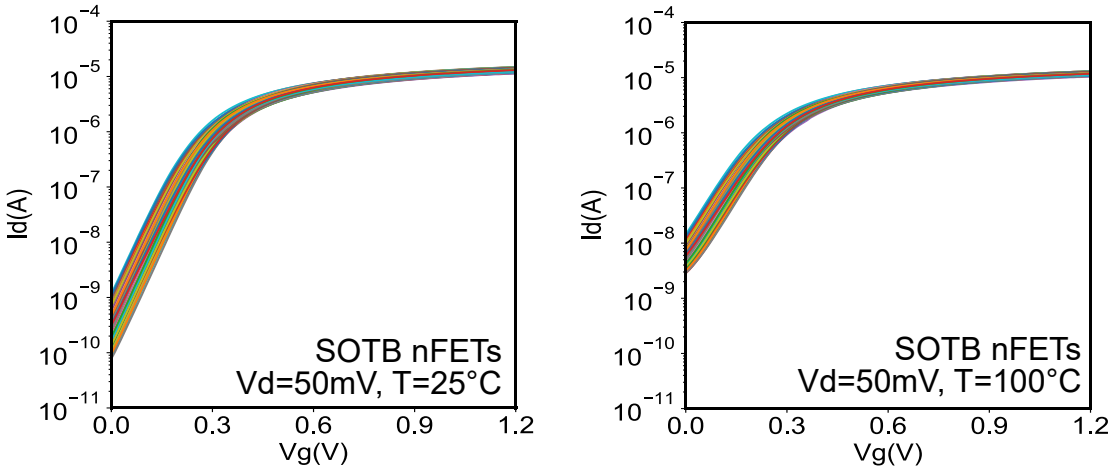

Fig.2.2 Measured I_d -V_g characteristics of 1k SOTB nMOSFETs at room and high temperatures.

Throughout this thesis, device figures of merit are extracted as shown in Fig 2.3. V_{th} is extracted using constant current method (reference current is defined at $I_d=10^{-7}\times W/L$). I_{on} is defined as I_{ds} at $V_g=1.2V$. SS is defined the reciprocal of the slope at the current $I_d= W/L\times10^{-7}A$. DIBL is defined as the V_{th} difference between low drain bias ($V_d=0.05V$, linear regime) and high drain bias ($V_d=1.2V$, saturation regime) normalized by drain bias difference, i.e. $DIBL=\Delta V_{th}/\Delta V_d$, where $\Delta V_{th}=V_{th\_lin}-V_{th\_sat}$, and $\Delta V_d=V_{d\_sat}-V_{d\_lin}$.

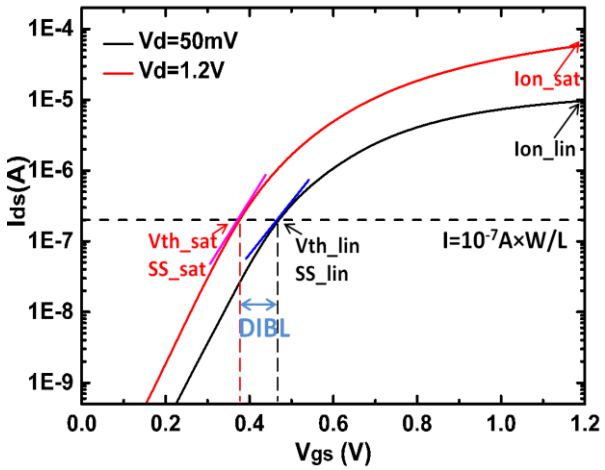

Fig.2.3 Definition of device figures of merit. (V_{th}, I_{on}, SS, DIBL)

2.3 Temperature Effect on MOSFET

Before discussing temperature effect on variability behavior in MOSFETs, we first examine the temperature effect on a single MOSFET. Here, bulk MOSFETs are measured at four different temperatures with intervals of increase set at 25°C, to examine whether temperature effect on key device figures of merit is consistent in a wide range.

Fig.2.4 shows the transfer characteristics of a typical bulk nMOSFET measured at four different temperatures (25°C, 50°C, 75°C and 100°C). Since off-current is not available in our measurement due to the leakage current in the DMA-TEG, here we only focus and discuss the parameters irrelevant to leakage current.

Then, key device figures of merit are calculated as mentioned in section 2.2. Fig.2.5 shows the measured temperature dependence of V_{th} and I_{on}, V_{th} and I_{on} degrade (decrease) at high temperature. Fig.2.6 shows the measured temperature dependence of SS and DIBL, SS and DIBL also degrade (increase) at high temperature.

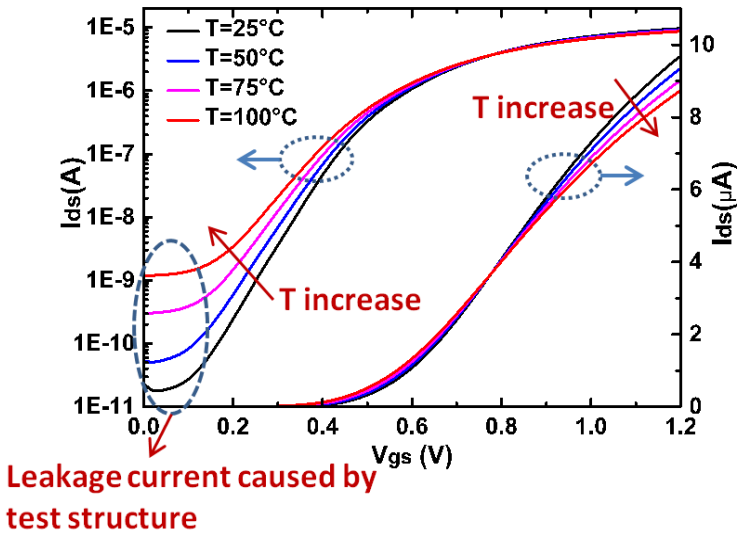

Fig.2.4 Measured I_d -V_g characteristics of a typical bulk nMOSFET at four different temperatures (25°C, 50°C, 75°C and 100°C), V_d is set at 50mV.

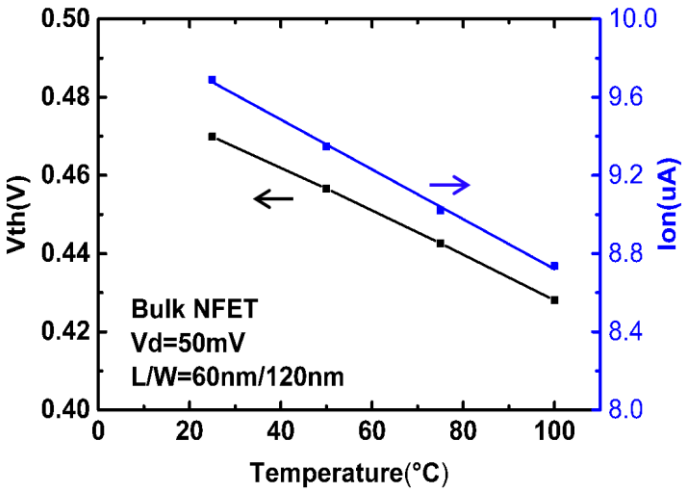

Fig.2.5 Measured temperature dependence of V_{th} and I_{on} in a bulk nMOSFET.

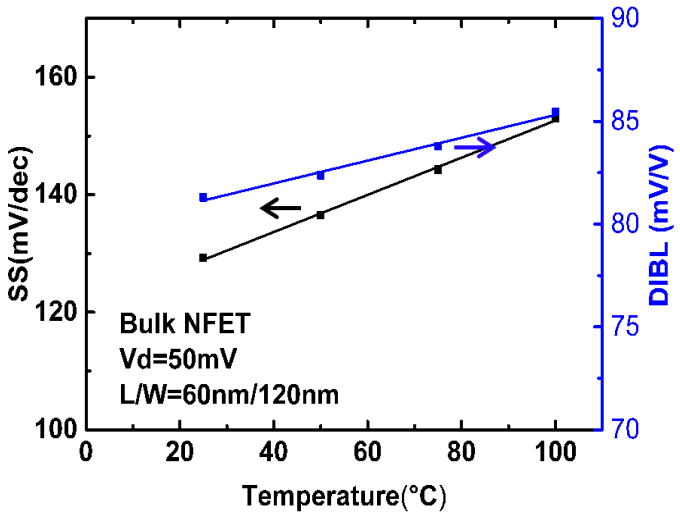

Fig.2.6 Measured temperature dependence of SS and DIBL in a bulk nMOSFET.

V_{th} decreasing at high temperature has been well studied [4-6] and can be explained from the analytical equation (1). The temperature dependence of V_{th} is related to the temperature dependence of E_g and φ_B as derived in equation (2), where T, E_g, φ_B, ε_{si}, N_a, N_c, N_v, q, C_{ox} are the temperature in kelvin, the energy gap of silicon, the Fermi potential of the neutral region, the silicon permittivity, the acceptor concentration, the effective density of states of conduction band, the effective density of states of valence band, the elementary charge, and the gate oxide capacitance, respectively. The factor m is the body-effect coefficient typically lies between 1.1 and 1.4 [6]. $d\varphi_B/dT$ stems from the temperature dependence of the intrinsic carrier

concentration, which can be evaluated in equation (3). Substituting equation (3) into equation (2) yields to equation (4), which can explain the temperature dependence of V_{th}.

$$V_{th} = -\frac{E_g}{2q} + \varphi_B + \frac{\sqrt{4\varepsilon_{Si} q N_a \varphi_B}}{C_{ox}} \quad (1)$$

$$\frac{dV_{th}}{dT} = -\frac{1}{2q}\frac{dE_g}{dT} + \left(1 + \frac{\sqrt{\frac{\varepsilon_{Si} q N_a}{\varphi_B}}}{C_{ox}}\right)\frac{d\varphi_B}{dT} \quad (2)$$

$$\frac{d\varphi_B}{dT} = \frac{d}{dT}\left(\frac{kT}{q}\ln\left(\frac{N_a}{\sqrt{N_c N_v}e^{-\frac{E_g}{2kT}}}\right)\right)$$

$$= -\frac{k}{q}\ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right) - \frac{kT}{q\sqrt{N_c N_v}}\frac{d\sqrt{N_c N_v}}{dT} + \frac{1}{2q}\frac{dE_g}{dT} \quad (3)$$

$$\frac{dV_{th}}{dT} = -(2m-1)\frac{k}{q}\left[\ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right) + \frac{3}{2}\right] + \frac{m-1}{q}\frac{dE_g}{dT} \quad (4)$$

The temperature dependence of I_{on} can be explained by carrier mobility which is very sensitive to temperature. Since the mobility tends to be limited by lattice scattering and is proportional to $T^{-3/2}$ [6], it is the dominant reason for the decrease of I_{on} at high temperature, and the current increased by the V_{th} decrease cannot surmounts the current decreased by the mobility degradation [7].

SS is a crucial parameter in MOSFETs that determines the I_{on}/I_{off} ratio, and it is well known to be a function of temperature. As shown in Fig.2.6, SS increases gradually with temperature raises up. The temperature dependence of SS can be easily explained by its definition as equation (5), where SS is proportional to temperature T if C_{dm} (capacitance of depletion layer) is considered to be constant.

$$\mathrm{SS} = \frac{\partial V_g}{\partial log_{10} I_d} = \frac{2.3kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \quad (5)$$

As for DIBL, it is a crucial indicator of short channel effects in MOSFETs referring originally to a reduction of V_{th} of the transistor at higher drain voltages (V_d). According to the measured data, it increases gradually from 81mV/V at room temperature to 85mV/V at high

temperature. In previous research papers, its temperature dependence related physical mechanism are still controversial [8,9]. Detailed analyses and discussion about temperature effect on DIBL and its variability will be carried out in chapter 4.

According to Figs.2.5 and 2.6, all the plots of device figures of merit versus temperature are almost rectilinear, which indicate that the temperature dependence of device figures of merit is proportional. Therefore, in the following sections, we study and discuss the temperature dependence of statistical variability in two typical temperature, room temperature (25°C) and high temperature (100°C).

2.4 Temperature Effect on Variability in MOSFETs

Fig.2.7 is the statistical distributions of V_{th} under different temperature and bias conditions. Since the plots are rectilinear, V_{th} variability exhibits a normal distribution at both room temperature and high temperature. The mean value of V_{th} (μV_{th}) decreases at high temperature, and the standard deviation of V_{th} (σV_{th}) also decreases at high temperature. This phenomenon has been studied and reported in Ref [10]. According to Pelgrom Plot [11], V_{th} variation caused by random dopant fluctuation (RDF) can be expressed as equation (6), where T_{inv} is the electrical thickness of the gate oxide at the inversion region, and W_{dep} is the width of depletion layer. The expression of W_{dep} is shown in equation (7). Thus the reduction in W_{dep} at high temperature is considered to be the main reason why σV_{th} decrease at high temperature [10].

$$\sigma V_{th} = \frac{qT_{inv}}{\varepsilon_{ox}} \sqrt{\frac{N_a W_{dep}}{3LW}} \quad (6)$$

$$W_{dep} = \sqrt{4\varepsilon_{Si}\varphi_B / qN_a} \quad (7)$$

Very similar to V_{th} variability, I_{on} variability (Fig.2.8) also exhibits a normal distribution. Its standard deviation σI_{on}decreases at high temperature. This phenomenon has been studied and reported in Ref [12,13]. The decrease of σI_{on} can be explained partly by the mobility trend with temperature and partly by the increased gate overdrive. According to the standard MOSFET low-field mobility theory, at higher temperature, the scattering component

associated with the silicon lattice becomes more important, therefore reducing the effect of the scattering component related to the dopant [13]. On the other hand, both V_{th} and σV_{th} decrease at high temperature, σI_{on} decreases since I_{on} is less effected by the fluctuation of gate overdrive voltage (V_{gs} -V_{th}).

Fig.2.9 describes the statistical distribution of SS. It is shown that SS variability deviates from normal distribution. The mean value μSS increases at high temperature. Surprisingly, σSS decreases at high temperature. It is a new finding in this thesis that SS variability is reduced at high temperature, which is opposite from simulation results reported in Ref [2,15,16]. Detailed analyses and explanation about the physical origin of this new finding will be performed in chapter 3.

DIBL variability behaves very similar to SS variability. As shown in Fig.2.10, DIBL variability deviates from normal distribution. The mean value μDIBL increases at high temperature. However, σDIBL decreases at high temperature. This is also a new finding of this thesis that DIBL variability is reduced at high temperature, which has not been studied before. Detailed analyses and explanation of this new finding will be performed in chapter 4.

2.5 Summary

In this chapter, we perform a systematic study about temperature dependence of characteristics variability in bulk and SOTB MOSFETs. Experimental results show that variability of V_{th}, I_{on}, SS and DIBL are all reduced at high temperature. Reduced V_{th} and I_{on} variability have been well studied in previous works. However, Reduced SS and DIBL variability have not been reported yet.

In section 2.4, we focus on the measurement results of n-type MOSFETs. In fact, p-type MOSFETs are also measured and analyzed, and measured temperature effects in pMOSFETs behave almost the same trend as in nMOSFETs. Table 2.1 is a summary of the measured temperature effects in both bulk and SOTB n/pMOSFETs in linear and saturation regimes. The new findings that SS and DIBL variability are reduced at high temperature preserve in both n-type and p-type MOSFETs.

By comparing the variability in bulk and SOTB MOSFETs, it is obvious that variability in SOTB is much smaller because the RDF influence thanks to the intrinsic channel. However,

SOTB also show the same trend of reduced variability at high temperature, which indicates that RDF is not the dominant reason for the reduced SS and DIBL variability at high temperature.

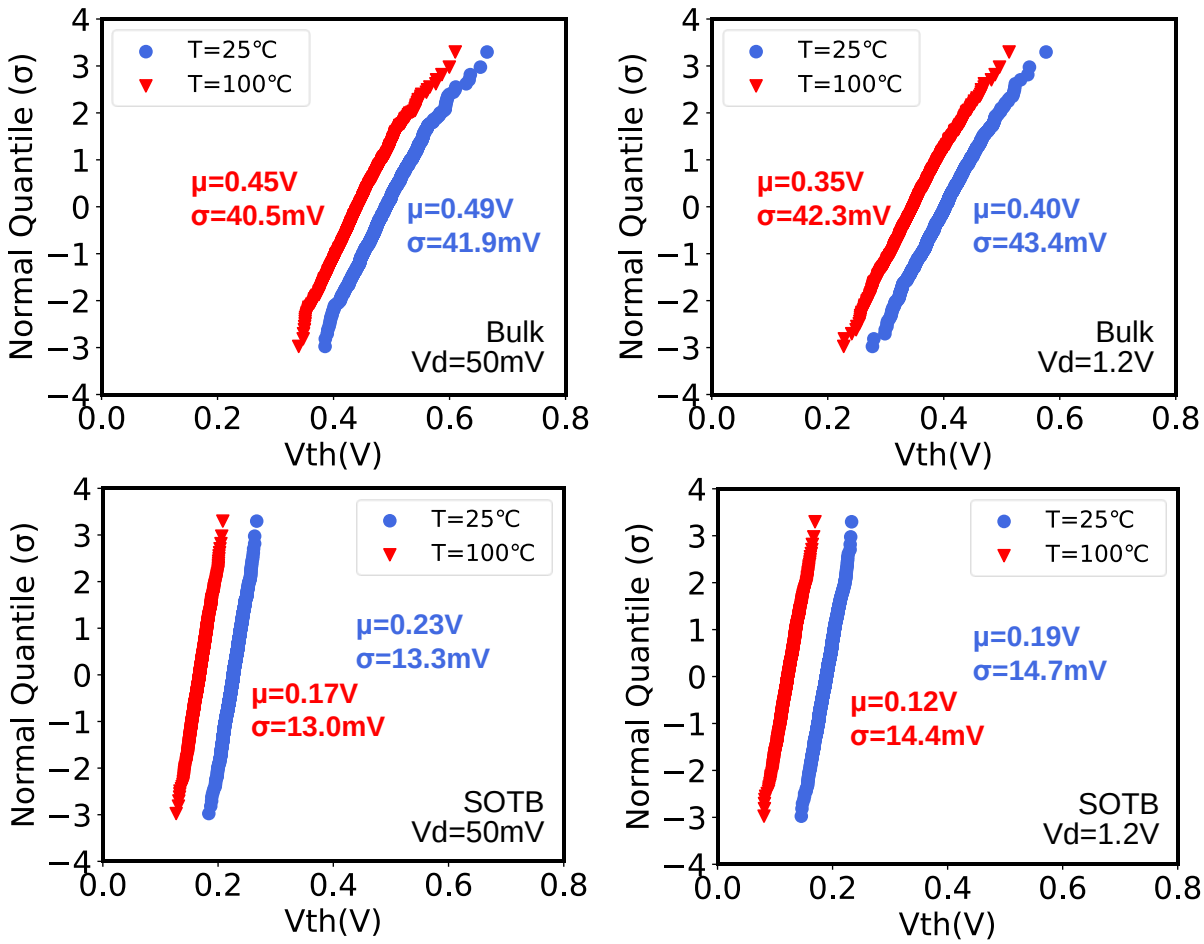

Fig.2.7 Statistical distributions of V_{th} at room and high temperatures, in 1k bulk (upper) and SOTB (lower) nMOSFETs. Mean value of V_{th} (μV_{th}) decreases at high temperature, and standard deviation of V_{th} (σV_{th}) also decreases at high temperature.

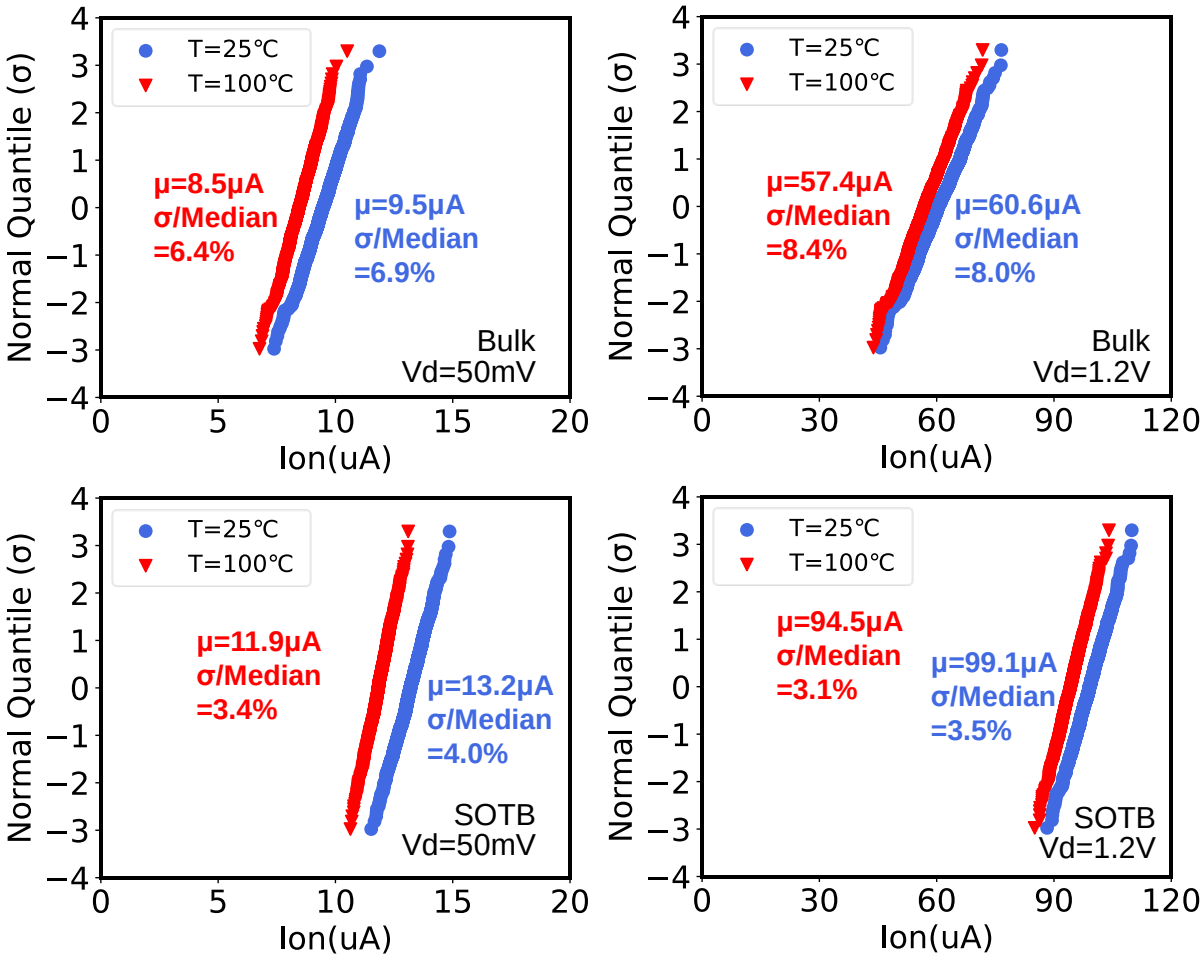

Fig.2.8 Statistical distributions of I_{on} at room and high temperatures, in 1k bulk (upper) and SOTB (lower) nMOSFETs. Mean value of I_{on} (μI_{on}) decreases at high temperature, and standard deviation of I_{on} (σI_{on}) also decreases at high temperature.

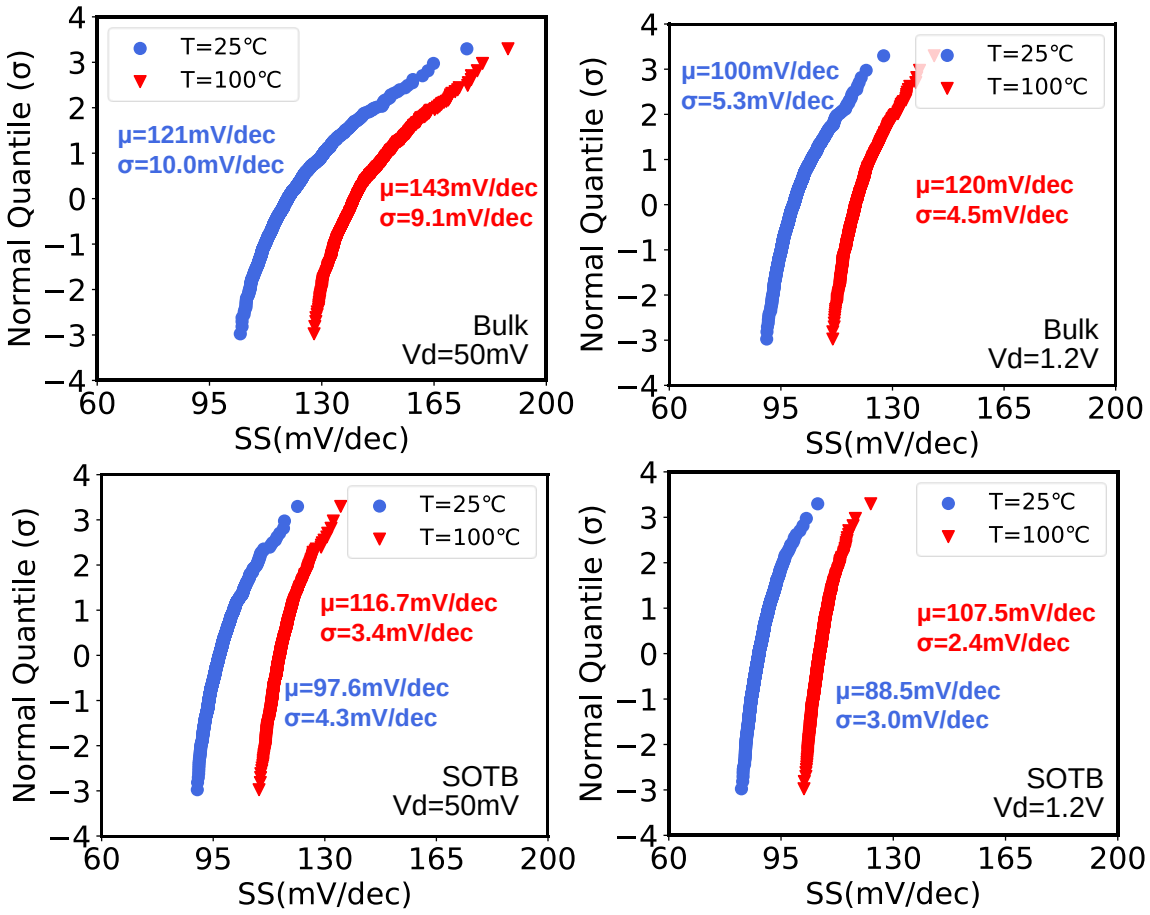

Fig.2.9 Statistical distributions of SS at room and high temperatures, in 1k bulk (upper) and SOTB (lower) nMOSFETs. Mean value μSS increases at high temperature, but σSS decreases at high temperature.

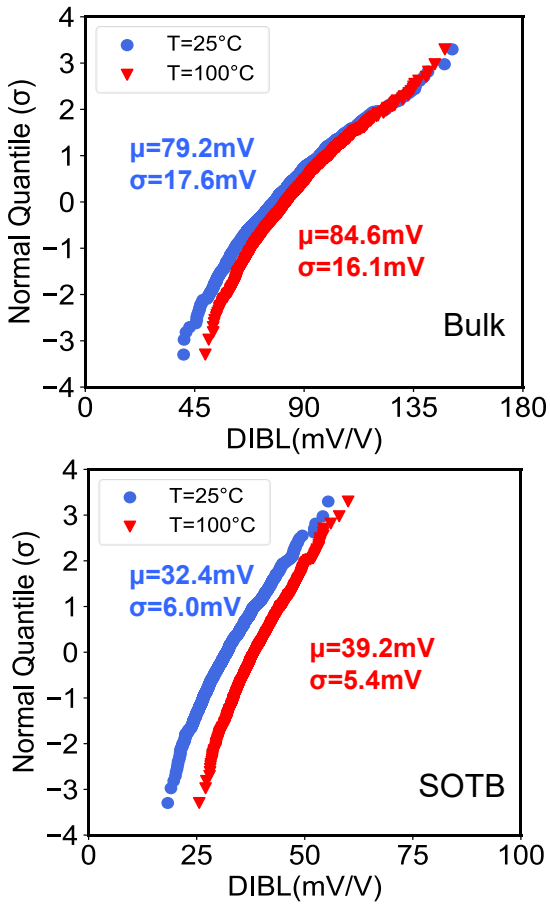

Fig.2.10 Statistical distributions of DIBL at room and high temperatures, in 1k bulk (upper) and SOTB (lower) nMOSFETs. Mean value μDIBL increases at high temperature, but σDIBL decreases at high temperature.

NMOS	Bulk (T25°C)	Bulk (T100°C)	SOTB (T25°C)	SOTB (T100°C)
σVth_lin (mV)	41.97	40.45	13.26	13.02
σVth_sat (mV)	43.37	42.34	14.72	14.42
σIon_lin (%)	6.91	6.37	4.00	3.44
σIon_sat (%)	8.42	8.00	3.45	3.14
σSSlin (mV/dec)	10.01	9.10	4.31	3.43
σSSsat (mV/dec)	5.25	4.50	2.95	2.44
σDIBL (mV/V)	17.33	15.82	6.01	5.42
PMOS	**Bulk (T25°C)**	**Bulk (T100°C)**	**SOTB (T25°C)**	**SOTB (T100°C)**
σVth_lin (mV)	27.46	25.60	12.47	12.35
σVth_sat (mV)	29.98	28.37	13.84	13.83
σIon_lin (%)	3.88	3.63	2.55	2.40
σIon_sat (%)	5.39	5.21	2.63	2.60
σSSlin (mV/dec)	11.25	9.76	4.03	3.51
σSSsat (mV/dec)	6.19	5.08	2.75	2.38
σDIBL (mV/V)	13.00	11.43	5.49	5.11

Table 2.1. Summary of the measured standard deviations of V_{th}, I_{on}, SS and DIBL in both bulk and SOTB n/pMOSFETs at room and high temperatures.

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3. Physical Mechanism of Temperature Effect on SS Variability

3.1 Introduction

Subthreshold slope (SS) is an important parameter that determines I_{on}/I_{off} ration in MOSFETs, and the understanding of SS variability is critical for low power and energy-efficient VLSIs. As mentioned in chapter 2, one of the new findings in this thesis is that SS variability reduces at high temperature, which is contrary to natural expectation and TCAD simulation results in Ref [1]. We investigate the physical origin of this effect by proposing an effective current path model.

In this chapter, first, temperature coefficient of SS (dSS/dT) are analyzed and discussed, and it is found that the negative correlation between SS and dSS/dT results in the reduced SS variability at high temperature. Next, we propose a simple parallel model, based on the assumption that effective current path in channel area is not uniform due to several origins of randomness, to explain the negative correlation between SS and dSS/dT. Then we generalize this model into random cases, and also perform 3D TCAD simulation to verify this assumption. As a result, the negative correlation between SS and dSS/dT is well reproduced in both parallel model-based calculation and 3D TCAD simulation. Therefore, physical mechanism of reduced SS variability at high temperature is well explained and understood. It is also confirmed that this phenomenon exists in deep subthreshold region.

3.2 Temperature Coefficient of SS

In section 2.4, we show the experimental results that SS (both linear and saturation region)

variability is reduced at high temperature, in bulk and SOTB nMOSFETs. To understand this phenomenon, we calculated the temperature coefficient of SS (dSS/dT=(SS(100°C)-SS(25°C))/(T(100°C)-T(25°C)), to describe how SS is degraded by high temperature.

Fig 3.1 shows the scatter plots between original SS (@T25°C) and its temperature coefficient dSS/dT. Negative correlations between SS and dSS/dT (ρ=-0.50 in bulk and -0.62 in SOTB) indicate an interesting phenomenon that a transistor whose SS is smaller tends to degrade more at high temperature. Due to this negative correlation, SS variability reduces at high temperature. From Fig 3.1, SOTB show much smaller σSS than bulk FETs because of reduced RDF influence, however, dSS/dT variability of SOTB FETs is comparable to that of bulk FETs, which indicates that RDF is not the dominant reason for the variability of dSS/dT. Similar results are also found at a higher drain voltage (V_d=1.2V, not shown here).

We also examine whether this effect is caused by short channel effect. Here, 1k relatively long channel bulk and SOTB nMOSFETs (channel length L=500nm, channel width W=120nm) are also measured. Fig.3.2 shows the negative correlations between SS and dSS/dT. Although variability is much smaller in long channel transistors, the negative correlations still exist which indicate that this effect is not caused by short channel effect.

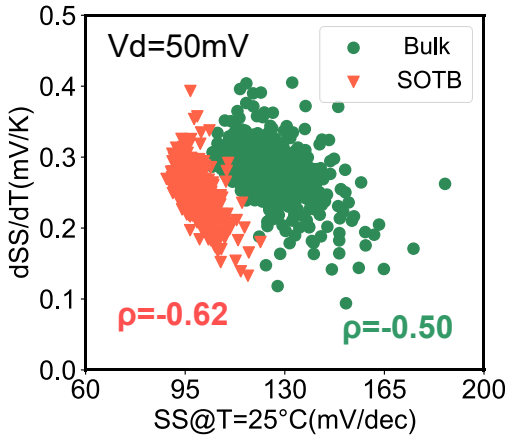

Fig 3.1 Correlations between SS (25°C) and dSS/dT in bulk and SOTB nMOSFETs (L=60nm, V_d=50mV)

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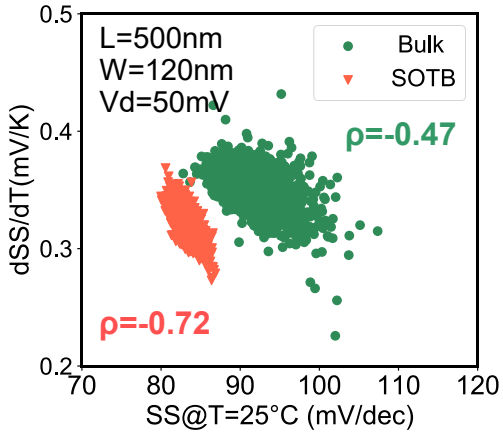

Fig 3.2 Correlations between SS (25°C) and dSS/dT in long channel bulk and SOTB nMOSFETs. (L=500nm, V_d=50mV)

3.3 Effective Current Path Model

It is well known that random variations are unpredictable and are caused by random uncertainties in the fabrication process such as RDF, line edge roughness (LER), and gate workfunction (WF) variability [2,3]. Therefore, current path in a MOSFET channel area is, in general, not uniform. Based on this, an effective current path model is proposed to explain the negative correlation between SS and dSS/dT.

Fig 3.3 is the schematic of the simple model. For simplicity, it was assumed that non-uniform current path is equivalent to channel area composed by different local V_{th}. Device A and B are simulated by 2D TCAD as two reference bulk nFETs with different, but uniform gate WF values, where V_{th}(A) is 0.1V lower than V_{th}(B). Therefore, the I_d-V_g curves of A and B will be completely the same except for a 0.1V horizontal shift. Now, consider a device C, where the channel potential is non-uniform along the width direction. Then, I_d(C) will be equal to I_d(D)+I_d(E) = I_d(A)/2+I_d(B)/2. Fig.3.4 compares I_d-V_g curves of A and C calculated in this way. I_d(C) is the sum of I_d(D) and I_d(E), whose I_d-V_g curves are the same by with 0.1V horizontal shift. As a result, the subthreshold current in C tends to saturate at a lower current level; i.e. at the same current level, the increase of I_d with V_g is “slower”, and SS becomes larger. This is because the increase of I_d(E) is “delayed” due to the higher local V_{th}. As a result, at a reference current 2×10^{-7}A, only 8% of the current of C flows through E at 25°C. Therefore,

compared to uniform case A, C shows worse SS due to the "delay" caused by E region (higher local V_{th}).

As shown in Fig.3.5, this "delay" effect is weakened at a higher temperature, since the subthreshold current level is raised up, and difference between D region and E region at the reference current becomes smaller due to degraded SS. Therefore, at 100°C, in C, 12% of the current flows through E region, and the "delay" effect becomes smaller compared to room temperature (25°C).

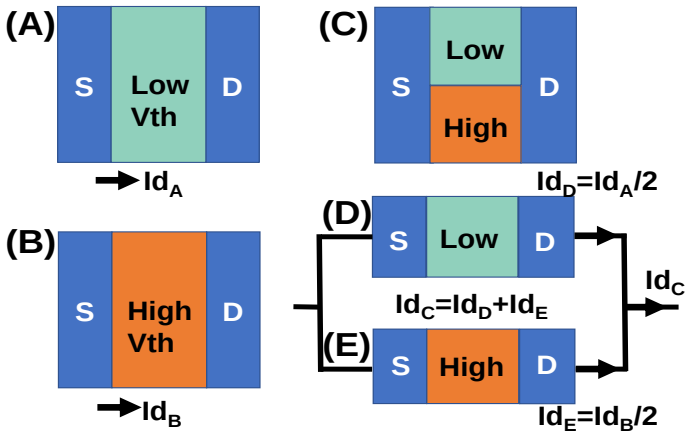

Fig 3.3 Schematic of effective current path model. A and B are ideal transistors with 0.1V V_{TH} difference. C is a transistor that is equivalent to D (half A) and E (half B) in parallel.

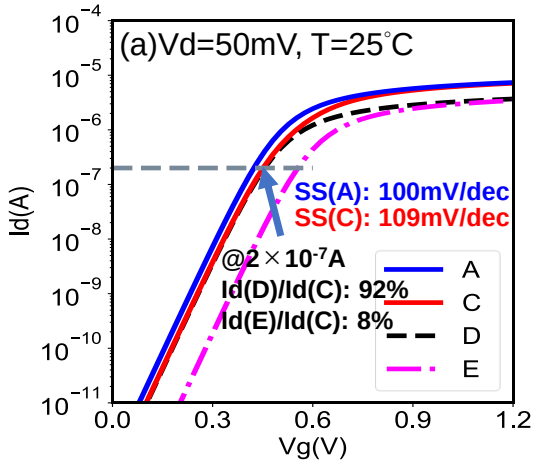

Fig 3.4 (T=25°C) Simulated I_d-V_g curve of A and calculated I_d-V_g curve of C by assuming $I_d(C) = I_d(D)+I_d(E) = I_d(A)/2+I_d(B)/2$. (Gray dash: reference current for SS)

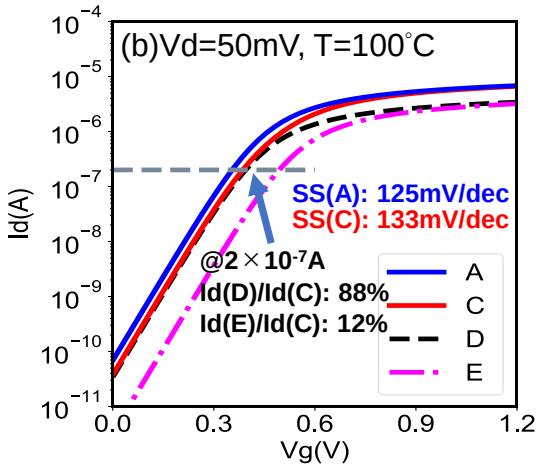

Fig 3.5 (T=100°C) Simulated I_d-V_g curve of A and calculated I_d-V_g curve of C by assuming $I_d(C) = I_d(D)+I_d(E) = I_d(A)/2+I_d(B)/2$. (Gray dash: reference current for SS)

Based on the discussion above, we can get that SS(C,100°C) - SS(A,100°C) < SS(C,25°C) - SS(A,25°C). Thus, non-uniform device C shows larger SS and smaller dSS/dT compared with uniform devices A and B.

This model can be generalized by considering n parallel connections of MOSFETs, as shown by a random device R in Fig.3.6. Here, for simplicity, it was assume that X% of the transistors have the same WF as A (lower local V_{th}) while the others have the same WF as B (higher local V_{th}), and $I_d(R)=X\%\times I_d(A)+(100-X)\%\times I_d(B)$. Fig.3.7 shows calculated I_d-V_g curves at 25°C and 100°C by changing the ratio of A component (X=1,2,…,100). Fig.3.8 shows calculated SS as a function of X (ratio of lower V_{th} component). As a result, the maximum value of SS happens at X~20%, and the minimum difference between SS(@25°C) and SS(@100°C) happens around X~15%. The scatter plot between SS(@25°C) and dSS/dT of calculated 100 transistors based on this simple model is shown in Fig.3.9, the negative correlation between SS and dSS/dT is well reproduced by this simple parallel model.

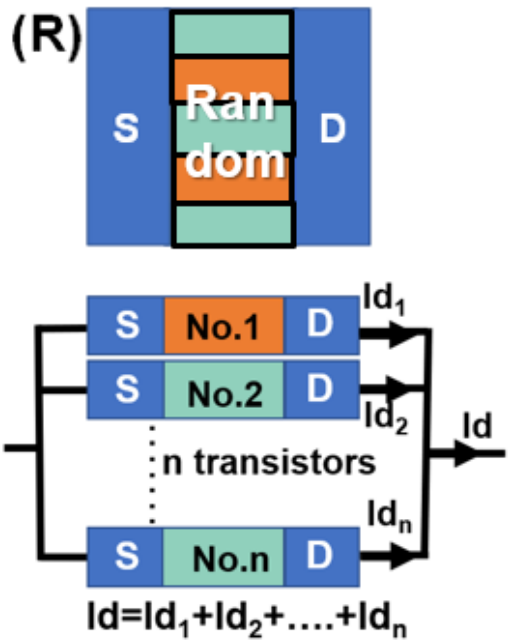

Fig 3.6 Schematic of simple parallel model. R is a random transistor that is equivalent to n transistors in parallel. I_d(R) is assumed to be the sum of currents flow through paralleled n transistors.

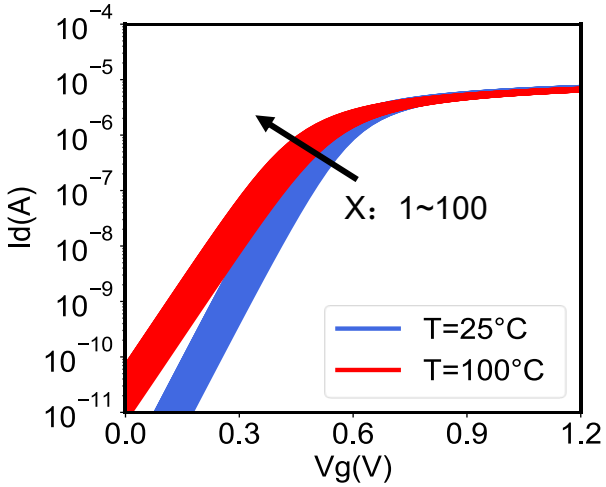

Fig 3.7 Calculated 100 I_d -V_g curves by assuming I_d(R)=X% × I_d(A)+(100-X)% × I_d(B), and changing X from 1~100. (blue) T=25°C, (red) T=100°C.

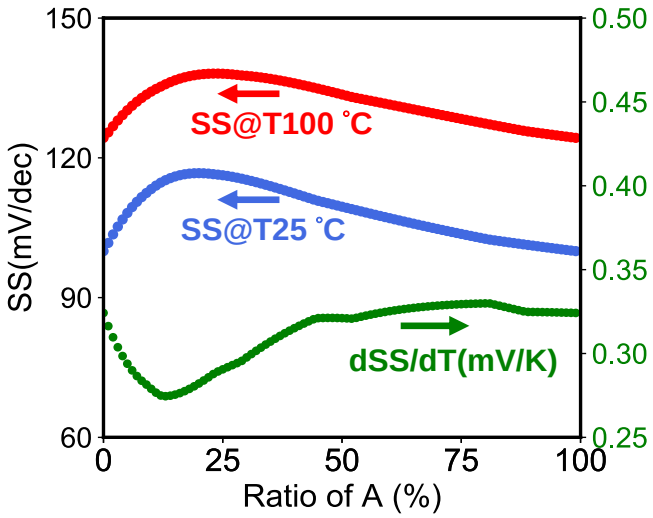

Fig3.8 Calculated SS and dSS/dT as a function of X (Ratio of A component).

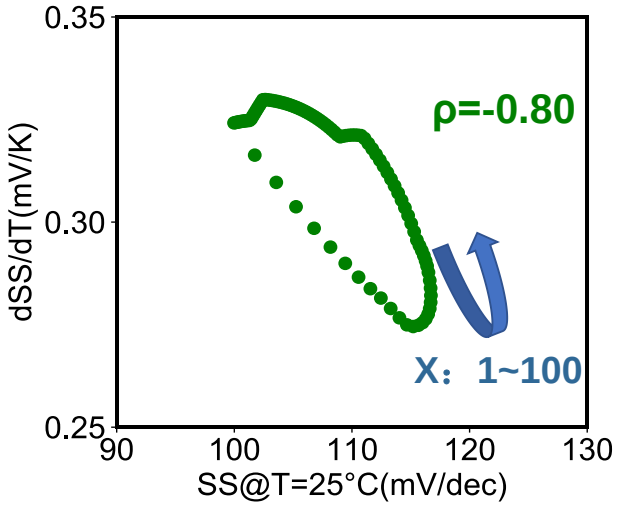

Fig.3.9 Negative correlation between SS (25°C) and dSS/dT (calculated 100 transistors by changing X from 1 to 100).

3.4 3D-TCAD Simulation

In section 3.3, we discuss the negative correlation between SS and dSS/dT based on simple parallel model. However, in real MOSFETs, randomness exists not only on the channel width direction, but also on all the other directions. Therefore, to verify the assumptions in section 3.3, 3D Monte Carlo TCAD simulations are carried out, where non-uniform channel was introduced by randomizing the grain size and position in the gate. This approach assumes that the gate consists of randomized grains of varying size and shape that can be characterized with an average grain size. It also assumes that the grains in the metal occur with a finite number of orientations, and the number of grains for each orientation can be characterized with a probability of occurrence. All grains of the same orientation are assumed to have the same WF, and the WF is different for each orientation [4].

Here, it was assumed that there are two possible grain orientations with 0.1eV WF difference, whose probabilities of occurrence are 50% and 50%, respectively. 100 bulk nMOSFETs with L/W=60nm/120nm and average grain size of 70nm are simulated. In this simulation, randomized electrostatic potential in the channel area leads to the randomized effective current path, and then leads to different SS and dSS/dT behavior.

Fig.3.10 shows an example of randomized channel potential by 3D TCAD simulation. The negative correlation (ρ=-0.86) between SS and dSS/dT (Fig.3.11) is in good agreement with the calculated results in section 3.3.

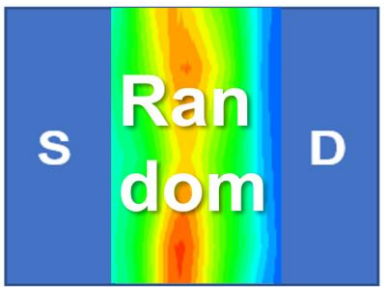

Fig.3.10 An example of randomized electrostatic potential distribution in channel area by 3D TCAD simulation.

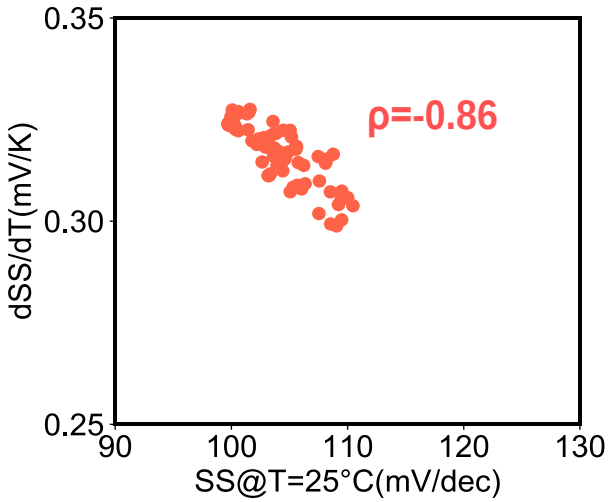

Fig.3.11 Negative correlation between SS (25°C) and dSS/dT (100 transistors by 3D TCAD simulation).

3.5 SS at Deep Subthreshold Region

As mentioned in chapter 2, due to the leakage current in our test structure, we cannot directly measure the off-state current and the current at very low level. Therefore, SS at relatively large $I_0=W/L\times10^{-7}A=2\times10^{-7}A$ is used and discussed so far.

However, in the calculation in section 3.3 and 3D TCAD simulation in section 3.4, we can reach to the SS defined at much lower current level. Here, we are safe to conclude that negative correlation between SS and dSS/dT should exist at deep subthreshold region (even at $I_0=1\times10^{-9}A$), as shown in Figs.3.12 and 3.13. Measurement results also show that the negative correlation is preserved at $I_0=5\times10^{-8}A$ (Fig.3.14).

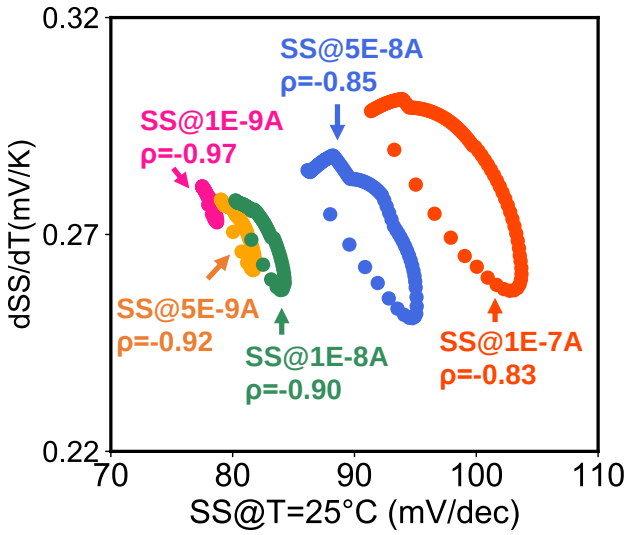

Fig.3.12 (Calculation) Correlations between SS (25°C) and dSS/dT (SS defined at reference current 1×10^{-7}A , 5×10^{-8}A, 1×10^{-8}A, 5×10^{-9}A, 1×10^{-9}A).

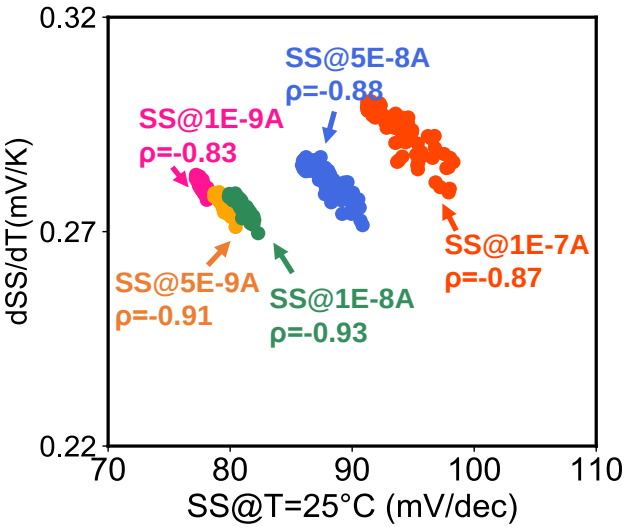

Fig.3.13 (3D-TCAD simulation) Correlations between SS (25°C) and dSS/dT (SS defined at reference current 1×10^{-7}A , 5×10^{-8}A, 1×10^{-8}A, 5×10^{-9}A, 1×10^{-9}A).

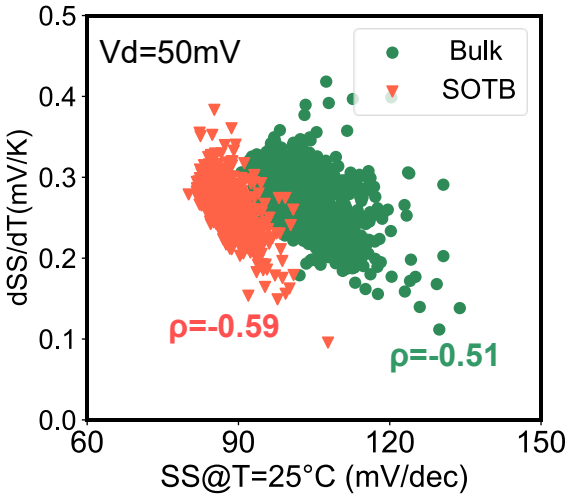

Fig.3.14 (Measurement) Correlations between SS (25°C) and dSS/dT in bulk and SOTB nMOSFETs (SS is defined at reference current 5×10^{-8}A).

3.6 Summary

In this chapter, we investigate the physical meachnism of the new finding that SS variability is reduced at high temperature, due to the negative correlation between SS and its temperature coefficient dSS/dT. This phenomenon can be explained by a simple non-uniform channel potential model, and it is also verified by 3D TCAD random simulation. This conclusion should exist even in deep subthreshold region.

From device point of view, as long as randomness exists in the channel width direction, this effect should exist. Here we only show the experimental results of planar bulk and SOTB MOSFETs, but it could be generalized to advanced structures like FinFET and gate all around (GAA) FET. From circuit point of view, if this effect can be exactly modeled, it will provide more exact margin estimation in circuit design.

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4. Physical Mechanism of Temperature Effect on DIBL Variability

4.1 Introduction

Drain-Induced-Barrier-Lowering (DIBL) is a crucial indicator of short channel effects in MOSFETs referring originally to a reduction of V_{th} of the transistor at higher drain voltages V_d. Here we define DIBL as the V_{th} difference between low drain bias (V_d=0.05V, linear regime) and high drain bias (V_d=1.2V, saturation regime) normalized by drain bias difference, i.e. DIBL=$\Delta V_{th}/\Delta V_d$, where $\Delta V_{th}=V_{th\_lin}-V_{th\_sat}$, and $\Delta V_d=V_{d\_sat}-V_{d\_lin}$.

It is reported that DIBL variability has significant impact on static random-access memory (SRAM) and analog circuits [1-3]. For SRAM, it is important because the pull-up (PU), pull-down (PD) and pass-gate (PG) transistors operate in different regimes during read and write operation. Therefore, V_{th} dependence of V_d bias is important and DIBL serves as a proxy for this. For analog devices, DIBL and its variability directly correlate to variability in output resistance (r_0), which in turn affects intrinsic gain and the maximum operating frequency of the device. The variability of DIBL has been comprehensively studied [1-4]. It is well studied and acknowledged that DIBL variability originates from source-drain positional asymmetry due to RDF, LER, WF variability and interface trapped charge.

DIBL is also reported to have temperature dependence [5-7]. To the best of our knowledge, however, temperature effect on DIBL variability has not been studied yet. In this chapter, temperature effect on DIBL is statistically studied for the first time. Experimental results show that the mean value of DIBL increases, but DIBL variability decreases as temperature rises, due to the negative correlation between DIBL and its temperature coefficient dDIBL/dT.

Physical mechanism of this new finding will be explained based on extreme cases simulation and 3D TCAD random simulations.

4.2 Temperature Coefficient of DIBL

Since DIBL is calculated by the difference between V_{th_lin} and V_{th_sat} normalized by drain bias difference, we first examine the shift of V_{th_lin} and V_{th_sat} between room temperature (RT=25°C) and high temperature (HT=100°C).

Figs 4.1 and 4.2 present scatter plots showing the correlations between V_{tRT} and V_{tHT}, in both linear and saturation region. Very strong correlations ($\rho \approx 1$) indicate that there is no anomalous change from room temperature to high temperature, which prove the accuracy of extracted DIBL and related temperature coefficients.

Figs.4.3 and 4.4 (left) present the Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$ in bulk and SOTB nMOSFETs. It is found that the mean value <DIBL> increases, but σDIBL decreases as temperature rises. DIBL variability reduces at high tempetaure owing to the negative correlation between $DIBL_{RT}$ and dDIBL/dT, as shown in Figs.4.3 and 4.4 (right). The negative correlations indicate that transistors with small $DIBL_{RT}$ are likely to degrade more at high temperautre, and this correlation exists in both bulk (ρ=-0.61) and SOTB (ρ=-0.50) MOSFETs.

Bulk MOSFETs have larger DIBL and dDIBL/dT variability than SOTB due to larger influence of RDF. Also, about 3% of bulk nFETs with larger $DIBL_{RT}$ show negative value of dDIBL/dT, but this phenomenon is not observed in SOTB nFETs.

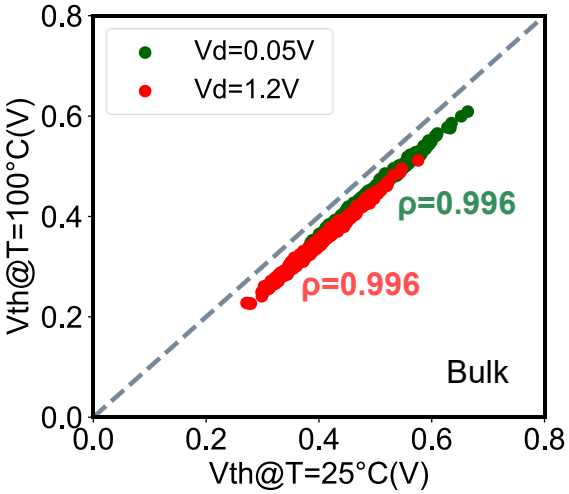

Fig.4.1 Correlation plots of V_{th_RT} and V_{th_HT} in 1k bulk nMOSFETs.

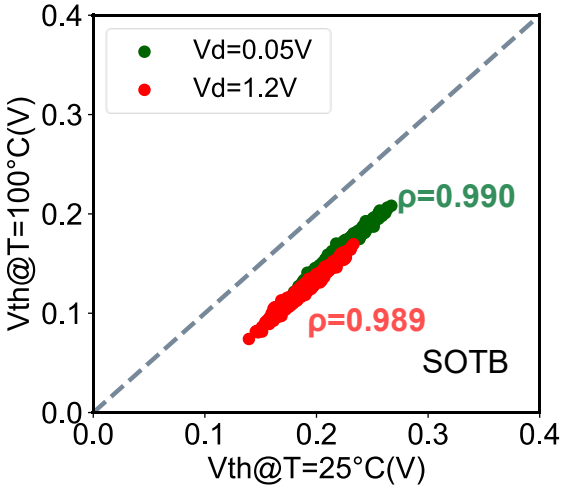

Fig.4.2 Correlation plots of V_{th_RT} and V_{th_HT} in 1k SOTB nMOSFETs.

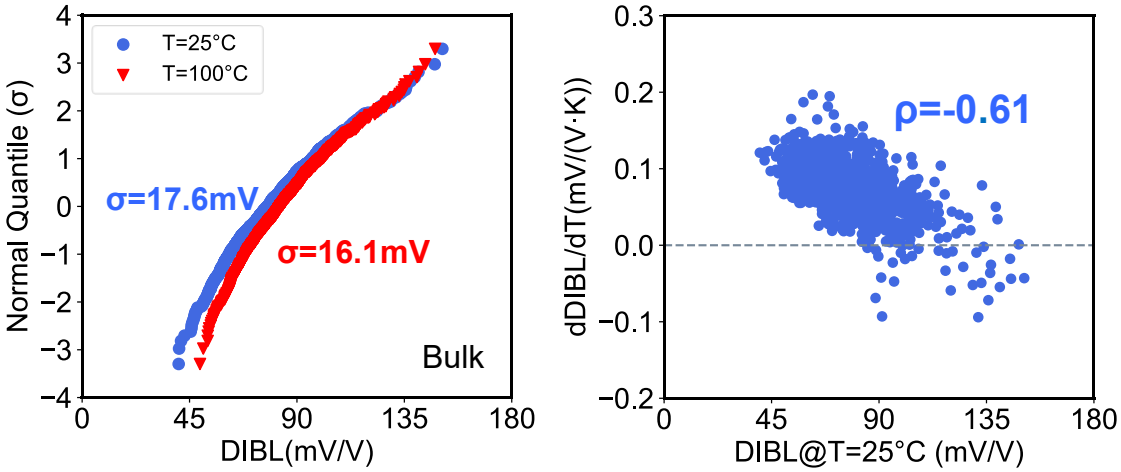

Fig.4.3 (left) Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$ (right) Negative correlation between $DIBL_{RT}$ and dDIBL/dT in 1k bulk nMOSFETs.

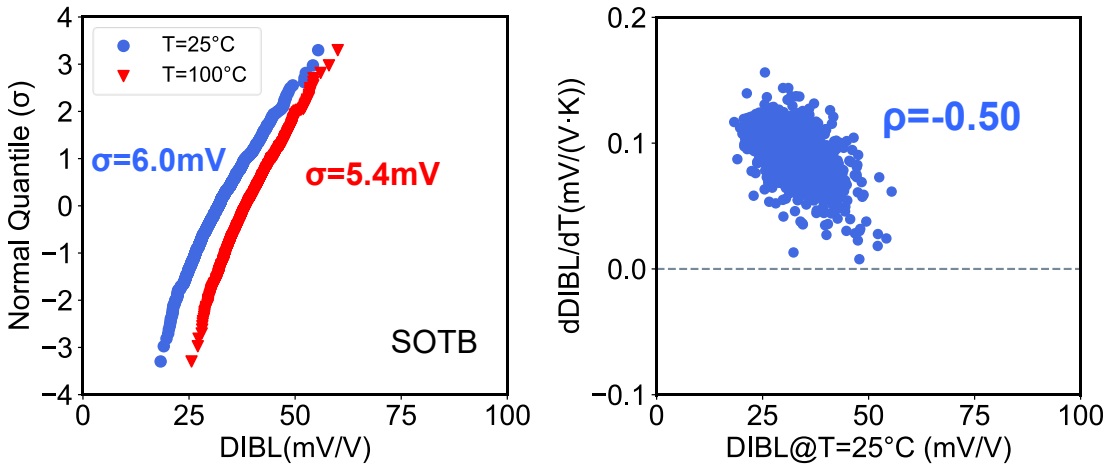

Fig.4.4 (left) Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$ (right) Negative correlation between $DIBL_{RT}$ and dDIBL/dT in 1k SOTB nMOSFETs.

The negative correlations between DIBL and its temperature coefficient dDIBL/dT look very similar to the correlation between SS and its temperature coefficient dSS/dT in chapter 3. We also examined the relationships between SS and DIBL, as well as the relationships between dSS/dT and dDIBL/dT. Very weak correlations in Fig.4.5 indicate that the physical mechanism of temperature effect on SS and DIBL variability originate from different perspectives.

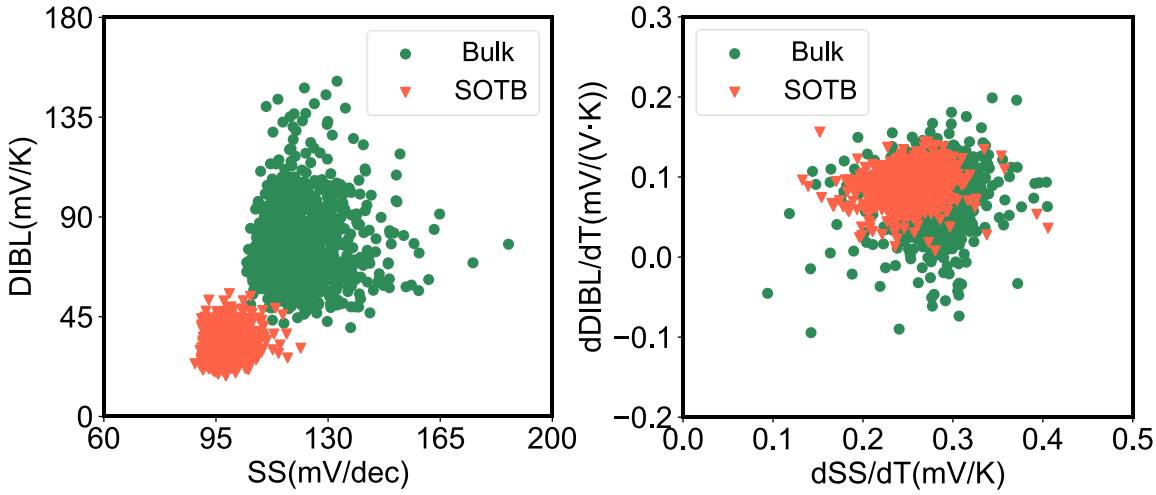

Fig.4.5 (left) Scatter plots between SS and DIBL in bulk and SOTB nMOSFETs. (right) Scatter plots between dSS/dT and dDIBL/dT in bulk and SOTB nMOSFETs.

4.3 dDIBL/dT Variability and Correlations

DIBL is an indicator of short channel effects in MOSFETs, but it still exists in not so aggressively scaled gate length (e.g. L=500nm). We also measured 1k long channel (L/W=500nm/120nm) as reference (Fig.4.6). Although DIBL and its variability are much smaller than that in short channel (L/W=60nm/120nm) case, the phenomenon that DIBL variability reduces at high temperature still exists, and the negative correlation between DIBL and dDIBL/dT becomes stronger (ρ=-0.84), which serve as informative extreme cases to understand the physical mechanism of temperature effect on DIBL variability.

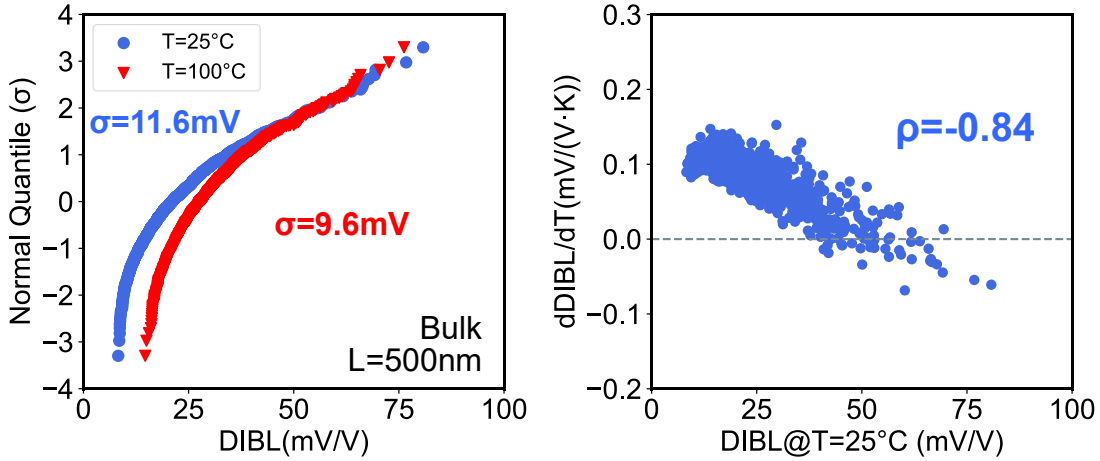

Fig.4.6 (L=500nm) (left) Q-Q plots of $DIBL_{RT}$ and $DIBL_{HT}$ (right) Negative correlation between $DIBL_{RT}$ and dDIBL/dT in 1k long channel bulk nMOSFETs.

DIBL is related to V_{tlin} and V_{tsat}, while temperature coefficient of DIBL (dDIBL/dT) is related to not only V_t and DIBL, but also the temperature coefficient of V_t ($|dV_{tlin}/dT|$ and $|dV_{tsat}/dT|$, here the absolute value is used to describe how much V_t is decreased by high temperature). Therefore, we examine the correlations between all the parameters contribute to the variability of dDIBL/dT. Fig 4.7 presents the scatter matrix of all related parameters (V_{tlinRT}, V_{tsatRT}, $DIBL_{RT}$ and their temperature coefficients $|dV_{tlin}/dT|$, $|dV_{tsat}/dT|$, dDIBL/dT) extracted from measured 1k short channel (L=60nm) and 1k long channel (L=500nm) bulk nMOSFETs. Since plots of long channel transistors show much stronger correlations, the interpretation of these correlation plots will start from long channel transistors (subplots L1~L15).

From the scatter matrix in Fig.4.7, firstly, it is obvious that V_t has positive correlations with its temperature coefficient $|dV_t/dT|$ (see subplots L2, L5 and S2, S5), which means transistors with higher V_t is decreased more by high temperature (have larger $|dV_t/dT|$), then leads to smaller V_t variability at high temperature, as reported in Ref [8]. This is because that depletion layer width (W_{dep}) shrinks at high temperature due to the increase of intrinsic carrier concentration at high temperature, leading to the decrease of potential Φ_B, and then results in the reduction of W_{dep} according to the equation [9].

$$W_{dep} = \sqrt{4\varepsilon_{Si}\varphi_B/qN_a}$$

Fig.4.8 presents a simple schematic of this phenomenon. As a result, transistors with higher V_t caused by larger dopant numbers (N_a) or non-uniform electrostatic potential profiles have thinner W_{dep}, which are more likely to be influenced by high temperature (have larger $|dV_t/dT|$). Therefore, the positive correlations in between V_t and $|dV_t/dT|$ could be explained, and it serve as the basic of the scatter matrix in Fig.4.7.

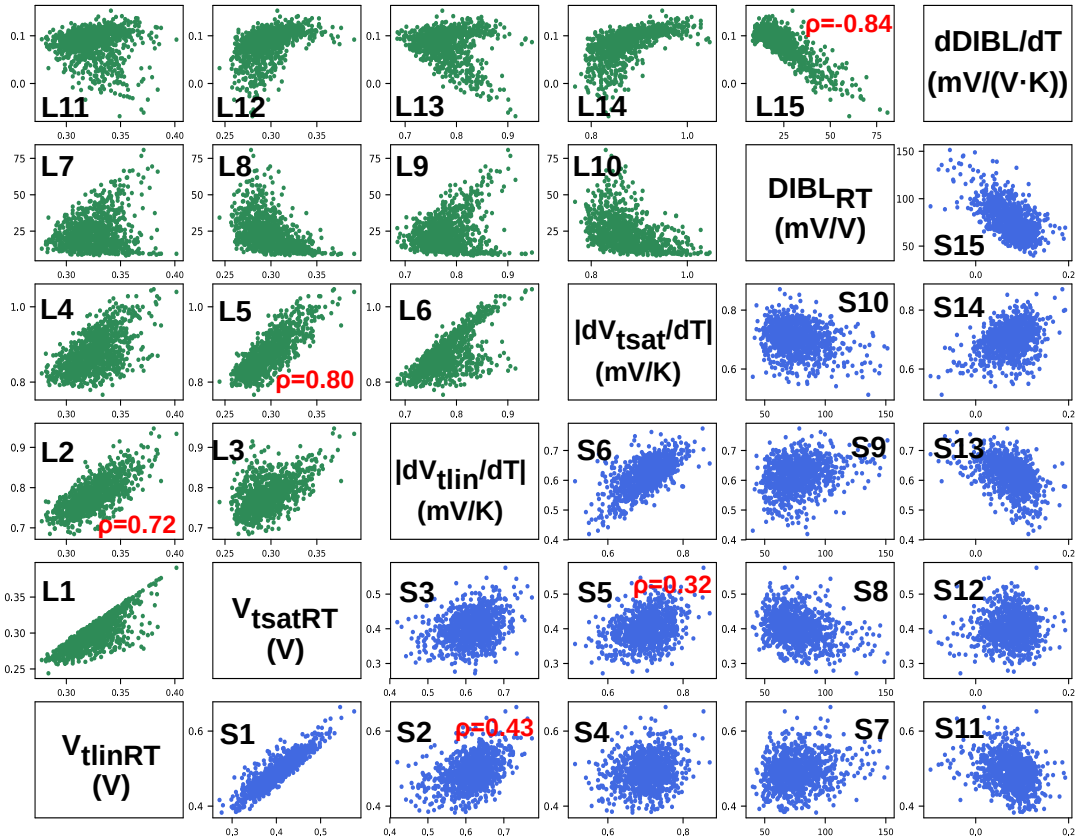

Fig.4.7 Scatter matrix of V_{tlinRT}, V_{tsatRT}, $DIBL_{RT}$ and their temperature coefficients. Green plots (Subplots L1~L15, long channel): 1k bulk nFETs with L=500nm. Blue plots (Subplots S1~S15, short channel): 1k bulk nFETs with L=60nm.

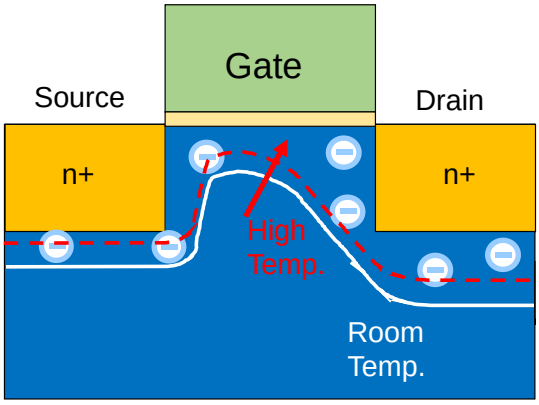

Fig.4.8 Schematic of reduced depletion layer width (W_{dep}) at high temperature, resulting in positive correlations between V_t and $|dV_t/dT|$.

Then we notice the peculiar triangular shapes for DIBL and dDIBL/dT related correlations (subplots L7~L14 in Fig.4.7). Triangular shapes of DIBL related correlations caused by source-drain asymmetry due to the RDF in heavily doped halo devices have been reported and analyzed in Ref [2]. As for temperature coefficients, dDIBL/dT related correlations also show triangular shapes (subplots L11~L14 in Fig.4.7).

To understand this, three extreme case bulk nMOSFETs, i.e. device A with symmetrical potential, device B with higher potential near source side and device C with higher potential near drain side, are simulated by TCAD. Here, the position of potential peak was modified by changing the gate WF distribution profile. Fig.4.9 show the schematic diagram of device A, B, C as well as their potential profiles. Apparently, compared to A and B, device C shows higher DIBL since its potential peak locates near drain side, and it is much easier influenced by high drain bias.

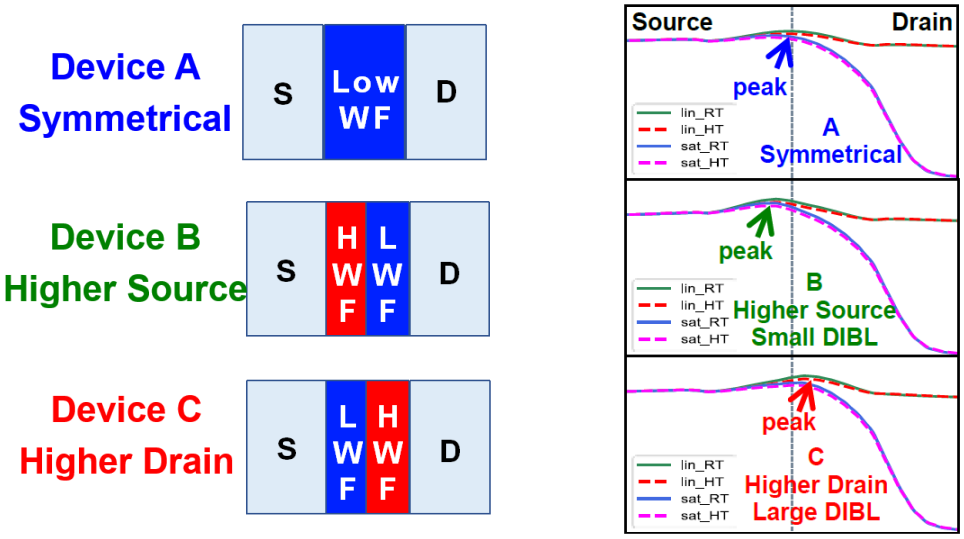

Fig.4.9 (left) Gate workfunction profiles and (right) electrostatics potential profiles at V_g=0.4V of three simulated extreme cases. Device A: symmetrical potential. Device B: higher potential near source side. Device C: higher potential near drain side.

V_t, DIBL and related temperature coefficients of simulated device A, B, C are calculated and the results are mapped on the scatter plots as in Fig.4.10. Grey plots are measured long channel devices in Fig.4.7 as reference shapes. The triangle shapes are well reproduced, and it can be confirmed that these three cases correspond to the corners of the triangles as in Ref [2]. Referring to Sim2 and Sim5, there are strong positive correlations between V_t and its temperature coefficient $|dV_t/dT|$. Devices B and C have similar V_{tlinRT}, but very different V_{tsatRT}, likewise for $|dV_{tlin}/dT|$ and $|dV_{tsat}/dT|$). As a result, $dDIBL/dT=dV_{tlin}/dT-dV_{tsat}/dT=|dV_{tsat}/dT|-|dV_{tlin}/dT|$ deviates between devices B and C, in spite of the similar V_{tlinRT} (Sim11), device B showing larger dDIBL/dT than C. As for DIBL, the relationship is reversed; device C shows larger DIBL than B (Sim7). This finally leads to negative correlation between DIBL and dDIBL/dT (Sim15).

As channel length reduces to 60nm (blue subplots in Fig.4.7), the difference between symmetrical and asymmetrical devices is not as obvious as that in long channel. Triangular correlations are weakened in subplots S7~14 in Fig.4.7 because more devices locate in the "middle-state", but their joint effects on the negative correlation between DIBL and dDIBL/dT should still exist.

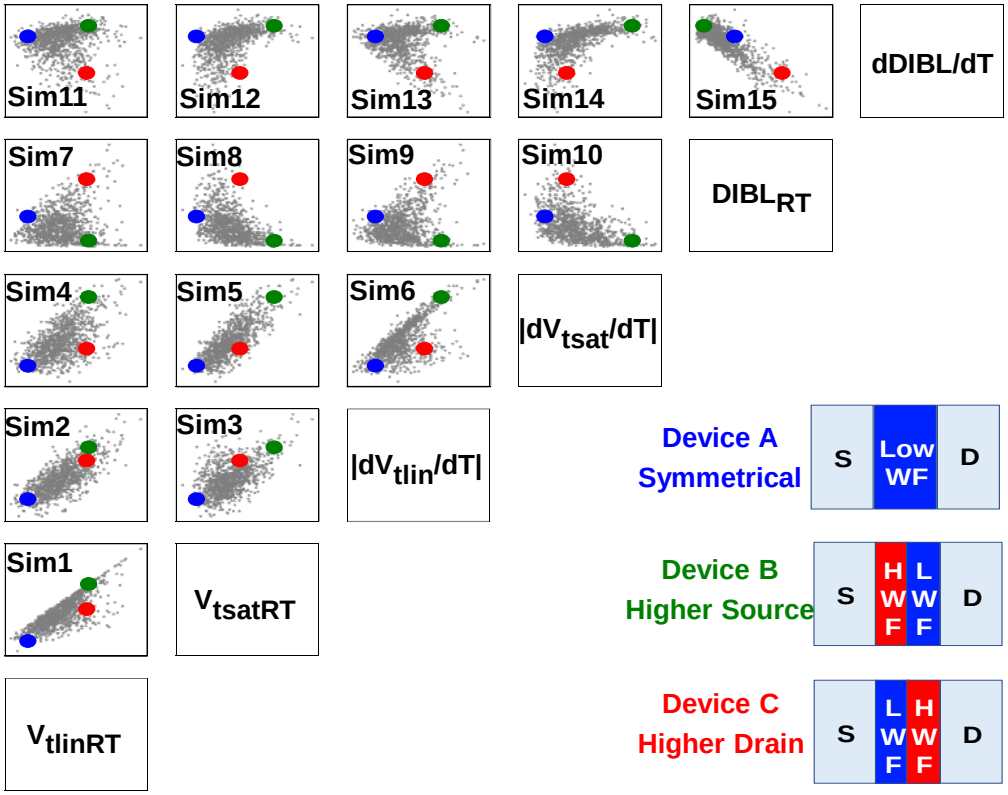

Fig.4.10 (Simulation) Scatter matrix of three typical devices. Blue: Device (A) with symmetrical potential distribution. Green: Device (B) with higher source potential. Red: Device (C) with higher drain potential. (Grey plots are measured long channel devices in Fig.4.7 as reference shapes)

4.4 Forward and Reverse Measurements

To investigate the impact of potential asymmetry induced variability, a method comparing the I-V characteristics operating in forward mode versus reverse mode is proposed in [10], and source-drain positional asymmetry due to RDF has been studied in [2,3] and results in asymmetric electrical characteristics between forward and reverse modes. Fig 4.11 is the scheme of forward and reverse measurement [3].

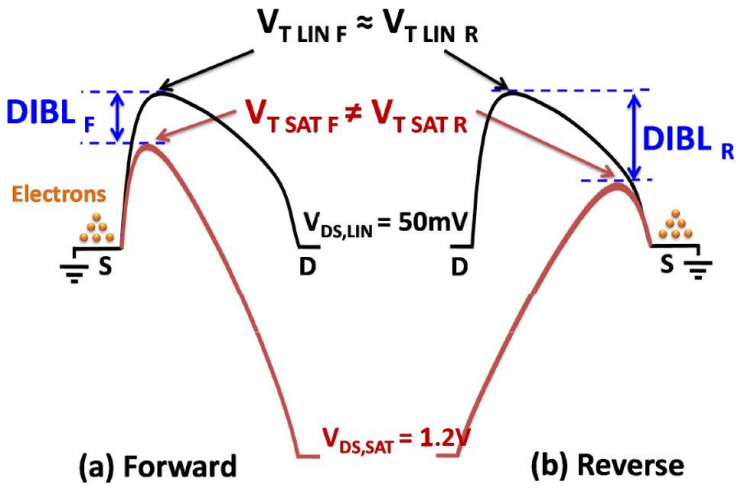

Fig.4.11. Scheme of potential profile across the source/channel/drain regions, in linear and saturation regimes of forward and reverse mode measurement [3].

To confirm the idea in section 4.3, reverse measurements by interchanging source/drain contacts are performed in long channel (L=500nm) bulk nMOSFETs, as shown in Fig 4.12. After interchanging source and drain contacts, higher source potential devices turn to higher drain potential devices, and vice versa. Transistors with large DIBL_forward and small DIBL_reverse, which are considered to be similar to device C, show exceptionally small dDIBL/dT_forward, in agreement with the above considerations.

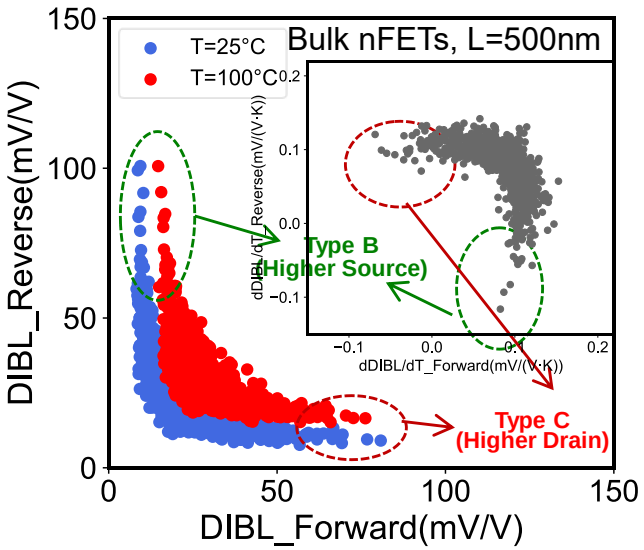

Fig.4.12 Comparison of forward and reverse measured $DIBL_{RT}$, $DIBL_{HT}$ and (inset) dDIBL/dT in bulk nFETs (L=500nm). Higher source potential devices turn to higher drain potential devices after changing S/D, and vice versa.

4.5 3D-TCAD Simulation

Finally, 3D Monte Carlo TCAD simulations are carried out in 200 random bulk nMOSFETs with L/W=60nm/120nm. In 3D TCAD simulation, the asymmetry of source/drain originates from randomized grain (with two different workfunction values) in the gate, as explained in section 3.4.

Here, 100 bulk nMOSFETs with smaller WF difference (0.1eV), while other 100 bulk nMOSFETs with larger WF difference (0.2eV) were simulated. Fig.4.13 shows the simulated negative correlation between $DIBL_{RT}$ and dDIBL/dT, which is in good agreement with measurement results. Also, negative dDIBL/dT is observed in some large variation cases (0.2eV WF difference), which is in good agreement with experimental results that negative dDIBL/dT only exists in bulk FET whose potential asymmetry is larger due to halo/pocket dopant and RDF.

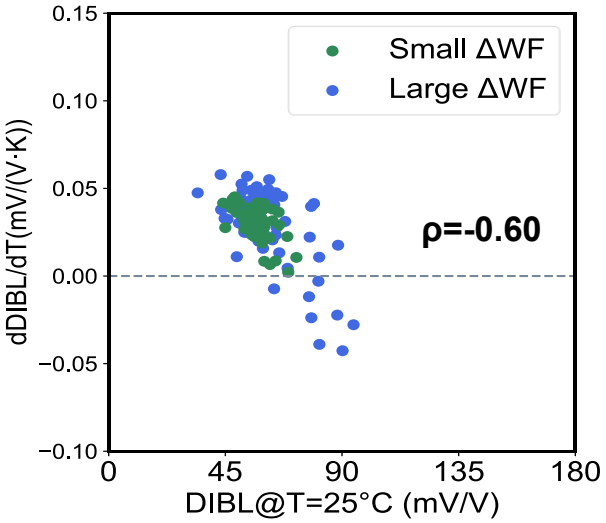

Fig.4.13 (3D-TCAD simulation) Negative correlations between $DIBL_{RT}$ and dDIBL/dT in 200 random bulk nMOSFETs. (Green) smaller WF difference (0.1eV). (Blue) larger WF difference(0.2eV).

4.6 Summary

In this chapter, we investigate the experimental new finding that DIBL variability is reduced at high temperature, due to the negative correlation between DIBL and dDIBL/dT. dDIBL/dT variability is also caused by the potential asymmetry between source and drain. This phenomenon is more obvious in long channel bulk MOSFETs, since the difference between symmetrical and asymmetrical devices are larger due to heavily doped halo structure. Physical mechanism of this effect is explained based on long channel bulk MOSFETs, combined with extreme cases simulation. This effect still exists in short channel bulk and SOTB MOSFETs. Therefore, statistical analyzes show that DIBL variability is reduced at high temperature, in scaled bulk and SOTB MOSFETs.

Fig.4.14 summarizes the physical mechanism of this phenomenon by comparing two measured transistors which are representative for higher source/drain potential devices, with almost same V_{tlin} and $|dV_{tlin}/dT|$. The difference and asymmetry between source and drain finally lead to different behavior of DIBL, as well as different dDIBL/dT.

Moreover, although the results that reduced SS variability and reduced DIBL variability at high temperature look very similar, the physical origins of these two effects are different, and the temperature coefficients dSS/dT and dDIBL/dT are weakly correlated. From the analyses in chapter 3 and chapter 4, we could conclude that temperature effect on SS variability are more related to the randomness along channel width direction, while temperature effect on DIBL variability are influenced more by the randomness along channel length direction.

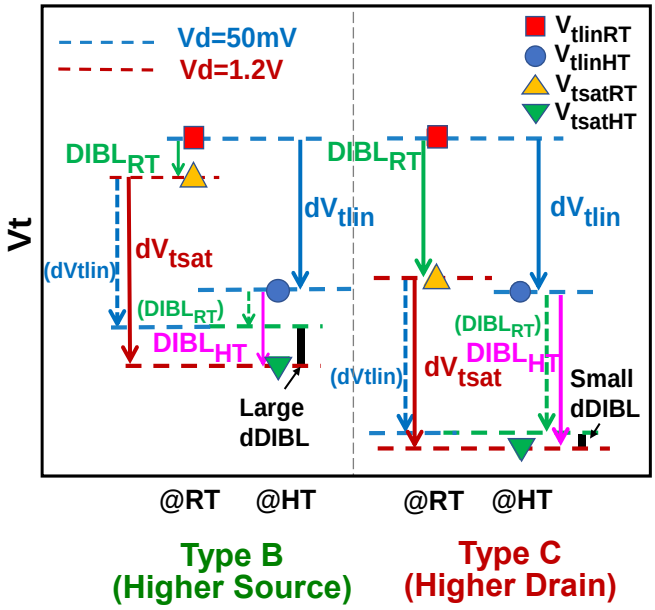

Fig.4.14 Comparison of two measured transistors representative for higher source /drain potential devices, with almost same V_{tlin} and $|dV_{tlin}/dT|$. Arrows stand for the decreased V_t by high temperature or DIBL. Dotted arrows are shifted copies for the calculation of dDIBL.

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5. Conclusions

In this thesis, temperature dependence of characteristics variability in scaled MOSFETs are systematically studied by experimental measurements combined with 3D TCAD simulation.

In chapter 2, we perform the experimental study about the impact of temperature on variability in bulk and SOTB MOSFETs fabricated by 65nm technology. Variability behavior at room temperature and high temperature of key device figures of merits (V_{th}, I_{on}, SS and DIBL) are measured and compared. Experimental results show that variability of V_{th}, I_{on}, SS and DIBL all reduce at high temperature. Reduced V_{th} and I_{on} variability at high temperature have been reported by previous study, however, reduced SS variability and reduced DIBL variability at high temperature have not been reported yet.

In chapter 3, physical mechanism of reduced SS variability at high is investigated. It is found that SS variability is reduced at high temperature due to the negative correlation between SS and its temperature coefficient dSS/dT. This negative correlation can be explained by non-uniform potential among channel width direction based on a simple parallel model, and it is also verified by 3D TCAD simulation.

In chapter 4, physical mechanism of reduced DIBL variability at high is investigated. Similar to SS, DIBL variability reduces at high temperature due to the negative correlation between DIBL and dDIBL/dT. However, the physical origin of temperature effect on SS and DIBL variability is different. DIBL and dDIBL/dT variability is more influenced by the potential variations along channel length direction (source-drain positional asymmetry). Explanation of it physical mechanism starts from long channel bulk MOSFETs, combined with extreme cases simulation. This effect still exists in short channel bulk and SOTB MOSFETs, and can be well reproduced by 3D TCAD simulation.

Throughout this thesis, we compared bulk and SOTB MOSFETs. Variability in SOTB is much smaller than bulk due to less RDF influence. However, temperature effect on variability behavior in bulk and SOTB show same trend that SS and DIBL variability is reduced at high temperature, and the variability of temperature coefficients in SOTB is comparable to bulk. These results provide us with information about randomness caused by LER, gate WF variability and interface traps.

From device point of view, as long as randomness exists in the device channel area, the effect in chapter 3 should exist. Also, if the source/drain area are asymmetrical, the effect in chapter 4 should exist. Here we only show the experimental results of planar bulk and SOTB MOSFETs, but it could be generalized to advanced device structures like FinFET and GAA-FET. From circuit point of view, if this effect can be exactly modeled, it will provide more exact margin estimation in circuit design. We hope this work could help to understand temperature effect on device performance and variability, for the prediction of characteristics variability in a wide temperature range.

List of Presentations

International Conferences

Shuang Gao, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi, Toshiro Hiramoto. "Temperature Effect on DIBL Variability in Bulk and SOTB MOSFETs." ***International Conference on Solid-State Device and Materials (SSDM*) *2018*, Tokyo, Japan, September, 2018. (to be presented)**

Shuang Gao, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi, Toshiro Hiramoto. "Reduced Subthreshold Slope Variability at High Temperature in Bulk and SOTB MOSFETs." ***IEEE Silicon Nanoelectronics Workshop (SNW) 2018*, pp 9-10, Honolulu, USA, June 17, 2018.**

Domestic Conferences

Shuang Gao, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi, Toshiro Hiramoto. "Reduced Subthreshold Slope Variability at High Temperature in Bulk and SOTB MOSFETs." ***The 79th JSAP Autumn Meeting,* September 20, 2018. (to be presented)**

Shuang Gao, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi, Toshiro Hiramoto. "Reduced Drain-Induced-Barrier-Lowering (DIBL) Variability at High Temperature in Bulk and SOTB MOSFETs." ***The 79th JSAP Autumn Meeting,* September 20, 2018. (to be presented)**

Shuang Gao, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi, Toshiro Hiramoto. "Understanding Temperature Effect on Subthreshold Slope Variability in Bulk and SOTB MOSFETs." **シリコン材料・デバイス研究会 (SDM), August 8, 2018. (to be presented)**