博士論文（要約）

Study on performance enhancement of ultra-thin-body Ge-on-Insulator pMOSFETs by Ge condensation method

（酸化濃縮法による極薄膜 Ge-on-Insulator pMOSFET の高性能化に関する研究）

AN ABSTRACT OF DISSERTATION

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Wu-Kang Kim （金 佑彊）

Supervisor Professor Shinichi Takagi

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For several decades, CMOS technology has been developed thanks to scaling, represented by Moore's law. However, with the upcoming fundamental limits the scaling, researchers focused in finding a new channel material for further enhancement. Among the many possible channel materials for next generation, Ge has been regarded as one of the most promising candidates for the new channel material due to the characteristics such as having both high hole and electron mobility which enables easy integration of the pMOSFET and nMOSFET to the CMOS. On the other hand, with the scaled MOSFETs, it is mandatory to suppress the short channel effect. Therefore it is important to also apply –OI (-on-insulator) structure to the channel. Consequently, the future CMOS is likely to be GOI (Ge-on-insulator) structure. There are several methods to fabricate GOI structure such as, wafer-bonding, smart-cut, epitaxial growth, and more. Among the GOI fabrication methods, one of the most promising methods is Ge condensation. Ge condensation method is condensing SiGe layer by oxidation. Since Si is oxidized before Ge, Ge remains when SiGe layer is oxidized. As the process proceeds, the Ge content in SiGe layer become higher and eventually only Ge remains after the process. The merit of Ge condensation is that this process is easy and cheap compared to other methods, as well as ability to form thin GOI layers, which can be easily applied to the CMOS industry. However, even with the merits, there also are some problems remaining. One of the problems is the poor crystalline in the GOI layer. When Ge get condensed and Si get oxidized, the difference of lattice constant will yield to the cracks and generation of defects in the SiGe layer. In addition, during the oxidation, as the Ge composition get higher, the strain relaxation occurs in the GOI layer. This causes not only the defect generation, but also disables to enhance pMOSFET performance, noting that compressive strain in Ge can lower the effective mass and therefore

enhance the pMOS mobility. Consequently, by suppressing the strain relaxation in GOI layer, we can improve both the crystalline and the performance. In this paper, I have successfully fabricated improved GOI crystalline with high temperature oxidation and intermixing. The main idea was to diffuse Ge into SiGe layer during the Ge condensation, to minimize the difference in lattice mismatch. The result of high temperature oxidation and intermixing, the generated defect in GOI layer reduced to 1/10 of conventional method. On the other hand, in spite of successfully suppressed defect generation, there are still problems remaining with strain relaxation during the process.

In order to solve the confronting problems, I have demonstrated a novel Ge condensation method which suppresses the strain relaxation during the process. The conventional Ge condensation, SiGe layer had to be put out of the furnace to check its composition, in order to perform oxidation at certain temperature to the nearest melting point where Ge composition can be. However, this consists of numerous cycles of rapid temperature change, which can affect the crystalline quality of SiGe-OIs and GOIs. Therefore, we neglected the temperature changes in the condensation process as well as introduction of slow cooling down process. Consequently, new Ge condensation process successfully realized compressively strained GOI layer with strain value of 1.6 %. The clear suppression of strain relaxation could be observed after Ge composition over 70 %, which starts relaxation as in the former process. In order to find out the evidence that rapid changes of the temperature cause the relaxation, I performed the same new recipe and changed the way of cooling down process. It was clear that the distribution and the mean amount of strain differed and the results indicated that slow cooling yields less relaxation. Moreover, rapid cooling down had least amount of strain. Therefore, it could be concluded that the repeated rapid cooling has been one of the main reasons for strain relaxation. Therefore, we have successfully suppressed the strain relaxation during the Ge condensation process. Also, with the compressive strained GOI layer, we enhanced GOI pMOSFET performance by enhancement factor of 2.5. The peak effective mobility of 1.17 % compressive strained GOI layer was 301 cm^2/Vs which was 2.5 times higher of the relaxed GOI pMOSFETs fabricated by former process technique.

Another issue in the GOI layer is to make ETB (Extreme-thin-body) GOI layer with thickness under 5 nm. According to ITRS (International technology roadmap for semiconductors), as the scaling of Ge channel advance, the thickness of Ge/GOI layer is expected to be less than 5 nm in the near future. Also, ETB structures became more important with the promising properties of fully depleted MOSFETs. However, even being possible to fabricate, conventional ways for fabricating GOI layer under 5 nm had huge degradation in performance, due to reasons such as scattering effect. We have fabricated GOI pMOSFETs with thickness less than 5 nm in several ways. The first method was by thermal oxidation after the Ge condensation process. Thermal oxidation after the Ge condensation would affect GOI layer with better passivation layer of GeO_x in between the BOX and Ge layer. However, as we tried further oxidation after the whole process, it was clear that thermal

oxidation would not enhance, but it degraded the performances of GOI pMOSFETs with thinner body thickness. The main reason of this result was due to the thinner body getting affected more by the difference in thermal expansion coefficient between the Ge and Si/SiO_2. Not only the performance and effective mobility got degraded, but also it showed higher hole concentration in thinner layers, and tensile strain on the body, which clearly means that difference of thermal expansion coefficient affected the crystalline of the GOI layer. However, we have successfully fabricated the 4.5 nm-thick GOI pMOSFET with compressive strain by thinning strained GOI layer with ECR plasma oxidation. ECR plasma oxidation is etching process, which enables us to etch GOI layer digitally. The experiments showed no strain relaxation by ECR plasma oxidation process. Therefore, we have successfully fabricated compressively strained GOI layer with thickness of 4.5 nm. The 4.5 nm-thick strained GOI pMOSFET showed superb performance with extreme on-off current ratio of over 10^7, which is most high among reported, and effective mobility of 138 cm^2/Vs, which is twice greater than the pMOSFET reported from other GOI fabrication methods.

In this thesis, I developed and realized several methods to enhance pMOSFET performance, as well as thinning the GOI body thickness for future technology. The main idea was by using Ge condensation to fabricate GOI layers. I have enhanced the Ge crystalline with high temperature oxidation and intermixing the annealing with dry nitrogen. Also, by neglecting the rapid temperature difference, I have successfully developed a new method to suppress the strain relaxation after Ge condensation method. Moreover, this led to enhancing GOI pMOSFET performance and to achieve higher effective mobility. As well as enhancing the GOI pMOSFETs, I have fabricated thin GOI layers with several methods. Especially, strained GOI layers thinned by ECR plasma oxidation had superb results. With the technologies I have developed, I have realized the best performing devices, which can help to develop future CMOS industry.