# 論文の内容の要旨

論文題目　Synthesis, Purification and Device Application of Horizontally Aligned Single-Walled Carbon Nanotubes

（水平配向単層カーボンナノチューブの合成・精製・デバイス応用）

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For the last several decades, the semiconductor industry has been improving the performance and reducing the economic cost of microelectronic devices by reducing the dimension of silicon transistors, motivated by Moore's law. The shrinking of transistors to 10 nm leads to 100 million transistors packed in each square millimeter. However, it is believed that the scaling of silicon transistors is approaching its end physically and technically. That is why the industry is investing on the development of new structures and also novel materials for further scaling (more Moore) and additional functions (more than Moore). In order to continuously drive the performance improvement of microelectronic devices, channel materials that have outstanding electric properties, *e.g.* high carrier mobility for both electrons and holes, and ultrathin body for the excellent gate control even at ultrascaled devices. In this sense, single-walled carbon nanotubes (SWNTs) are one of the best candidates for alternative materials of silicon in high-performance electronics. SWNTs are hollow, cylindrical nanomaterials composed of a single layer of carbon atoms (graphene), which have exceptional physical and thermal properties, too. A theoretical study predicted that SWNT-based digital systems will outperform silicon-based devices with the same technology node by several times in terms of both switching time and energy efficiency. Furthermore, researches recently fabricated SWNT transistors with ultrascaled gate lengths

(down to 5 nm) or footprints including source/drain contacts (down to 40 nm), demonstrating large current density in on-state and superb switching behavior. In addition to such excellent performances in individual transistor level, three-dimensional digital systems that incorporated more than one million SWNT-based inverters were built for the sensing environments, and then the storing and processing of information. This proved that SWNT-based large-scale systems can work reliably and also possess unique functions.

These very recent progresses on SWNT-based transistors both in small-sale and large-scale encouraged researchers towards continuous efforts on the research field of SWNTs. However, it is still quite difficult to simultaneously achieve the large-scale integration of ultrasmall transistors because of the difficulty in obtaining "good" SWNT starting materials suitable for the device fabrication. We should start the fabrication from aligned arrays of high-density (>100 SWNTs/μm) but individual, purely semiconducting (>99.9999%) SWNTs over a large area. One promising approach to prepare such materials is to separate s-SWNTs *via* liquid-phase chemical processes, and then assemble them on wafers into aligned arrays with controlled density and alignment. Although wet separation methods successfully obtained high-purity semiconducting SWNTs (99.99%), and even single-chirality SWNTs in solution, surfactants needed for dispersion of SWNTs contaminate the SWNTs, and ultrasonication makes SWNTs shorter and defective during the separation processes. Assembly of SWNT solution into aligned arrays has high controllability of the density, but it has a high chance of crossing and bundling of SWNTs, making the ultrascaled transistor leaky (large off-state current) due to weak electrostatic control by gate.

In this thesis, fabrication of the high-density s-SWNT arrays is studied from two points of view; synthesis and post-growth purification. SWNTs can be obtained in a horizontal array morphology by the chemical vapor deposition (CVD) method on single-crystal substrates, such as sapphire and quartz. This growth method of SWNT arrays is favorable for high-performance transistors. Recent experiments revealed that density and chirality of aligned SWNTs can be highly controlled by the design of catalysts together with substrates preparation. As theoretical studies indicate, the control of spatial uniformity of SWNT density, i.e. length and nucleation probability, and chirality needs further improvement. To understand the growth mechanism of application-oriented long SWNT arrays in detail, a digital-coded isotope labeling method is demonstrated. Binary-like codes are embedded in SWNTs. The programmed sequence of the digital-coded isotope labels identify time-resolved growth evolution of individual long SWNTs (>100 μm), including the information about growth rate, incubation time, lifetime, and even pause time. As a simple example of the application of the method, we elucidate that the SWNTs usually start growing after certain time of incubation, and are elongated without changing the growth rate

until abrupt termination. The SWNTs follow so-called base-growth mode under the present condition. One exception of non-constant growth rate along an SWNT (from an identical catalyst particle) is spontaneous chirality change via intramolecular junctions. The growth under modulated conditions can also be traced, such as temperature and the partial pressure of carbon feedstocks. This leads to finding of unusual phenomena, such as the growth suspension induced by sudden increase of ethanol pressure. These findings enabled by the digital-coded isotope labeling method will accelerate the further control of spatial and structural uniformities of SWNTs towards SWNT-based microelectronics.

Even if high-density homogeneous SWNT arrays are grown on substrates, impurities of metallic (m-) SWNTs must be removed, while preserving s-SWNTs perfectly, in order to simultaneously obtain large on-state current density and small leakage current. Joule self-heating can selectively cut m-SWNTs without damage to the s-SWNTs because of the difference in the electric transport properties of the two types of SWNTs. In addition, compatibility with high-density arrays (>100 SWNTs/μm) makes this method a suitable tool for the fabrication of high-performance devices. One of the drawbacks of electrical breakdown is the difficulty in large-scale fabrication because only local portions (~100 nm) of m-SWNTs are removed and one-by-one voltage application is required for a number of electrode pairs. The author have recently proposed an extended method of electrical breakdown for the long-length removal of m-SWNTs over >10 μm, in which organic films assist the propagation of SWNT burning. Importantly, a single treatment of full-length m-SWNT removal would enable the robust integration of a number of transistors without sacrifice of the on current through the use of the resultant long s-SWNT arrays. However, variation in the burning length and limited reproducibility of the technique, which originate from a poor understanding of the mechanism for SWNT burning, must be resolved to establish this as a practical method.

As a first step, water- and polymer-assisted burning is developed as an on-substrate purification method for the stable removal of long m-SWNTs. Poly(methyl methacrylate) (PMMA) is employed as an organic film material to enhance the removal of m-SWNTs. The burning length of m-SWNTs is increased by an average of more than thirty times (>5 μm) by the introduction of water vapor into the ambient gas. A simulation of SWNT burning is also conducted to elucidate the role of polymer films and to obtain further guidance toward successful full-length burning of m-SWNTs. Partial removal of m-SWNTs is attributed to one-way burning from a random position of breakdown.

To understand this one-way burning phenomenon, voltage-driven unidirectional anode etching of SWNTs at nanogaps is studied. Field emission current at SWNT gaps and the increased

gap size of broken SWNTs by application of a DC voltage is carefully observed. The dependence of the gap size on the applied voltage and ambient humidity is investigated, well agreeing with a field enhancing model. Based on the experimental results, it is considered that electrochemical etching at the SWNT tips due to physisorbed water and enhanced electric field is the driving force behind the gap extension.

Since these knowledge implies a reliable strategy for on-chip sorting of s-SWNTs over a large area, the fabrication of purely s-SWNT arrays and a number of scaled transistors is demonstrated. In the last chapter of the thesis, a method for the full-length burning of m-SWNTs is presented by overcoming the problems with water- and polymer-assisted (WPA) burning. Since the gap formation process and subsequent burning process can be separated, full-length burning is achieved after nanogaps in m-SWNTs are formed in a small designated area. Multiple transistors are then successfully fabricated along the resultant s-SWNT array, and thereby show large on-state conductance (4.6 μS per single s-SWNT) and superb switching behavior (on/off ratio ~$10^5$) for all devices with various dimensions. WPA burning from the pre-formed nanogaps lowers the voltage required to initiate burning, which reduces the damage to s-SWNTs through the sorting. A simple modeling of field enhancement at SWNT tips implies the applicability to the arrays with ~100 SWNTs/μm density or more, so that the sorting method could lead to the large-scale integration of ultrascaled SWNT transistors for high-performance logic applications.

In conclusions, the thesis focuses on the fabrication of large-area purely semiconducting SWNT arrays from synthetic approaches and post-synthesis sorting processes, while synergizing the characteristics of both aspects. Basic studies on horizontally aligned SWNTs reveals important knowledges behind the growth process which have been hidden under the observation of bulk SWNT samples or *ex situ* characterizations. This will leads to the better control of chirality, density, and homogeneity of SWNT arrays for the successful sorting process developed in this study. Starting from a finding of unusual phenomenon about electrical breakdown of SWNTs, a reliable method for full-length burning of m-SWNTs, i.e. on-chip sorting of long s-SWNT arrays is developed and applied. SWNT-based transistors with various dimension are fabricated to demonstrate advantages over those fabricated through other methods. The thesis therefore highly contributes to the realization of SWNT-based next-generation microelectronics beyond silicon.