博士論文（要約）

Fabrication and spin-dependent transport of spin field-effect transistors: Vertical spin field-effect transistors (V-Spin-FETs) and current-in-plane spin-valve field-effect transistors (CIP-SV-FETs)

(スピン電界効果トランジスタの作製とスピン依存伝導特性：縦型スピン電界効果トランジスタと面内伝導型スピンバルブ電界効果トランジスタ)

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In this doctor thesis, the author describes the spin-dependent transport properties of vertical spin field-effect transistors (V-Spin-FETs) and current-in-plane spin-valve field-effect transistors (CIP-SV-FETs). This doctor thesis consists of 7 chapters.

In Chapter 1, the background of this thesis is described. Now that the minitualization of Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs), which has been pulling forward improvement of electronics devices, is facing a physical limitation, we have come to a stage that we have to come up with novel technologies to satisfy increasing demands for new devices and integrated circuits with low-power consumption. Spintronics, in which a spin degree of freedom is actively utilized, has been generating considerable attention. Among numerous spintronics devices proposed thus far, a spin MOSFET, in which the source and drain electrodes are composed of ferromagnetic materials, is one of the most promising devices because of its compatibility with existing well-established semiconductor technologies and a variety of possible applications. To demonstrate spin MOSFET operation, we need to control the current not only by the gate voltage but also by the magnetization configuration. Previous studies on spin MOSFETs are briefly introduced. One of the most serious problems we have to solve is small magnetoresistance (MR) ratios; the largest MR ratio reported so far was 0.1% even at low temperature.[1–3]

In Chapter 2, the author shows the study on a vertical spin MOSFET using ferromagnetic semiconductor GaMnAs as source and drain electrodes and GaAs as a channel layer. In order to obtain spin MOSFET operation with a large MR ratio, we proposed a vertical spin MOSFET. In the vertical spin MOSFET, the source and drain GaMnAs electrodes and the GaAs channel layer are stacked on a GaAs substrate in a vertical direction by epitaxial growth. By applying a gate voltage from the side surface of the mesa, we can control the current flowing between the source and the drain perpendicular to the plane. The vertical structure is preferable in terms of not only electrical transport but also spin-dependent transport; for electrical transport, vertical spin MOSFETs are expected to have high immunity to short channel effect and to show steep switching behavior because the gate-electric field affects the electrical potential in the channel effectively in comparison with the case in lateral spin MOSFETs.[4] For spin-dependent transport, the vertical spin MOSFET is also preferable because an atomically flat thin channel, which is crucially important for a large MR ratio, can be easily obtained. Here, the author describes the basic properties of a ferromagnetic semiconductor GaMnAs, which will frequently appear in this thesis. A GaMnAs-based heterostructure is one of the most ideal material systems because large MR ratios were reported in GaMnAs / semiconductor / GaMnAs heterostructures.[5–9] We fabricated a GaMnAs-based vertical spin MOSFET with a cylindrical 200-μm mesa in diameter and a 27-nm-thick Al_2O_3 gate insulator thin film using standard fabrication processes (i.e. photolithography and wet etching) and atomic layer deposition (ALD) of gate insulator thin films. ALD is suitable for our study because various insulating materials can be deposited at relatively low substrate temperature and uniformly. We successfully modulated the drain-source current not only by the gate voltage (~0.5%) but also by the magnetization configuration (~60%). We confirmed that other effects such as the gate leakage current and electric-field effect on parasitic resistance were negligibly small and the electric-field effect on the intermediate GaAs channel layer was mainly responsible for the current modulation. The obtained MR ratio is more than 100 times larger than the values obtained in the previous studies. The MR ratio was also modulated by the gate voltage. Our results demonstrate the possibility that our device can provide desired properties of spin MOSFET when the device is reduced to a sub-micron or nanometer scale.[10]

In Chapter 3, the author describes the study on a V-spin-FET using a GaMnAs-based heterostructure and an ionic liquid. The problem of the vertical spin MOSFET presented in Chapter 2 is small current modulation ratio. To enhance the current modulation ratio, we decreased a width of each mesa down to ~220 nm by electron-beam lithography because our electric-field calculation showed that the electrical potential in the intermediate GaAs layer is affected only within ~5 nm from a side surface of a mesa because of a short channel length. In addition, we utilized an ionic liquid, which is reported to have a large capacitance per area. We fabricated a V-spin-FET with an ionic liquid as a gate capacitor, which we refer to as a spin electric double-layer transistor (spin EDLT). We investigated the spin-dependent transport properties of the spin EDLTs and successfully observed a large current modulation ratio (~20%) and a large magnetoresistance ratio (~37%). Moreover, by measuring the in-plane magnetic-field-direction dependence of the tunneling magnetoresistance (TMR) ratio with various gate voltages, we found that the magnetic anisotropy in

our spin EDLT was modulated by applying the gate voltage from the side surfaces of the mesas. To understand the influence of the gate voltage on the magnetic anisotropy quantitatively, we calculated and reproduced the in-plane magnetic-field dependence of the TMR ratios using Stoner-Wohlfarth coherent rotation model with a domain wall nucleation/propagation energy. By comparing the experimental data with the calculation results, we found that the domain wall nucleation/propagation energy of the GaMnAs layers was modulated by the gate voltage. Although the detailed mechanism has not been clarified yet, our results indicate that a new functionality of magnetic-anisotropy control can be utilized in vertical spin FETs.

In Chapter 4, the author presents the study on a vertical spin MOSFET. The vertical spin EDLTs presented in Chapter 3 showed the large current modulation ratio and the large MR ratio. However, EDLT, in which an ionic liquid is used, is not compatible with today's electronics. To demonstrate an all-solid-state vertical spin FET with a large current modulation ratio, we fabricated a vertical spin MOSFET using a GaMnAs-based heterostructure and a HfO_2 layer as a gate insulator. To further enhance the current modulation ratio, we minitualized the width of each mesa down to ~500 nm. We successfully obtained a large current modulation ratio up to ~130%. This current modulation ratio is the largest in vertical spin FETs reported thus far. To understand the origin of this large current modulation ratio, we performed two-dimensional electric-field simulation. We found that the electric-field effect on indirect tunneling via defect states in the channel layer is responsible for the large drain-source current modulation. We also showed TMR up to ~7%, indicating that the drain-source current can be controlled by the magnetization configuration. Furthermore, we found that the TMR ratio tended to increase with decreasing the gate-source voltage from 0 V in the negative direction, which probably originates from electric-field modulation of the magnetic anisotropy of the GaMnAs ferromagnetic electrodes as well as the potential modulation of the semiconductor GaAs channel layer. Our results provide an important insight for realizing practical spin MOSFETs.

In Chapter 5, the author studies V-Spin-FETs which can operate at room temperature. In Chapter 2-4, we demonstrated ferromagnetic-semiconductor GaMnAs-based vertical spin FETs and showed current modulation by the magnetization configuration as well as by the gate voltage. However, the low Curie temperature of GaMnAs (< 200 K) prevented room-temperature operation. To demonstrate a vertical spin FET operating at room temperature, we used a ferromagnetic metal with higher Curie temperature than room temperature and an oxide semiconductor as a channel layer. We fabricated a vertical spin FET using a heterostructure and successfully obtained current modulation not only by the magnetization configuration but also by the gate voltage.

In Chapter 6, the author presents CIP-SV-FETs using a GaMnAs-based heterostructure. In Chapter 2-5, the author has investigated vertical spin FETs and they exhibited the large MR ratios in compared with those of lateral spin MOSFETs. Despite experimental demonstrations of lateral spin MOSFETs and vertical spin FETs, there still remain problems to overcome for practical applications in the present research status. In the lateral spin MOSFETs, the small MR ratio is a crucial problem. This is caused by the difficulty of efficient spin injection from ferromagnetic metals into semiconductors and of the coherent spin transport with a long distance in semiconductor channels. In the vertical spin MOSFETs, although the MR ratio is large, the current controllability by a gate voltage is small in the present status and further improvement is necessary. Motivated by that necessity, we proposed an alternative spintronics device, current in-plane spin-valve field-effect transistor (CIP-SV-FET). A CIP-SV-FET comprises a ferromagnet / non-magnet / ferromagnet trilayer channel and a gate electrode and can offer functionality similar to spin MOSFETs. In CIP-SV-FETs, the resistance of the channel is controlled by the magnetization configuration through current-in-plane spin-valve effect induced by the two ferromagnetic layers. The channel resistance is also controlled by the electric-field effect on the top ferromagnetic layer. Ideally, we can expect that the current is switched on/off by applying the gate electric field. Thus, we can use this device as a transistor. Moreover, if the thickness of the top ferromagnetic film is sufficiently thin, the magnetic properties can be modulated by the gate electric field. Therefore, we can reduce power consumption for writing data using the electric-field-assisted magnetization reversal. For this proof-of-concept study, we used a GaMnAs-based heterostructure because CIP-SV was observed in it[11–13] and the resistance and ferromagnetism of GaMnAs thin films can be modulated by the gate electric field.[14] We fabricated a ferromagnetic-semiconductor GaMnAs-based CIP-SV-FET and demonstrated its basic operation of resistance modulation by a gate voltage (14%) as well as by the magnetization configuration (0.17%). Furthermore, we also demonstrated the electric-field-assisted magnetization

reversal in our device. These results indicate that the CIP-SV-FET is a hopeful candidate for an alternative type of a spin MOSFET.[15]

In Chapter 7, the author mentions concluding remarks and future outlooks.

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