博士論文

Research on Ultra-Low Power CMOS Circuits for Battery Management

（バッテリーマネジメント向け超低消費電力CMOS回路の研究）

平成 29 年 12 月 1 日提出

指導教員　桜井貴康　教授

東京大学大学院工学系研究科
電気系工学専攻

37-157075
染谷　晃基
Teruki Someya

Abstract

The internet of things (IoT) is creating a new world where objects are connected to the internet, and we can collect much information from edge nodes easily. The IoT is expected to achieve new applications that enhance productivity and quality of our lives. In the IoT, the lifetime of IoT nodes determines the total cost and the quality of the applications. It is clear that to prolong and improve the lifetime of the IoT node is challenging issue for the future expansion of the IoT. However, the size and capacity of battery in IoT node are limited, which reduces the total amount of energy for the operation. In such situations, low-power circuit designs are essential to improve the lifetime. This study focuses on circuits that comprise battery management in an IoT node and proposes new ultra-low power techniques to reduce the power consumption of the circuits in the battery management.

This thesis is organized into six chapters. Chapter 1 describes an introduction of this thesis. Chapter 2 presents an ultra-low power CMOS voltage reference that generates a constant standard voltage for the components in the battery management. Chapter 3 proposes a programming technique to obtain appropriate standard voltages for each circuit in the battery management. In Chapter 4, voltage detectors for RF energy harvesting and for battery monitoring are presented. In Chapter 5, an ultra-low power temperature sensor for small capacity batteries is proposed. Chapter 6 concludes the research with a summary of this dissertation.

In chapter 2, a 90 pA voltage reference for ultra-low power IoT node is presented. The voltage reference generates a temperature and V_{DD} independent constant voltage that becomes a standard voltage of the analog circuits in the battery management. The 90 pA voltage reference proposed in Chapter 2 is robust to the V_{DD} change compared with conventional low power voltage references. The simulated line sensitivity and the PSRR are 21μV/V and -70dB, respectively. The voltage reference is a fundamental circuit that is applied to a programmable voltage reference in Chapter 3, a voltage detector in Chapter 4, and a temperature-to-digital converter in Chapter 5.

In Chapter 3, an ultra-low power post-fabrication programming method for a voltage reference that realizes the programmability of the reference voltage (V_{REF1}) by users, is proposed with a theoretical analysis. A multiple voltage duplicator (MVD) is newly

proposed to eliminate a tradeoff between the temperature dependence of V_{REF1} and the power consumption of the programmable voltage reference. Also, a fine voltage subtraction (FVS) method is presented to achieve fine and linear programmability of V_{REF1}. The measurement results of the test chip fabricated in 250-nm CMOS process shows that the proposed programming method achieves a 6-bit, linear and monotonous programmability with the power consumption of sub-1nA and the temperature coefficient of 15.2μV/°C. The programming method is applied to a voltage detector in Chapter 4 which realizes programmability of the detection voltage by users.

In Chapter 4, voltage detectors for RF energy harvesting and battery monitoring are presented. A voltage detector (VD) watches a node voltage and once the node voltage reaches a predefined voltage (V_{DETECT}), the VD generates a signal. The proposed VD assumed to be applied to RF energy harvesting is fabricated in 250-nm CMOS process. The measured VD achieves 248 pW, glitch-free operation that the VD does not generate a glitch even though the input and supply voltage for the VD is close to 0V. Moreover, the VD has a trimming method to realize the accurate voltage detection by using the MVD in Chapter 3. These advantages open the way to realize energy autonomous applications that operate with harvested RF energy. The VD for battery monitoring enables users to program the detection voltage of the VD. The programmability mitigates the cost of VDs originated from variations of batteries, users, or applications. The programmable VD is fabricated in 250-nm. The measurement results show 6-bit programmability of the detection voltage ranging from 902 mV to 4904mV with the resolution of 62.5 mV. The resolution covers the ±1% of the charging voltage of lithium ion battery while the detection range covers operation voltages of most batteries.

In Chapter 5, a new principle of temperature sensing based on a sub-threshold MOSFET operation at sub-thermal drain voltage is proposed. The proposed temperature sensor realizes an external-reference-free temperature-to-digital converter with on-chip proportional-to-absolute-temperature (PTAT) digital output. The temperature sensor achieves the lowest power consumption of 13nW at 0.8V among the published temperature sensors. The ultra-low power operation is useful to sense the states of small batteries which have small capacity and large cell resistance. It is implemented using op-amp-free current generators and relaxation oscillator based current-to-frequency converters using the voltage reference in Chapter 2 for ultra-low power operation.

Measurement results from 8 chips fabricated in a 180-nm CMOS process achieve 110mK resolution and -0.7/+1.3°C inaccuracy over a temperature range of -20°C to 80°C.

Chapter 6 gives conclusions of the thesis.

Acknowledgement

Finally, I could complete the thesis and Ph. D. course at the University of Tokyo. In the process of my research, sometimes I met with difficulties, but I could get over them thanks to a lot of support from many people. Then, I would like to express my gratitude to them.

At first, I would like to thank Professor Takayasu Sakurai for giving me an opportunity to receive the Ph. D. degree and providing an excellent environment to me throughout my research. In addition, his perspective on the entirety of the society and the future world inspired me to study harder. I would also like to acknowledge Professor Makoto Takamiya that he supported me writing and submitting paper and journals. His helpful suggestions improved the papers and journals to be more understandable and sophisticated. In the project of smart temperature sensing, Dr. A.K.M. Mahfuzul Islam and I worked together. The third year of the Ph. D course was the most exciting and unforgettable year that I concentrated on the project and tried to develop the low power temperature sensor. I really appreciate that Dr. Mahfuzul gave me the chance to start the project and had beneficial meetings frequently.

I would like to thank all members of Sakurai laboratory. Dr. Hiroshi Fuketa, Dr. Ryo Takahashi, and Dr. Shunta Iguchi created a good environment for students and researchers to work. Dr. Koutaro Miyazaki often invited me to eat outside like friends. I want to express him special gratitude. I could share the hardships in the Ph. D course with my colleges, Chung-Shiang Wu and Sungjun Lee. I am delighted that we were in the same year in the laboratory. I want to thank Mr. Jihoon Park. His unique personality brought an atmosphere of friendliness into the laboratory. I sincerely thank all secretaries in Sakurai laboratory. I can’t list all of the names, but I enjoyed the daily life with all members of Sakurai laboratory.

I would like to acknowledge Mr. Hiroki Morimura and Mr. Kenichi Matsunaga in NTT Device Innovation Center, NTT Corporation, for many technical discussions in the project of RF energy harvesting. I would also like to acknowledge Mr. Keiji Takeuchi in NTT Data Institute of Management Consulting, Inc. for giving me the opportunity to be a part of flesh and exciting works. Mr. Shunichi Kaeriyama contributed to my enjoyable internship in Renesas Electronics. His expert work and knowledge in power electronics inspired me to improve my engineering skills.

VLSI fabrications in the research were supported by to VLSI Design and Education Center (VDEC), the University of Tokyo.

Finally, I would like to express my greatest gratitude to my family. Without their understanding and support, I could not complete the research in this three years. I hope they stay well forever.

Teruki Someya

Table of Contents

Chapter 1: Introduction

1.1. Background

The internet of things (IoT) is creating a new world where objects are connected to the internet, and we can collect much information from edge nodes easily. The IoT has an unrevealed possibility that makes our lives much more convenient and efficient.

Prolonging lifetime of IoT node is a key issue to be solved in the IoT. In many IoT applications, the performance and quality are largely dependent upon the number of the nodes in a network. The short lifetime of edge nodes increases the cost of replacement and reduces the quality and reliability of the application. On the other hand, some applications including wearable and implantable devices prefer small battery due to the limitation of the size or weight. For example, a millimeter-scale IoT node [1.1] employed a millimeter-scale rechargeable thin film battery [1.2] to pursue the extremely small node size. An IoT node with such a small battery is required to operate at ultra-low power consumption because the energy in the battery is restricted. For example, assume the real-time operation of an IoT node with the battery [1.2] for 24 hours without charging process, the allowable average current of the node is limited to 20μA. Therefore, the ultra-low power operation of the IoT nodes is indispensable to expand the IoT applications with small capacity battery.

1.2. Battery management in IoT node

Although an IoT node is composed of many functions such as sensing, processing, and communication, this thesis focuses on components of a battery management and shows the strategies to reduce the power consumption of them. Fig. 1.1 shows a target battery management system for an IoT node. The target battery is a 2nd battery that has a small capacity (< 1mAh). The Voltage generator supplies standard voltages to other circuits in the battery management. Using the standard voltages, the Power module, the Protection, and the State of battery works appropriately. The power module mainly works as a charger that converts external electrical energy into the battery. Since the lifetime of lithium-ion battery is sensitive to the charging characteristics including charging voltage and charging current [1.3], the Power module must charge the battery properly and safely. The Protection is indispensable component in the battery management for the safety. The protection watches the battery voltage, battery current or battery temperature to ensure

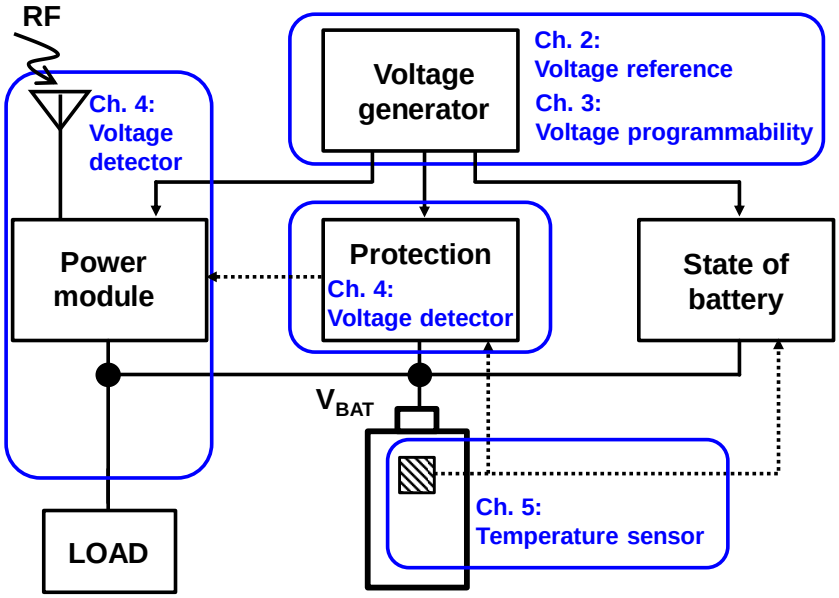


Fig.1.1 Block diagram of target battery management.

that the battery never operates outside of the safe operating area [1.4]. The State of battery estimates the battery states such as state of charge (SoC), state of health (SoH), and state of power (SoP). For the accurate estimation, some parameters are monitored during the battery operation. The temperature sensor is essential because the states of batteries are functions of the heat. Also, the safe operating area where battery can operate safely involves the temperature range. Therefore, the temperature measured by the temperature sensor is sent to the Protection and the State of battery.

This thesis presents some key circuits that are related to the functions of the battery management shown in Fig. 1.1. The point is to reduce the power consumption of the circuits to negligibly small compared to the energy storage in the battery. This section gives summaries of these circuits in terms of the features and functions in the battery management.

1.2.1. Voltage Generator

The components in the battery management shown in Fig. 1.1 require proper standard voltage (V_{REF}) for their operation. For example, the charger in the Power module refers the voltage to realize a constant current for battery charging [1.19]. A voltage detector in the Protection also uses V_{REF} to achieve the voltage detection by comparing V_{REF} and the input battery voltage as shown in Fig. 1.2. The voltages must be constant and robust

against the change of ambient environment including the temperature and the supply voltage (V_{DD}). Also, the required standard voltages are different according to the applications. The two main functions of the Voltage generator are (i) to generate a constant voltage that is robust against the temperature and V_{DD}, and (ii) to convert the V_{REF} into suitable voltages for other circuits in the battery management without the deterioration of the robustness. Chapter 2 shows a 90 pA voltage reference that generates a temperature/V_{DD}-independent standard voltage (V_{REF}). A typical voltage reference is based on Bandgap voltage reference (BGR) that achieves low temperature coefficient with little process variations of 1% [1.5-1.7]. The drawbacks include the implementation of large resistors which cost large areas, a relatively high V_{DD} (> 1V) that limits the V_{DD} scaling, relatively large power consumption over 10nW ([1.5-1.7]). To challenge these issues, some research proposed voltage references utilizing the threshold voltage of MOSFET for generating V_{REF}. This type of voltage reference is called V_{TH} based voltage reference in this chapter. Among them, V_{TH} based voltage reference presented in [1.8] removes the high resistors and achieves ultra-low power (< 10 pW), low voltage (=0.5V) operation. The challenges of the V_{TH} based voltage reference [1.8] are (1) to improve the V_{DD} sensitivity in V_{REF}, (2) to achieve higher V_{REF}, and (3) to mitigate the process dependence. The V_{DD} dependence occurs due to the Drain-Induced Barrier Lowering (DIBL) that decreases V_{TH} of MOSFET according to the rise of V_{DD}. Since V_{REF} is based on V_{TH}, the DIBL effect causes the V_{DD} dependence of V_{REF}. The low V_{REF} referred as issue (2) is inherent to V_{TH} based voltage reference implemented in CMOS process because the voltage reference utilizes V_{TH} of CMOS that is less than 0.5V typically [1.9] for generating V_{REF}. To challenge issues (1) and (2), Chapter 2 introduces a V_{DD}-independent V_{DD}-Regulated Voltage Reference (VRVR). The VRVR achieves the reduction of the line sensitivity to 21μV/V while the power consumption is 90pA and the temperature coefficient is 15μV/°C in the temperature range of 0 °C to 100 °C. Also, the proposed VRVR can be extended to a derivation that doubles V_{REF} in order to overcome the inherent low voltage V_{REF} of V_{TH} based voltage reference.

In contrast to BGR, V_{TH} voltage reference shows process variability since V_{TH} of MOSFET differs from each fabrication technology (issue (3)). The process dependence makes it difficult to supply proper and suitable V_{REF} to the components in Fig. 1.1. Chapter 3 proposes a programming method that realizes programmability of V_{REF} with

little power loss (≈ 1nA). The programmability is realized by the combination of a proposed multiple voltage duplicator (MVD) and a proposed fine-voltage subtraction (FVS) method. The programmability is beneficial to generate various standard voltages (= V_{REF1}) that are required to the various circuits. The programmable voltage reference is a vital component that contribute to the ultra-low power battery management shown in Fig. 1.1. In Chapter 3, the measurement results of test chips fabricated in 250-nm CMOS process show the 6-bit programmability of V_{REF1} with small power overhead of 675 pA.

By the combination of the VRVR and the programming method, the Voltage generator in Fig. 1.1 supplies various standard voltages to other components in the battery management.

1.2.2. Voltage Detector for Battery Monitoring

Battery voltage (V_{BAT}) monitoring is also a critical element in the battery management. The overcharge or over-discharge make severe effects on a battery's life. The measured results [1.3] show that by setting the maximum voltage of a lithium-ion battery at 4.25 V (=1.2% over than typical maximum voltage of lithium-ion battery), the degradation rate of the battery's capacity at 500 cycles becomes double compared with a typical case. Furthermore, the overcharged status also causes severe safety hazards [1.10]. To ensure the reliability and safety of the battery, the voltage monitoring is achieved with voltage detectors (VDs) in the Protection. The VD is connected to the battery and the output of the VD is triggered when the battery voltage (V_{BAT}) arrives at the pre-defined voltage (V_{DETECT}). If the VD is designed for the overcharging protection, the V_{DETECT} is set to the maximum voltage of the battery. Once the VD detects the overcharging, the output stage of the VD changes, which enables the system to disconnect the battery from the charger. As previously mentioned, the accuracy of the VD is important because it is relevant to the life-time and reliability of the battery. The simple architecture of the VD is shown in Fig. 1.2. The voltage detection is realized by comparing a divided V_{BAT} (V_{IN1}) and a reference voltage (V_{REF}). A proper V_{IN1} or V_{REF} must be obtained to achieve appropriate V_{DETECT}. On the other hand, the "appropriate V_{DETECT}" differs from applications, batteries, or events that the VD detects, which requires the costly special trimming. Moreover, sometimes multiple V_{DETECT}'s need to be detected (e.g., $6V_{DETECT}$ in [1.20]), which increases the number of the VDs.

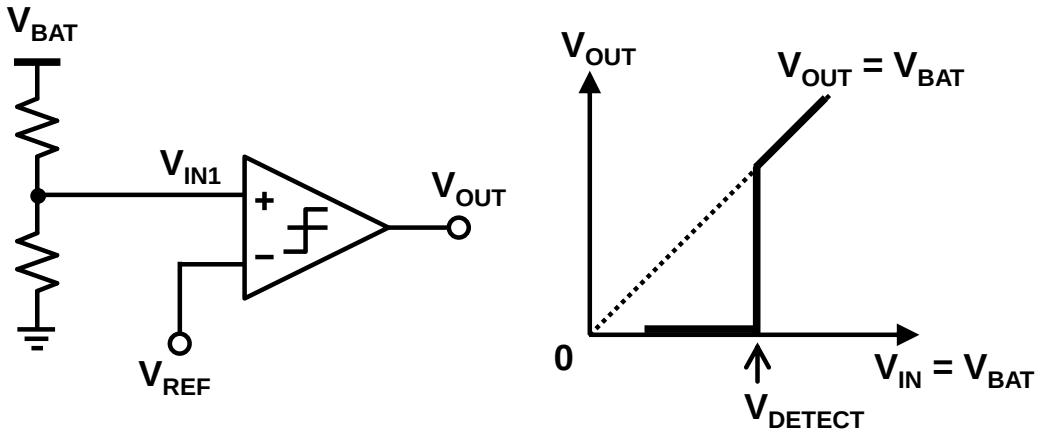


Fig.1.2 Block diagram of a simple voltage detector.

To address these issues, a programmable voltage detector (PVD) that users can program V_{DETECT} freely, is proposed in Chapter 4. The proposed PVD enables the wide V_{DETECT} programming in the range from 902 mV to 4904 mV that covers the operating voltages of most battery cells. The resolution of the programmed V_{DETECT} is 62.5 mV, which is finer voltage than the ±1% of the maximum operating voltage for typical lithium-ion batteries (=±42 mV). The programmability of V_{DETECT} enables the filed programming by end-users that saves the cost of special trimming in the battery management system. The proposed PVD fabricated in 5V, 250-nm CMOS process shows the measured power consumption of 1.3 nA at 5V and the temperature coefficient of 0.33mV/°C in -20°C to 60°C.

1.2.3. Voltage Detector for RF Energy Harvesting

Energy harvesting is an attractive technique to extend the battery lifetime and even, has a possibility to realize energy autonomous applications. Up to the present, many ambient energy sources and harvesting methods are presented. Among them, RF energy harvesting is one of the harvesting techniques that collects ambient RF signal and converts it into electronic energy. In the battery management shown in Fig. 1.1, an RF energy harvesting is assumed to be incorporated in the Power module to save the battery energy. Fig. 1.3 shows a typical RF energy harvesting circuit. The system is composed of an antenna that harvests RF energy, a charge pump that rectifies the RF signal into DC voltage and boost up the voltage, the output switch, and a VD. The VD monitors storage capacitor to detect the charging completion. Once the voltage of the storage capacitor gets

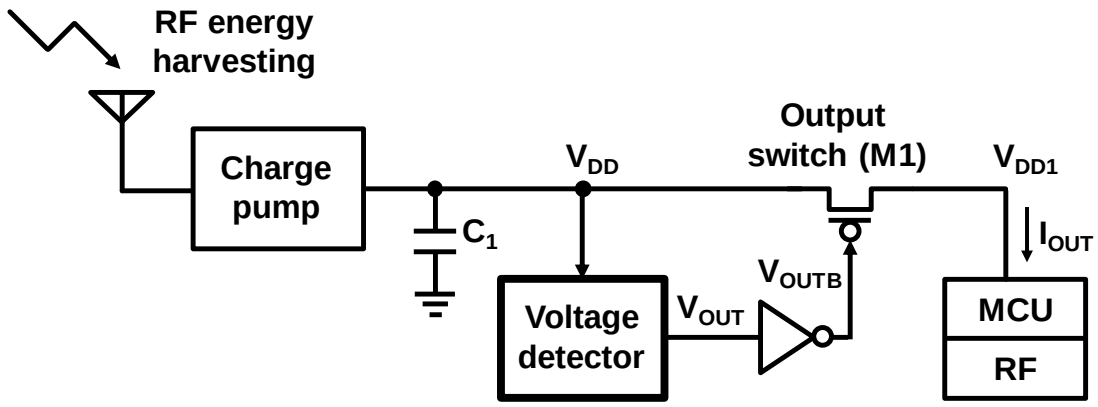


Fig.1.3 Circuit schematic of RF energy harvesting system.

to a predefined voltage V_{DETECT}, the load circuits start the operation. The VD is required to be much lower consumption than the harvested energy. This is challenging because the output power of the charge pump is sometimes very small (e.g., 1 nA [1.11] or 1 μA [1.12]). Moreover, the VD is forced to operate at ultra-low supply voltage when the power of the input signal is small. Especially, at the start of the harvesting, the voltage of C_1 is zero. Even in that situation, VD must function normally. Otherwise the VD mistakenly turns the output switch on and spoils the energy harvesting. Voltage detectors in the market consumes over 20 nA [1.13-1.15] and have the minimum operation voltage (e.g., 0.9 V [1.13]). These restrictions prevent the VDs from being applied to the RF energy harvesting.

In Chapter 4, a VD for RF energy harvesting is presented. The proposed VD fabricated in 250-nm CMOS process realizes an ultra-low power consumption, (248pW at 1V), a glitch-free operation that removes instability of the output of the VD when the input and supply voltage for VD is near 0V. Furthermore, the VD has a V_{DETECT} programmability that improves the accuracy of the V_{DETECT} with the resolution of less than 49 mV.

The VD opens the way to achieve an energy autonomous IoT node with RF energy harvesting.

1.2.4. Temperature Sensing

Temperature of battery is critical information to ensure the reliability of the battery in an IoT node. In the battery management shown in Fig. 1.1, the measured temperature of the battery is shared with the Protection and the State of battery. Since the safety of a battery is affected by the battery temperature, an operating temperature range is

determined for the battery (e.g., -20 °C to 70 °C [1.2]). The Protection ensures that the battery does not operate outside the safe operating area. The information of the temperature is also important for the State of battery. The temperature affects the characteristics of the battery, such as the cell impedance, the self-discharge current, and the deterioration rate of the capacity. Therefore, the temperature is one of the essential parameters to estimate the battery's state precisely [1.16-1.18]. In Chapter 5, a new principle of temperature sensing based on a sub-threshold MOSFET operation at sub-thermal drain voltage is proposed. The proposed external-reference-free temperature-to-digital converter with on-chip proportional-to-absolute-temperature (PTAT) digital output achieves the low power consumption of 13nW at 0.8V. Measurement results from 8 chips fabricated in a 180-nm CMOS process achieve 110mK resolution and -0.7/+1.3°C inaccuracy over a temperature range of -20°C to 80°C which covers active temperature range for batteries.

1.3. Thesis organization

The dissertation is organized as follows. Chapter 1 described the background of the research. Chapter 2 presents a 90 pA voltage reference with the robustness against V_{DD} and the temperature changes. Chapter 3 proposes low power V_{REF}-programming method that is used in voltage detectors in the thesis. Chapter 4 presents a voltage detector for RF energy harvesting and a voltage detector for battery monitoring. Chapter 5 shows an ultra-low power temperature sensor. Chapter 6 gives conclusions of the thesis.

References

[1.1] Y. Chen, N. Chiotellis, L. Chuo, C. Pfeiffer, Y. Shi, R. Dreslinski, A. Grbic, T. Mudge, D. Wentzloff, D. Blaauw, and H. Kim, "Energy-Autonomous Wireless Communication for Millimeter-Scale Internet-of-Things Sensor Nodes," *IEEE Journal on Selected Areas in Communications*, vol. 34, no. 12, pp. 3962–3977, 2016.

[1.2] CBC005, Cymbet corporation

[1.3] S. Choi and H. Lim, "Factors that affect cycle-life and possible degradation mechanisms of a Li-ion cell based on LiCoO2," *Journal of Power Sources*, vol. 111, pp. 130–136, 2002.

[1.4] L. Lu, X. Han, J. Li, J. Hua and M. Ouyang, "A review on the key issues for lithium-ion battery management in electric vehicles," *Journal of Power Sources*, vol. 226, pp. 272–288, 2013.

[1.5] Y. Osaki , T. Hirose , N. Kuroki and M. Numa "1.2 V supply, 100 nW, 1.09 V bandgap and 0.7 V supply, 52.5 nW, 0.55 V subbandgap referencecircuits for nanowatt CMOS LSIs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, 2013.

[1.6] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff and B. H. Calhoun "A 32 nW bandgap reference voltage operational from 0.5 V supply for ultra-low power systems," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 94–95, 2015.

[1.7] K. K. Lee, T. S. Lande and P. D. Häfliger, "A Sub-µW Bandgap Reference Circuit With an Inherent Curvature-Compensation Property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 1–9, 2015.

[1.8] M. Seok, G. Kim, D. Blaauw and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, 2012.

[1.9] K. N. Muriithi, T. Nakura and K. Asada, "Numerical and theoretical analysis on voltage and time domain dynamic range of scaled CMOS circuits," in *17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*, pp. 282–285, 2014.

[1.10] L. Xiao, X. Ai, Y. Cao and H. Yang, “Electrochemical behavior of biphenyl as polymerizable additive for overcharge protection of lithium ion batteries,” *Electrochim. Acta*, vol. 49, no. 24, pp. 4189–4196, 2004.

[1.11] S. Oh and D. Wentzloff, “A -32dBm Sensitivity RF Power Harvester in 130nm CMOS,” in *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 483–486, 2012.

[1.12] R. Shigeta, T. Sasaki, D. M. Quan, Y. Kawahara, R. J. Vyas, M. M. Tentzeris, and T. Asami, “Ambient RF Energy Harvesting Sensor Device With Capacitor-Leakage-Aware Duty Cycle Control,” *IEEE Sensors J.*, vol. 13, no. 8, pp. 2973–2983, 2013.

[1.13] Datasheet of TPS3839, Texas Instruments.

[1.14] Datasheet of S-1000, Seiko Instruments Inc.

[1.15] Datasheet of AP4400A, Asahi Kasei Microdevices Corporation.

[1.16] V. Pop, H. Bergveld, P. Notten, and P. Regtien, "State-of-the-art of battery state-of-charge determination," *Measurement Science and Technology*, vol. 16, pp. R93–R110, 2005.

[1.17] Y. Xing, W. He, M. Pecht, and K. Leung Tsui “State of charge estimation of lithium-ion batteries using the open-circuit voltage at various ambient temperatures,” *Applied Energy*, vol. 113 pp. 106–115, 2014.

[1.18] G. Plett., “Extended Kalman filtering for battery management systems of LiPB-based HEV battery packs Part 2. Modeling and identification,” *Journal of Power Sources*, vol. 134, pp. 262–276, 2004.

[1.19] Data sheet of LTC4054L-4.2, Linear Technology.

[1.20] Datasheet of BQ25504, Texas Instruments.

Chapter 2: Sub-threshold CMOS Voltage Reference

2.1. Introduction

Voltage reference supplies a constant voltage (V_{REF}) that is independent of temperature changes, supply voltage (V_{DD}) variations, load current, and so on. In a sensor node, V_{REF} is applied to many circuits including analog to digital converter (ADC), digital to analog converter, voltage regulator, and precise control systems. In the battery management system shown in Fig. 1.1, V_{REF} generated by a voltage reference is referred as a standard voltage for some circuits. For example, the charger refers V_{REF} to generate a constant current for charging the battery [2.14]. The voltage detector detects the battery overcharge by comparing the battery voltage to a constant voltage based on V_{REF}. Since V_{REF} is a standard voltage in the analog circuits and control systems, to achieve the robustness and accuracy of the voltage reference is required to ensure the reliability of the circuits and systems. Recently, demands for low power circuits and systems are increasing with the spread of the Internet of Things (IoT). In such applications, the power consumption of the voltage reference should be reduced without the deterioration of the performance and robustness.

Bandgap voltage reference (BGR) is a common voltage reference in integrated circuits. Since the first commercially available BGR was presented, the performance has been improved. Recently, several low power BGRs were presented [2.1-2.3], on the other hand, their power consumptions are still over 1 nW. Apart from BGR, voltage reference utilizing threshold voltage (V_{TH}) of MOSFETs for generating a reference voltage (V_{REF}) were presented [2.4-2.11]. Among the V_{TH} based voltage references, [2.4] presented a voltage reference that is composed of only two transistors (2T) operating in the sub-threshold region as shown in Fig. 2.1. [2.4] reported the power consumption can be reduced to 2.2 pW with the temperature coefficient (TC) of 19.4 ppm/°C (The definition of TC is described in the Appendix at the end of this chapter). Although it is ultra-low power and has a robustness against the temperature changes, it is vulnerable to the V_{DD} change or fluctuation. Since the drain voltage of M_2 is directly connected to the supply line (=V_{DD}), M_2 suffers from V_{TH} variation due to the drain induced barrier lowering (DIBL). Then, V_{REF} that is a function of V_{TH} becomes sensitive to V_{DD}. The LS of the voltage reference

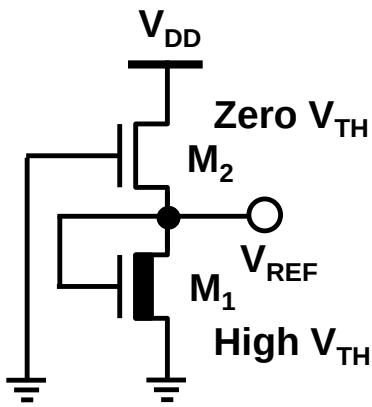


Fig. 2.1 Circuit schematic of the 2-tranistors voltage reference [2.4].

must be minimized as it directly affects PSRR of other circuits connected to the voltage reference [2.12].

In this chapter, a new V_{TH} based voltage reference is proposed. The feature of the voltage reference is an ultra-low power consumption of 90 pA, the line sensitivity (the definition of the line sensitivity in this thesis is described in Appendix) of 21μV/V and PSRR of -70dB at 100Hz.

2.2. V_{DD} Regulated Voltage Reference (VRVR)

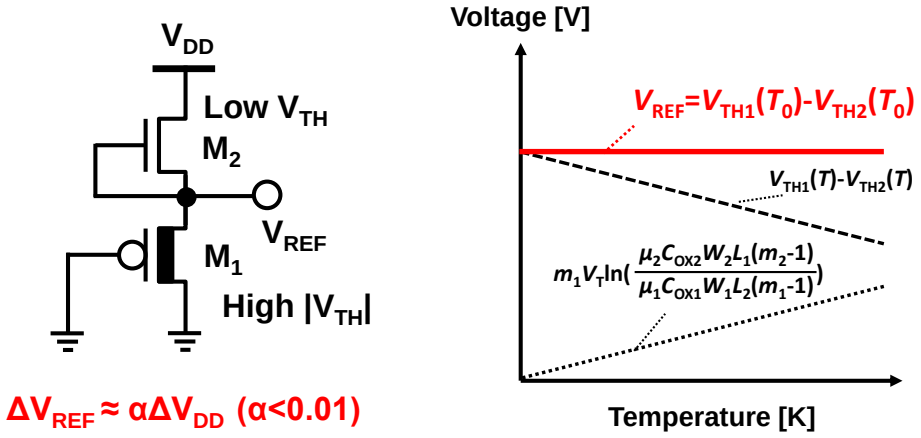
Fig. 2.2 (a) shows the core part of the proposed temperature/V_{DD}-independent voltage reference. A high $|V_{TH}|$ M_1 and a low V_{TH} M_2 composes 2-transistors voltage reference that concept of generating temperature-independent V_{REF} is similar to [2.4]. First, the theoretical V_{REF} is introduced. The currents of M_1 and M_2 are introduced as follows [2.5]:

$$I_1 = \mu_1 C_{OX1} \frac{W_1}{L_1} V_T^{\,2} \exp\left(\frac{V_{REF} - |V_{TH1}|}{m_1 V_T}\right), \tag{2.1}$$

$$I_2 = \mu_2 C_{OX2} \frac{W_2}{L_2} V_T^{\,2} \exp\left(\frac{-V_{TH2}}{m_2 V_T}\right), \tag{2.2}$$

where μ_1 (μ_2) is the mobility of M_1 (M_2), C_{OX1} (C_{OX2}) is the unit gate capacitance of M_1 (M_2), V_T is the thermal voltage, m_1 (m_2) is the sub-threshold swing parameter of M_1 (M_2), W_1 (W_2) is the gate width of M_1 (M_2), L_1 (L_2) is the gate length of M_1 (M_2), and V_{TH1} (V_{TH2}) is the threshold voltage of M_1 (M_2). From (2.1) and (2.2), V_{REF} is introduced as follows:

$$V_{REF} = (|V_{TH1}| - V_{TH2}) + m_1 V_T \ln\left(\frac{\mu_2 C_{OX2} W_2 L_1 (m_2 - 1)}{\mu_1 C_{OX1} W_1 L_2 (m_1 - 1)}\right). \tag{2.3}$$



(a) (b)

Fig. 2.2 (a) Circuit schematic of the core 2-tranistors voltage reference in the proposed voltage reference and (b) the concept of temperature-independent V_{REF} generation.

The V_{TH} of MOSFET is expressed as [2.13]

$$V_{TH} = V_{TH}(T_R) - k_1(T - T_R), \tag{2.4}$$

where k_1 is a temperature coefficient for V_{TH} and T_R is a reference temperature. The temperature characteristics of each term and V_{REF} are shown in Fig 2.2 (b). In (2.3), the first term and second term show opposite characteristics against the temperature, that is, one shows complementary to the absolute temperature (CTAT) characteristic while the other one shows the proportional to the absolute temperature (PTAT) characteristic. By taking the proper size ratio of M_1 and M_2, V_{REF} is expressed as follows:

$$V_{REF} = |V_{TH1}(T_0)| - V_{TH2}(T_0) \tag{2.5}$$

where $V_{TH1}(T_0)$ and $V_{TH2}(T_0)$ are the V_{TH} of M_1 and M_2 at 0 K. Eq.(2.5) shows that V_{REF} is independent of the temperature or V_{DD}. The problem is, however, $V_{TH2}(T_0)$ dependent on V_{DD} due to the DIBL effect, which deteriorates the LS of α (≈0.5%/V). The problem is common among the voltage references based on the 2-transistor voltage reference.

To solve the issue, a V_{DD} Regulated Voltage Reference (VRVR) is proposed. Fig. 2.3 shows the circuit schematic of the proposed VRVR. M_1 and M_2 compose the core of the voltage reference which outputs temperature-independent V_{REF} similar to (2.5). The point is a voltage regulator keeps the drain node of M_2 at a constant voltage that has small line sensitivity of 2α. The voltage regulator is achieved with five transistors M_3, M_4, M_5, M_6, and M_7. M_3 and M_4 composes 2-transistor voltage reference as similar to Fig. 2.2 (a).

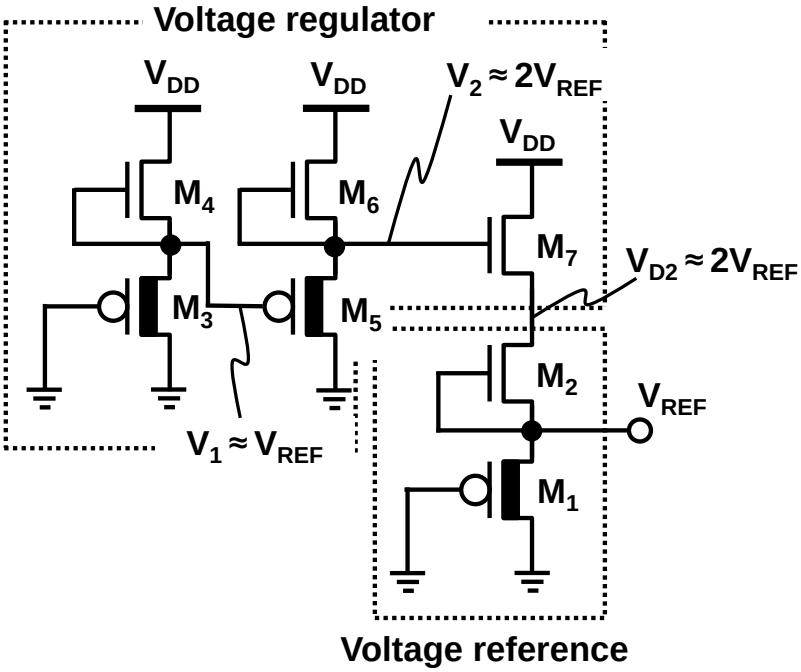


Fig. 2.3 Circuit schematic of the proposed V_{DD}-regulated voltage reference (VRVR).

M_5 and M_6 are also 2-transistor voltage reference that generates $2V_{REF}$. The current I_3 (=I_4) and I_5 (=I_6) are reduced to 30% of I_1 (=I_2) to save the current. The voltage level of V_2 (= $2V_{REF}$) is copied to V_{D2}, since V_{GS} of M_2 and M_7 are 0V. This is the reason why V_{D2} is regulated to a constant voltage $2V_{REF}$. Owing to the regulation, the line sensitivity of V_{REF} (=$\Delta V_{REF}/\Delta V_{DD}$) becomes $2\alpha^2$ while that of 2-transistor voltage reference without the regulator is α. The validity of the VRVR is discussed with the SPICE simulation in the next section.

2.3. Simulation Results

SPICE simulations in 250-nm CMOS process are conducted to confirm the performance of the proposed VRVR. Fig. 2.4 shows the temperature characteristics of the proposed VRVR. In the temperature range of 0°C to 100°C, the temperature coefficient shows 15μV/°C (=34 ppm/°C, normalized at V_{REF} of 25°C). The result shows that the TC is sufficiently small that can be competitive to [2.4]. Fig. 2.5 shows the simulated V_{DD} dependence of V_{REF}. To compare the characteristics, 2-transistor voltage reference (labeled as conv. VR) in Fig. 2.2 (a) is also implemented and simulated. The simulated line sensitivity of the VRVR is 21μV/V, which is 1% of that of the conventional VR (=1.9mV/V). Fig. 2.6 shows the power supply rejection ratio (PSRR) of the two voltage

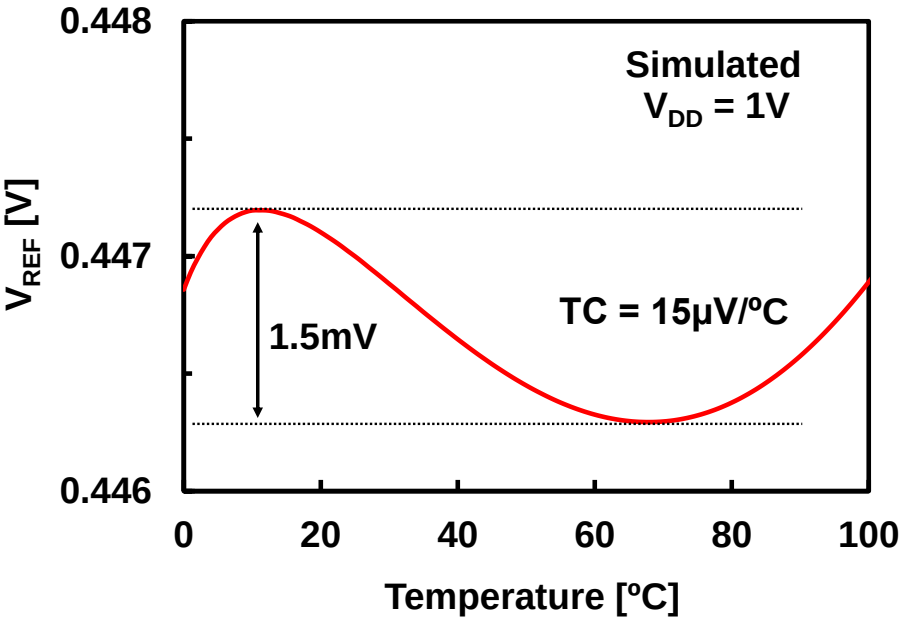


Fig. 2.4 Simulated temperature characteristics of the proposed VRVR.

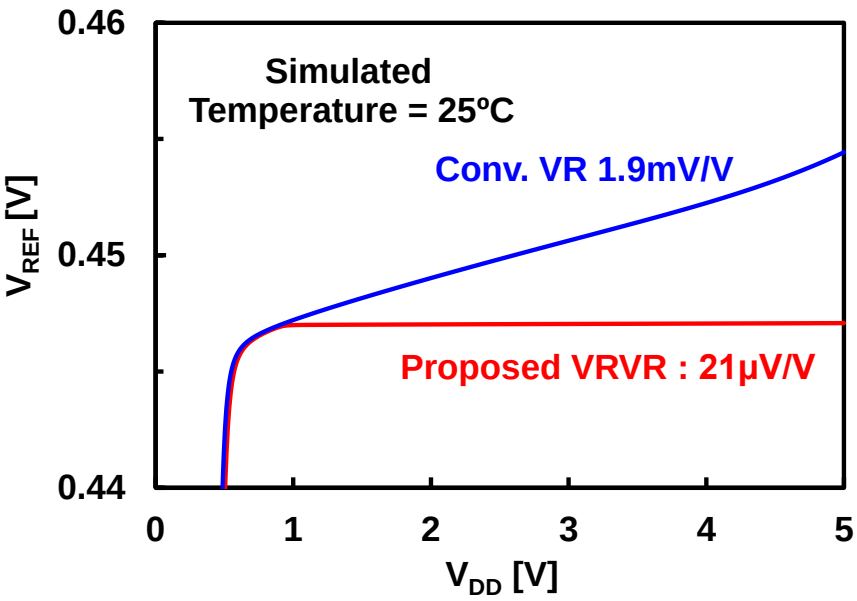


Fig. 2.5 Simulated V_{DD} dependence of the VRVR and the conventional voltage reference.

references. Thanks to the proposed regulator, the PSRR is improved to -70dB at 100 Hz while that of the conventional VR is -48dB. Fig. 2.7 shows the power consumption of the voltage references. The total power of the voltage reference is 90pA including the power overhead of the regulator (=30pA). Fig. 2.8 summarizes the performance of the proposed

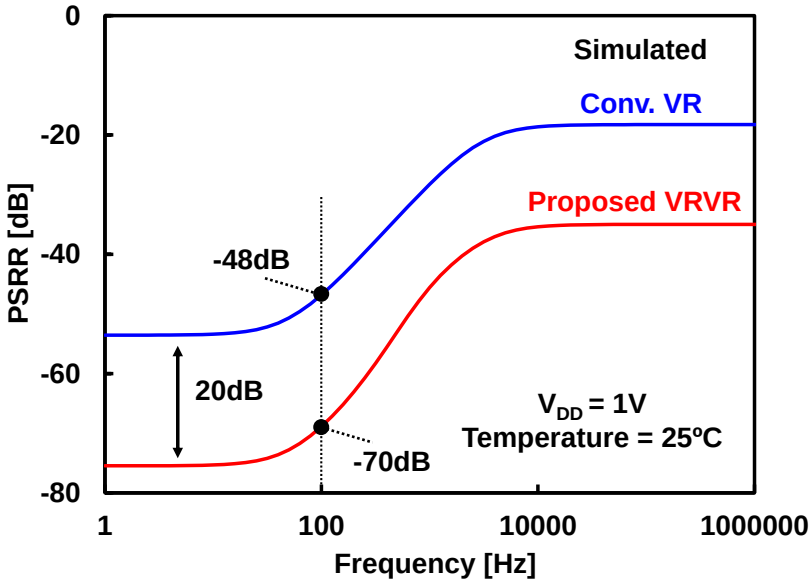


Fig. 2.6 Simulated PSRR of the VRVR and the conventional voltage reference.

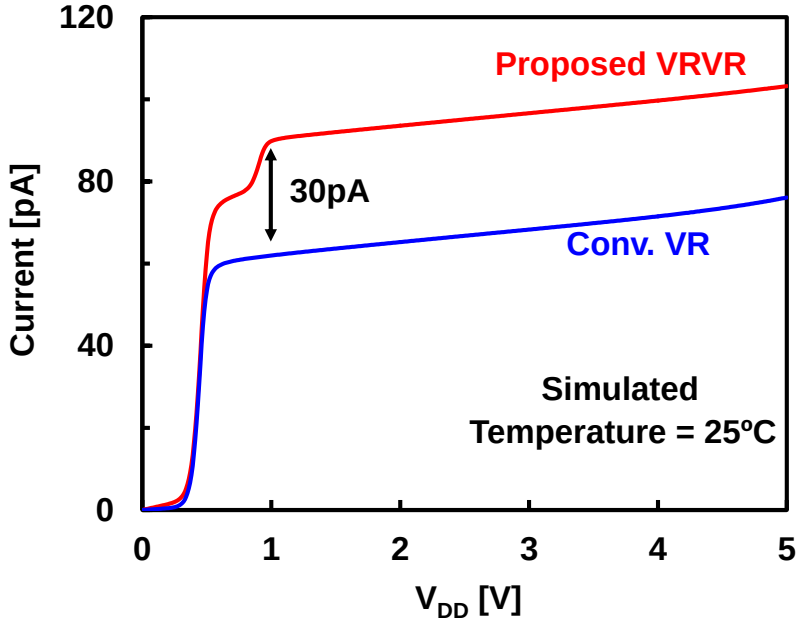


Fig. 2.7 Simulated power consumption of the VRVR and the conventional voltage reference.

VRVR, re-implemented [2.4] and other state-of-the-art CMOS voltage references. Due to the voltage regulation technique, the proposed VR achieves the lowest LS of 0.0047%/V and -70dB at 100Hz.

Table 2.1 COMPARISON WITH PREVIOUS VOLTAGE REFERENCES

	This work (Simulated)	CICC'09 [2.4]	Re-implemented [2.4]	A-SSCC'17 [2.6]	ESSCIRC'17 [2.7]
Technology	250nm	130nm	250nm	180nm	65nm
V_{REF}	0.45V	0.175V	0.45V	1.17V	0.343V
Temperature range	0ºC to 100ºC	-20ºC to 80ºC	0ºC to 100ºC	0ºC to 170ºC	-40ºC to 60ºC
Supply voltage	1V-5V	0.5V-3.3V	0.7V-5V	1.8V-3.6V	0.4V to 1.2V
TC	33ppm/ºC	62ppm/ºC	N/A	64ppm/ºC	252ppm/ºC
Current	90pA at 1V (25ºC)	4.4pA at 0.5V (25ºC)	60pA at 0.7V (25ºC)	76pA at 1.8V (27ºC)	1.1pA at 0.4V (20ºC)
Line sensitivity	0.0047%/V	0.033%/V	0.19%/V	0.09%/V	0.47%/V
PSRR	-70dB @100Hz	-53dB* @100Hz	-48dB @100Hz	-38dB @100Hz	N/A

*With 0.8pF output capacitor

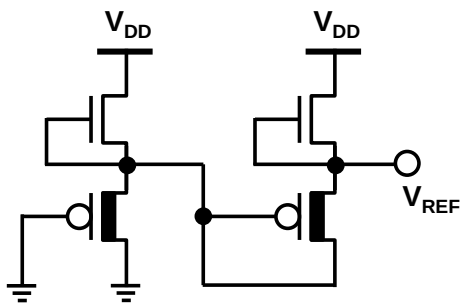


Fig. 2.8 Schematic of the 4-T voltage reference [2.4]. The pair of the transistors is modified.

2.4. Two-Stages V_{DD}-Regulated Voltage Reference

The output voltage of the V_{TH} based voltage reference tends to be lower voltage than that of BGR. In [2.4], as a variation of the 2-transistor (2-T) voltage reference, a 4-T voltage reference is proposed to achieve a higher output voltage. The schematic of the 4-T voltage reference is expressed in Fig. 2.8. The combination of the transistors is modified to the same one to the VRVR. By adding an offset to the source voltage of the 2-T voltage reference, the output of V_{REF} increases compared with the 2-T voltage reference. However, to double V_{REF}, the first stack must supply the sufficient current for the second stack, which is the increase in the power consumption of the 4-T voltage

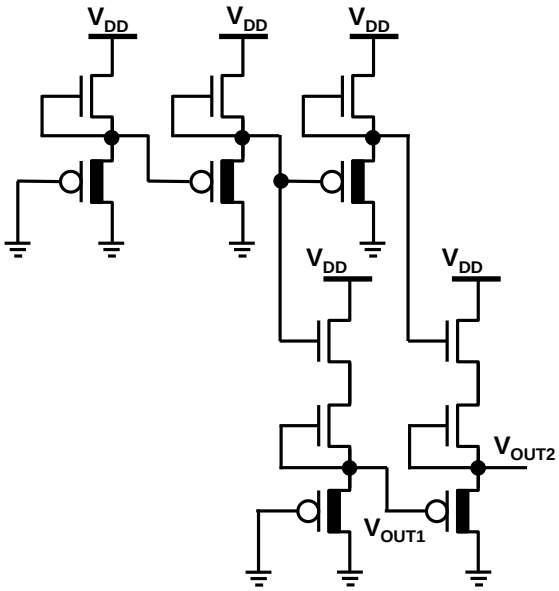


Fig. 2.9 Schematic of the two-stages VRVR

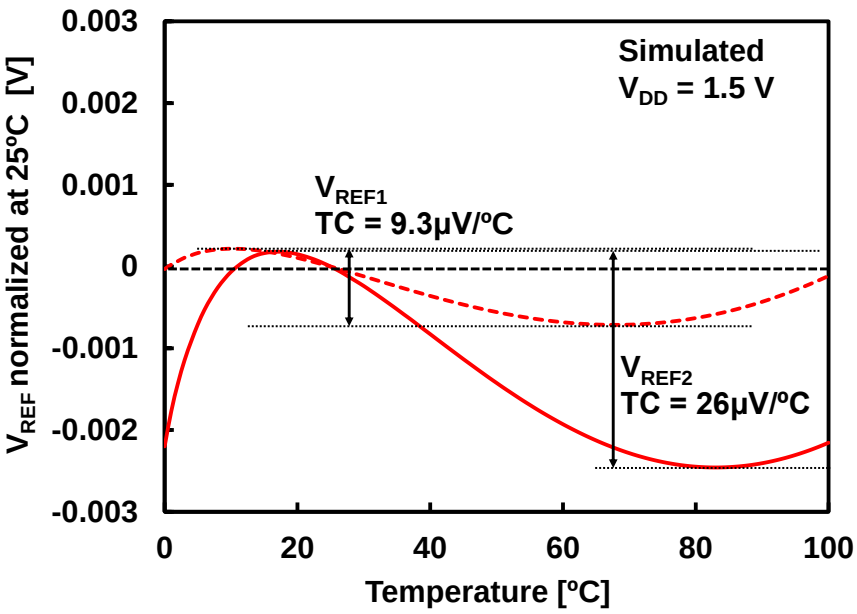


Fig. 2.10 Simulated temperature characteristics of V_{REF1} and V_{REF2} in the two-stages VRVR. The voltage is normalized at 25 ºC. V_{REF1} and V_{REF2} are corresponding to V_{OUT1} and V_{OUT2} in Fig. 2.11, respectively.

reference. To double V_{REF}, the proposed VRVR can be extended to a two-stages VRVR that doubles V_{REF}. Fig. 2.9 shows the schematic of the two-stages VRVR where V_{OUT2} is a double of V_{OUT1}. Fig. 2.10 and Fig. 2.11 show the temperature and V_{DD} characteristics of V_{OUT1} and V_{OUT2}, respectively. In the figures, V_{REF1} and V_{REF2} correspond with the reference voltages in V_{OUT1} and V_{OUT2}, severally. The temperature characteristic of V_{REF2}

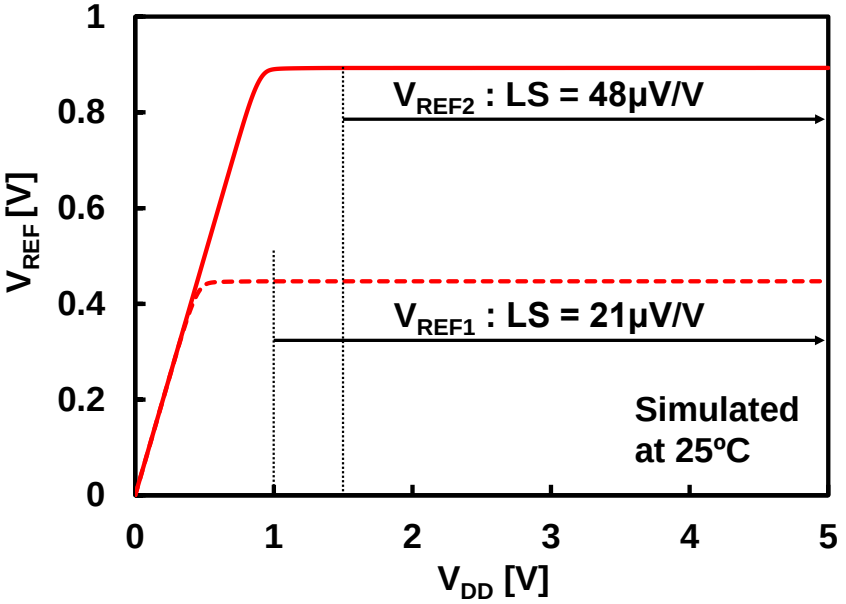


Fig. 2.11 Simulated V_{DD} dependence of V_{REF1} and V_{REF2} in the two-stages VRVR.

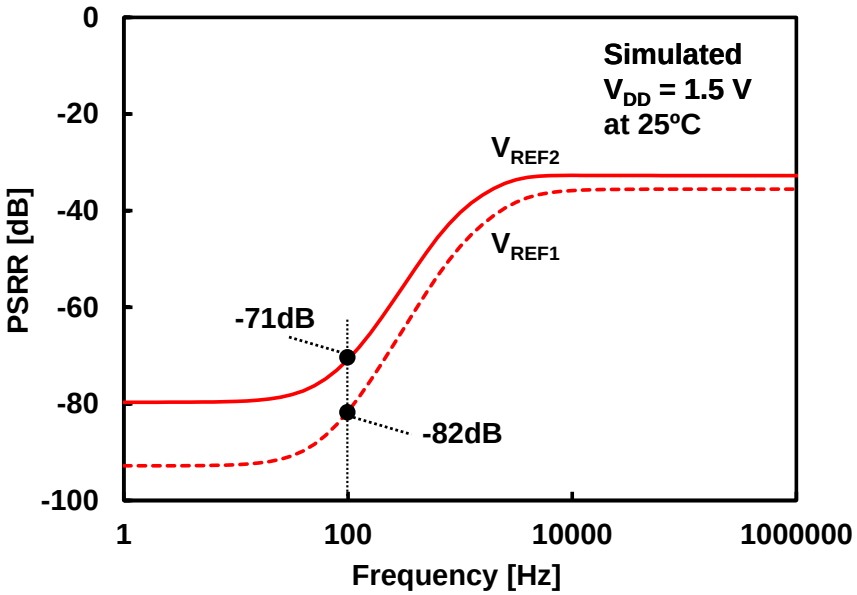


Fig. 2.12 Simulated PSRR of V_{REF1} and V_{REF2} in the two-stages VRVR.

is a competitive TC of 26 μV/ºC in Fig. 2.8. The line sensitivities of V_{REF1} and V_{REF2} are 21μV/V and 48μV/V, respectively. Though the line sensitivity of V_{REF2} is as twice as the line sensitivity of V_{REF1}, the line sensitivity of V_{REF2} is sufficiently small among the previous research shown in Table 2.1. Fig. 2.12 shows the PSRR of V_{REF1} and V_{REF2}, the both PSRRs at 100 Hz are suppressed to less than -70 dB. Fig. 2.13 shows the power consumption of the two-stages VRVR and the single stage VRVR. The power

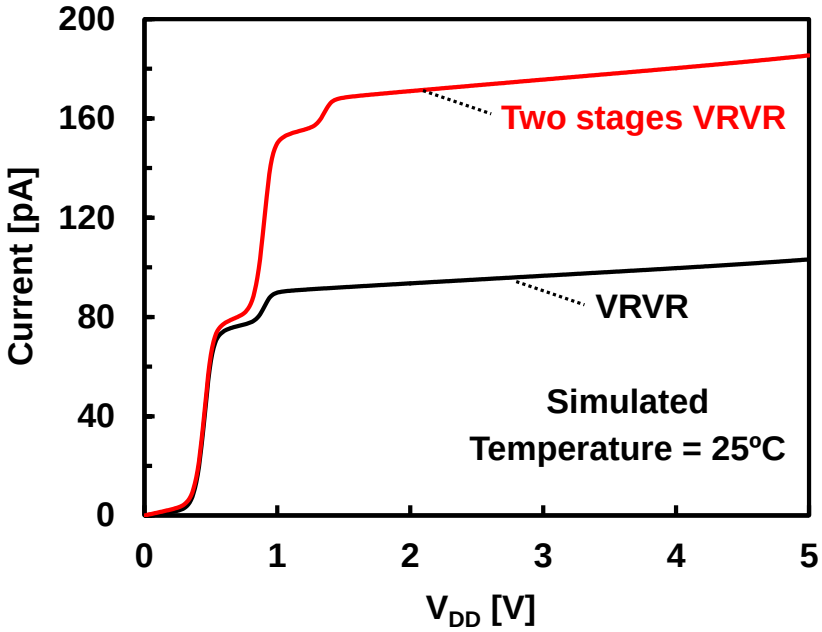


Fig. 2.13 Simulated power consumption of the two-stages VRVR.

consumption of the two-stages VRVR is 170 pA that is as twice as that of the VRVR. The overhead of the power loss originated from multi-stages scheme is the only 80 pA.

2.5. Summary

This chapter proposed a 90 pA, V_{DD}-independent voltage reference. The proposed V_{DD} regulated voltage reference (VRVR) improve the line sensitivity of the conventional 2-transistors voltage reference thanks to the proposed voltage regulator at the cost of only 30 pA. The simulation results show that the temperature coefficient in the temperature range of 0 °C to 100 °C is 20 μV/°C, the line sensitivity is 21 μV/V, the PSRR is -70 dB at 100 Hz, and the power consumption is 90 pA. The simulation results show that the proposed VRVR achieves both low-power and V_{DD}-independent operation. As a variation of the VRVR, a two stage VRVR is proposed. The two-stages VRVR doubles the output of the VRVR with little performance deteriorations. The two-stages method mitigates the issue that the output of the V_{TH} based voltage reference is smaller than that of BGR. The proposed VRVR is a fundamental circuit in the battery management shown in Fig. 1.1 in that V_{REF} is applied to almost all circuits in the battery management.

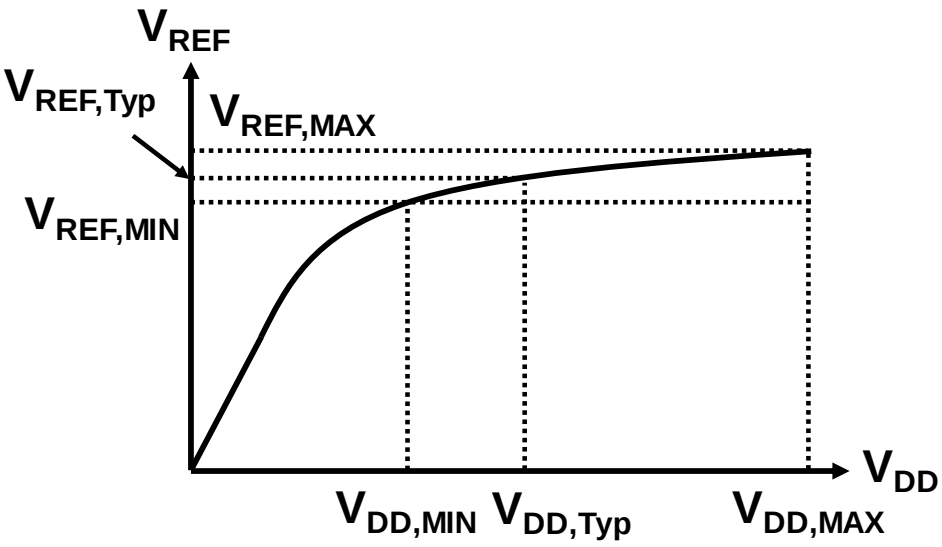


Fig. 2.14 Typical characteristics of an output of voltage reference against V_{DD}.

2.6. Appendix

2.6.1. Definition of Line Sensitivity

Fig. 2.14 shows a typical output voltage (V_{REF}) of a voltage reference against V_{DD}. In this thesis, the line sensitivity (LS) of the voltage reference is defined as follows:

$$LS = \frac{V_{\mathrm{REF,MAX}} - V_{\mathrm{REF,MIN}}}{V_{\mathrm{DD,MAX}} - V_{\mathrm{DD,MIN}}} \times 10^6 \quad [\mu \mathrm{V/V}] \tag{2.6}$$

or

$$LS = \frac{V_{\mathrm{REF,MAX}} - V_{\mathrm{REF,MIN}}}{V_{\mathrm{DD,MAX}} - V_{\mathrm{DD,MIN}}} \times \frac{1}{V_{\mathrm{REF,Typ}}} 10^2 \quad [\%/\mathrm{V}] \tag{2.7}$$

where $V_{DD,MAX}$ ($V_{DD,MIN}$) is maximum (minimum) operating voltage of the voltage reference, the $V_{REF,MAX}$ ($V_{REF,MIN}$) is V_{REF} corresponding to $V_{DD,MAX}$ ($V_{DD,MIN}$), $V_{DD,typ}$ is a typical V_{DD}, and $V_{REF,Typ}$ is V_{REF} corresponding to $V_{DD,typ}$. The difference between two definitions of LS shown in (2.6) and (2.7) is whether the LS is normalized at a typical V_{REF} or not. The definition (2.7) is normalized at a typical V_{REF} to shows relative impact of the VDD dependence. In Table 2.1, the definition (2.7) is used to express the LS of the voltage reference. In other sections, (2.6) is frequently used.

2.6.2. Definition of Temperature Coefficient

Fig. 2.15 shows a typical V_{REF} of a voltage reference against temperature. In this thesis, the temperature coefficient (TC) of the voltage reference is defined as follows:

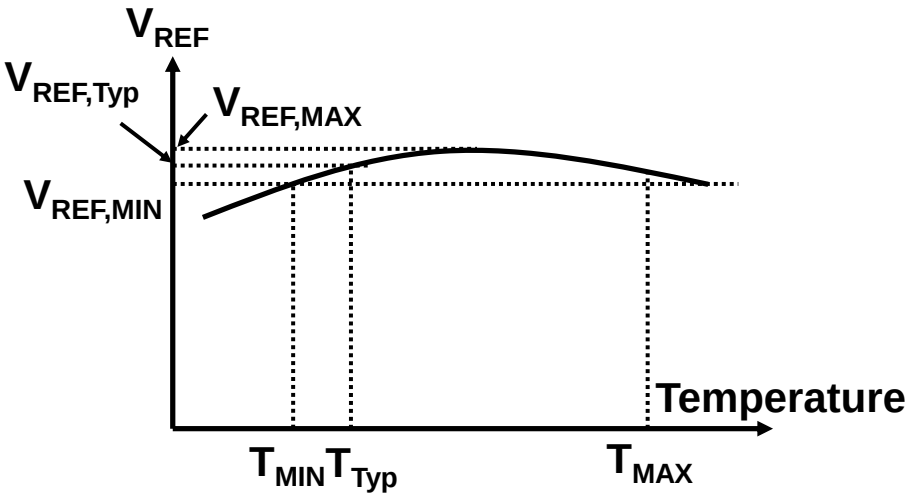


Fig. 2.15 Typical characteristics of an output of voltage reference against V_{DD}.

$$TC = \frac{V_{\text{REF,MAX}} - V_{\text{REF,MIN}}}{T_{\text{MAX}} - T_{\text{MIN}}} \qquad [\text{V}/^\circ\text{C}] \tag{2.8}$$

or

$$TC = \frac{V_{\text{REF,MAX}} - V_{\text{REF,MIN}}}{T_{\text{MAX}} - T_{\text{MIN}}} \times \frac{1}{V_{\text{REF,Typ}}} \times 10^6 \qquad [ppm/^\circ\text{C}] \tag{2.9}$$

where T_{MAX} (T_{MIN}) is the maximum (minimum) temperature of the temperature range of the voltage reference, $V_{REF,MAX}$ ($V_{REF,MIN}$) is the maximum (minimum) V_{REF} in the temperature range, and T_{Typ} is a typical temperature in the target application of the voltage reference. In the thesis, if "μV/°C" or "mV/°C" are used for the unit of TC, it follows the definition in (2.8), and if "ppm/°C" is used, the definition (2.9) is used to express the TC.

References

[2.1] Y. Ji, C. Jeon, H. Son, B. Kim, H. J. Park and J. Y. Sim, "A 9.3nW all-in-one bandgap voltage and current reference circuit," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 100–101, 2017.

[2.2] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff and B. H. Calhoun, "A 32nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 94–95, 2015.

[2.3] J. M. Lee et al., "A 29nW bandgap reference circuit," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 100–101, 2015.

[2.4] M. Seok, G. Kim, D. Sylvester and D. Blaauw, "A 0.5V 2.2pW 2-transistor voltage reference," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, 2009, pp. 577–580.

[2.5] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference, " *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, 2011.

[2.6] I. Lee, D. Sylvester and D. Blaauw, "Subthreshold voltage reference with nwell/psub diode leakage compensation for low-power high-temperature systems," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 265–268, 2017.

[2.7] H. Wang and P. P. Mercier, "A 420 fW self-regulated 3T voltage reference generator achieving 0.47%/V line regulation from 0.4-to-1.2 V," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, pp. 15–18, 2017.

[2.8] K. Ueno, T. Hirose, T. Asai and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, 2009.

[2.9] Y. Wang, Z. Zhu, J. Yao and Y. Yang, "A 0.45-V, 14.6-nW CMOS Subthreshold Voltage Reference With No Resistors and No BJTs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 7, pp. 621–625, 2015.

[2.10] I. Lee, D. Sylvester and D. Blaauw, "A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1443–1449, 2017.

[2.11] J. Lee and S. Cho, "A 210 nW 29.3 ppm/°C 0.7 V voltage reference with a temperature range of −50 to 130 °C in 0.13 µm CMOS," in *Symposium on VLSI Circuits - Digest of Technical Papers*, pp. 278–279, 2011.

[2.12] Z. Zhu, J. Hu and Y. Wang, "A 0.45 V, Nano-Watt 0.033% Line Sensitivity MOSFET-Only Sub-Threshold Voltage Reference With no Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 9, pp. 1370–1380, 2016.

[2.13] K. von Arnim, E. Borinski, P. Seegebrecht, H. Fiedler, R. Brederlow, R. Thewes, J. Bethold, C. Pacha, "Efficiency of body biasing in 90-nm CMOS for low-power digital circuits", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, pp. 1549–1559, Jul. 2005.

[2.14] Data sheet of LTC4054L-4.2, Linear Technology.

Chapter 3: Programmable Voltage Reference utilizing Multiple Voltage Duplicator and Fine Voltage Subtraction

3.1. Introduction

In Chapter 2, a 90 pA voltage reference that supplies a temperature/V_{DD}-independent constant voltage was proposed. The main topic in Chapter 2 was to generate robust V_{REF} for other circuits in the battery management shown in Fig. 1.1. However, sometimes the voltage level of V_{REF} is not preferable for an application. For example, a voltage detector for battery supervisor needs a reference voltage. By comparing a battery voltage and the reference voltage, the voltage detector detects several events such as charging completion, overcharge and over-discharge. On the other hand, the detection voltage level varies according to the batteries, which indicates V_{REF} must be an appropriate voltage level that suits to achieve the event detection. Another example is a battery charging. The charger refers V_{REF} to achieve a constant current for battery charging. However, the charging current is different from batteries. Then, V_{REF} should be tunable to cover various batteries. For these reasons, a post-fabrication programming technique to get a proper reference voltage is considered. Chapter 3 proposes a field programmable voltage reference that users can program the reference voltage freely. The fine programmability of the reference voltage also covers the process dependence of the voltage reference in Chapter 2. By the programming, the variation of V_{REF} among fabrication technologies is mitigated and a sole standard voltage is achieved. The key techniques are a multiple voltage duplicator (MVD) and a fine subtraction voltage (FVS) method. Owing to these techniques, the filed programmability of the voltage reference is achieved with small overheads of the power loss and the temperature dependence.

Chapter 3 is organized as fallows. In Section 3.2, the issues with a conventional programmable voltage reference are summarized. In Section 3.3, the MVD that mitigates the trade-off between the power consumption of the programmable voltage reference and the temperature characteristics of the output voltage is presented. Section 3.4 presents the FVS method for a high-resolution programmable voltage reference. Section 3.5 gives a summary of the chapter.

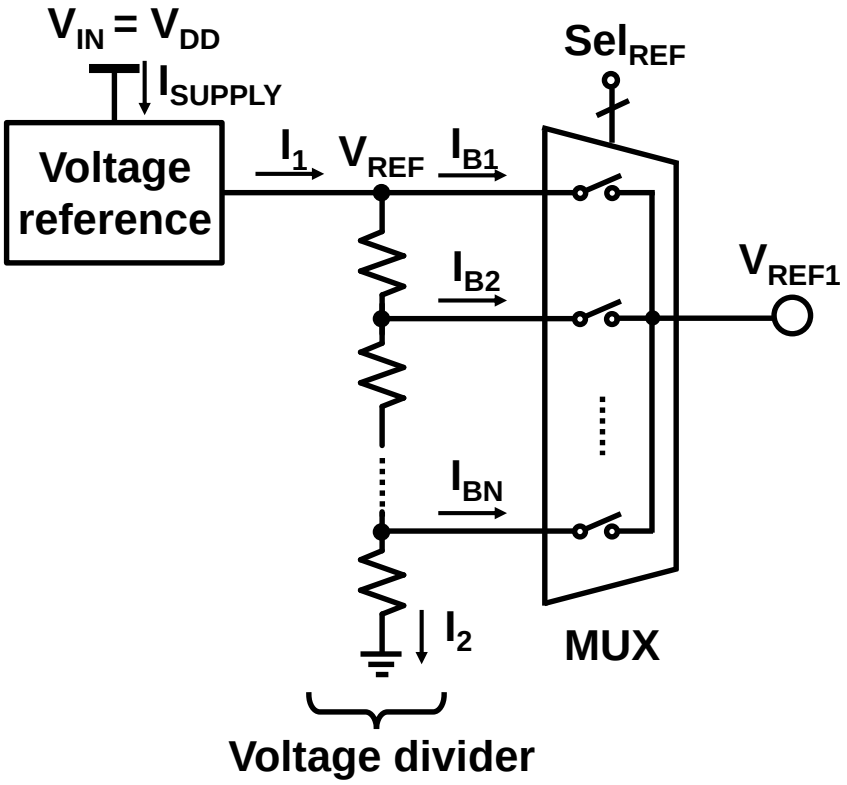


Fig. 3.1 Circuit schematic of a String digital-to-analog converter (DAC).

3.2. Issues with conventional programmable voltage reference

This section describes the issues of the conventional V_{REF} programming method. The concept of the proposed programmable voltage reference (PVREF) is based on a digital-to-analog converter (DAC). Since there are a lot of DAC architectures, we need to pick up an architecture that is suitable for the ultra-low power battery management shown in Fig. 1.1. Assumed IoT node spends almost all time in deep sleep mode and the oscillator is assumed to be disabled to save the power loss. Therefore, some DAC architectures that use external clock are not proper as the PVREF because PVREF is always on. Besides, the current based DAC architectures including R-2R are not suitable for low power PVREF since it needs large resistances that convert a current into a voltage. For these reasons, a String DAC based PVREF is proposed in this chapter.

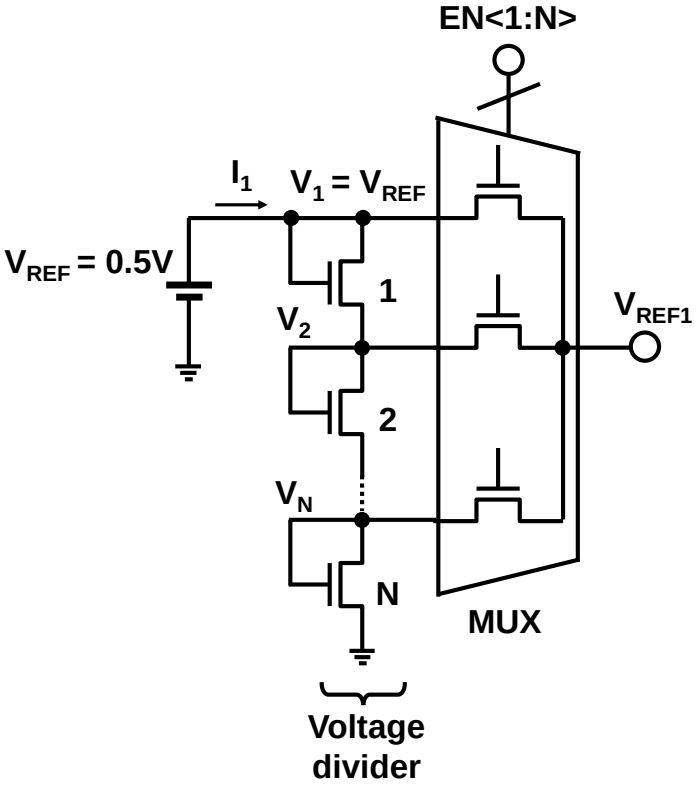
The most straightforward idea for realizing a post-fabrication PVREF is to use a voltage reference with a string (resistive ladder) as shown in Fig. 3.1 (named as String DAC in this thesis). A multiplexer (MUX) which is implemented with transistor switches is used to select the output voltage of the PVREF from the taps. An N bit programmability

is achieved with 2^N equal resistors and 2^N switches. By adding an N bit digital input, an appropriate voltage is selected from the ladder. The resistive ladder is not restricted to use resistors. To reduce the area and the power loss on the ladder, diode-connected MOSFETs are also available. The programmability is linear and monotonic with the condition that all the resistors are equal. The drawback of the architecture is the numerous number of the resistors and switches to achieve high resolution.

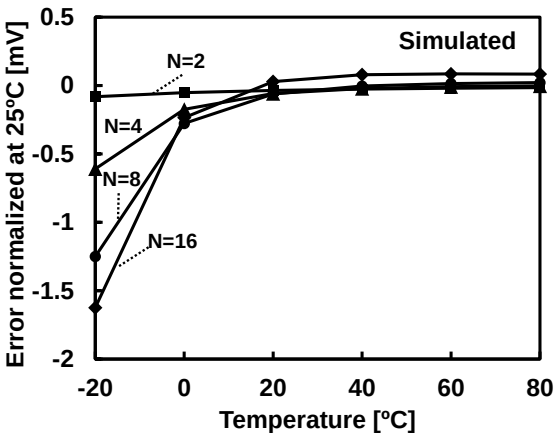
Notably, the large number of MOS switches cause a tradeoff between the temperature dependence of the output voltage of the PVREF (V_{REF1}) and the power consumption required to generate V_{REF1}. Ideally, the MUX has no leakage current, that is, I_{B1}, I_{B2}, and I_{BN} = 0 and I_1 = I_2. Then, V_{REF} is equally divided to achieve a monotonic, linear programmability. In the situation, the TC of V_{REF1} is expressed as $(m/N)\beta_{REF}$, where m ($1 \leq m \leq N$) is the selected tap in the ladder, N is the number of resistors, and β_{REF} is the TC of V_{REF}. On the other hand, the switches in the MUX have leakage currents [3.1] which cause voltage drops and temperature drifts at each tap in the ladder. The temperature-independent V_{REF1} and the high resolution of the programmability are incompatible without increasing the current I_1 sufficiently larger than the total leakage currents of the switches. To clarify the problem, a test circuit in 180-nm CMOS process shown in Fig. 3.2 (a) is simulated on the condition that V_{REF} is 500mV, I_1 is a constant 500pA at 25°C. The body node of each transistor in the ladder is connected to its source node to keep the resistances of all the transistors identical. The V_{REF1} in the temperature range of -20°C to 80°C is simulated when N=2, 4, 8, 16. Fig. 3.2 (b) shows the worst temperature characteristics of V_{REF1} among all patterns of the input digital code. Fig. 3.2 (c) shows the TC of V_{REF1} on the same condition as Fig. 3.2 (b). The result shows that the increase in the number of switches causes the deterioration of the TC of V_{REF1}.

The architecture shown in Fig. 3.1 also has another factor that increases the power consumption of the voltage reference. To prevent a voltage-drop and a temperature dependence of V_{REF}, the voltage reference must drive I_1, which causes an increase in the power consumption of the voltage reference. Together with the previously mentioned issue, I_{SUPPLY}, I_1 and total leakage current of the switches must fulfill the relationship as follows

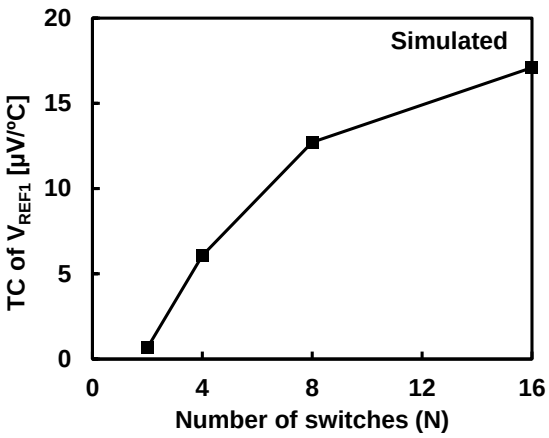
$$\sum_{i=1}^{N} I_{Bi} \ll I_1 \ll I_{SUPPLY}. \tag{3.1}$$



(a)



(b)



(c)

Fig. 3.2 (a) Circuit schematic of a String DAC for simulation. (b) Error of V_{REF1}. (c) Simulated N dependence of TC of V_{REF1}

At the end of the section, I sum up the problems of the programmable voltage reference shown in Fig. 3.1.

Issue (i): The high resolution and the low TC of V_{REF1} are incompatible because the increase in the number of the switches causes the inaccuracy and the deterioration of the TC in V_{REF1}. Therefore, we have the limit of the number of the switches that meet the allowable inaccuracy of V_{REF1}.

Issue (ii): The supply current for the voltage reference (I_{SUPPLY}) must be sufficiently larger than the current on the ladder. Together with Issue (i), the I_{SUPPLY} must fulfill the condition shown in (3.1).

Issue (ii) is mitigated by using a multiple voltage duplicator proposed in Section 3.3. Issue (i) is solved by a Fine Voltage-Step Subtraction (FVS) Method described in Section 3.4.

3.3. Multiple Voltage Duplicator for Programmable Operation

3.3.1. Multiple Voltage Duplicator

To solve the tradeoff between the power consumption and the temperature dependence of the PVREF as described in the previous section (Issue (ii)), a multiple voltage duplicator (MVD) is newly proposed and inserted between the voltage divider used for the voltage reference and the MUX in the PVREF shown in Fig. 3.1. The programmable voltage reference with the MVD is shown in Fig. 3.3. The MVD is a multiple-input and multiple-output voltage buffer. In the MVD, M0 is the current source with a subthreshold leakage current of I_{C0}, and the other transistors (M1, M2, and MN) are serially stacked. The source currents (I_{C0}, I_{C1}, I_{C2}, and I_{CN}) are sufficiently larger than the leakage currents (I_{B1}, I_{B1}, and I_{BN}) of the switches to avoid the voltage drop and the temperature dependence of selectable output nodes (V_{REF}', V_2', and V_N'). Then, an interesting characteristic of the MVD is that each input voltage is duplicated to each output voltage ($V_{REF} = V_{REF}$', $V_1 = V_1$', and $V_N = V_N$') because $I_{C0} = I_{C1} = I_{C2} = I_{CN}$ and $V_{GS} = 0$ for all transistors in the MVD. Thus, in the MVD, multiple input voltages are simultaneously copied to multiple output voltages. Figs. 3.4 show the simulated output characteristics of the MVD in the condition of V_{REF} = 400mV. The MUX is removed to show the pure characteristics of the MVD. The simulation results show that the MVD successfully copies each input to each output with the small temperature deterioration of 30μV/°C. Although the MVD has a line sensitivity (LS) of 3mV/V, the LS is removed with a method shown in Section 3.2.4.

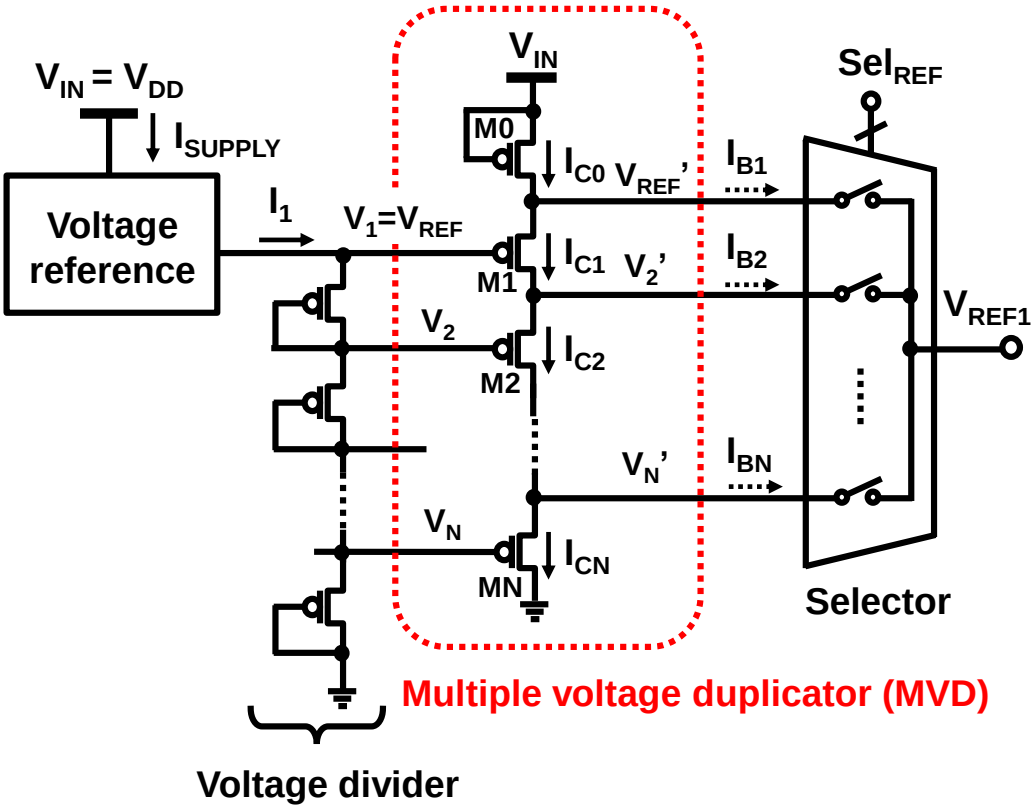
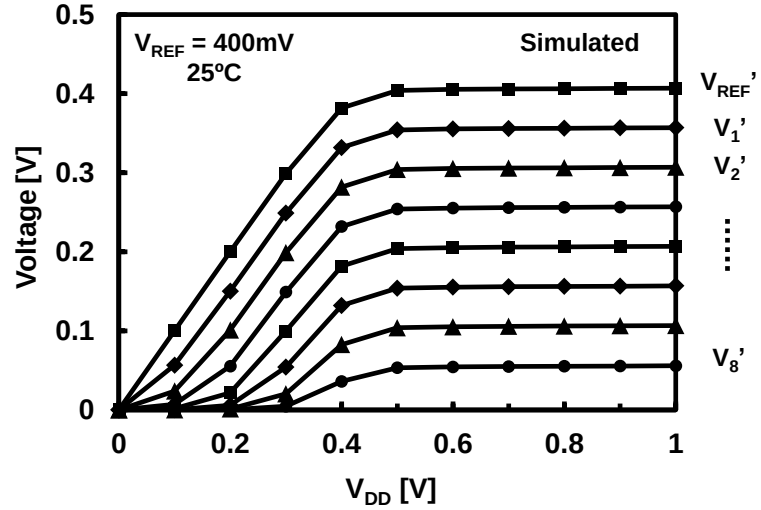


Fig. 3.3 Circuit schematic of the proposed programmable voltage reference with a multiple voltage duplicator (MVD).

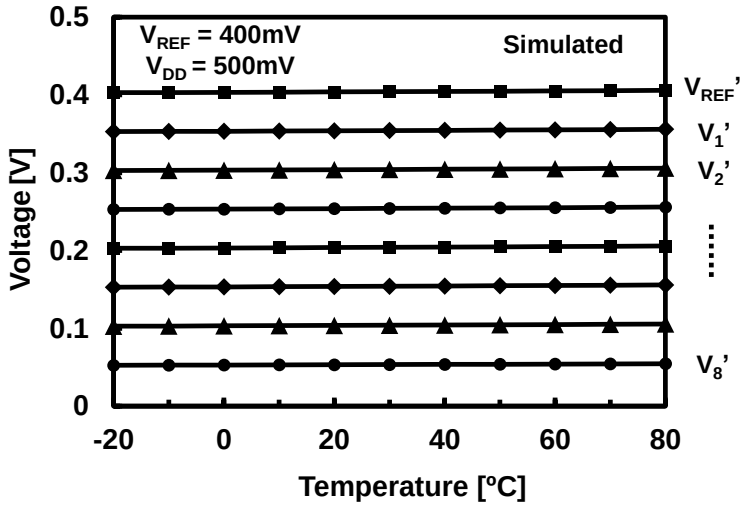
By inserting the MVD between the resistive ladder and the MUX, I_1 can be greatly reduced compared with I_1 in Fig. 3.1, which enables the power reduction in the voltage reference in Fig. 3.3. Thus, the tradeoff between the power consumed to generate V_{REF1} and the temperature dependence of V_{REF1} in the PVREF in Fig. 3.1 (Issue (ii)) is solved by using the MVD. The current on the MVD (I_0) is should be determined to sufficiently larger than the total leakage current of the MUX. In the next section, the relationship between the current on the MVD and the accuracy of the duplication is described.

3.3.2. Design Consideration and Theoretical Analysis of MVD

In Section 3.3.1, MVD was newly proposed as a multiple-input and multiple-output voltage buffer. Ideally, the MVD copies multiple input voltages to the multiple output nodes simultaneously without any duplication errors. In fact, owing to the load current in each output node, a slight error, which is the difference between the input voltage and



(a)



(b)

Fig. 3.4 Simulated input and output characteristics of the MVD. (a) V_{DD} dependence and (b) temperature dependence.

output voltage, is generated in the duplication as described in Issue (i) in Section 3.1. The duplication error is a function of the current in the MVD and the load current (the leakage current of the switches in the MUX) in each output node. In this section, the design consideration and theoretical analysis of the MVD are introduced to clarify the relationship between the current in the MVD and the accuracy of the duplication.

The model used for the analysis is shown in Fig. 3.5. $\Delta V_i = V_i' - V_i$ (i =1, 2, …, N) is the duplication error in each output node. Assuming that each transistor is sufficiently large, the effect of random variation is neglected. To simplify the analysis, each load

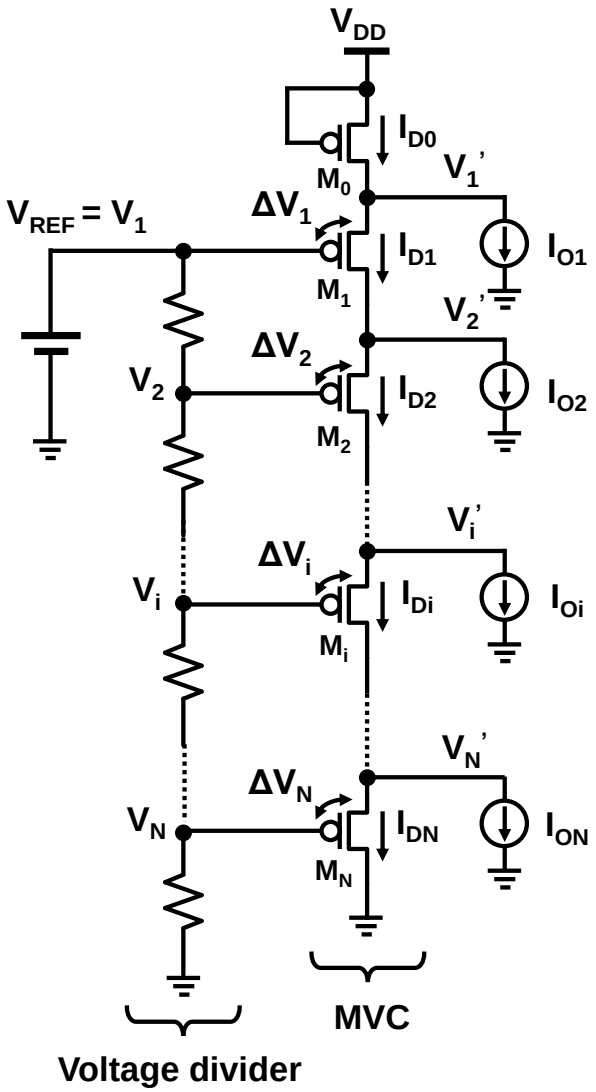


Fig. 3.5 Circuit schematic of the MVD for theoretical analysis.

current is assumed to be the same ($I_{O1} = I_{O2} = \ldots I_{ON} = I_O$). Assuming that V_{DS} of each transistor is sufficiently large (> $3V_T$), the drain currents of M_0 and M_i are expressed as follows:

$$I_{D0} = I_S \exp\left(\frac{-|V_{TH}|}{mV_T}\right) \tag{3.2}$$

$$I_{Di} = I_{D0} - \sum_{k=1}^{i} I_{Ok} = I_S \exp\left(\frac{\Delta V_i - |V_{TH}|}{mV_T}\right) \tag{3.3}$$

where

$$I_S = \mu C_{OX} \frac{W}{L} V_T^{\ 2} \tag{3.4}$$

where μ and C_{OX} are the mobility and gate capacitance of the transistor respectively. From (3.2) and (3.3), the ratio of I_{D0} to I_{Di} is

$$\frac{I_{Di}}{I_{D0}} = \exp\left(\frac{\Delta V_i}{mV_T}\right) = 1 - \frac{I_{LEAK,i}}{I_{D0}} \tag{3.5}$$

where

$$I_{LEAK,i} = \sum_{k=1}^{i} I_{Ok} \tag{3.6}$$

From (3.5) and (3.6), ΔV_i is given as follows.

$$\Delta V_i = mV_T \ln\left(1 - \frac{I_{LEAK,i}}{I_{D0}}\right) \tag{3.7}$$

When $I_{LEAK,i}/I_{D0}$ is sufficiently small (< 0.1), ΔV_i is approximated as

$$\Delta V_i \approx -mV_T \frac{I_{LEAK,i}}{I_{D0}} \tag{3.8}$$

From (3.8), the conditions for the worst ΔV_i are introduced.

1) The absolute value of the duplication error ($|\Delta V_i|$) is the largest when i = N. That is, designers have to consider ΔV_N to evaluate the worst duplication error in the MVD.
2) The TC of ΔV_i is positive as shown in Fig. 3.6 since the temperature dependence of $-1/I_{D0}$ is dominant in (3.8). It implies that the $|\Delta V_i|$ is the largest at the lowest temperature in the designer's target temperature range.

To verify the consistency of the analysis, SPICE simulations were conducted. Fig. 3.6 shows a comparison of the SPICE simulation results for the temperature dependence of ΔV_N in the target range of -20 °C to 80 °C with that given by (3.8). The body-effect coefficient m is determined from the characteristics of the pMOSFET at -20 °C in the SPICE simulation. $I_{LEAK,N}/I_{D0}$ is set to 0.1 at -20 °C. The SPICE simulation results are in agreement with (3.8) within an error of 11%. The simulation results and (3.8) show that the TC of ΔV_N is positive and that the largest $|\Delta V_N|$ occurs at the lowest temperature in the target range. From (3.8), ΔV_N and I_{D0} have a tradeoff relationship. Fig. 3.7 shows the relationship between $I_{LEAK,N}/I_{D0}$ and ΔV_N. ΔV_N is proportional to $I_{LEAK,N}/I_{D0}$. This means

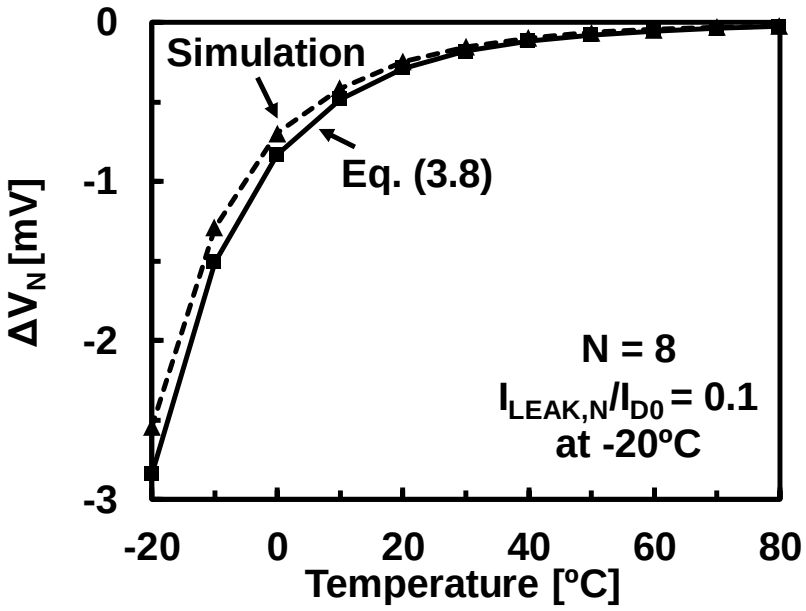


Fig. 3.6 Comparison of SPICE simulation result and (3.8) for temperature dependence of ΔV_N when N = 8 and $I_{LEAK,N}/I_{D0}$ = 0.1 at a temperature of -20 °C.

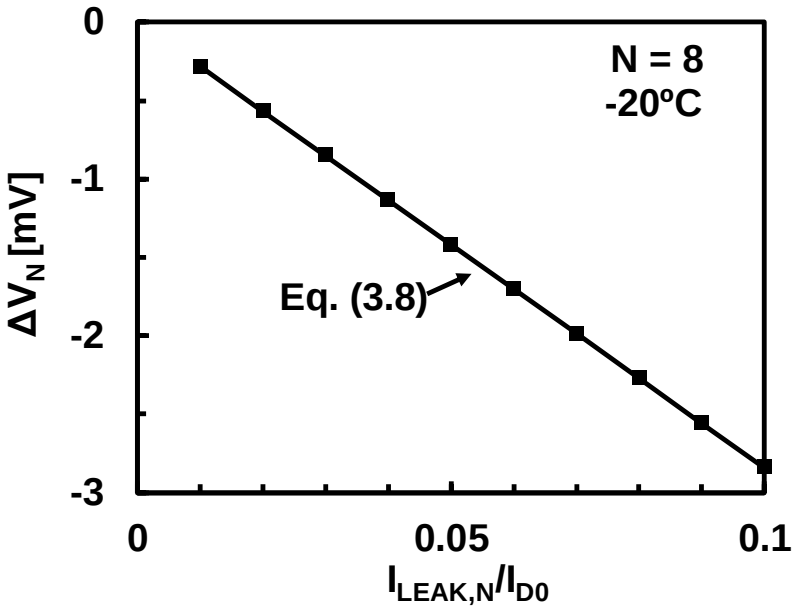


Fig. 3.7 Dependence of ΔV_N on supply current to load current ratio ($I_{LEAK,N}/I_{D0}$) obtained by SPICE simulation and (3.8) when N = 8 and the temperature is -20 °C.

that to reduce the duplication error in the MVD to within a certain voltage (=ΔV_{URS}), the MVD requires a sufficient value of I_{D0}. To maintain the duplication error in the MVD

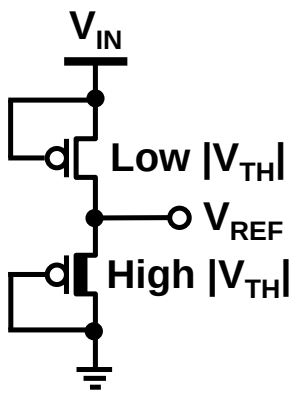


Fig. 3.8 Circuit schematic of the voltage reference implemented in the PVREF.

(=ΔV_N) below ΔV_{URS}, the following equation must be satisfied:

$$I_{D0} \geq I_{D0,min} = \frac{mk_B T_{MIN} I_{LEAK,N}}{q} \frac{1}{\Delta V_{URS}} \tag{3.9}$$

where T_{MIN} is the lowest target temperature and ΔV_{URS} is the acceptable error defined by designers. Eq.(3.9) means that once T_{MIN}, $I_{LEAK,N}$, and ΔV_{URS} are defined by designers, the optimum I_{D0} (=$I_{D0,min}$) is automatically given by (3.9).

3.3.3. Measurement Results of Programmable Voltage Reference

The proposed PVREF shown in Fig. 3.3 is fabricated in 250-nm CMOS process. The proposed PVREF includes the diode chain comprising 16 transistors, a MUX composed of 8 pMOSFET switches, and a voltage reference. The circuit schematic of the voltage reference is shown in Fig. 3.8. The concept of the voltage reference is based on N-type 2-transistors voltage reference [3.2]. However, the proposed voltage reference saves an overhead of the area in p-type substrate CMOS process since it is composed of pMOSFETs and does not require Deep N-well technology. A 3-bit digital code which <000> and <111> corresponds to the top node V_1' and the bottom node V_8', respectively is added to the MUX. Fig. 3.9 shows the chip photograph. The core area of the proposed PVREF is 0.054 mm^2. Typical temperature characteristics of the PVREF in a chip is shown in Fig. 3.10. The average temperature coefficient of V_{REF1} (TC) among 3 chips is 73 μV/°C. Figs. 3.11 (a) (b) show a V_{DD} dependence and line sensitivity (LS) of each output. The worst LS of 2 mV/V occurs when V_1' is selected as V_{REF1}. The relatively large LS is due to the DIBL effect on M0 that source node is directly connected to V_{DD}. In Section 3.3.4, a method to suppress the LS of the MVD by the combination of the VRVR

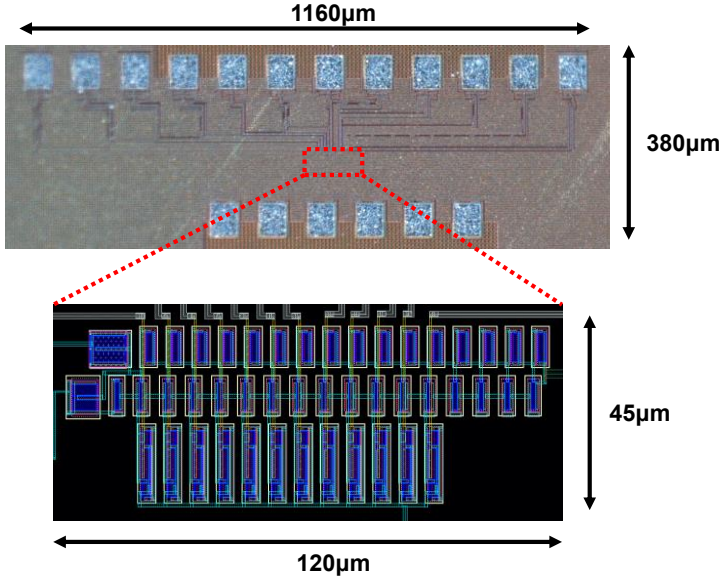


Fig. 3.9 Die photograph and layout of the proposed PVREF fabricated in 250-nm CMOS process.

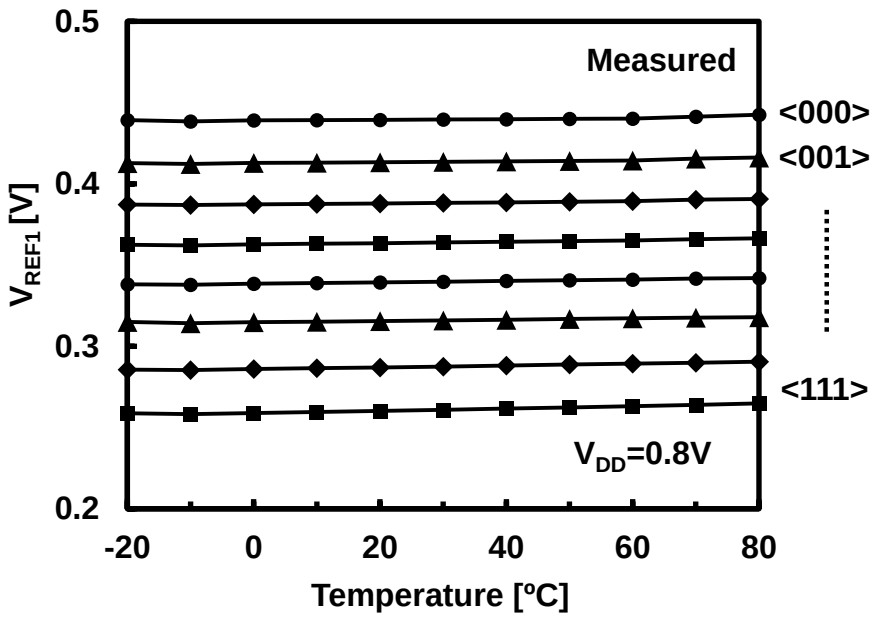
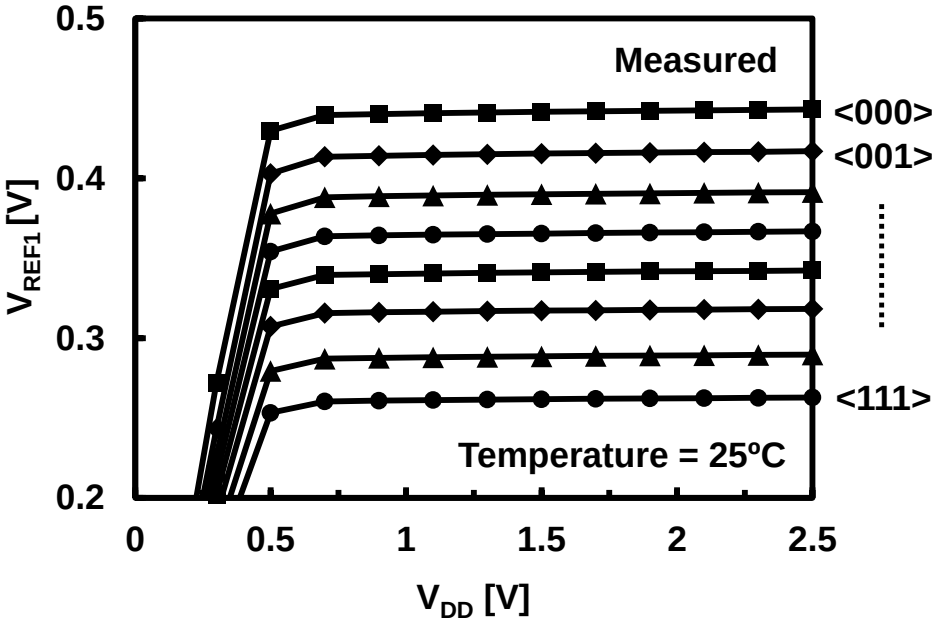
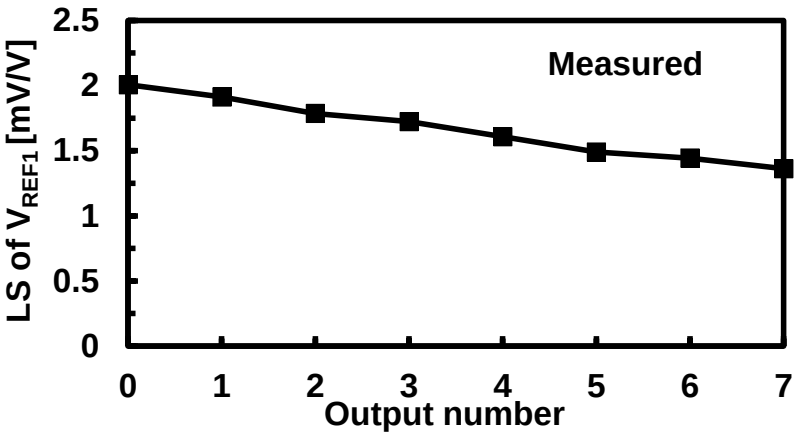


Fig. 3.10 Meausred temperature characteristics of V_{REF1}. In the figure, measurement result of just one chip is shown as a representative.

and the MVD, is proposed. Fig. 3.12 shows the power consumption of the entire PVREF among 3 chips. The power consumption is 84 pA at 0.8 V including the power consumption of MVD (56 pW in simulation). Fig. 3.13 shows the TC for V_{REF1} against the power consumption of the PVREF. The TC of V_{REF1} in Fig. 3.1 (named as PVREF



(a)



(b)

Fig. 3.11 (a) Measured V_{DD} characteristics of V_{REF1} and (b) LS of each output.

w/o MVD) which is a function of the supply current, is obtained by SPICE simulation. The voltage reference shown in Fig. 3.8 is also applied to the PVREF w/o MVD. The variation of I_1 is achieved by changing the transistor gate width of the voltage reference. In the case of the PVREF w/o MVD, as the power supply current is reduced, the TC increases, which indicates the tradeoff between the power consumption and the TC of V_{REF1} as described in Section 3.1 (Issue (ii)). In contrast, the measurement results of the 3 chips show that by introducing the MVD, the tradeoff is solved, and both a low supply current and a low TC of V_{REF1} are simultaneously achieved.

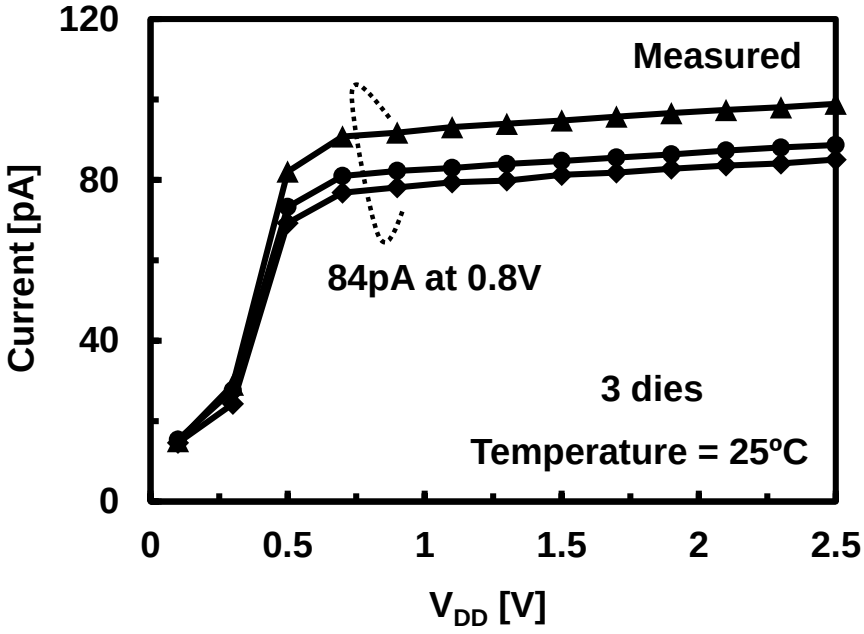


Fig. 3.12 Power consumption of the PVREF.

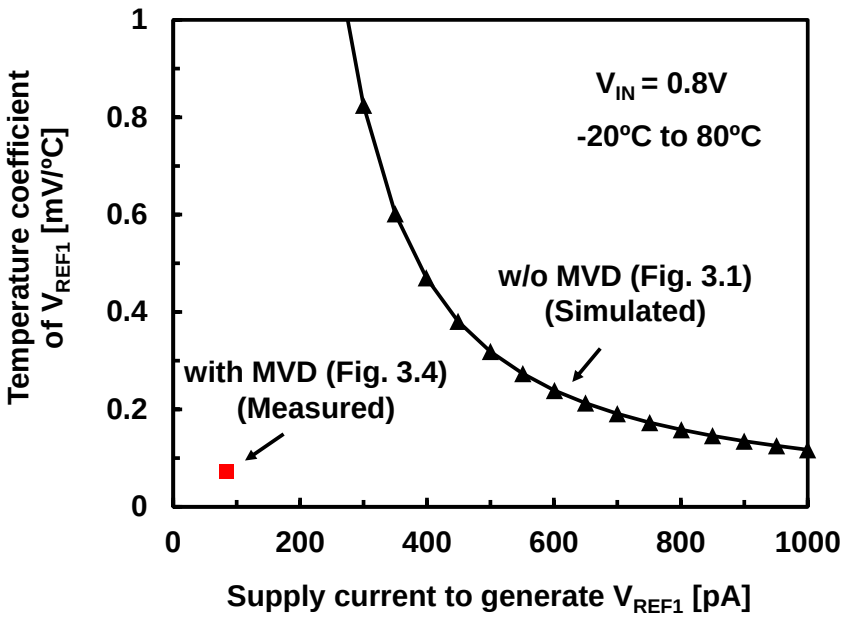


Fig. 3.13 Power supply current dependence of temperature coefficient for V_{REF1} with and without proposed MVD. The TC and power consumption of the PVD with MVD are obtained from measured 3 chips.

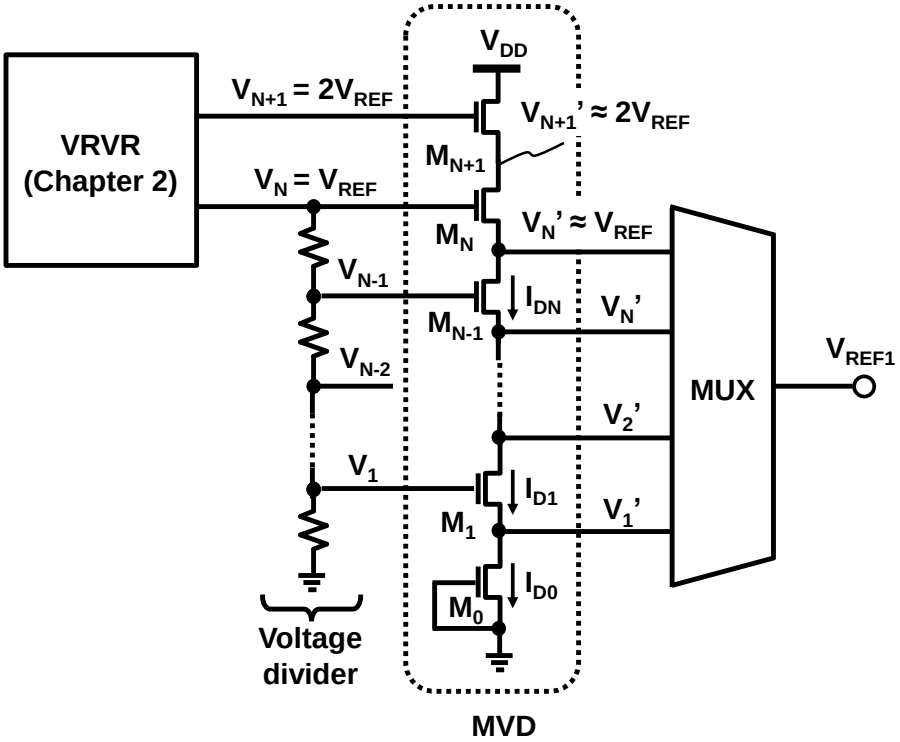
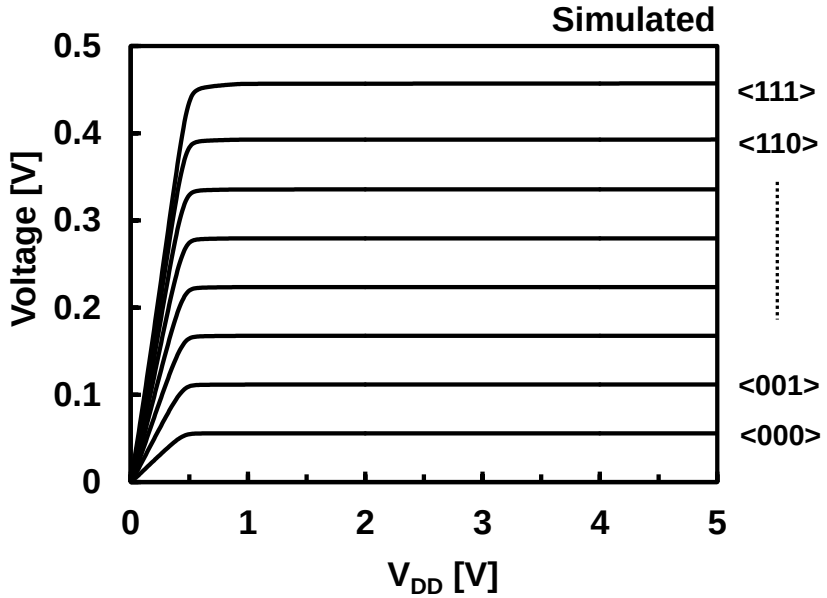


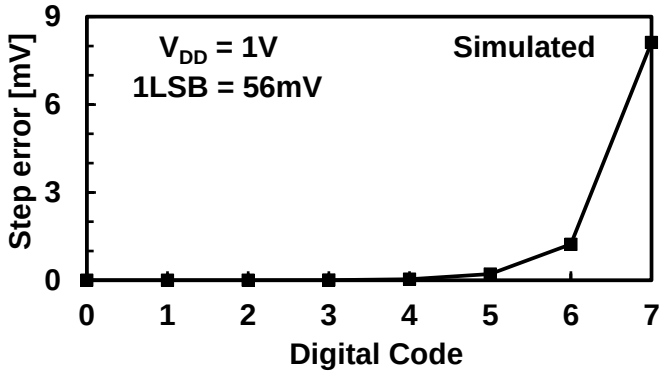
Fig. 3.14 Circuit schematic of the V_{DD}-insensitive PVREF.

3.3.4. V_{DD}-Insensitive Programmable Voltage Reference

As shown in Fig. 3.11, the proposed PVREF shown in Fig. 3.4 has a little V_{DD} independence of 2mV/V which is much larger LS than that of the VRVR proposed in Chapiter 2. To solve the problem, a V_{DD}-insensitive programmable voltage reference utilizing a variation of the MVD is proposed as shown in Fig. 3.14. The modified PVREF comprises the modified N-type MVD and VRVR for the voltage reference. The principle of the voltage duplication is similar to that of the MVD in Fig. 3.4. M_0 operates as the current source for the MVD in Fig. 3.14 corresponding to M0 in Fig. 3.4. Since M_1, M_2, … , M_{N+1} are in series, the current of each transistor is identical to I_0. As a result, the stacked nMOSFETs works as the MVD that copies each input voltages to each output voltages without a temperature deterioration. The point is the gate node of the top nMOSFET M_{N+1} is connected to V_2 in the VRVR shown in Fig. 2.2 (a) that makes the drain node of M_N (V_{N+1}') a constant voltage of $2V_{REF2}$. By keeping the drain node insensitive to V_{DD}, the LS of each node in the MVD is reduced. Fig. 3.15 (a) shows the simulated V_{DD}-dependence of the modified MVD with the VRVR. The worst LS is reduced to 120μV/°C which is 6% of the measured LS of the PVD with the MVD in



(a)



(b)

Fig. 3.15 (a) Measured V_{DD} characteristics of V_{DD}-insensitive PVREF and (b) programming step error.

Fig. 3.4. The simulated results show that the V_{DD} dependence of the PVREF is improved by the combination of the MVD and the VRVR. However, though the LS is sufficiently small, the step interval of the MSB is a little larger than other bits as shown in Fig. 3.15 (b). The application that the DNL characteristics are critical for the performance should not use the top tap for the programming. This is a tradeoff between the dynamic range of the PVREF and the linearity of the programmability.

3.4. Fine Voltage-Step Subtraction Method

3.4.1. Principle of Fine Voltage-Step Subtraction

In Section 3.2, two issues are listed as the challenge of the programmable voltage reference based on Fig. 3.1. In Section 3.3, the MVD is presented to reduce the power consumption of the voltage reference without the degradation of the TC of V_{REF1}, which solves Issue (ii). On the other hand, the resolution of the PVREF with the MVD is still limited due to the two reasons. The first reason is similar to Issue (i) that the current of the MVD needs to be sufficiently larger than the leakage currents of the switches. The error introduced as (3.8) follows the improvement of the resolution in the PVREF. The second reason is the restriction on the duplication capability of the MVD. When the number of the resistors is increased, the voltage drop per resistor is reduced and the drain-source voltage (V_{DS}) of MOSFET's in the MVD is reduced. The reduced V_{DS} degrades the capability of the multiple voltage duplication in the MVD and increases the TC since the transistors composing the MVD enter the triode region. Given that the programming method is applied to voltage references that are ultra-low power, but relatively low output voltage (e.g., 0.45 V [3.3], 0.5V [3.4], and 0.55 V [3.5]), the stage number of the MVD is limited. For these reasons, a new topology to achieve the fine resolution of the PVREF is discussed in this section. The proposed PVREF with a Fine Voltage-Step Subtraction (FVS) Method achieve both fine programmability of the PVREF and the low TC of the output voltage.

Fig. 3.16 shows a circuit schematic of the proposed PVD with the FVS method. The circuit implementation of resistors for a voltage divider, and the MUX's, is similar to what the previously mentioned in Section 3.3.1. The MVD presented in Section 3.3.4 is implemented in the PVREF to improve the V_{DD} dependence of the output voltage. Instead of increasing N in the voltage divider in Fig. 3.4, coarse and fine programming that involves the 1st ladder for m-bit coarse programming and the 2nd ladder for n-bit fine programming is used to achieve a total of m+n bit programmability. ΔV_{REF} is a coarse voltage step and $\Delta V_{REF}/n$ is a fine voltage step. In FVS, the fine programmed V_{REF2} levels are achieved by subtracting the fine voltage steps of $\Delta V_{REF}/n$ from the coarsely varied V_{REF1} in steps of ΔV_{REF}. The linear V_{REF} programmability is achieved because the fine voltage step is generated from the coarse voltage step. An equation for V_{REF2} is derived below.

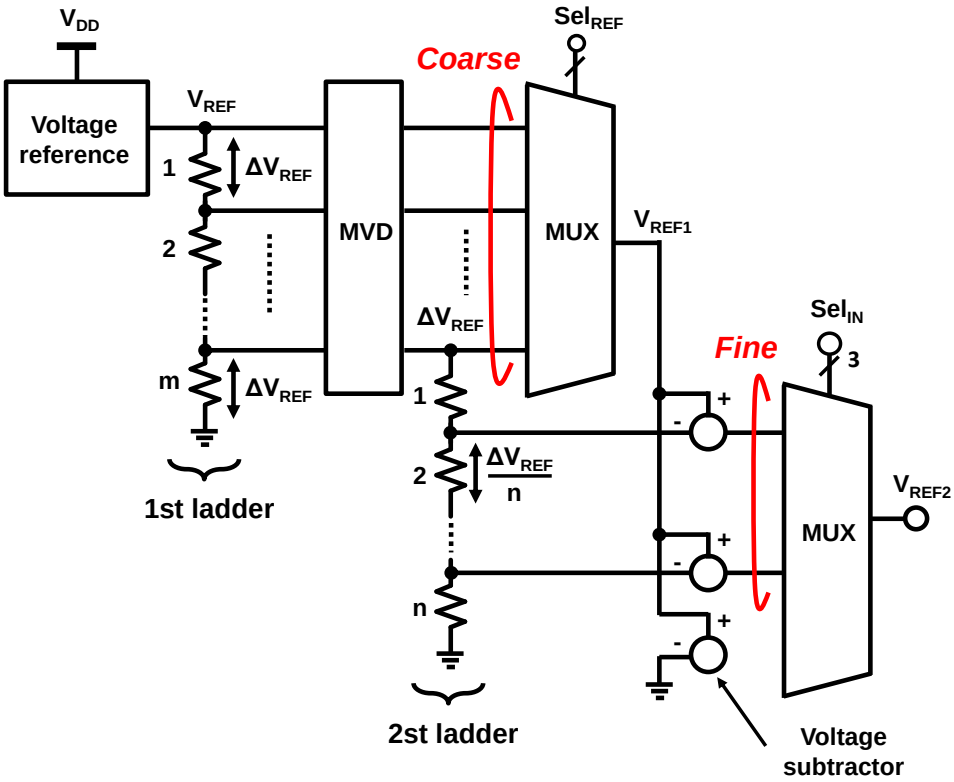


Fig. 3.16 Circuit schematic of the proposed PVREF with the FVS method.

$$\Delta V_{\mathrm{REF}} = \frac{V_{\mathrm{REF}}}{m} \tag{3.10}$$

$$V_{\mathrm{REF1}} = \frac{i}{m} V_{\mathrm{REF}} \quad (i = 0,1,\ldots,m-1) \tag{3.11}$$

$$V_{\mathrm{REF2}} = V_{\mathrm{REF1}} - \frac{j}{n} \Delta V_{\mathrm{REF}} \ (j = 0,1,\ldots,n-1) \tag{3.12}$$

Substituting (3.10) into (3.12),

$$V_{\mathrm{REF2}} = V_{\mathrm{REF1}} - \frac{j}{mn} V_{\mathrm{REF}} \tag{3.13}$$

Substituting (3.11) into (3.13), V_{REF2} is introduced as follows,

$$V_{\mathrm{REF2}} = \left(\frac{i}{m} - \frac{j}{mn} \right) V_{\mathrm{REF}}. \tag{3.14}$$

As shown in (3.14), by adding coarse voltage steps of V_{REF}/m and fine voltage steps of V_{REF}/mn, both linear V_{REF2} programmability and fine V_{REF2} steps are achieved. Thus, in the proposed PVD with FVS, the fine V_{REF2} steps and the linear V_{REF2} programmability are achieved.

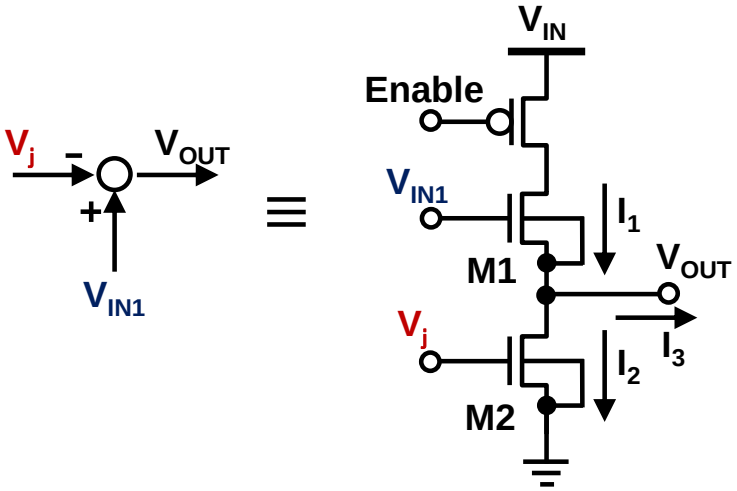


Fig. 3.17 Circuit schematic of the proposed voltage subtrctor.

In the FVS, low power voltage subtractors in Fig. 3.16 are one of the key building blocks. Fig. 3.17 shows a circuit schematic of the proposed voltage subtractor and its operation principle. M1 and M2 are in the sub-threshold region, and $I_3 \approx 0$, because the input impedance of the MUX is high. When $I_3 = 0$ and M1 and M2 are operating in the saturation region, $V_{IN1} - V_{OUT1}$ is the same voltage of V_j. As a result, V_{OUT} is expressed as $V_{IN1} - V_j$, and the voltage subtraction is achieved. The proposed voltage subtractor is low power since all transistors are designed to operate in the sub-threshold region. To reduce the power consumption of the multiple voltage subtractors in the PVREF, a power gating switch is added as shown in Fig. 3.17 and non-selected voltage subtractors are turned off.

The proposed FVS method decreases the number of switches in the MUX from 2^{M+N} to M+N, which solves the Issue (i) discussed in Section 3.1.

3.4.2. Measurement Results of Programmable Voltage Reference with Fine Voltage Subtraction Method

The proposed PVREF with the FVS method is fabricated in 250-nm CMOS process. In the measurement, a 600mV external voltage is added to the chip as V_{REF}. The 1st ladder and the 2nd ladder corresponds 12 diode-connected pMOSFETs and 8 diode-connected pMOSFETs, which set the resolutions of the coarse programming and the fine programming as 50 (=600/12) mV and 6.25 (50/8) mV, respectively. 3-bit MUX's for the coarse programming and fine programming achieves total 6-bit programmability of the PVREF. For the programming linearity, the top tap of the MVD is not used in the coarse

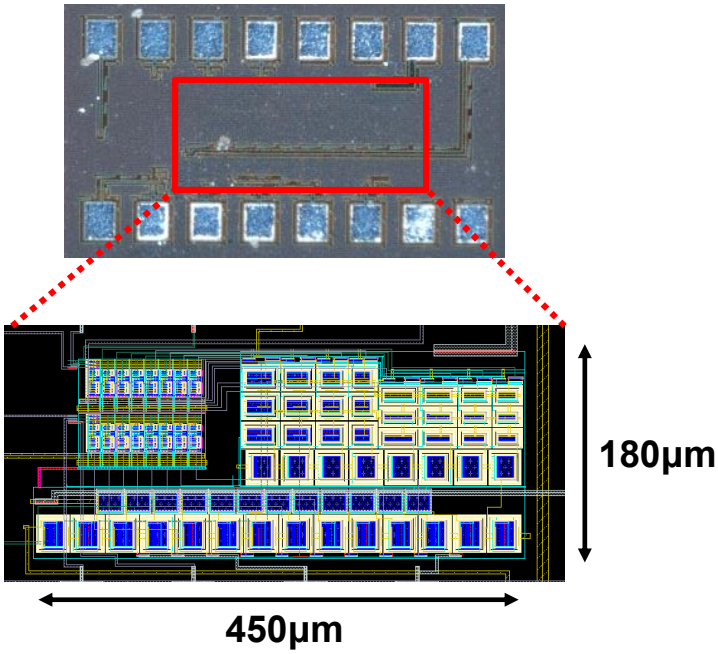
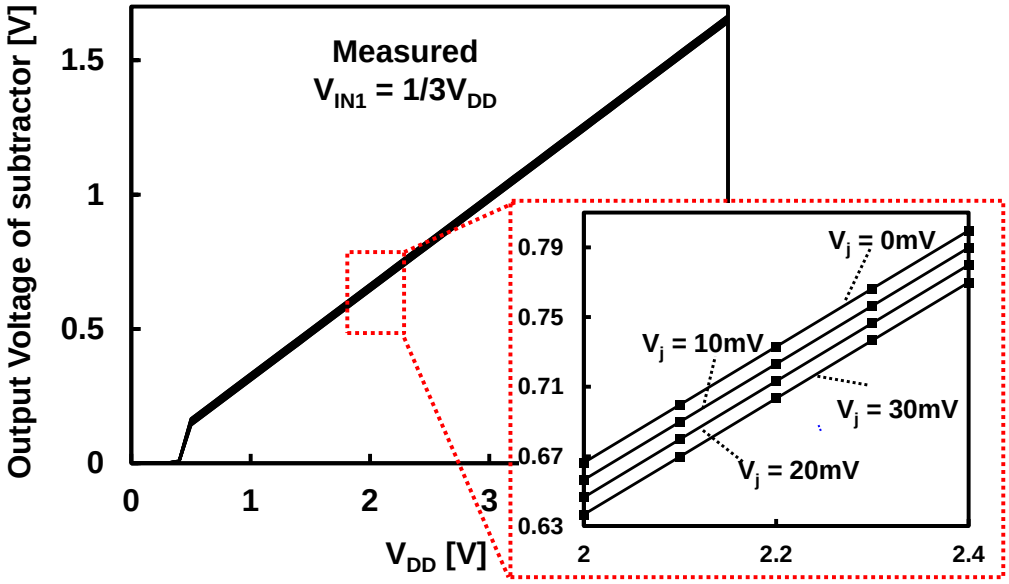
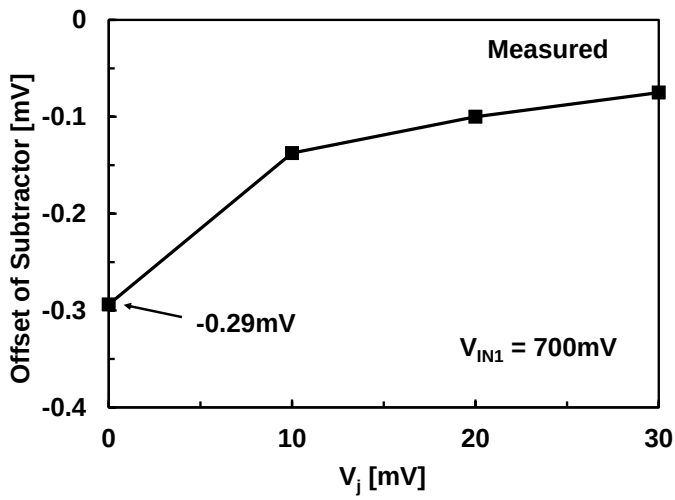


Fig. 3.18 Chip photograph and layout of the proposed PVREF with FVS method.

programming as described in Section 3.3.4. Fig. 3.18 shows the die photo of the proposed PVREF. The core area is 0.081mm^2. Fig. 3.19 (a) shows the input and output characteristics of the proposed subtractor. To demonstrate the performance of the subtractor, 1/3V_{DD} for V_{IN1} and constant voltages from 0 mV to 30 mV in steps of 10 mV for V_j are supplied, externally. As shown in the enlarged view in Fig. 3.19 (a) and Fig. 3.19 (b), the subtractor subtracts V_j from V_{IN1} with an accuracy of 300μV. Fig. 3.20 (a) shows the programmability of the PVREF. The PVREF achieves 6-bit, linear, equal steps programmed V_{REF2} ranging from 100 mV to 493 mV with the resolution of 6.14 mV. Fig. 3.20 (b) shows the DNL of the PVREF. The DNL of each digital code is within -0.13/0.18 LSB. Fig. 3.20 (c) shows the measured offset of V_{REF2} compared with the theoretical value of programmed V_{REF2}. The measured result shows that the offset of V_{REF2} corresponding to each digital code is less than 1.32 mV. Figs. 3.21 shows the V_{DD} dependence of each programmed V_{REF}. In the V_{DD} range of 1.2V to 2.4V, the averaged LS is 12.9μV/V while the worst LS is sufficiently small 30μV/V. Fig. 3.21 (b) shows a typical characteristic of V_{REF2} as a function of V_{DD}. Figs. 3.22 shows the temperature characteristics of the programmed V_{REF}. In the temperature range of -20°C to 60°C, the



(a)



(b)

Fig. 3.19 (a) Measured input and output characteristics of the subtractor. V_{IN1} is 1/3V_{DD} and V_j is biased at 0 mV to 30 mV in steps of 10 mV. (b) Offset of the subtractor when V_{IN1} is 700 mV and V_j is biased at 0mV to 30mV.

averaged TC is 15.2 μV/°C while the worst TC is 26.1μV/°C. These temperature characteristics are competitive to the VRVR in Chapter 2. Fig. 3.22 (b) shows a typical temperature characteristic of a programmed V_{REF}. The power consumption of the PVREF is shown in Fig 3.23. The power consumption is 675pA at the room temperature of 20°C when V_{DD} = 1.5V. Thanks to the proposed FVS method, the linear and monotonous, ultra-low power PVREF with the little temperature dependence is achieved. As described in

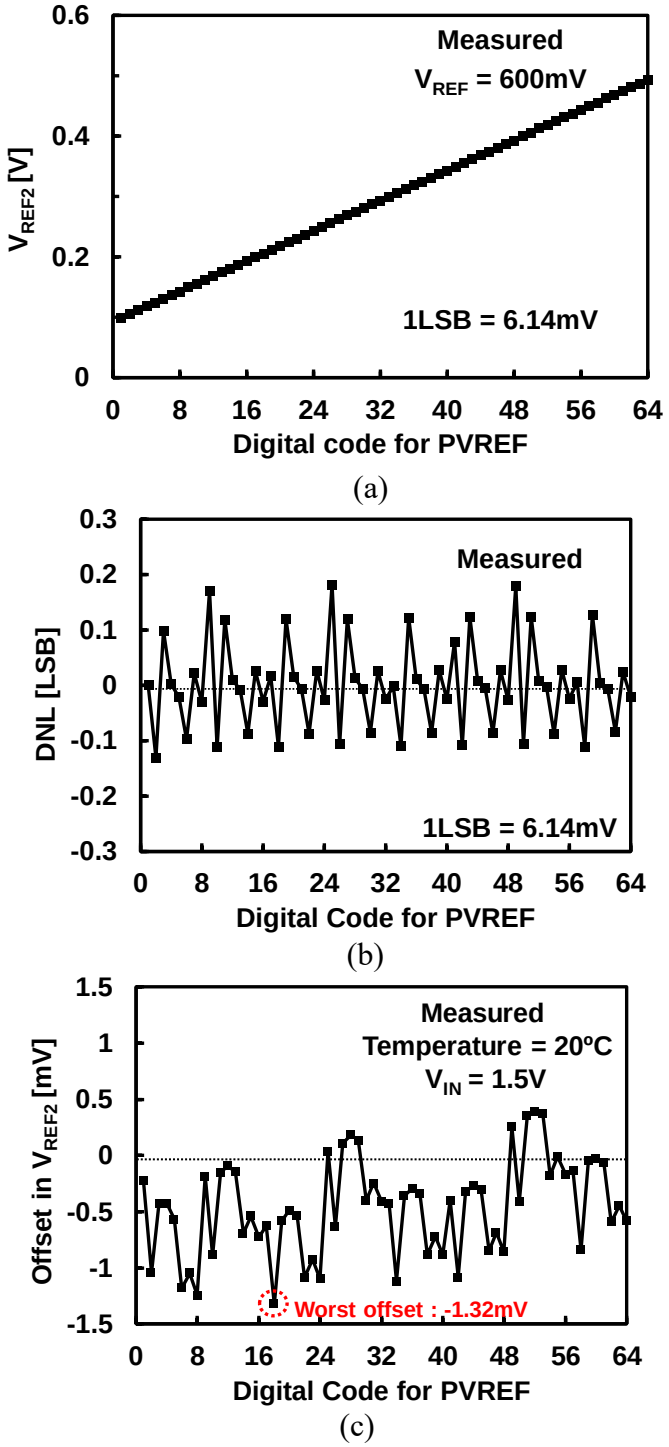
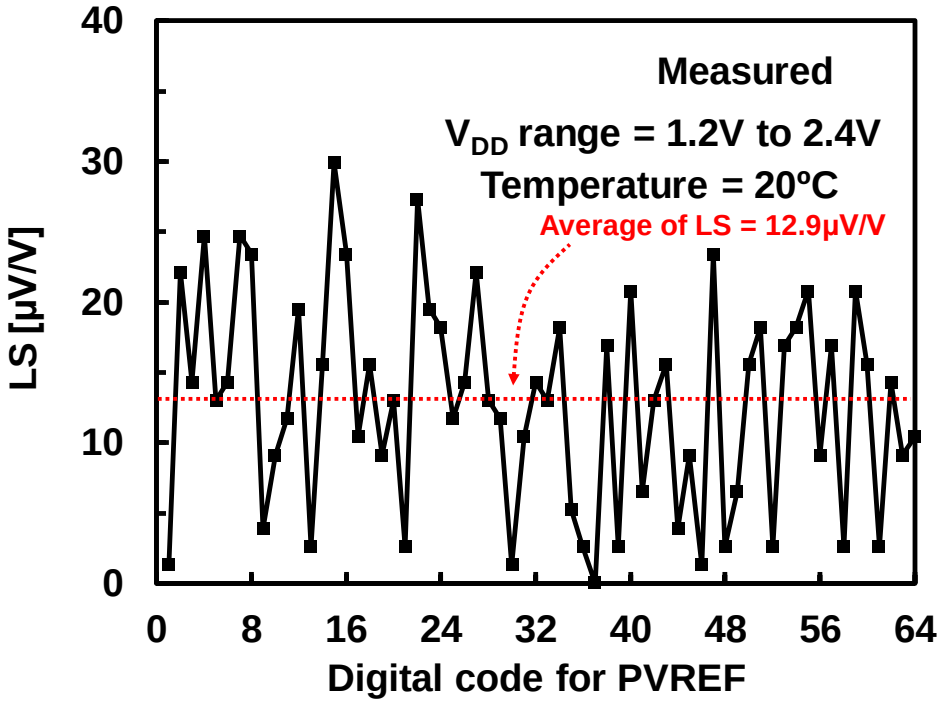
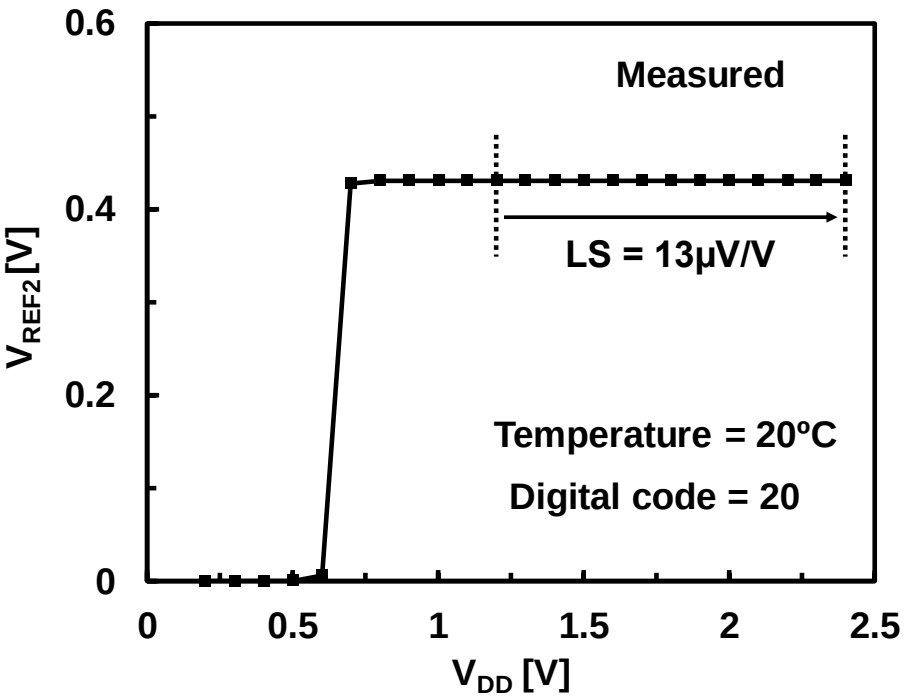


Fig. 3.20 (a) Measured programmed V_{REF2}, (b) DNL and (c) offset of the programmability. 600mV is added to the PVREF as V_{REF} externally.

this section, the proposed FVS method overcomes the Issue (i) in Section 3.2 with little overhead of the power loss and the temperature dependence.

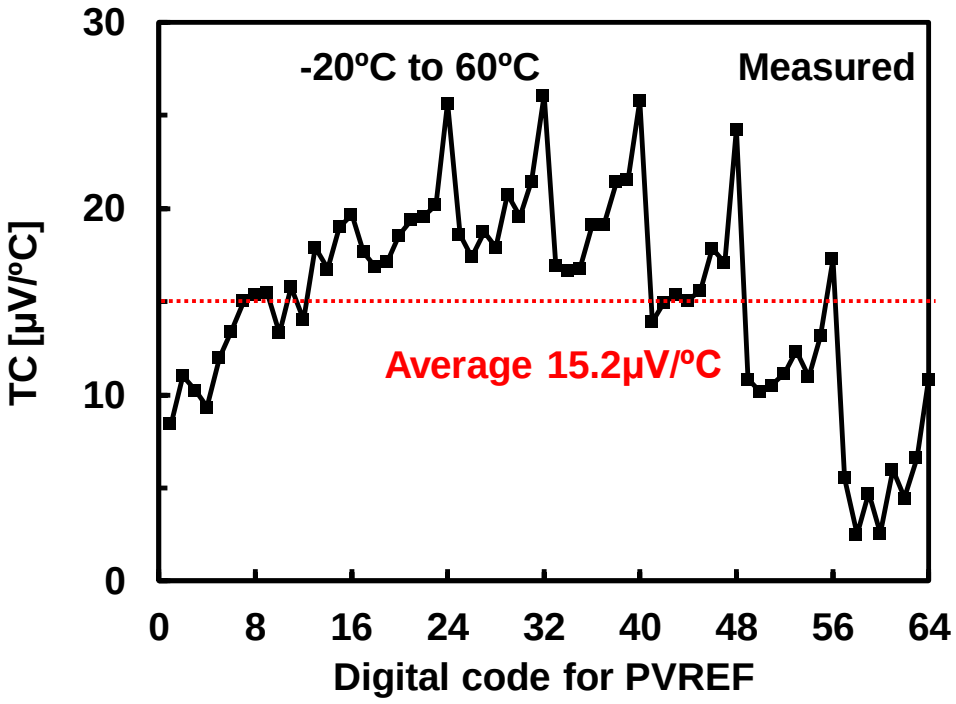


(a)

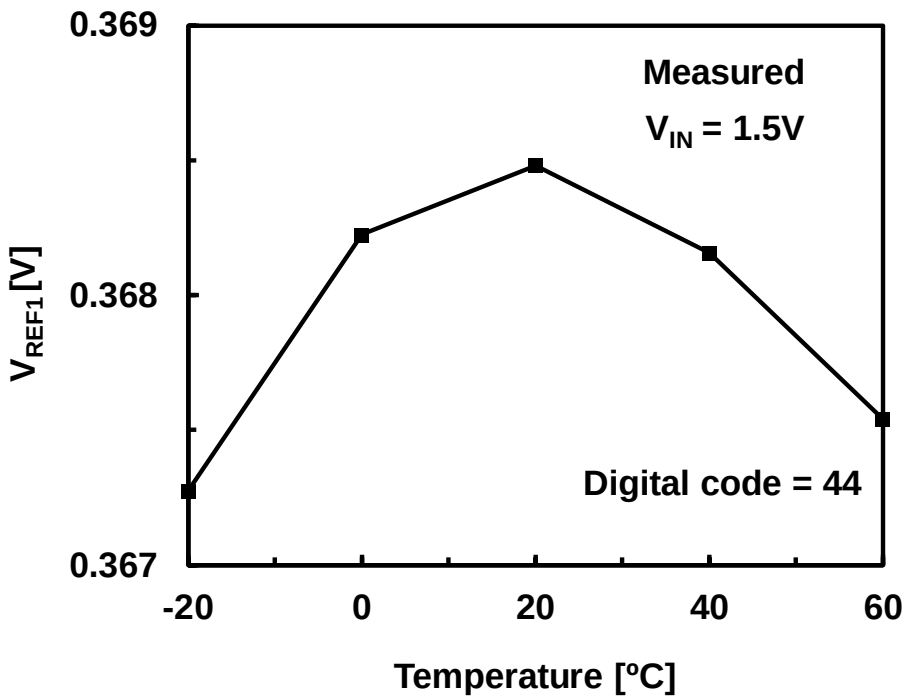


(b)

Fig. 3.21 (a) Measured LS of programmed V_{REF2} and (b) typical V_{DD} characteristics.



(a)



(b)

Fig. 3.22 (a) Measured TC of programmed V_{REF2} and (b) typical temperature characteristics.

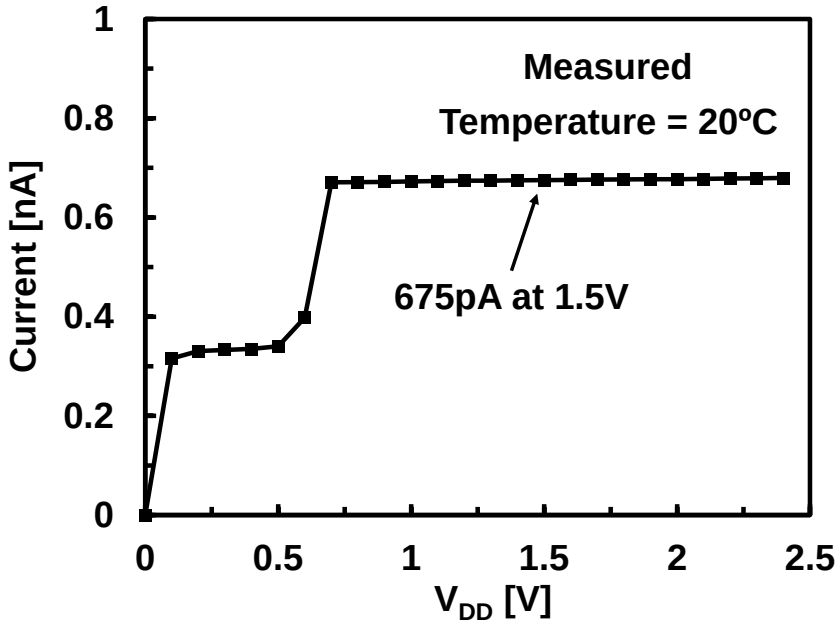


Fig. 3.23 (a) Measured power consumption of the proposed PVREF.

3.5. Summary

This chapter proposed a programmable voltage reference with a multiple voltage duplicator (MVD) and a fine voltage subtraction (FVS) method for battery management. The programmable voltage reference (PVREF) is used to achieve appropriate standard voltages for the circuits in the battery management. The proposed PVREF is based on a String digital to analog converter (DAC) that is composed of a resistive ladder and a MUX. The issues of the DAC are a tradeoff between the temperature characteristics of the output voltage and the power consumption of the voltage reference, and a tradeoff between the resolution of the programmability and the temperature characteristics of the PVREF.

The MVD is effective to reduce the power consumption of the programmable voltage reference drastically without the deterioration of the temperature characteristics. The first test chip of the PVREF with the MVD is fabricated in 250-nm CMOS process. The measurement results of the first chip show that 3-bit programmability of the PVREF with the power consumption of the 84pA at 0.8V. The temperature coefficient of the output is 73μV/°C in the range of -20°C to 80°C that shows the MVD does not deteriorate the TC of the voltage reference in the PVREF. These measurement results demonstrate that the MVD is useful to mitigate the trade-off relationship of the temperature dependence of the output voltage and the power consumption of the voltage reference in the string DAC.

The proposed FVS method overcomes the tradeoff between the temperature characteristics of the output and the resolution of the PVREF. The FVS method includes an N-bit coarse programming and M-bit fine programming for achieving N+M bit programmability of the PVREF. Thanks to the FVS method, the number of the switches in the MUX's reduces from 2^{N+M} to N+M, which results in the higher resolution and the better temperature characteristics of the PVREF. The proposed PVREF with the FVS method is fabricated in 250-nm CMOS process. The measurement results show that a linear and monotonous 6-bit programmability of the output voltage ranging from 100mV to 492mV with the resolution of 6.25mV. The power consumption is 675pA at 1.5V while the TC of the output voltage is 15.2μV/°C. These measurement results show that the proposed PVREF with the FVS method is beneficial for achieving a higher resolution without the deterioration of the temperature characteristics or the power loss.

References

[3.1] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs, “A Very Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2446–2456, 2004.

[3.2] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, “A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, 2012.

[3.3] L. Liu, J. Mu and Z. Zhu, "A 0.55-V, 28-ppm/°C, 83-nW CMOS Sub-BGR With UltraLow Power Curvature Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 95–106, 2018.

[3.4] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff and B. H. Calhoun, "A 32nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 1–3, 2015.

[3.5] Y. Osaki, T. Hirose, N. Kuroki and M. Numa, "1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, 2013.

Chapter 4: Voltage Detectors for Battery Management

4.1. Introduction

Voltage detector (VD) is commonly used as reset IC in order to monitor a state of a system. They are critical elements in systems in that they enhance the reliability and the quality of the applications. Figs. 4.1 (a) and (b) show a circuit schematic and an input-output characteristic of commercially available VDs [4.1-4.3], respectively. The VD is composed of a voltage divider for V_{IN}, a voltage reference, and a comparator. When the input voltage (V_{IN}) is lower or higher than V_{DETECT}, V_{OUT} is low or high, respectively. V_{DETECT} is expressed as follows:

$$V_{\mathrm{DETECT}} = \frac{V_{\mathrm{REF}}}{k} \quad (0 < k < 1), \tag{4.1}$$

where k is the division ratio of the voltage divider for V_{IN} and V_{REF} is the supply voltage from the voltage reference circuit. Since V_{REF} is well designed to have the robustness against the temperature or V_{DD}, the V_{DETECT} is independent of the temperature or V_{DD}, too. In most cases, V_{DETECT} is trimmed by changing the value of k. This chapter presents two voltage detectors (VDs) in the battery management system shown in Fig. 1. 1. The VDs have special features which are customized to their usages. The VD presented in Section 4.2 is for an RF energy harvesting in the IoT node. The VD achieves an ultra-low power and ultra-low voltage operation which are challenging issues in the RF energy harvesting. The VD in Section 4.3 achieves a filed programmability of V_{DETECT} for battery

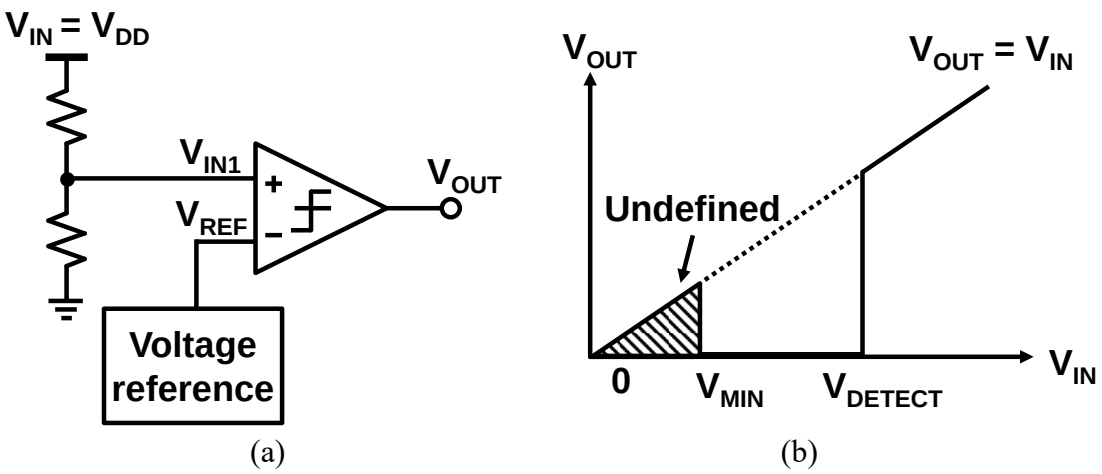


Fig. 4.1 (a) Circuit schematic of a voltage detector [4.1-4.3] and (b) its input and output characteristics.

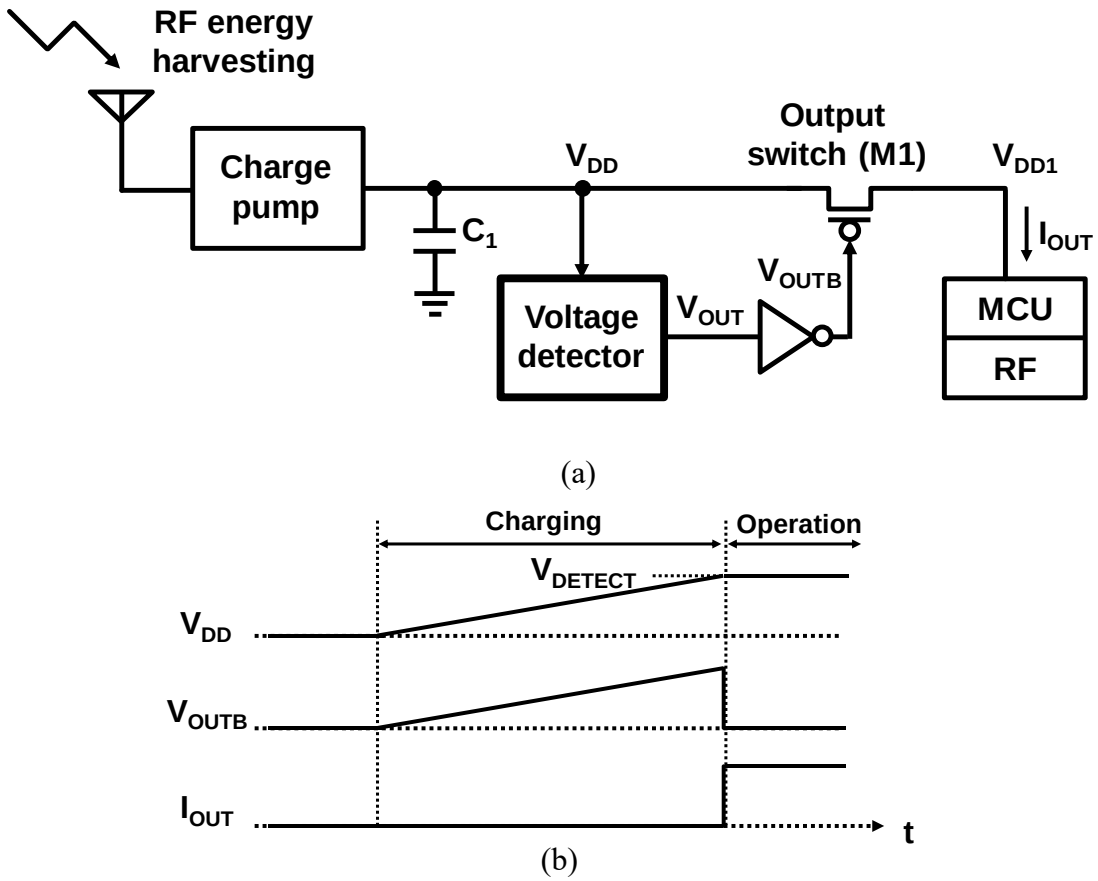


Fig. 4.2 (a) Circuit schematic of RF energy harvesting system and (b) timing diagram.

event detection. The programmability of V_{DETECT} that end-users can determine V_{DETECT} freely, is beneficial to reduce the number of VDs or remove the trouble of the special factory trimming according that trims V_{DETECT} according to user's requirement.

4.2. Ultra-Low Voltage Ultra-Low Power Voltage Detector for RF energy harvesting

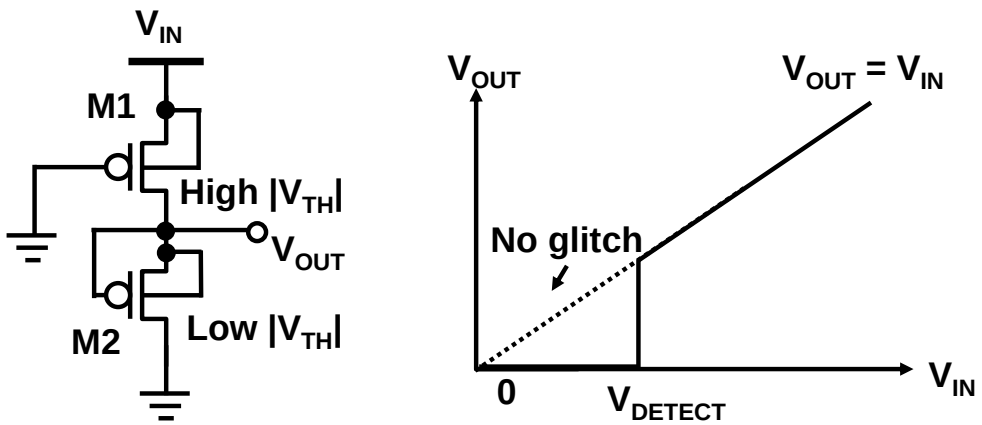
4.2.1. Motivation

Energy harvesting has attracted considerable attention since it can extend battery life and it may realize energy autonomous applications. In the research, several battery-free applications using energy harvesting have been proposed [4.4]–[4.8]. RF energy harvesting [4.9] is one of the energy harvesting approaches that produces energy from ambient RF signals. Although harvested power is small, in some cases, it is more stable than energy harvesting from solar and wind energy [4.10]. Fig. 4.2 (a) shows a block diagram of a typical IoT node with RF energy harvesting. The antenna receives an RF

signal (e.g., 920 MHz). Then, the charge pump (e.g., Dickson charge pump [4.24]) converts the RF signal into a DC voltage (V_{DD}) and charges the output capacitor C_1. Since the charging current is very small (e.g., 1 μA [4.11] or 1 nA [4.9]), during the charging period, the output switch M_1 must be turned off completely to prevent the charging current from flowing into the output load. The voltage detector (VD) monitors V_{DD} and turns the output switch M1 on or off depending on the value of V_{DD}. Fig. 4.2 (b) shows an operation sequence of the IoT node shown in Fig. 4.2 (a). At the start of the charging, V_{DD} gradually increases from 0 V since the output power of the antenna is very small. While the charge pump charges C_1, the VD keeps M_1 off. When V_{DD} reaches a predefined detection voltage (V_{DETECT}), the VD turns M_1 on and the load circuits start their operation. Since the VD is directly connected to the output node of the charge pump, it must have very low power consumption of less than 1 nA [4.9]. The VD must operate from 0 V without any glitch in V_{OUT}, otherwise it will mistakenly turn M1 on and spoil the energy harvesting. Furthermore, V_{DETECT} must be robust against variation in the process, voltage, and temperature (PVT).

4.2.2. Issues with Conventional Voltage Detector

One problem of the conventional VDs is the large power consumption (>10 nW). The voltage reference circuit is an important part in that it dominates the power consumption of the VD and determines the temperature dependence of V_{DETECT}. Typical voltage reference circuit is bandgap reference (BGR), on the other hand, the power consumption of BGR is usually over 10nW [4.12-4.14]. BGR also limits the operation voltage of the VD since the typical minimum operation voltage of BGR is over 1 V. An ultra-low power 2-transistor voltage reference was proposed in [4.15]. Though it operates sub-10pW power consumption and 0.5 V supply voltage, V_{REF} is sensitive to the process variation because V_{REF} is a strong function of the threshold voltages of the transistors composing the voltage reference circuit. With the voltage reference [4.15], the power consumption of the VD is reduced, on the other hand, V_{DETECT} varies by the process variation. Some post-fabrication trimming methods are required to compensate for the variation in V_{DETECT}. In this work, a post-fabrication trimming method utilizing the programmable voltage reference in Section 3.3 is proposed.



(a) (b)

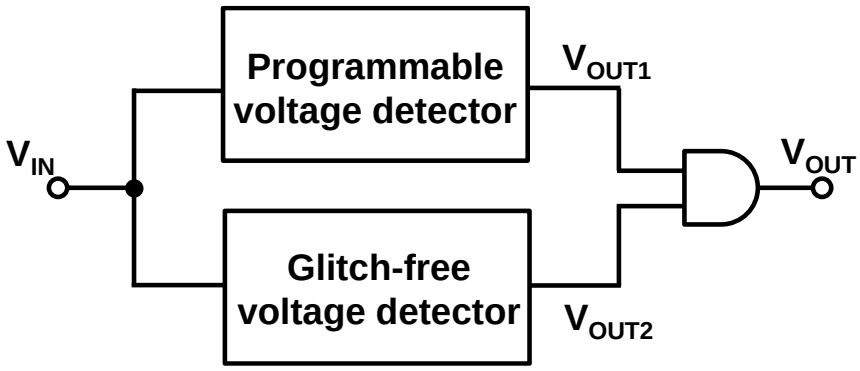
Fig. 4.3 (a) Circuit schematic and (b) input-output characteristic of glitch-free voltage detector [4.16].

Another problem of the conventional VD is the glitch in V_{OUT}. Compared with VDs for hardware reset detection such as Brown-out Reset (BOR), VDs for energy harvesters with small output power must operate even though V_{IN} is near 0 V. The minimum operating voltage (V_{MIN}), however, is defined in commercially available VDs. As shown in Fig. 4.1 (a), when V_{IN} is between 0 V and V_{MIN}, V_{OUT} is undefined and sometimes a glitch is generated, which spoils the power charging in the energy harvesting as described in Section 4.2.1.

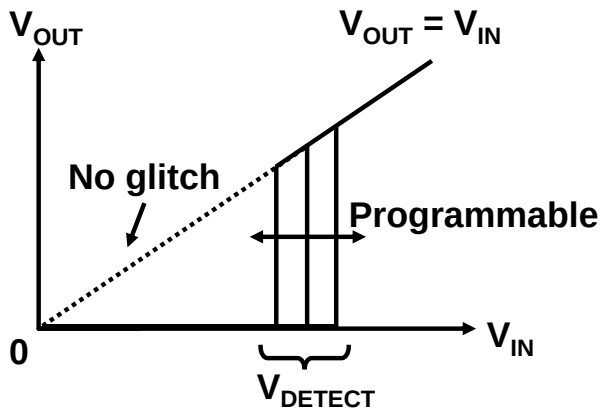
Fig. 4.3 shows a 1.6 nW glitch-free VD proposed in [4.16]. As shown in Fig. 4.3 (b), the VD has no glitch in V_{OUT}, whereas V_{DETECT} is fixed. In addition, V_{DETECT} has a large temperature coefficient (TC) which is calculated to be 2.0 mV/°C using typical transistor parameters. In [4.17], a VD for miniature sensor nodes was proposed. Although the VD realized sub-1 nW operation, the robustness to the process variation and the solution to mitigate the variation of V_{DETECT} were not discussed. Furthermore, V_{DETECT} had a large TC of 1.5 mV/°C.

4.2.3. Proposed Glitch-Free Programmable Voltage Detector

Figs. 4.4 (a) and (b) show a block diagram and the concept of the proposed glitch-free programmable VD, respectively. As shown in Figs. 4.4, by combining the programmable VD with the glitch, and the glitch-free VD with a fixed V_{DETECT}, both glitch-free and programmable operation are achieved when $V_{MIN} < V_{DETECT2} < V_{DETECT1}$, where $V_{DETECT1}$



(a)



(b)

Fig. 4.4 (a) Block diagram and (b) concept of proposed glitch-free programmable voltage detector.

and $V_{DETECT2}$ are the detection voltages of the programmable VD and the glitch-free VD respectively. Fig. 4.5 shows a schematic of the entire circuit of the proposed VD. All MOSFETs operate in the subthreshold region, which enables the ultra-low power consumption of the proposed VD. The body node and the source node are shorted in pMOSFETs in the proposed VD to avoid the body effect. Assuming that the proposed VD is applied to the RF energy harvesting shown in Fig. 4.2, the output node of the VD (V_{OUTB}) is designed to be high/low when V_{IN} is lower/higher than V_{DETECT}.

The programmable VD is based on the programmable voltage reference with an MVD presented in Section 3.3. As we discussed in Section 3.3, the programmability is achieved with little overhead of the power consumption and the temperature dependence. The voltage reference is implemented with two stacked pMOSFETs with different threshold voltages (V_{TH}) shown in Fig. 3.8, which is a similar concept to [4.15], in which two

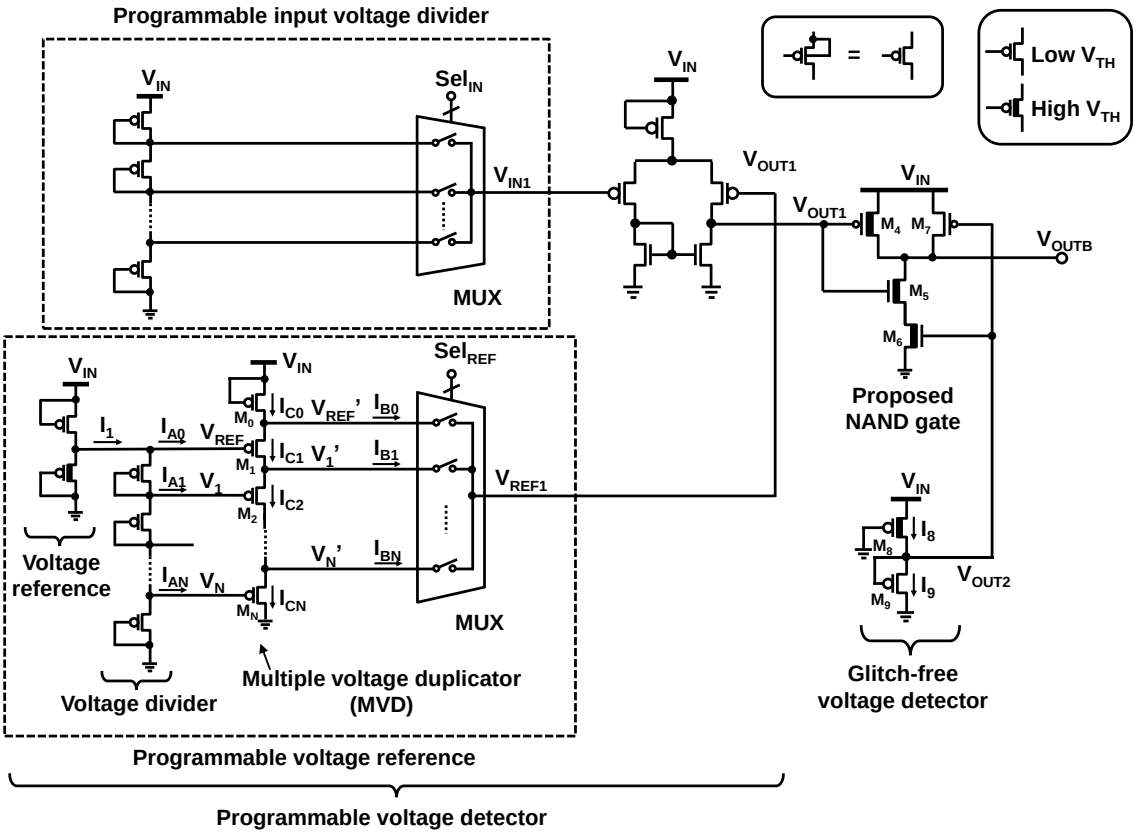


Fig. 4.5 Schematic of the proposed glitch-free programmable voltage detector.

stacked nMOSFETs with different values of V_{TH} are implemented. The V_{TH} difference is approximately 0.4 V. In the design, the target V_{DETECT} is set to 0.7 V. On the other hand, from the corner analysis in the SPICE simulation, the target V_{DETECT} varies ±60 mV with the process variation of the pMOSFETs. Then, the programmability in V_{DETECT} is set to cover the effect of the process variation. To improve the step of the programmable V_{DETECT}, voltage divider and MUX are also added to V_{IN}. The MUX in the proposed VD adopts low-V_{TH} MOSFETs as the switches to enable the low voltage operation of the VD and achieve the low voltage V_{DETECT}. When V_{IN} is lower voltage than the V_{TH} of the low-V_{TH} MOSFET, the programmable VD does not operate properly, which causes the glitch in V_{OUT1}. On the other hand, the glitch in V_{OUTB} is removed thanks to the glitch-free VD.

In this work, a glitch-free temperature-variation-tolerant VD is newly proposed. As shown in Fig. 4.5, the VD is composed of two stacked pMOSFETs M_8 and M_9 with different V_{TH}. When V_{IN} is lower than $V_{DETECT2}$, the current on M_9 (I_9) is much larger than

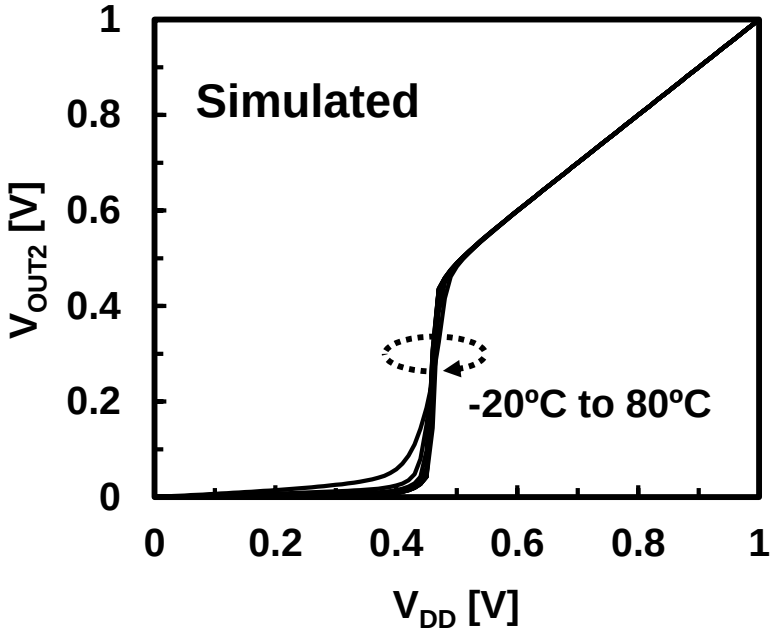


Fig. 4.6 Simulated input and output characteristics of the proposed glitch-free VD.

the current on M_8 (I_8), then V_{OUT2} is kept to 0 V. As V_{IN} increases, I_8 increases exponentially, and once I_8 exceeds I_9, the voltage level of V_{OUT2} changes from 0 V to V_{IN}. At the point, the drain to source voltages of M_8 and M_9 are over $3V_T$. The currents of M_8 and M_9 are expressed as follows [4.18]:

$$I_8 = \mu_8 C_{OX8} \frac{W_8}{L_8} V_T^{\,2} \exp\left(\frac{V_{IN} - |V_{TH8}|}{m_8 V_T} \right) \tag{4.2}$$

$$I_9 = \mu_9 C_{OX9} \frac{W_9}{L_9} V_T^{\,2} \exp\left(\frac{-|V_{TH9}|}{m_9 V_T} \right) \tag{4.3}$$

where m_8 (m_9), V_{TH8} (V_{TH9}), and μ_8 (μ_9) are the body-effect coefficient, the threshold voltage of transistor M_8 (M_9), and the mobility of the transistor, respectively. V_T is the thermal voltage ($=k_BT/q$), k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. W_8 (W_9) and L_8 (L_9) are the gate width and length of each transistor and C_{OX8} (C_{OX9}) is the gate capacitance per unit area of each transistor. From (4.2) and (4.3), $V_{DETECT2}$ is calculated as follows.

$$V_{DETECT2} = (|V_{TH8}| - \frac{m_8}{m_9}|V_{TH9}|) + m_8 V_T \ln\left(\frac{\mu_9 C_{OX9} W_9 L_8}{\mu_8 C_{OX8} W_8 L_9} \right) \tag{4.4}$$

In (4.4), by sizing M_8 and M_9 properly, the temperature dependence of the $V_{DETECT2}$ can be mitigated since the TC of the first and the second terms are opposite characteristics

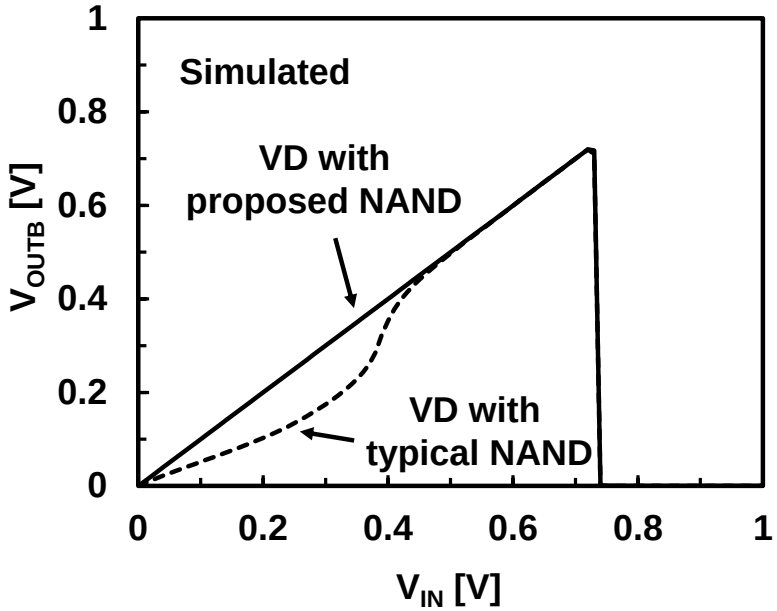


Fig. 4.7 Input-output characteristic of the voltage detector with or w/o the proposed NAND obtained by a SPICE simulation.

[4.19]. In this design, the sizing ratio of the glitch-free VD (W_9L_8/W_8L_9) is decided by the SPICE simulation to minimize the temperature dependence of the $V_{DETECT2}$. $V_{DETECT2}$ is expressed as about the difference of threshold voltages between high-V_{TH} pMOSFET and low-V_{TH} pMOSFET. Fig. 4.6 shows the input-output characteristics of the glitch-free temperature-tolerant VD obtained by SPICE simulation. The simulated TC of $V_{DETECT2}$ is less than 0.1 mV/°C.

The conventional AND or NAND gate for the VD shown in Fig. 4.4 (a) has a minimum operating voltage (V_{MIN2}) [4.20] which may cause a glitch in V_{OUTB}. To eliminate this possibility, a new NAND gate is proposed as shown in Fig. 4.5. Using the proposed NAND gate, V_{OUTB} is fixed to V_{IN} when $V_{IN} < V_{MIN2}$. The NAND gate is composed of M_4, M_5, and M_6, which are high-V_{TH} transistors, and M_7, which is a low-V_{TH} transistor. When V_{IN} is 0 V, the gate-to-source voltage of all the transistors is 0 V, then the leakage current of M_7 is much larger than the currents in the other transistors because V_{TH} of M_7 is lower than that for other transistors. While V_{IN} is increasing, the leakage current on M_7 increases V_{OUTB} to V_{IN}. Fig. 4.7 shows the input-output characteristics of the proposed VD with a conventional NAND gate and with the proposed NAND gate, obtained by SPICE simulation. With the conventional NAND gate, a glitch is generated in V_{OUTB}

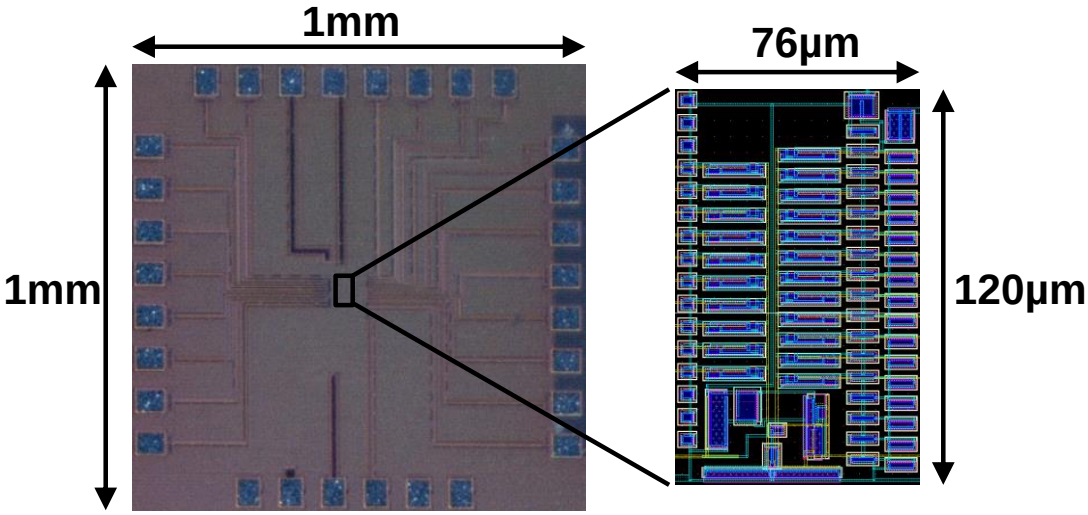


Fig. 4.8 Die photograph and layout of the proposed glitch-free programmable voltage detector fabricated in 250 nm CMOS process.

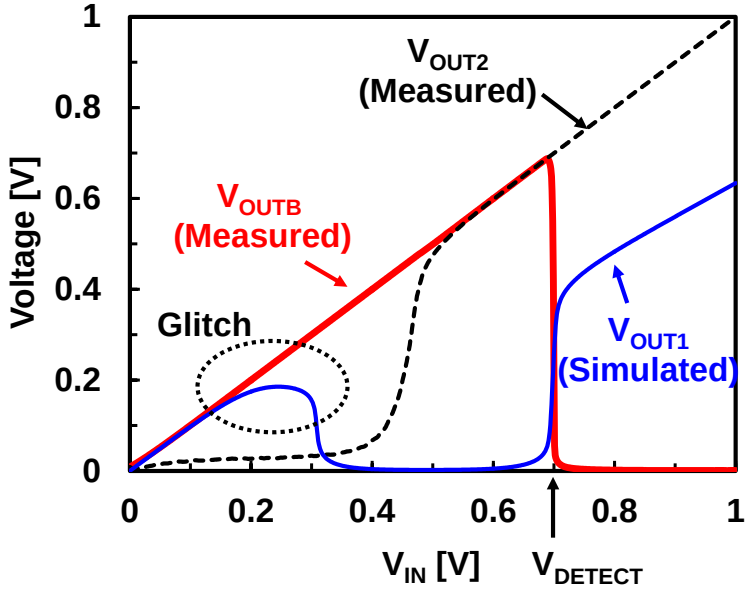


Fig. 4.9 Simulated and measured input-output characteristics of the proposed glitch-free programmable voltage detector.

when V_{IN} is less than 0.5 V. In contrast, the glitch in V_{OUTB} is removed with the proposed NAND gate.

4.2.4. Measurement Results

A test chip is fabricated in a 2.5 V 250-nm CMOS process. Fig. 4.8 shows a chip photograph of the proposed VD. The core area is 76 μm by 120 μm. Fig. 4.9 shows the simulated and measured input-output characteristics of V_{OUT1}, V_{OUT2}, and V_{OUTB} for the

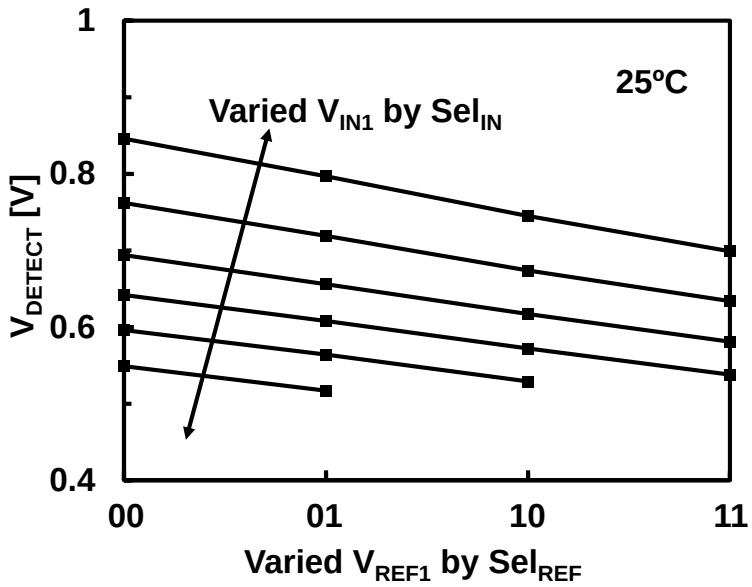
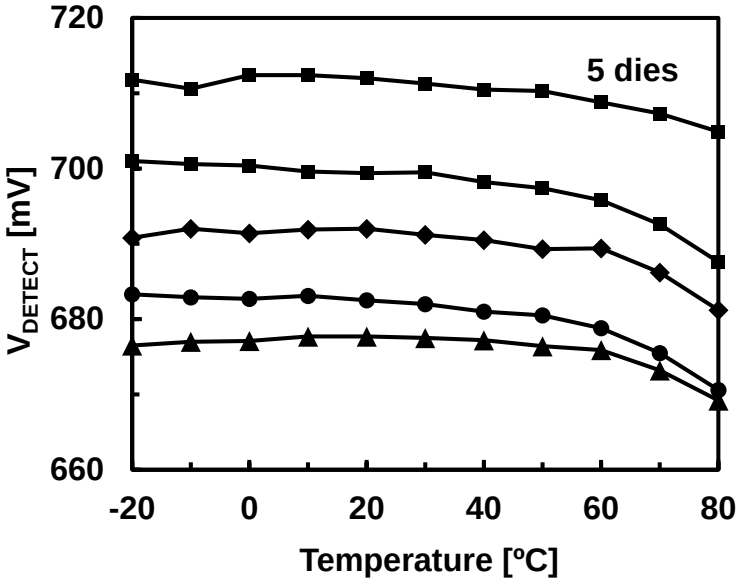
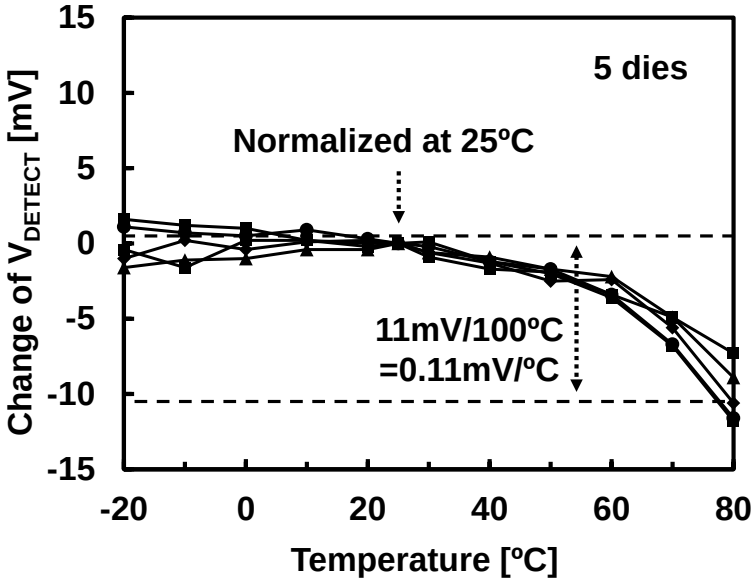


Fig. 4.10 Measured programmable V_{DETECT} in the proposed glitch-free programmable voltage detector.

proposed glitch-free programmable VD in Fig. 4.5. When V_{IN} is near 0 V, there is a glitch in V_{OUT1}. Owing to the combination of the glitch-free VD and the programmable VD, the glitch is removed from V_{OUTB}. The voltage level of V_{OUTB} is maintained at V_{IN} when V_{IN} is lower than V_{DETECT}. Fig. 4.10 shows the measured programmable V_{DETECT} in the proposed glitch-free programmable VD. The programmable range of V_{DETECT} is from 0.52 V to 0.85 V in steps of less than 49 mV. The programming step ensures the safe operating tolerance V_{DD} of ±5% in the load circuit. Fig. 4.11 (a) shows the measured temperature dependence of V_{DETECT} for five dies. Fig. 4.11 (b) shows the change of V_{DETECT} normalized by the values at 25 °C. The measured TC of V_{DETECT} is 0.11 mV/°C from -20 °C to 80 °C. The cause of the negative TC is assumed to be the temperature characteristics of the 2-transistor voltage reference. The diode chain connected to the output of the voltage reference draws the current of the 2-T voltage reference, which puts the currents of 2 transistors out of balance. To address this issue, we need to reduce the current of the diode chain or increase the current of the voltage reference. Also, the measured V_{TH} of the pMOSFETs in the VD is slightly higher than it was expected, which causes the negative temperature dependence of V_{REF} and V_{DETECT} in the design of this work. Other assumed reason for the negative TC is the mismatch in the comparator. It is



(a)



(b)

Fig. 4.11 Measured temperature dependence of the V_{DETECT} for five dies of the proposed glitch-free programmable voltage detector and (b) change of V_{DETECT} normalized by the values at 25 °C.

improved by enlarging the size of transistors. Fig. 4.12 shows the power consumption of the proposed VD for five dies and the breakdown of the power consumption. The power consumption is 248 pW at V_{IN} = 1.0 V. Since the gate to source voltage of the transistors

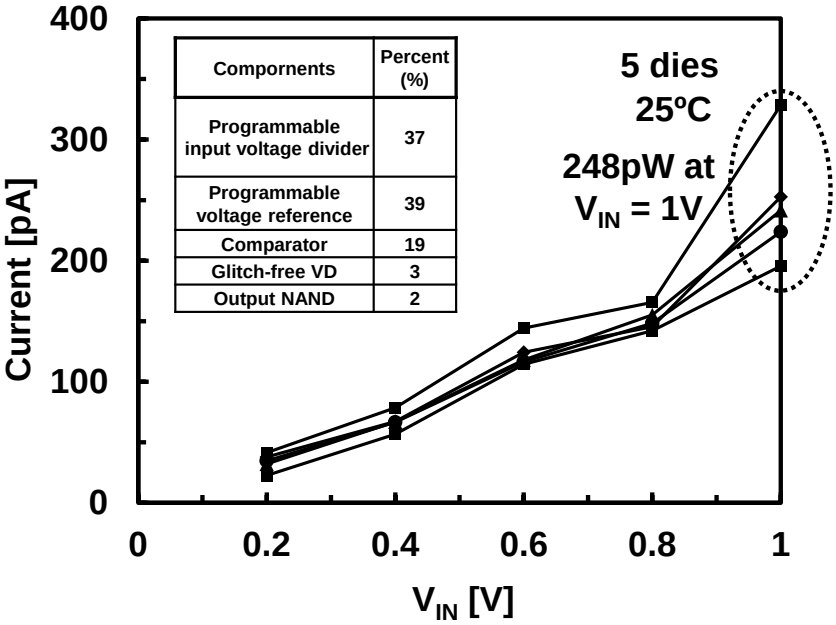


Fig. 4.12 Measured power consumption for five dies of the proposed glitch-free programmable voltage detector.

in the voltage divider increases slightly in association with V_{DD}, the current in the voltage divider increases almost linearly in the V_{DD} range of 0 V to 1 V, which causes the linear increase of the power consumption of the VD. In Table 4.1, the results of this work are compared with those for conventional VDs. In this work, the operating supply voltage is defined as the voltage region where the VD does not generate a glitch in the output node. The proposed VD achieve a minimum operating voltage of 0 V owing to the glitch-free operation, which is essential for energy harvesting. The demonstrated programmable V_{DETECT} covers 0.52 V to 0.85 V in steps of less than 49 mV to compensate for a die-to-die variations of V_{DETECT}. The proposed PVD with MVD enables a programmable VD with the lowest reported power of 248 pW and a competitive TC of 0.11 mV/°C.

4.2.5. Short Summary

In this section, an ultra-low power, glitch-free, and PVT-variation-tolerant voltage detector (VD) is proposed and implemented in a 250-nm CMOS process. The proposed VD achieves a programmable and glitch-free operation thanks to the combination of a programmable VD and a glitch free VD. All MOSFETs operate in the subthreshold region to reduce the power consumption of the VD, which realizes the 248 pW measured power

Table 4.1 COMPARISON WITH PREVIOUS VOLTAGE DETECTORS

		TPS3839	AP4400A	JSSC'12	VLSI'12	This Work
CMOS process		N/A	N/A	65nm	180nm	250nm
Operating supply voltage	Max	6.5V	5.5V	N/A	N/A	1.0V
	Min	0.9V	0.8V	0V		0V
Detection voltage (V_{DETECT})	Max	4.38V	4.2V	0.46V (Fixed)	3.58V (Fixed)	0.85V
	Min	0.9V	2.0V			0.52V
	Step	> 150mV (Trimming)	100mV (Trimming)			< 49mV (Programmable)
Power (25ºC)		180nW @1.2V	68nW @3.4V	1.6nW @0.46V	286pW @3.6V	248pW @1.0V
Temperature coefficient of V_{DETECT}		0.055mV/ºC	0.75mV/ºC	2.0mV/ºC (Calculated)	1.5mV/ºC	0.11mV/ºC
Temperature range		-40ºC to 85ºC	-15ºC to 85ºC	N/A	0ºC to 80ºC	-20ºC to 80ºC

consumption of the VD. To realize programmability in the VD with little power loss, a programmable voltage reference with a multiple voltage duplicator is applied. Due to the programmable voltage reference presented in Section 3.3, the programmability of the V_{DETECT} is realized without the increase of the power loss and the TC deterioration. Measurement results show that the power consumption of the proposed VD is the ultra-low power 248 pW and the temperature coefficient (TC) is a competitive value of 0.11 mV/°C. The steps of the programmable detection voltage ranges over 0.52 V to 0.85 V in steps of less than 49 mV. In addition, the glitch-free operation is achived. The presented VD is expected to be particularly advantageous for applications that require power consumption of less than 1 nW or ultra-low voltage operation such as energy-harvesting systems.

4.3. Filed Programmable Voltage Detector for Battery Management

4.3.1. Motivation

In the applications of batteries (e.g. lithium-ion batteries), a voltage detector is one of the key building blocks in a battery management system. Fig. 4.13 shows the definition of the voltage detector in this section. When the input voltage (V_{IN}) is higher than a pre-determined detection voltage (V_{DETECT}), the output voltage (V_{OUT}) is low. In contrast, when V_{IN} is lower than V_{DETECT}, V_{OUT} is high. In the recent battery management system for the lithium-ion batteries, both precise control of V_{DETECT} (e.g. ±1% (= ±42mV) of the battery voltage (4.2V) [4.21]) and various V_{DETECT}'s (e.g. at least 2 V_{DETECT}'s to start charging or discharging, and typically 6 V_{DETECT}'s [4.22]) are required. In the conventional voltage detectors [4.1-4.3], however, have 3 problems: (1) V_{DETECT} is not programmable (= factory-trimmed) and users cannot change V_{DETECT}, (2) V_{DETECT} resolution (e.g. 100mV [4.3]) is larger than the target resolution of ±42mV, and (3) multiple voltage detectors are required for multiple V_{DETECT}'s, which increases cost and area. Though a programmable voltage detector (PVD) with V_{DETECT} ranging from 0.52V to 0.85V for a RF energy harvesting is reported in Section 4.2, the PVD cannot be used for the lithium-ion batteries, because the V_{DETECT} range does not fit the voltage range (e.g. 3.0V to 4.2V) of the lithium-ion batteries.

Therefore, in this paper, a new PVD with a programmable 6-bit V_{DETECT} ranging from 902 mV to 4904 mV in steps of 62.5 mV is proposed for the battery management system. The 62.5-mV step (= ±32mV) programmability satisfies the target resolution of ±42mV for the lithium-ion batteries. Compared with previous publications, the 62.5-mV step is the smallest and the 64-level programmability is the largest. Thanks to the

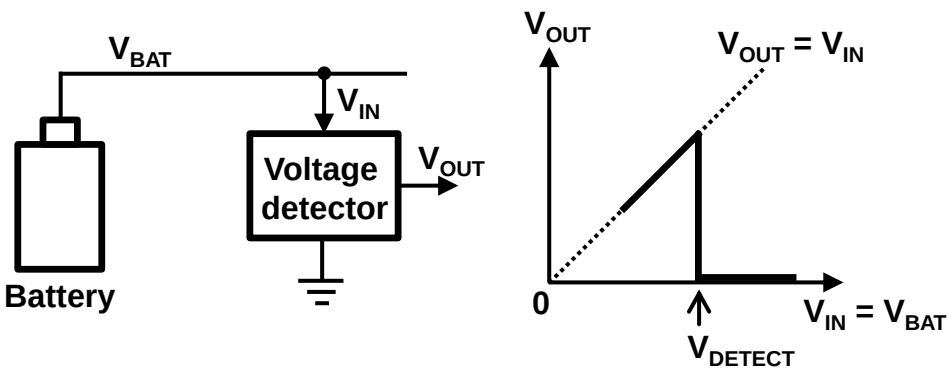


Fig. 4.13 Definition of voltage detector for battery management.

programmability, the proposed PVD can be a general-purpose component and users can freely change V_{DETECT}.

In this work, to achieve PVD with wide V_{DETECT} range, fine V_{DETECT} steps, and linear V_{DETECT} programmability, a fine voltage-step subtraction (FVS) method in Section 3.4 is applied. In PVD, a low power operation is also required in battery-operated mobile devices and IoT nodes, because PVD always operates to monitor the battery. In the conventional voltage detectors, however, the power consumption is dominated by the bandgap reference circuits (32nW [4.13] to 100nW [4.14]). Though a low power voltage reference (VR) circuit is reported [4.16], PVD with the VR circuit shows a non-linear V_{DETECT} programmability, because the line sensitivity of the VR is large (= 2mV/V) as described in Chapter 2. To solve the problem, a V_{DD}-regulated voltage reference (VRVR) proposed in Chapter 2 is applied.

4.3.2. Conventional Programmable Voltage Detector

It is shown that the PVD in Section 4.2 [4.23] has 2 problems in the programmability: (1) linear V_{DETECT} programmability is not available, and (2) both fine V_{DETECT} steps and low temperature coefficient (TC) of V_{DETECT} are not achieved. Fig. 4.14 shows a simplified circuit schematic of the PVD, where a multiple voltage duplicator (MVD) is a multiple-input multiple-output voltage buffer presented in Section 3.3. Fig. 4.15 shows an operation principle of the PVD. The offset of V_{REF1} is varied by m and the gradient of V_{IN1} is varied by n. Points at the intersection of V_{REF1}'s with V_{IN1}'s are V_{DETECT}'s. As shown in Fig. 4.15, V_{DETECT} changes non-linearly and non-monotonously with control-bits. A straightforward method to obtain both linear V_{DETECT} programmability and fine V_{DETECT} steps is to change V_{REF1} at fixed V_{IN1} with increasing m. However, as described in Section 3.1, the increase of the number of the switches causes the power increase or temperature coefficient of the output voltage in PVREF. Therefore, the programmable voltage reference with a FVS method presented in Section 3.4 is utilized to achieve the fine resolution, linear and monotonous programmability of V_{DETECT}.

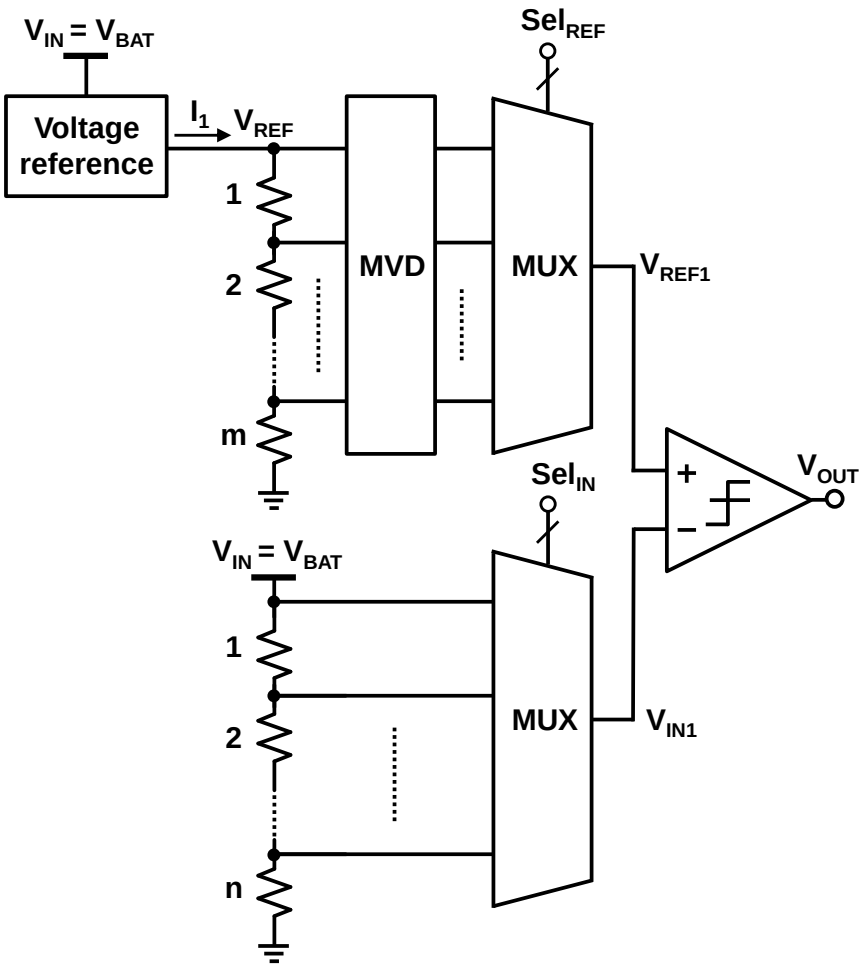


Fig. 4.14 Simplified circuit schematic of the programmable voltage detector (PVD) described in Section 4.2.

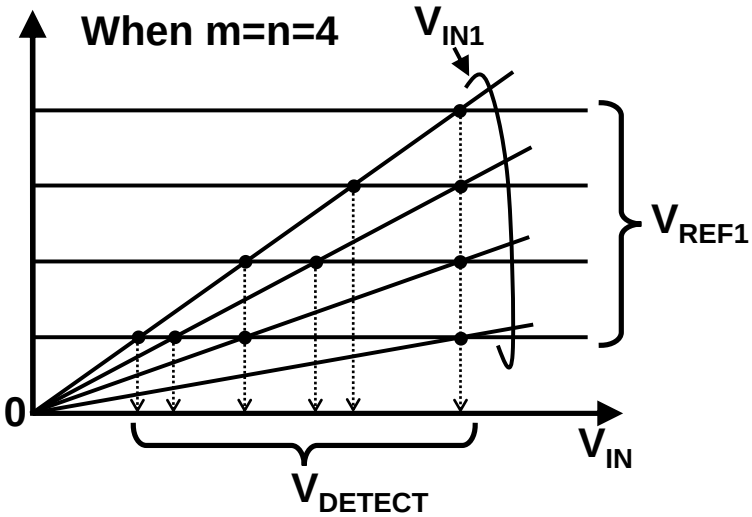


Fig. 4.15 Operation principle of the PVD in Section 4.2.

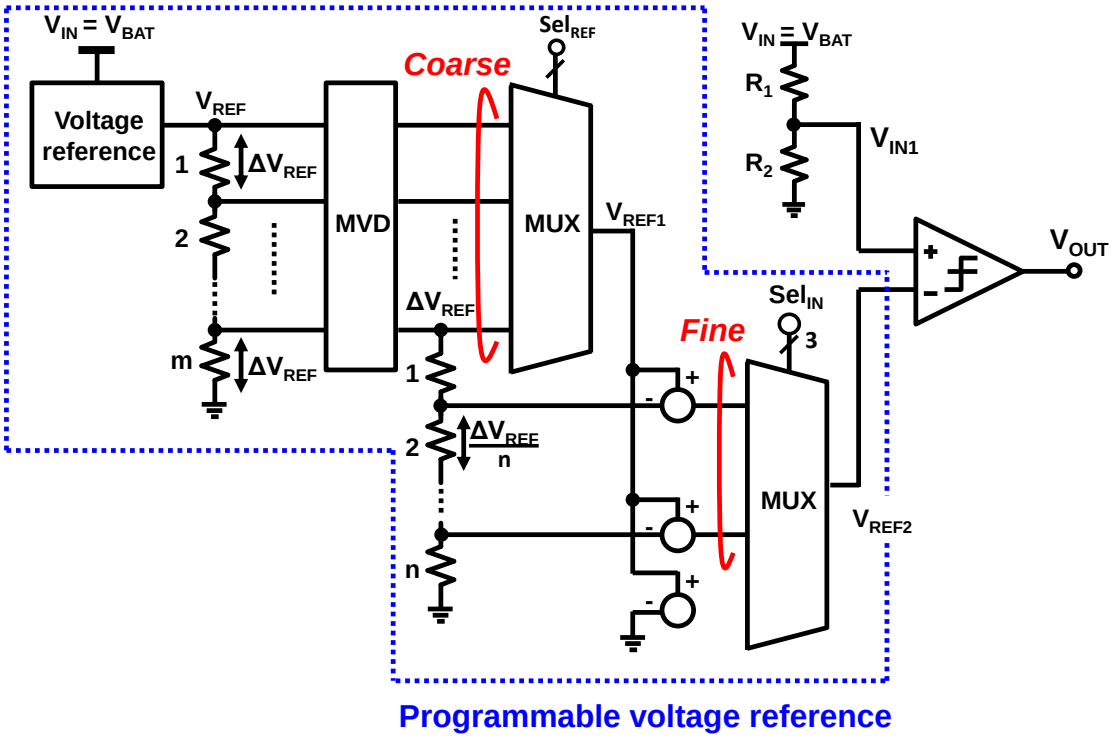


Fig. 4.16 Circuit schematic of proposed PVD with fine voltage-step subtraction (FVS) method.

4.3.3. Proposed Programmable Voltage Detector

Fig. 4.16 shows a circuit schematic of a proposed PVD utilizing the programmable voltage reference (PVREF) with a FVS method. The voltage reference is achieved with the V_{DD}-Regulated Voltage Reference (VRVR) in Chapter 2. In the design, the VRVR achieves ultra-low power sub-1nW power consumption. As mentioned in Chapter 2, the VRVR supplies a temperature/V_{DD}-tolerant V_{REF}. The V_{DD}-independent MVD with the VRVR is applied in the coarse programming. As described in Section 3.4, the PVREF with the FVS method gives the linear and monotonous programmable V_{REF2}. The V_{DETECT} is described as follows:

$$V_{\mathrm{DETECT}} = \frac{1}{k} V_{\mathrm{REF2}} \qquad (0 < k < 1) \tag{4.5}$$

where k is the division ratio of the voltage divider for V_{IN}. By substituting (3.14) into (4.5), the programmed V_{DETECT} is expressed as follows

$$V_{\mathrm{DETECT}} = \frac{1}{k}\left(\frac{i}{m} + \frac{j}{mn}\right) V_{\mathrm{REF}}. \tag{4.6}$$

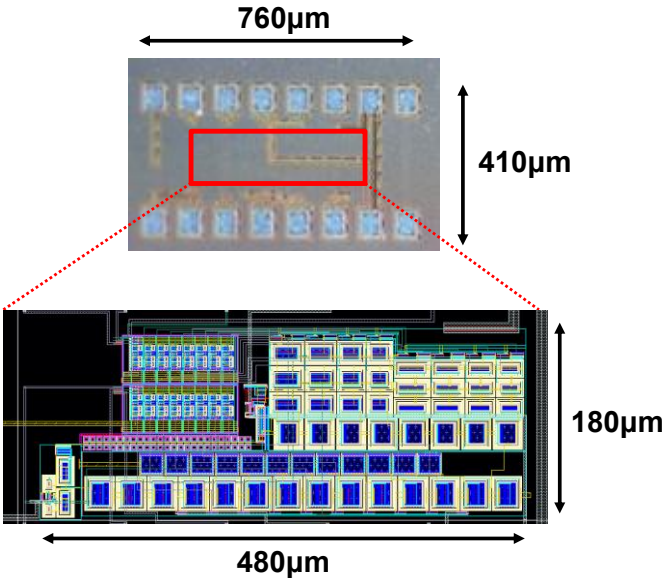
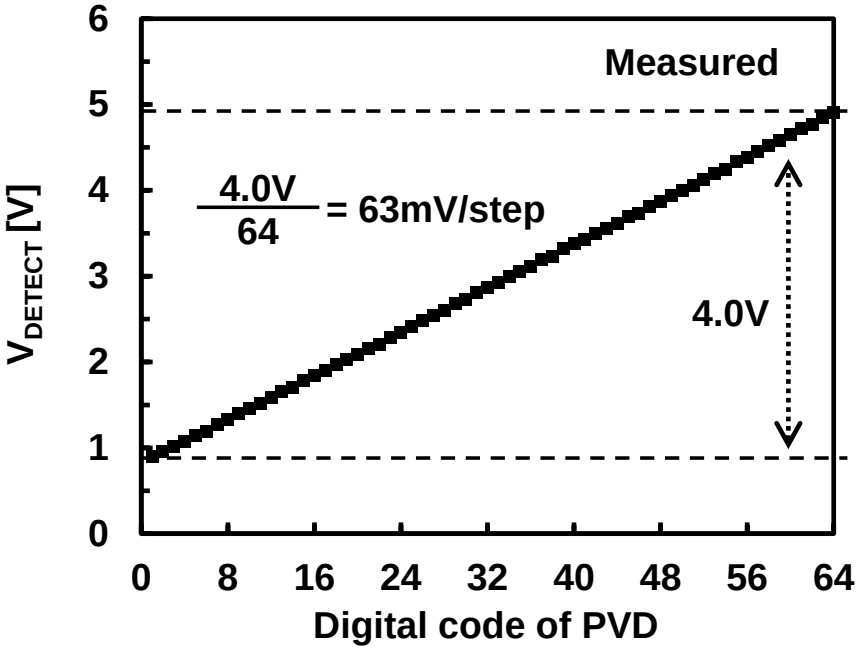


Fig. 4.17 Chip photograph of the proposed PVD..

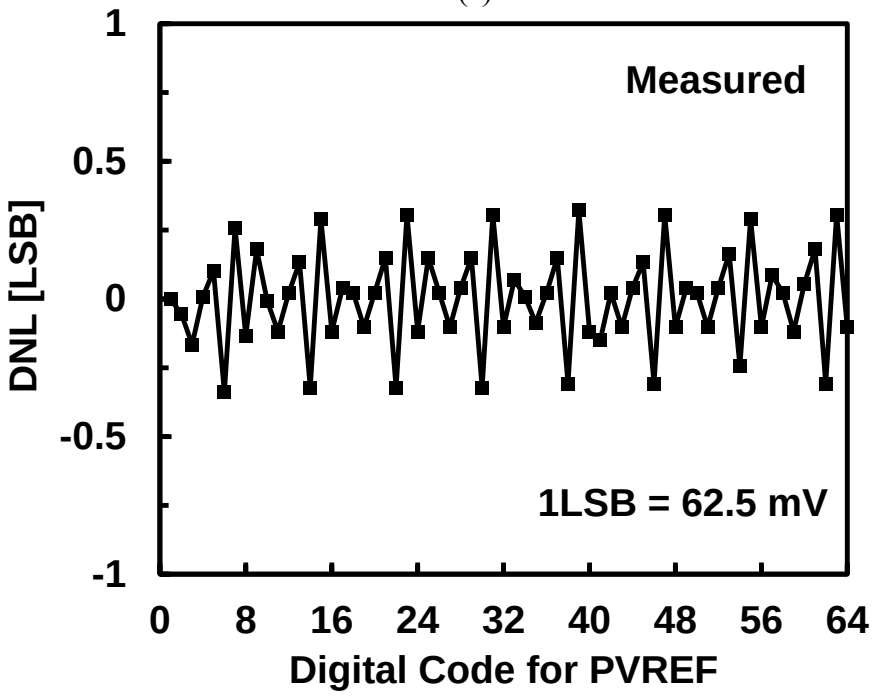
where i and j are selected tap in the voltage dividers for the coarse and fine programming, respectively. As shown in (4.6), by adding coarse voltage steps of V_{REF}/m and fine voltage steps of V_{REF}/mn, both linear V_{DETECT} programmability and fine V_{DETECT} steps are achieved. Thus, in the proposed PVD with the FVS, wide V_{DETECT} range, fine V_{DETECT} steps, linear V_{DETECT} programmability are achieved.

4.3.4. Measurement Results

Fig. 4.17 shows a die photo and a layout of the proposed PVD fabricated in 5V, 250-nm CMOS process. The core area is 480μm by 180μm. Fig. 4.18 (a) shows a measured V_{DETECT} dependence on digital code of the PVD. The PVD with linear 64-level V_{DETECT} ranging from 902mV to 4904mV in steps of 62.5mV is achieved. Fig. 4.18 (b) shows the DNL of the programmed V_{DETECT}. The DNL achieves within -0.26/+0.27 LSB. Fig. 4.19 shows the power consumption of the PVD. The current at 20°C is 1.3nA. Fig. 4.20 shows a measured temperature dependence of V_{DETECT}. The averaged TC is 0.33mV/°C in the temperature range of -20°C to 60°C. In Table 4.2, this work is compared with the previously published voltage detectors. The 64-level programmability of V_{DETECT} ranging from 902 mV to 4904 mV is the largest and the 62.5 mV step is the smallest.



(a)



(b)

Fig. 4.18 (a) Measured V_{DETECT} dependence on digital code of the PVD and (b) its DNL.

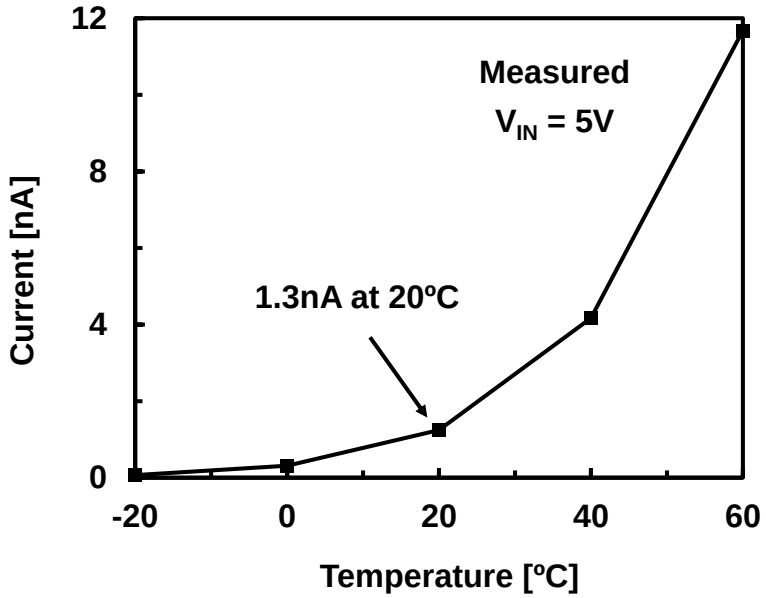


Fig. 4.19 Measured power consumption of the proposed PVD.

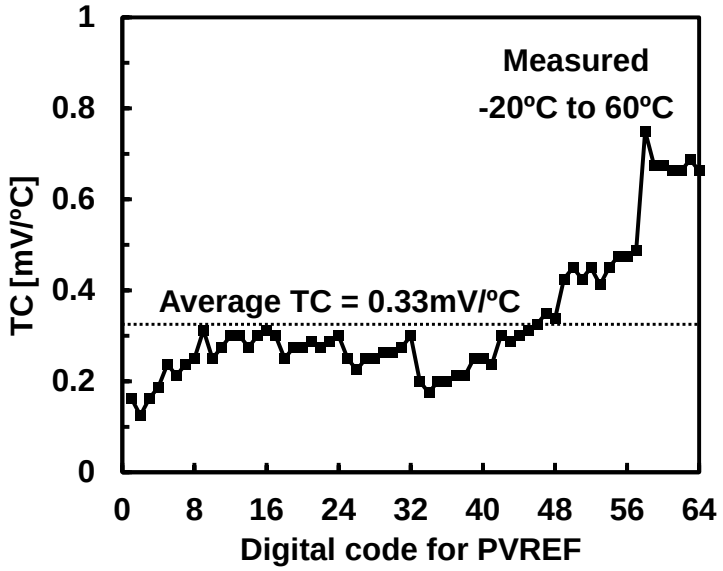


Fig. 4.20 Measured TC of the proposed PVD.

4.3.5. Short Summary

Thanks to the proposed FVS and VRVR, a programmable voltage detector (PVD) with linear 64-level V_{DETECT} ranging from 902 mV to 4904 mV, covering the range for the lithium-ion batteries, in steps of 62.5 mV (=±31.3mV) (<±1% of battery voltage) is achieved for the first time. Thanks to the programmability, the proposed PVD can be a general-purpose component and users can freely change V_{DETECT}. The 64-level programmability is the largest and the 62.5 mV step is the smallest. PVD fabricated in 5V,

Table 4.2 COMPARISON WITH PREVIOUS VOLTAGE DETECTORS

		TPS3839	AP4400A	VLSI'12	ESSCIRC'15	This work
CMOS process		N/A	N/A	180nm	250nm	250nm
Detection voltage	Programmability	No	No	No	Yes	Yes
	Max	4.38V	4.2V	3.58V (Fixed)	0.85V	0.90V
	Min	0.9V	2.0V		0.52V	4.90V
	Range	3.48V	2.2V		0.33V	4.0V
	Number of Steps	9	23	1	21	64
	Uniform step	No	Yes (100mV step)		No	Yes (62.5mV step)
Power		150nA @1.2V (25°C)	20nA @3.4V (25°C)	79pA @3.6V (25°C)	248pA @1.0V (25°C)	1.25nA @5V (20°C)
Temperature coefficient of V_{DETECT}		0.055mV/°C	0.75mV/°C	1.5mV/°C	0.11mV/°C	0.33mV/°C
Temperature range		-40°C to 85°C	-15°C to 85°C	0°C to 80°C	-20°C to 80°C	-20°C to 60°C

250-nm CMOS process shows the measured power consumption of 1.3nA at 20°C and TC of 0.33mV/°C in -20°C to 60°C.

4.4. Effect of Line Sensitivity of Voltage Reference on Programmed V_{DETECT}

Line sensitivity of voltage reference causes a non-linearity of the programmed V_{DETECT}. In this section, the non-linearity of the programmed V_{DETECT} caused by the line sensitivity of the voltage reference is discussed. Fig. 4.21 shows a PVD using a String DAC. The typical characteristics of V_{REF1} and V_{IN1} are shown in Fig. 4.22. The points where V_{REF1} and V_{IN1} intersect are acquired V_{DETECT}. As shown in the figure, the programmed V_{DETECT} has error that causes the non-linearity of the programmed V_{DETECT}. In the PVD, the programmed V_{DETECT} is expressed as fallows

$$V_{\mathrm{DETECT}} = \frac{1}{k}\frac{i+m-l}{m}V_{\mathrm{REF}} \qquad (1 \le i \le l) \tag{4.7}$$

where i and k (0<k<1) mean the selected switch in the programming and divided ratio of V_{IN} shown in Fig. 4.21. Assumed the line sensitivity of V_{REF} (=α) is linear against the V_{DD}, V_{REF} is expressed as follows

$$V_{\mathrm{REF}} = V_{\mathrm{REF,R}} + \alpha(V_{\mathrm{IN}} - V_{\mathrm{IN,R}}) \tag{4.8}$$

where $V_{REF,R}$ is V_{REF} at a reference voltage $V_{IN,R}$. By substituting (4.8) into (4.7) the programmed V_{DETECT} is expressed as follows

$$V_{\mathrm{DETECT}} = \frac{1}{k}\frac{i+m-l}{m}\left(V_{\mathrm{REF,R}} + \alpha(V_{\mathrm{DETECT}} - V_{\mathrm{IN,R}})\right) \tag{4.9}$$

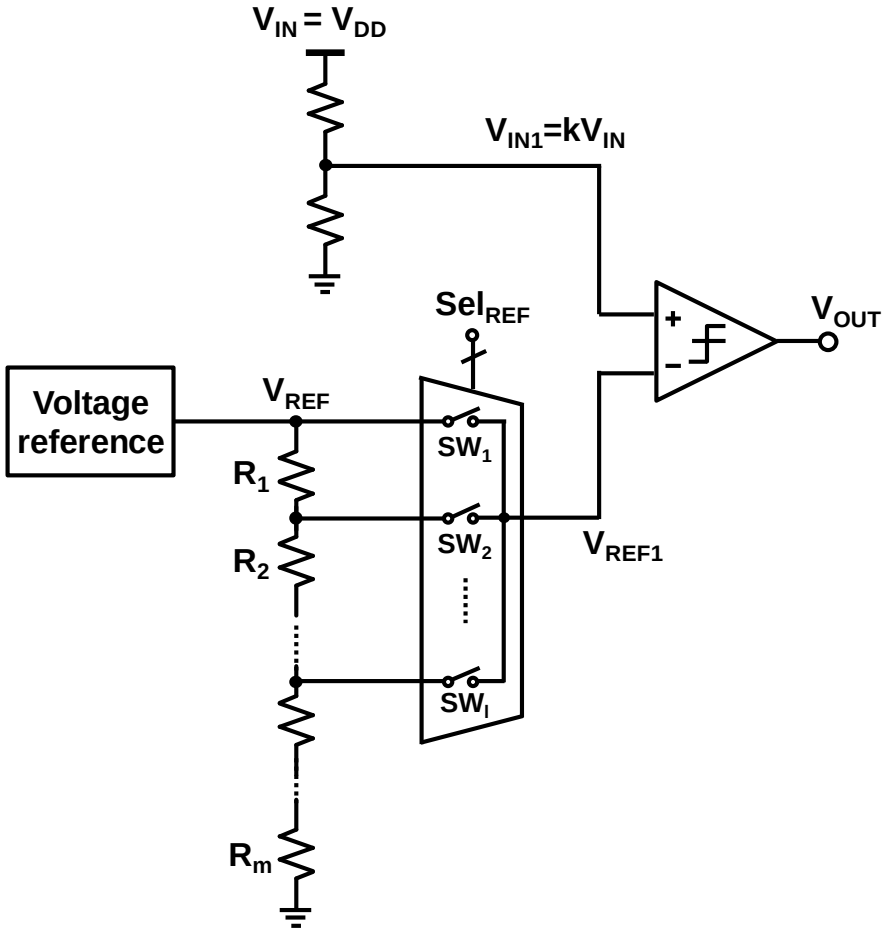


Fig. 4.21 PVD with a String DAC.

From (4.9), error of programmed V_{DETECT} that is defined as the difference between the acquired V_{DETECT} and theoretical V_{DETECT} is expressed as

$$\Delta V_{\text{DETECT,ERROR}} = \frac{1}{k}\frac{i+m-l}{m}\alpha(V_{\text{DETECT}} - V_{\text{IN,R}}) \tag{4.10}$$

Eq.(4.10), shows the error of the programmed V_{DETECT} increases as higher bit of the digital code. The PVD is simulated as shown in Fig. 4.23 with the case of α=2mV/V and 0.02mV/V replicating the LS of re-implemented [4.15] and a proposed VRVR in Chapter 2. $V_{REF,R}$ is set to 0.6V at $V_{IN,R}$ = 0V. The design parameters m, l and k are set to 12, 8 and 1/8, which determine the resolution of the PVD (= 400mV). Compared with theoretical programmed V_{DETECT}, the error of programmed V_{DETECT} at α=2mV/V increases the error as the digital code get closer to MSB. The error causes the non-linearity of the programmed V_{DETECT}. Figs. 4.24 shows the error of the programmed V_{DETECT} that

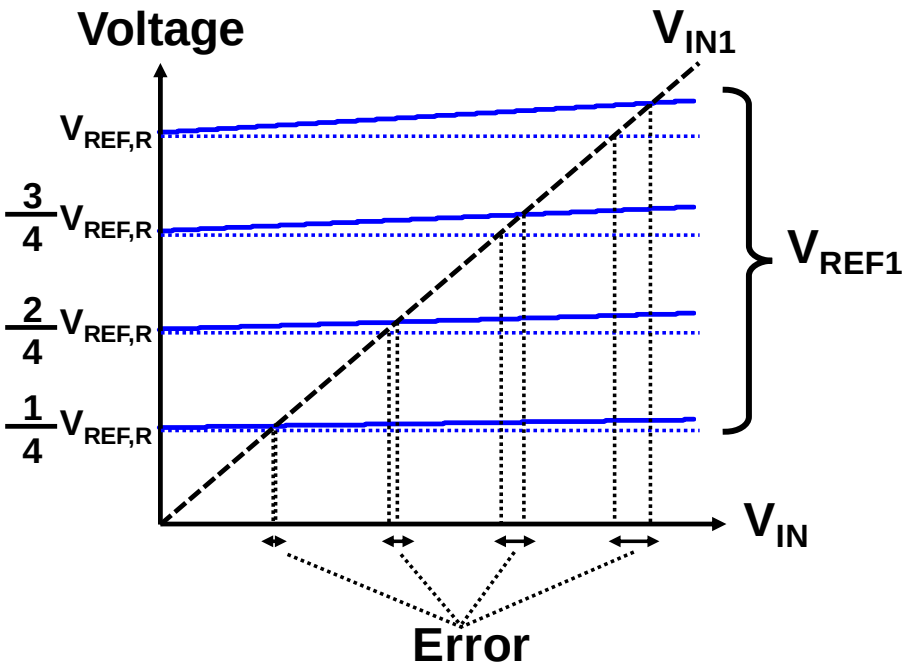


Fig. 4.22 Characteristics of V_{REF1} and V_{IN1} against V_{DD}.

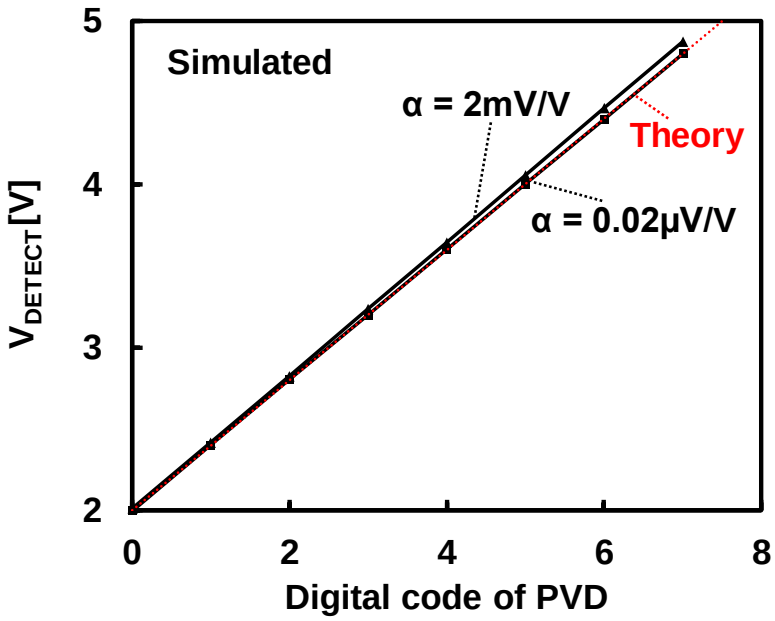
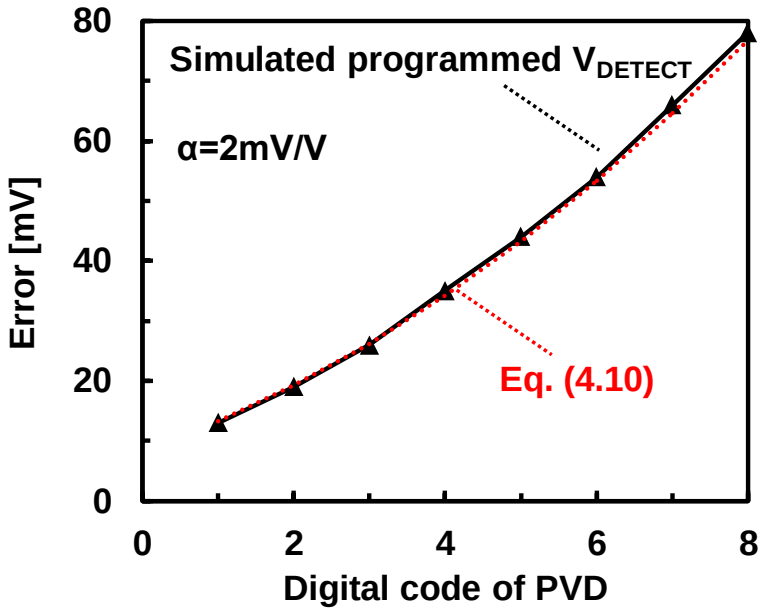
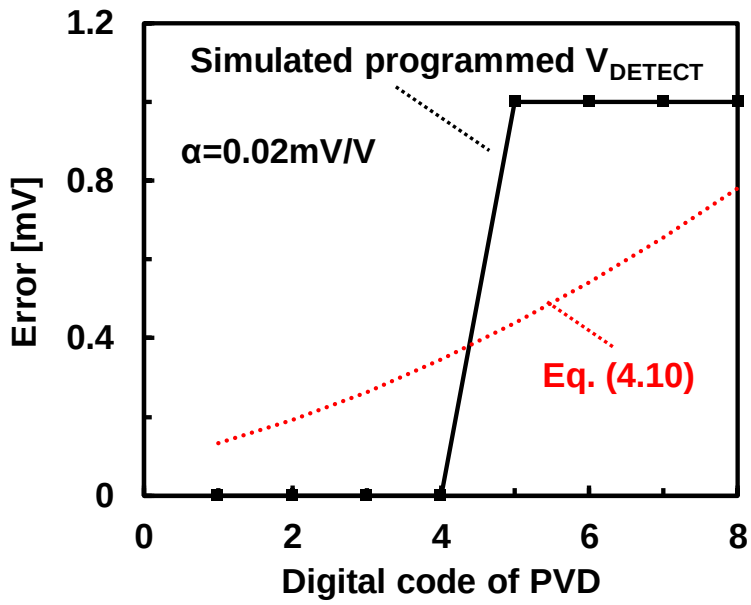


Fig. 4.23 Simulated programmed V_{DETECT}. α is set to 2 mV/V and α is 0.02 mV/V.

obtained by comparing the simulated programmed V_{DETECT} and theoretical programmed V_{DETECT}. On the condition of α is 2 mV/V, the error of the programmed V_{DETEDT} reaches 80mV, that is 20% of the 1LSB (=400mV). On the contrast, in the case of α=0.02μV/V as shown in Fig. 4.24 (b), the error is expressed as 0mV ($1 \leq i \leq 4$) or 1mV ($5 \leq i \leq 8$). The simulated step-like form arise from the resolution of the simulated V_{DETECT} that is 1mV.



(a)



(b)

Fig. 4.24 Simulated error programmed V_{DETECT}. (a) α = 2 mV/V. (b) α = 0.02 mV/V.

From the theoretical analysis and the simulated results, the programmed V_{DETECT} with the voltage reference that has LS of 0.02μV/V reduces the error to less than 1mV. Therefore, the LS of the VRVR shown in Chapter 2 is sufficiently small not to effect on the accuracy of the programmed V_{DETECT}.

4.5. Summary

This chapter introduced two voltage detectors for battery management. The extension of the battery life and the enhancement of the safety are critical issues in the battery management. The two voltage detectors are promising circuits to overcome these issues. The VD proposed in Section 4.2 is proposed for a battery management with RF energy harvesting. RF energy harvesting is expected to extend the battery life and realize the energy autonomous applications. For the RF energy harvesting, a VD needs to operate at ultra-low power since it is always-on. Also, the VD must operate properly even though V_{IN} is close to 0V since the glitch generated by the VD at low V_{DD} spoils the energy charging for the storage. The proposed VD fabricated in 250-nm CMOS process realizes the ultra-low power (248pW), glitch-free operation with the little temperature coefficient of 0.11mV/°C in -20°C to 80°C. In addition, the post fabrication trimming method that mitigates the process variation of the V_{DETECT} is proposed. A multiple voltage duplicator (MVD) proposed in Section 3.3 realizes the V_{DETECT} trimming in the accuracy of 49mV with little increase in the temperature coefficient and the power consumption. The VD stands out in the applications which the input voltage is small or the robust V_{DD} is not available. In Section 4.3, a field programmable voltage detector (PVD) utilizing a programmable voltage reference with the fine voltage subtraction method described in Section 3.4 is proposed. The typical usage of the PVD is battery management including battery protection and battery charge/discharge control. The PVD achieves user-end programmability of V_{DETECT} in the range of operating voltage of most of batteries (e.g., 3.0 V to 4.2 V for a lithium-ion battery). The programmability is beneficial in that it decreases the cost of the VD because we can reduce the number of the VDs. The test-chip is fabricated in 250-nm CMOS process. The measurement results show that the programmability covers 6-bit programmable V_{DETECT} in the range of 902 mV to 4904 mV in steps of 62.5mV. The DNL is a sufficiently small value of -0.26/+0.27 LSB. The power consumption is 1.3 nA at 20 °C. The programmability covers the operating voltage of lithium-ion batteries with a sufficiently fine resolution of 62.5 mV. The range and the resolution of the programmed V_{DETECT} show that the VD has applicability to small capacity lithium-ion batteries that require the detection accuracy of ±42 mV for battery charging.

4.6. Appendix

4.6.1. Variation of Programmable Voltage Detector with Fine Voltage Subtraction

In Section 4.3, a PVD utilizing the FVS method is proposed to achieve linear, monotonous programmability. Fig. 4.25 shows a variation of the PVD with FVS method. Fig. 4.26 shows the operation principle of the PVD. A hierarchy of a coarse voltage divider for V_{REF1} and fine voltage divider of V_{IN1} is used. The difference between the PVD in Section 4.3 and the PVD in Fig. 4.25 is the fine step voltage ($=\Delta V_{REF}/n$) is subtracted from V_{IN1} ($=V_{IN}/k$) which is the divided voltage of V_{IN}. The theoretical programmed V_{REF} is introduced to (4.6). Fundamentally, the two PVDs show about the same characteristics. Fig. 4.27 shows the programmed V_{DETECT} achieved by PVD in Fig. 4.25. 56 level programmable V_{DETECT} with the resolution of 50mV is achieved. The V_{DETECT} ranges from 1.88V to 4.67V. The obtained characteristics of programmed V_{DETECT} is slightly different from the measurement results in Section 4.3, this is due to the difference of design parameters including the number of the resistors for the ladders, the selected tap in the ladders for the programming and V_{REF1}. The measurement results of Fig. 4.25 topology is also described in [4.25].

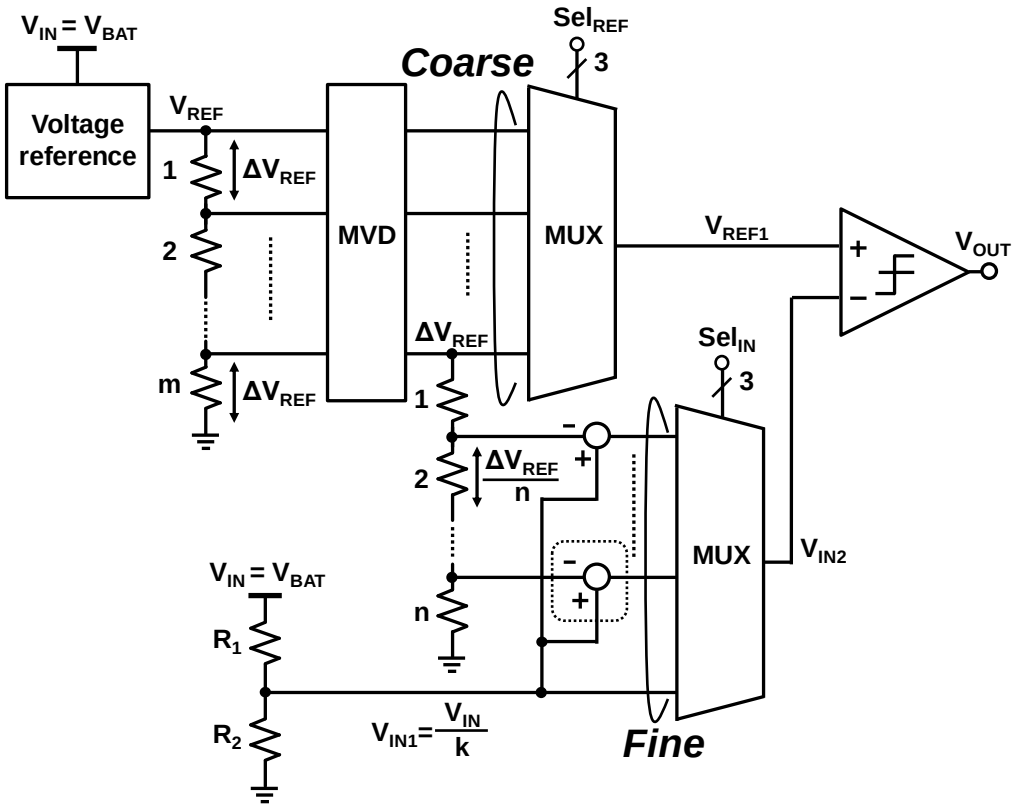


Fig. 4.25 Variation of PVD with FVS.

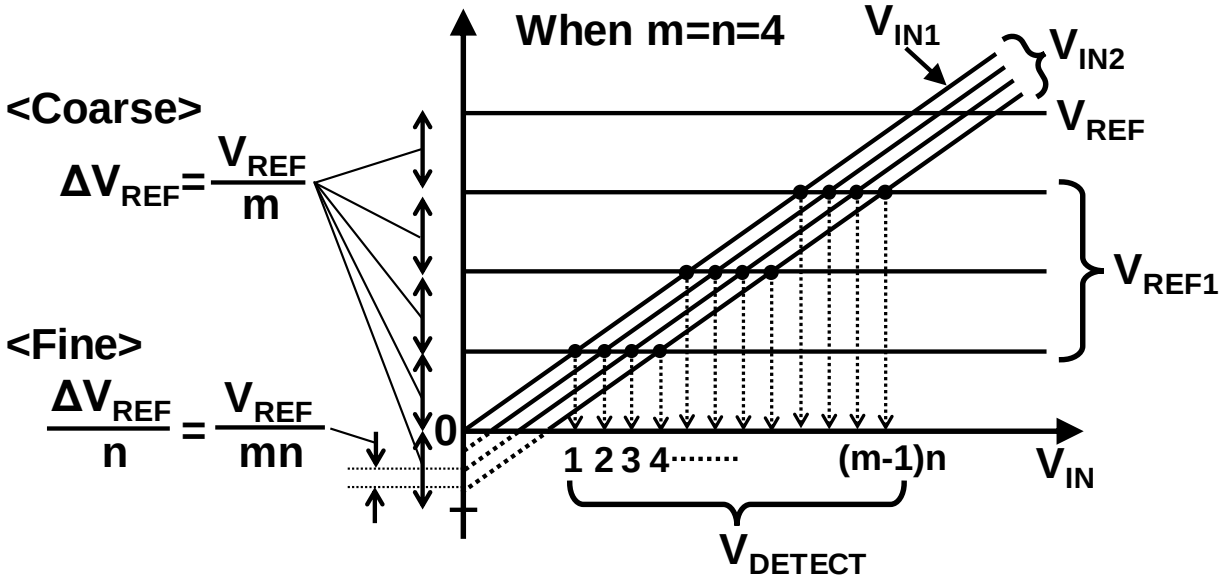


Fig. 4.26 Concept of the PVD with FVS.

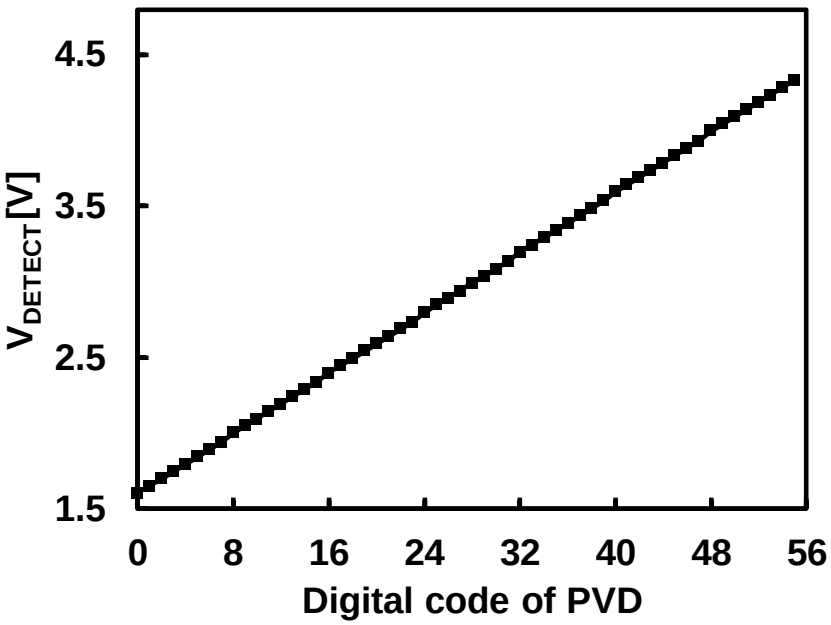


Fig. 4.27 Simulated programmed V_{DETECT}.

References

[4.1] Datasheet of TPS3839, Texas Instruments.

[4.2] Datasheet of S-1000, Seiko Instruments Inc.

[4.3] Datasheet of AP4400A, Asahi Kasei Microdevices Corporation.

[4.4] S. Takahashi, N. Yoshida, K. Maruhashi, and M. Fukaishi, "Real-Time Current-Waveform Sensor with Plugless Energy Harvesting from AC Power Lines for Home/Building Energy-Management Systems," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 220–221, 2011.

[4.5] F. Zhang, Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, B. Otis, and B. Calhoun, "A Batteryless 19μW MICS/ISM-band Energy Harvesting Body Area Sensor Node SoC," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 298–299, 2012.

[4.6] H. Kitayoshi, K. Sawaya, and H. Kuwano, "Experimental Study on Low-Power Wireless Monitor of Rotary Motion using Improved Energy Harvesting System with Piezoelectric Element," in *Proc. IEEE SENSORS*, pp. 174–177, 2014.

[4.7] D. Balsamo, G. Gallo, D. Brunelli, and L. Benini, "Non-Intrusive Zigbee Power Meter for Load Monitoring in Smart Buildings," in *Proc. IEEE Sensors Applications Symp.*, pp. 1–6, 2015.

[4.8] P. C. Jain, "Recent Trends in Energy Harvesting for Green Wireless Sensor Networks," in *Proc. IEEE Int. Conf. Signal Processing and Communication*, pp. 40–45, 2015.

[4.9] S. Oh and D. Wentzloff, "A -32dBm Sensitivity RF Power Harvester in 130nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium*, pp. 483–486, 2012.

[4.10] R. Shigeta, T. Sasaki, D. M. Quan, Y. Kawahara, R. J. Vyas, M. M. Tentzeris, and T. Asami, "Ambient RF Energy Harvesting Sensor Device With Capacitor-Leakage-Aware Duty Cycle Control," *IEEE Sensors J.*, vol. 13, no. 8, pp. 2973–2983, 2013.

[4.11] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, 2011.

[4.12] Y. Osaki , T. Hirose , N. Kuroki and M. Numa "1.2 V supply, 100 nW, 1.09 V bandgap and 0.7 V supply, 52.5 nW, 0.55 V subbandgap referencecircuits for nanowatt CMOS LSIs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, 2013.

[4.13] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff and B. H. Calhoun "A 32 nW bandgap reference voltage operational from 0.5 V supply for ultra-low power systems," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 94–95, 2015.

[4.14] K. K. Lee, T. S. Lande and P. D. Häfliger, "A Sub-μW Bandgap Reference Circuit With an Inherent Curvature-Compensation Property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 1-9, 2015.

[4.15] M. Seok, G. Kim, D. Sylvester, and D. Blaauw, "A 0.5V 2.2pW 2-transistor voltage reference," in *Proc. IEEE Custom Integtated Circuits Conference (CICC)*, pp. 577–580, 2009.

[4.16] P. H. Chen, K. Ishida, K. Ikeuchi, X. Zhang, K. Honda, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "Startup Techniques for 95 mV Step-up Converter by Capacitor Pass-on Scheme and VTH-tuned Oscillator with Fixed Charge Programming," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1252–1260, 2012.

[4.17] I. Lee, S. Bang, Y. Lee, Y. Kim, G. Kim, D. Sylvester, and D. Blaauw, "A 635pW Battery Voltage Supervisory Circuit for Miniature Sensor Nodes," in *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, pp. 202–203, 2012.

[4.18] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, 2011.

[4.19] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, 2012.

[4.20] H. Fuketa, R. Takahashi, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Variation-Aware Subthreshold Logic Circuit Design," in *Proc. Int. Conf. ASIC*, pp. 95–98, 2013.

[4.21] S. Dearborn, "Charging Li-ion Batteries for Maximum Run Times," *Power Electronics Technology*, pp. 1–10, 2005.

[4.22] Datasheet of BQ25504, Texas Instruments.

[4.23] T. Someya, H. Fuketa, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "Voltage detector with multiple voltage duplicator for energy harvesting," in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, pp. 249–252, 2015.

[4.24] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 1976.

[4.25] T. Someya, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "56-Level Programmable Voltage Detector in Steps of 50mV for Battery Management," in *Proc. Asian Solid-State Circuits Conference (A-SSCC)*, pp. 49–52, 2016.

Chapter 5: Ultra-Low Power Temperature Sensor

5.1. Introduction

Real time thermal management using a temperature sensor is one of the typical applications in the Internet of Things (IoT). The temperature sensing is also critical for battery management including battery state estimation and battery protection. Recently, miniature thin-film batteries have been developed for IoT devices. They are so thin and small that they are suitable for applications that are required to be small or light although the capacities are limited. One feature of the batteries is the large internal resistance R_{BAT} (e.g., 60kΩ after 1000 cycles [5.1]) that limits the maximum supply current. Assuming that R_{BAT} is 60kΩ and the acceptable voltage drop is 100mV, the maximum instantaneous current from the battery (I_{MAX}) is limited to the only 1.7μA. In such situations, reducing the maximum current of the IoT node becomes critical. As a temperature sensor is just one among many components in the system, reducing the average current of the sensor to less than 1% of I_{MAX} (=17nA) is a challenging issue. Recently, ultra-low power temperature sensors that convert the temperature to time or frequency without ADC to reduce the power consumption [5.2,5.3,5.5,5.6] have been proposed. [5.5] shows that a reference-free current-to-frequency converter (CFC) based temperature sensor with an appropriate fitting model can achieve high accuracy of -0.76/+0.76°C. [5.5], however, requires off-chip processing due to the nonlinear fitting model, preventing real-time thermal management. [5.2,5.3] propose on-chip sensors with PTAT digital output that does not require off-chip processing. [5.2] utilizes a proportional to absolute temperature (PTAT) voltage generator, while [5.3] utilizes a linear approximation of the ratio between two sub-threshold currents operating at different gate voltages. Though [5.6] presents 113pW temperature-to-digital converter, the temperature range of -20°C to 40°C does not fit typical battery operating temperature range (e.g., -20°C to 70°C [5.1]).

In this chapter, a sub-14nW temperature-to-digital converter with PTAT digital output is proposed. Related to the temperature sensor, (1) a new temperature sensing principle that is highly linear to temperature, (2) a new sub-thermal drain voltage (V_{DS}) based current generator, and (3) relaxation oscillator based current-to-frequency converter and asynchronous counter based frequency ratio computation for digital output, are reported. The temperature-to-digital converter achieves the lowest power consumption of 13nW at

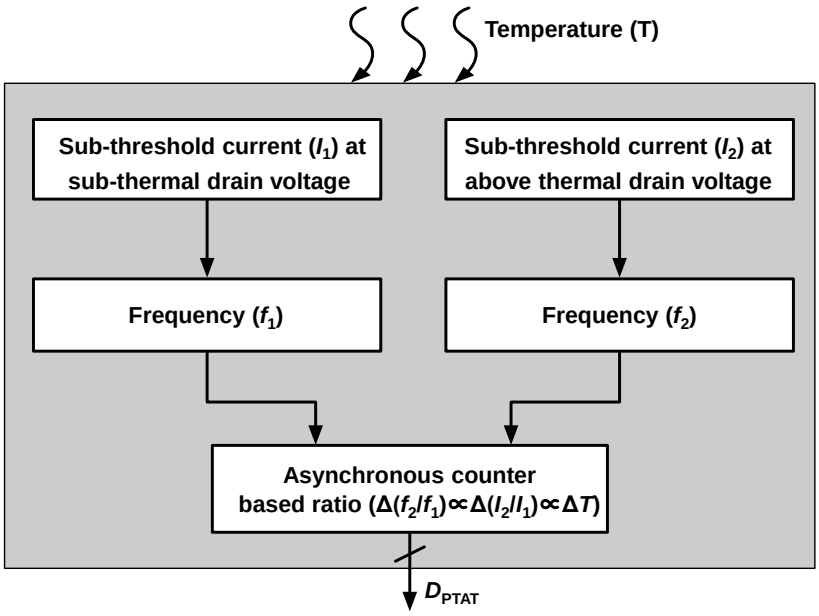


Fig. 5.1 Flow chart of the proposed temperature-to-digital converter.

0.8V supply with 110mK resolution and -0.7/+1.3°C inaccuracy over the temperature range of -20°C to 80°C.

5.2. Design of Proposed Temperature-to-Digital Converter

Fig. 5.1 shows the flow chart of the proposed temperature-to-digital converter. The sensor includes generation of two sub-threshold currents with different drain voltages (I_1, I_2), the current conversion into frequencies (f_1, f_2), frequency ratio (f_2 / f_1) calculation for PTAT digital output (D_{PTAT}).

A. Proposed temperature sensing mechanism

Figs. 5.2 show the operating principle of the proposed temperature sensing mechanism. A pair of MOSFETs operating in sub-threshold region is biased with two different V_{DS} values. A sub-thermal drain voltage (STV) less than the thermal voltage V_T (=26mV at 27°C) is applied to V_{DS1} of M_{A1}, while above thermal drain voltage (ATV) more than $3V_T$ is applied to V_{DS2} of M_{B1}. As a result, drain currents of M_{A1} operating in the deep triode region and M_{B1} operating in the saturation region are expressed as follows:

$$I_1 = K \cdot e^{\frac{q(V_{GS1}-V_{TH})}{nkT}} \cdot (1 - e^{\frac{-qV_{DS1}}{kT}}) \tag{5.1}$$

$$I_2 = K \cdot e^{\frac{q(V_{GS1}-V_{TH})}{nkT}} \tag{5.2}$$

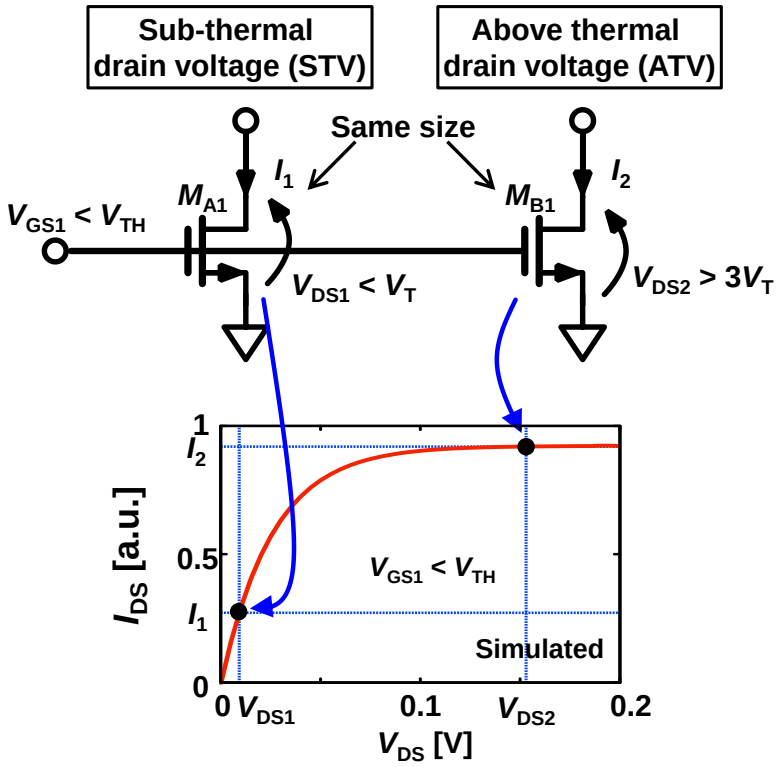
where k is the Boltzmann constant, q is the electron charge, T is the absolute temperature, n is the sub-threshold swing parameter, V_{TH} is the threshold voltage, and K is a pre-exponential factor that is dependent on the temperature. The current ratio of I_2/I_1 becomes a function of V_{DS1} and T as follows:

$$\frac{I_2}{I_1} = \frac{1}{1-e^{\frac{-qV_{DS1}}{kT}}} \approx \frac{kT}{qV_{DS1}} + C \tag{5.3}$$

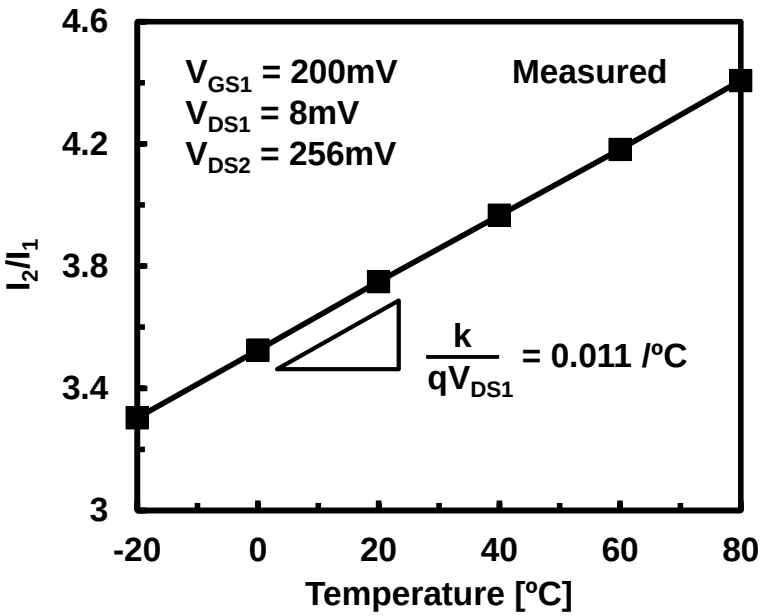
where C is a temperature-independent constant that can be removed by calibration. Eq. (5.3) shows that $\Delta(I_2/I_1)$ is proportional to ΔT which is confirmed from a single transistor current measurement in Fig. 5.2 (b). With a V_{DS1} value of 8 mV, the current ratio has a high sensitivity of 0.011/°C. The theoretical slope (=0.0108/°C) matches with the measured slope. The sensitivity is further improved by adding finer V_{DS1}.

B. Temperature-to-current conversion

To implement the proposed principle of the temperature sensor shown in Fig. 5. 2 (a) and Eq. (5.3), temperature and supply voltage-independent V_{DS1} is required. Therefore, an op-amp-free V_{DS1} bias circuit required is proposed. Fig. 5. 3 (a) shows the proposed op-amp-free current generator including the V_{DS1} bias circuit. Firstly, a reference voltage (V_{REF}) is divided by a 50-stage diode chain to generate small ΔV (=V_{REF}/50) value of around 8 mV. ΔV is then copied as V_{DS1} of the STV MOSFET (M_{A1}) utilizing stacked MOSFETs. As the STV MOSFET operates in the deep triode region, V_{DS1} does not settle to ΔV for the case where only one stacked device (k=1) is used. By increasing the stack number (k), the V_{DS1} value becomes closer to ΔV and the temperature dependence gets reduced. Fig. 5.3 (b) shows the simulated temperature characteristics of V_{DS1} with various k. The stack value of k=16 achieves a temperature dependence of 2.2μV/°C which is small enough not to affect the sensor accuracy. As the ATV MOSFET (M_{B1}) operates in the saturation region, V_{DS2} is equal to $V_A - V_B$ which is around 128 mV. Thus, the proposed technique achieves constant V_{DS1} and V_{DS2} without the use of power-hungry op-amps.

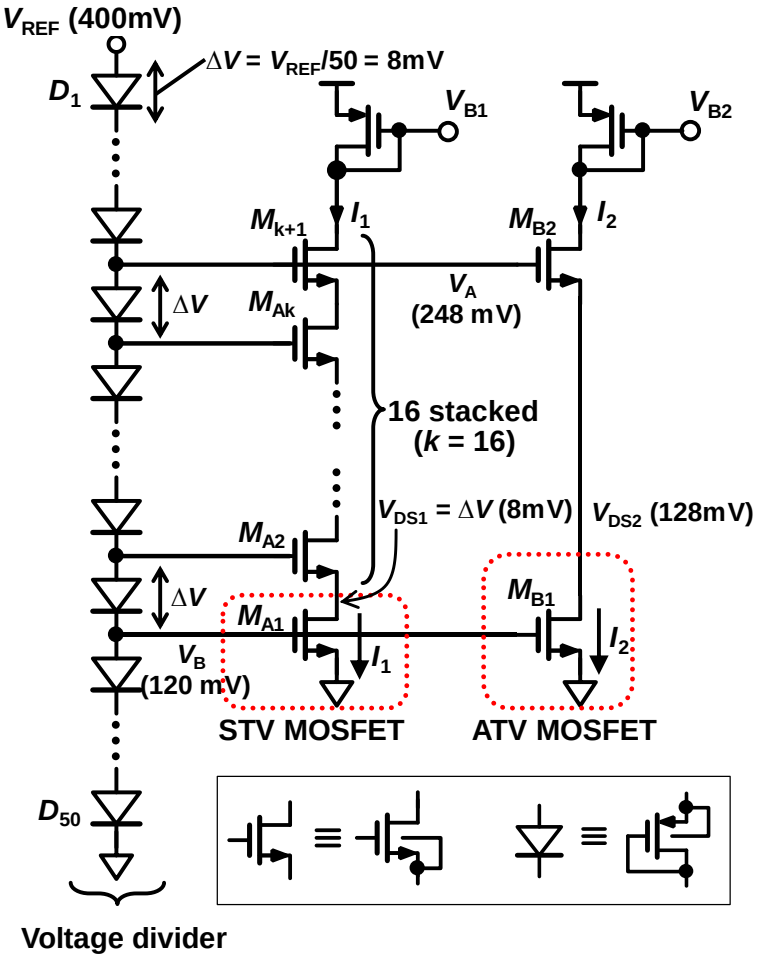


(a)

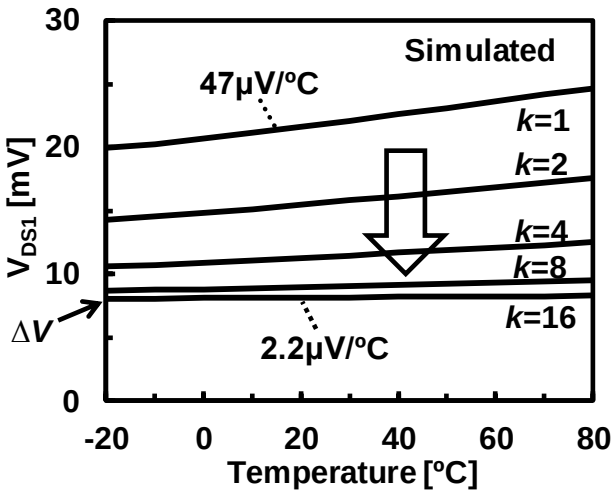


(b)

Fig. 5.2 Proposed temperature sensing mechanism. (a) V_{DS} biasing of a MOSFETs for deep triode and saturation region operation, and the sub-threshold drain current vs V_{DS}. (b) Measured I_2/I_1 of a single transistor.



(a)



(b)

Fig. 5.3 (a) Circuit schematic of current generator using STV and ATV MOSFETs. (b) Temperature dependence of V_{DS1}.

C. Proposed temperature-to-digital converter

Fig. 5.4 shows the overall block diagram of the proposed temperature-to-digital converter. Two CFCs along with two counters provide on-chip digital conversion of I_2/I_1 without the help of external clock reference. The current ratio I_2/I_1 is converted into f_2/f_1 using two CFCs. CLK2 edge is counted until CLK1 edge is counted 1024 times achieving a resolution of around 110mK. The output of counter 2 is then latched and kept until the next measurement.

For high accuracy and wide supply operation, the oscillation frequency needs to be highly linear to I_1 or I_2. This is achieved by employing relaxation oscillator based CFCs as shown in Fig. 5.5 (a). The oscillation period of the CFC1 is expressed as follows:

$$T_{\mathrm{OSC},1} = N_{\mathrm{CELL}} \cdot \left(\frac{CV_{\mathrm{REF2}}}{I_1} + t_{\mathrm{C,FALL}} + t_{\mathrm{C,RISE}} \right) \tag{5.4}$$

where N_{CELL} is the number of the delay cells in the CFC1, $t_{\mathrm{C,FALL}}$ and $t_{\mathrm{C,RISE}}$ are propagation delays in Fig. 5.5 (b). V_{REF2} is the threshold voltage for comparators in the delay cells obtained from the diode chain in Fig. 3 (a). The oscillation period of the CFC2 ($=T_{\mathrm{OSC},2}$) is also achieved from (4) by exchanging I_1 with I_2. $t_{\mathrm{C,FALL}}$ and $t_{\mathrm{C,RISE}}$ need to be as small as possible since it decreases the linearity of the temperature-to-digital converter. Fig. 5.5 (a) shows a delay cell used in the CFCs that utilizes a two-stage op-amp. Fig. 5.5 (b) shows the timing diagram of the proposed delay cell in the CFCs. In the op-amp, the 1st stage is a common-source amplifier with a pMOSFET current mirror load working as a comparator. The negative input is biased at V_{REF2} ($<V_{\mathrm{TH}}$) so that the threshold voltage of the comparator is set to V_{REF2}. In the 2nd stage, a common-source amplifier with large load resistor is implemented to reduce $t_{\mathrm{C,RISE}}$. In order to achieve sub-1nW static power consumption in the delay cell, the resistor (R) should be large (e.g. 5GΩ) which is implemented with an off-transistor. However, the large R increases $t_{\mathrm{C,FALL}}$ due to the limited current I_{R}. To reduce $t_{\mathrm{C,FALL}}$, a feed-forward path composed of SW1 and SW2 is added in the 2nd stage in Fig. 5.5 (a). When IN changes from low to high, OUT is pulled down by SW2 and $t_{\mathrm{C,FALL}}$ is reduced. In the temperature range of -20°C to 80°C, simulated peak-to-peak temperature inaccuracy using I_2/I_1 from the current generator is 0.48°C after 2-point calibration. After the conversion to frequency ratio (f_2/f_1) using the CFCs of Fig. 5.5 (a), the peak-to-peak inaccuracy degrades only to 0.58°C. Thus, ultra-

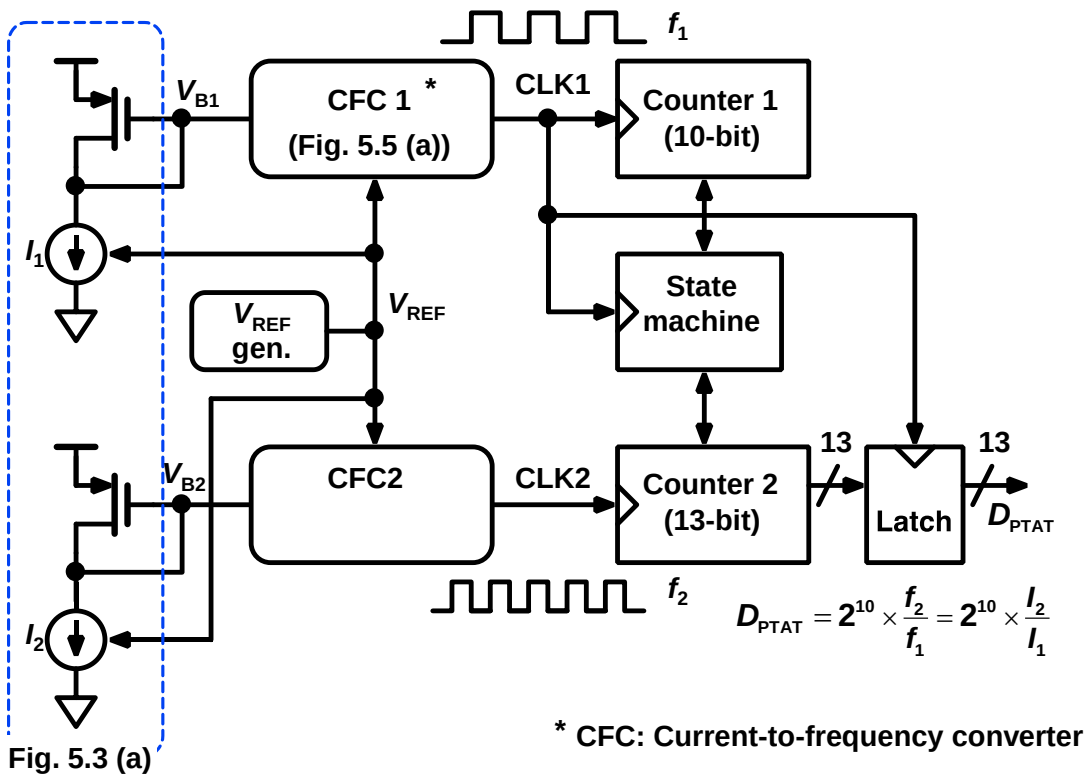
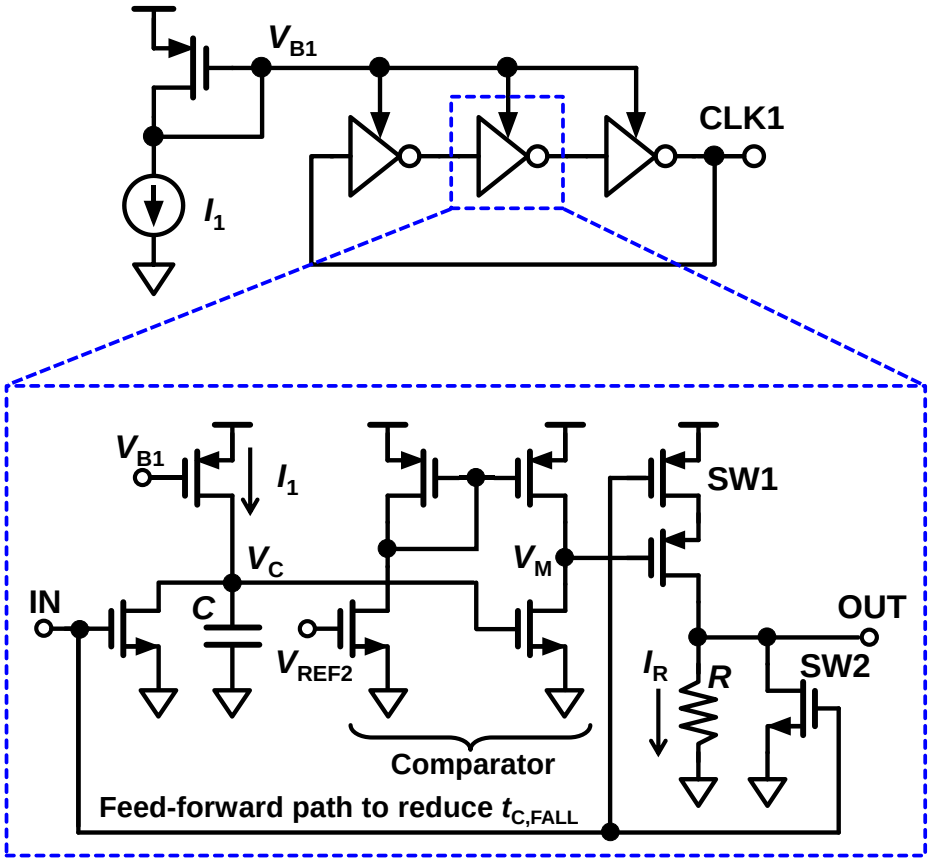


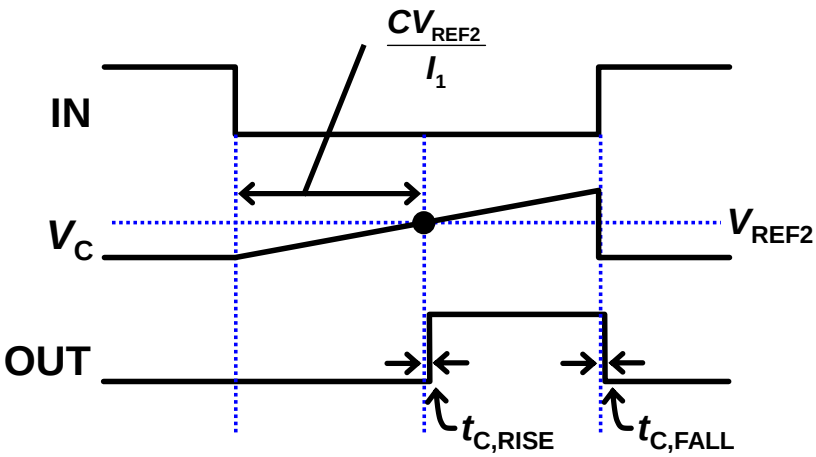
Fig. 5.4 Overall block diagram of the proposed temperature-to-digital converter.

low-power frequency conversion has been achieved without the degradation of temperature sensing accuracy.

The voltage reference for V_{REF} generator in Fig. 5.4 is a key circuit that makes the temperature-to-digital converter reference-free and insensitive to V_{DD}. In the design, a V_{DD}-regulated voltage reference (VRVR) in Chapter 2 is used.



(a)



(b)

Fig. 5.5 Current-to-frequency converter. (a) Schematic. (b) Timing diagram.

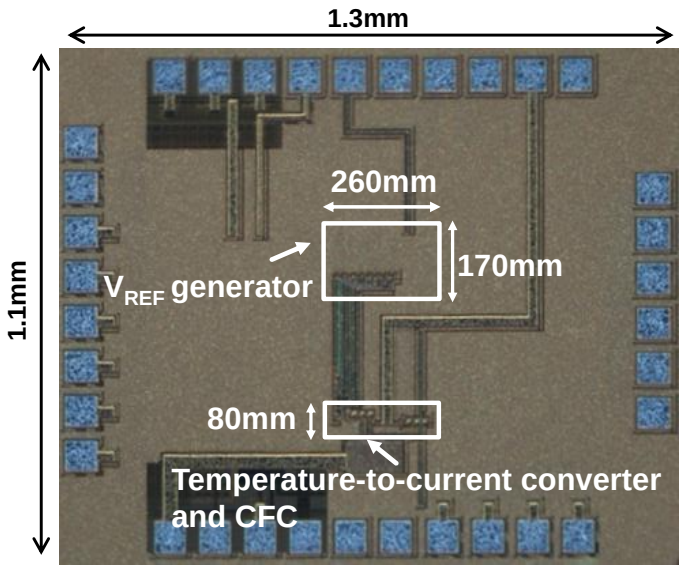


Fig. 5.6 Die photo of the proposed temperature-to-digital converter.

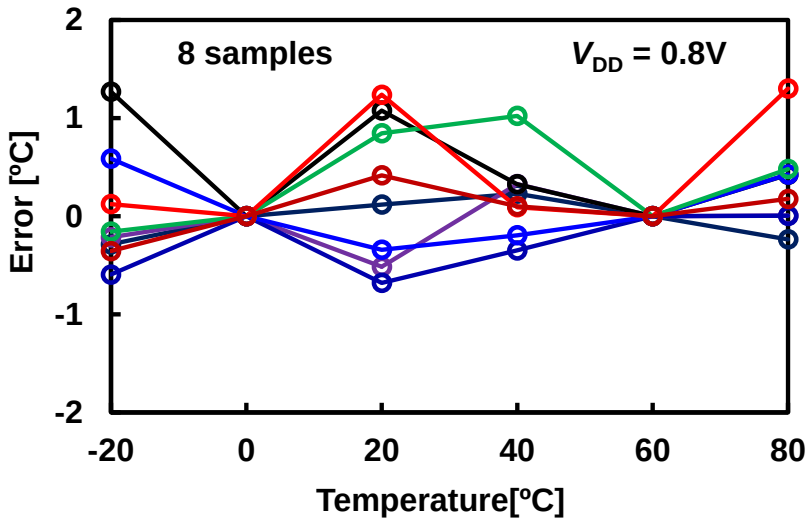


Fig. 5.7 Measured temperature inaccuracy.

5.3. Measurement Results

To verify the proposed temperature-to-digital converter, analog blocks shown in Fig. 5.4 are fabricated in 1.8V, 180-nm CMOS. f_1 and f_2 are measured with the oscilloscope and the temperature characteristics are obtained from f_2/f_1. The digital blocks in Fig. 5.4 are designed with the standard cells and the power consumption of the digital block is simulated. Fig. 5.6 shows a die photo of the proposed temperature-to-digital converter. The sensor has a total area of 0.065 mm^2. Fig. 5.7 shows the measured

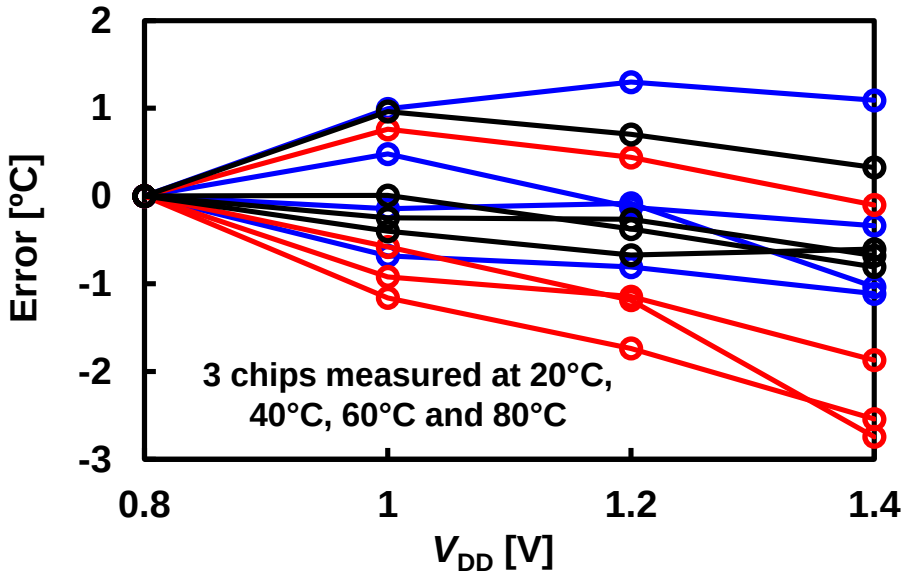


Fig. 5.8 V_{DD} dependence of temperature inaccuracy.

temperature inaccuracy for 8 chips operating at 0.8V. After a 2-point calibration, the peak-to-peak inaccuracy is -0.7/+1.3°C. Fig. 5.8 shows the measured V_{DD} dependence of temperature inaccuracy for 3 chips at 20°C, 40°C, 60°C and 80°C. Taking f_2/f_1 at 0.8V as reference, peak-to-peak inaccuracy over a V_{DD} range from 0.8 to 1.4 V is -2.7/+1.3°C for a wide temperature range of 20 to 80°C. The worst peak-to-peak line sensitivity among 3 chips for different temperature measurements is 4.6°C/V.

Fig. 5.8 summarizes the measurements and compares MOSFET based temperature sensors. The proposed sensor consumes the lowest power of 13nW at room temperature of 25°C while achieving inaccuracy of -0.7/+1.3°C. Current generators and CFCs consume 6.2 nW, V_{REF} generator and digital backend consumes 0.24 nW and 6.4 nW, respectively.

5.4. Summary

An ultra-low power external-reference-free temperature-to-digital converter utilizing sub-threshold MOSFET operation at sub-thermal drain voltage was proposed. The proposed temperature-to-digital converter realizes PTAT digital output that eliminates an off-chip processing with nonlinear fitting model. The total power consumption is 13nW at room temperature, which is the lowest power consumption among previous publications thanks to the current-ratio based temperature sensing principle and op-amp-free current generation circuits. Measurement results show that the proposed temperature-

to-digital converter fabricated in 180-nm CMOS realizes -0.7/+1.3°C inaccuracy over a temperature range of -20°C to 80°C with a resolution of 110mK.

Table 5.1 COMPARISON WITH MOSFET BASED LOW POWER TEMPERATURE SENSORS

	[5.2]	[5.3]	[5.4]	[5.5]	This work
CMOS process [nm]	180	65	65	180	180
PTAT digital output	Yes	Yes	Yes	No	Yes
Area [mm^2]	0.09	0.022	0.004	0.22	0.065
Supply voltage	1.2	0.4	0.85 ~ 1.05	1.2	0.8 ~ 1.4
Power [nW]	71	280	154000	570	13
Energy/conversion [nJ]	2.2	7	3.4	4.6	11
Temp. range [ºC]	0 ~ 100	0 ~ 100	0 ~ 100	-20 ~ 80	-20 ~ 80
Inaccuracy [ºC]	-1.4/+1.5 (2-point)	-1.6/1.0 (2-point)	-0.9/0.9 (2-point)	-0.76/0.76 (2-point)	-0.7/1.3 (2-point)
Resolution [mK]	300	250	300	90	110
Resolution FoM [nJ·K^2]	0.19	0.44	0.3	0.037	0.14

Resolution FoM = (Energy/Conversion) × (Resolution)^2

References

[5.1] Datasheet of CBC005, Cymbet corporation.

[5.2] S. Jeong, Z. Foo, Y. Lee, J. Y. Sim, D. Blaauw and D. Sylvester, "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," *IEEE J Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[5.3] W. Zhao, R. Pan, Y. Ha and Z. Yang, "A 0.4V 280-nW Frequency Reference-less Nearly All-Digital Hybrid Domain Temperature Sensor," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 301–304, 2014.

[5.4] T. Anand, K. A. A. Makinwa and P. K. Hanumolu, "A VCO Based Highly Digital Temperature Sensor With 0.034 °C/mV Supply Sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2651–2663, 2016.

[5.5] K. Yang, Q. Dong, W. Jung, Y. Zhang, M. Choi, D. Blaauw and D. Sylvester, "A 0.6nJ −0.22/+0.19°C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 160–161, 2017.

[5.6] H. Wang and P. P. Mercier, "Near-Zero-Power Temperature Sensing via Tunneling Currents Through Complementary Metal-Oxide-Semiconductor Transistors," *Scientific Reports*, vol. 7, no. 1, pp. 2045–2322, 2017.

[5.7] T. Someya, K. Matsunaga, H. Morimura, T. Sakurai and M. Takamiya, "56-Level Programmable Voltage Detector in Steps of 50mV for Battery Management," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 49–52, 2016.

Chapter 6: Conclusions

This thesis introduces several ultra-low power circuits for battery management in Internet of Things (IoT) sensor nodes. For small and light IoT applications, miniature batteries are developed. Though the batteries are useful to miniaturize the devices, the capacity is limited. In the energy-limited applications, the circuits must challenge the low power operation. This thesis focuses on circuits for battery management in IoT node. From Chapter 2 to Chapter 5, ultra-low power CMOS circuits for battery management are presented.

In Chapter 2, a V_{DD}-Regulated Voltage Reference (VRVR) is presented. A voltage reference is a fundamental circuit in all analog components. To meet the demand for low power voltage reference, the VRVR achieves 90 pA operation. In addition, compared with previously published ultra-low power voltage references, the VRVR realizes a low line sensitivity (LS) and low power supply rejection ratio (PSRR) thanks to the proposed voltage regulation technique that regulates the supply voltage for the voltage reference. Simulation results show that the proposed VRVR generates a 0.45 V reference voltage (V_{REF}) with the temperature coefficient of 33 ppm/°C. The line sensitivity and PSRR are 0.0047%/V and -70dB (at 100Hz), respectively. The power consumption is competitive 90 pA at 1V. The simulation results show that the VRVR achieves both low power and V_{DD}-independent operation.

Chapter 3 presents a programming method to convert a fixed V_{REF} into various reference voltages (V_{REF1}). The programmability is useful to supply appropriate voltages that are various according to the applications. A multiple voltage duplicator (MVD) that solves a tradeoff between the increase in the power consumption of the programming and the deterioration of the temperature characteristics of V_{REF1} is presented. In addition, a fine voltage subtraction (FVS) method is presented to obtain a higher resolution of the programmed V_{REF1} with little power loss. To verify the performance of the programmable voltage reference with the MVD and the FVS, test chips are fabricated in 250-nm CMOS process. The measurement results show that the 6-bit programmed V_{REF1} ranging from 100 mV to 493 mV with the resolution of 6.14 mV is achieved when external V_{REF} (=600mV) is added to the programming circuit. The measured power consumption of the programming circuit is 675 pA at 1.5V and the temperature coefficient of V_{REF1} is

15.2μV/°C. The measurement results show that the programming circuit can be used as a programmable voltage reference that supplies various standard voltages with little power loss and the deterioration of the temperature dependence of V_{REF1}.

In Chapter 4, voltage detectors for RF energy harvesting and battery monitoring are presented. The voltage detector (VD) for RF energy harvesting challenges the ultra-low power and ultra-low voltage operation that must be considered to realize the RF energy harvesting. The VD also has a post-fabrication trimming method to improve the accuracy of the VD which mitigates the effect of the process variation. The VD is fabricated in 250-nm CMOS process. The measurement results show that the VD achieves ultra-low power 248 pW, glitch-free operation that enables the VD to operate at low voltage (≈0 V), normally. Also, the VD achieves the programmability of the detection voltage in steps of less than 49 mV from 0.52V to 0.85V. The VD expands the possibility of the realization of energy autonomous IoT sensor nodes. Another voltage detector is for battery monitoring. In the battery monitoring, the detection voltage of the voltage detector must be changed according to the batteries or applications, which increases the cost of trimming. Besides, some applications impose VDs to detect multiple voltages of a battery. To overcome the issues that increase the cost of VDs, a programmable VD (PVD) is presented. The PVD achieves the programmability of the detection voltage thanks to the combination of the programming method presented in Section 3 and the VRVR presented in Chapter 2. The proposed PVD is fabricated in 250-nm CMOS process. In the measurement, the programmability of the detection voltage ranging from 902 mV to 4904 mV in steps of 62.5 mV is achieved. The measured power consumption is 1.25nA at 5V V_{DD} and the temperature coefficient of the detection voltage is 0.33mV/°C in -20 °C to 60 °C. The resolution and the range of the programmed detection voltage show that the VD covers operation voltages of almost all batteries and has a sufficiently fine resolution to apply the VD to lithium-ion batteries.

In Chapter 5, an ultra-low power temperature sensor for miniature size batteries is presented. The batteries have the large cell resistances that limit the maximum supply current. Therefore, to obtain the temperature information from the batteries, the temperature sensor is designed to be ultra-low power consumption. The proposed temperature sensor uses a new principle of temperature sensing utilizing two sub-threshold nMOSFETs operating in the deep triode region and the saturation region.

The ratio of two currents of the nMOSFETs shows good temperature linearity. A circuit that converts the two currents into frequencies and the ratio of the frequencies into PTAT digital output is also presented. The temperature sensor fabricated in 180-nm CMOS process achieves the inaccuracy of -0.7 °C /+1.3 °C in the temperature range of -20 °C to 80 °C with the resolution of 110 m°C. The measured power consumption is 13 nW which is the lowest power consumption in the previously published low-power temperature sensors. The temperature sensor is suitable for a battery that power is limited.

The IoT attracts many people because it has great potential to realize unprecedented applications and services that people have never seen, which enrich human lives and works. In the IoT, how to supply energy, or how to extend battery life are critical issues that determine the quality of the IoT. This thesis focused on circuits required in battery management and proposed several techniques to reduce the power consumption of the circuits. Although the proposed circuits need further evaluations to put them into practical use, the power reduction techniques are useful for future low power battery management in miniature-sized applications. Furthermore, the proposed circuits are also applicable to many applications that require ultra-low power operation.

Publication List

Transactions

1. T. Someya, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "Design and Analysis of Ultra-Low Power Glitch-Free Programmable Voltage Detector based on Multiple Voltage Copier," *IEICE Transaction on Electronics, Vol.E100-C*, No.4, pp.349–358, 2017.

International Conferences

1. T. Someya, A.K.M. M. Islam, T. Sakurai, and M. Takamiya, "A 13nW Temperature-to-Digital Converter Utilizing Sub-threshold MOSFET Operation at Sub-thermal Drain Voltage," *IEEE Custom Integrated Circuits Conference (CICC), 2018. (accepted)*
2. T. Someya, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "56-Level Programmable Voltage Detector in Steps of 50mV for Battery Management," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 49–52, 2016.
3. T. Someya, H. Fuketa, K. Matsunaga, H. Morimura, T. Sakurai, and M. Takamiya, "248pW, 0.11mV/°C Glitch-Free Programmable Voltage Detector With Multiple Voltage Duplicator for Energy Harvesting," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 249–252, Sept. 2015.
4. H. Fuketa, M. Hamamatsu, T. Yokota, W. Yukita, T. Someya, T. Sekitani, M. Takamiya, T.Someya, and T. Sakurai, "Energy-Autonomous Fever Alarm Armband Integrating Fully Flexible Solar Cells, Piezoelectric Speaker, Temperature Detector, and 12V Organic Complementary FET Circuits," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 296–297, 2015.

Domestic Conferences/Workshops

1. 小野寺尚人，染谷晃基，イスラム マーフズル，松永賢一，森村浩季，高宮真，桜井貴康，"可変キャパシタを用いた自動LC共振最適化機能を有するRFエネルギーハーベスティング回路の設計と評価," 電子情報通信学会，信学技報，ICD2017-85, pp. 139–139，石垣島, 2017年12月.
2. 小野寺尚人，染谷晃基，松永賢一，森村浩季，高宮 真，桜井貴康,"可変キャパシタを用いた自動LC共振最適化機能を有するRFエネルギーハーベステ

ィング回路の設計,” 電子情報通信学会総合大会, C-10-5, 名古屋, 2017 年 3 月.

3. 染谷晃基, 松永賢一, 森村浩季, 桜井貴康, 高宮 真, “バッテリーマネジメント向け 56 段階、50mV 刻みプログラマブル電圧検出回路,” 信学技報 (IEICE Technical Report), vol. 116, No. 364, pp. 1–5, 東京, 2016 年 12 月.
4. 濵松昌宗, 更田裕司, 横田知之, 雪田和歌子, 染谷晃基, 関谷 毅, 高宮 真, 染谷隆夫, 桜井貴康, "室内光で発電し音で発熱を知らせる腕章型発熱アラームの提案と有機回路による実証," 電子情報通信学会, LSI とシステムのワークショップ, ポスターセッション 学生部門, PS-8, 北九州, 2015.年 5 月.

Patents

1. 松永賢一, 森村浩季, 高宮 真, 染谷晃基, 桜井貴康, “電圧検出回路,” 特願 2016-183818, 2016 年 9 月 21 日出願.
2. 松永賢一, 森村浩季, 染谷晃基, 更田裕司, 高宮 真, 桜井貴康, “電圧検出回路,” 特願 2015-178342, 2015 年 9 月 10 日出願.
3. 松永賢一, 森村浩季, 染谷晃基, 更田裕司, 高宮 真, 桜井貴康, “分圧バッファ回路,” 特願 2015-178346, 2015 年 9 月 10 日出願.