博士論文

Negative-Capacitance FETs based on Ferroelectric Hafnium Oxide for Low-Power VLSIs

（低消費電力 VLSI のための強誘電性ハフニウム酸化膜を用いた負性容量 FET に関する研究）

Kyungmin Jang

蒋 京珉

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Professor Toshiro Hiramoto

Abstract

To realize highly energy-efficient internet-of-things (IoT) platform, an ultralow power transistor with steep subthreshold slope (SS) is strongly required. The negative-capacitance FET (NCFET) which uses ferroelectric (FE) thin film as a gate insulator is a promising steep slope transistor. Thanks to recently explored ferroelectricity in hafnium oxide (HfO_2) thin film, the FE:HfO_2-based NCFET is highly expected as a solution for the ultralow power CMOS technology because of its following advantages: (1) high on-current, (2) symmetric operation and use of the same circuit layout with conventional CMOS devices, and (3) CMOS process compatibility.

Recently, a growing number of groups are exploring FE:HfO_2-based NCFET and many excellent characteristics have been reported. However, even though NCFETs have been intensively studied and steep SS characteristics have been demonstrated, the physical origin of the NC effect is not considered to be very clear yet, and steep SS characteristics in FeFET have not been understood sufficiently. Furthermore, there has not been sufficient number of reports on systematic comparison of the NC model and experiments. Therefore, a systematical study on both of simulations and experiments is now strongly required to understand steep SS characteristics in FeFETs. In this work, to investigate the physical origin of the NC effect and understand steep SS in FeFET, FE:HfO_2-based NCFETs have been studied by both of simulations and experiments.

Device simulation on the static characteristics of multi-gate NCFET was conducted based on the NC model, in which the design points can be obtained. Clear device design guidance to obtain the steep SS in FE:HfO_2-based NCFET was addressed based on the NC model.

Dynamic characteristics and operation speed of FE:$HfZrO_2$ (HZO)-based NCFET were simulated based on the single-domain (SD)-based Landau-Khalatnikov (LK) equation. Our simulation results revealed that the operation speed of FE:HZO-based NCFET can be limited by the polarization switching. Then, by incorporating the multiple-domain (MD) effect and domain-domain interaction effect into the SD-LK model, the MD-LK was successfully developed and experimentally validated as a dynamic model for FE:HZO. The MD-LK model is able to reproduce the various experimental results in FE:HZO capacitors with high fitting accuracy.

To clarify the physical origin of the NC effect and understand the phenomena of steep SS in FeFET, steep SS was experimentally explored in our fabricated FE:HZO-based metal-FE-metal-insulator-semiconductor (MFMIS)-FETs. First, based on the NC model, bulk NCFET was designed and characterized systematically. However, in our experiments, steep SS was not observed as expected by the NC model. The non-steep SS can be attributed to the

“charge injection” into the internal gate. Second, we experimentally explored the steep SS in MFMIS-FETs based on the nonlinear dielectric (NLD) model and “polarization switching”, which is an alternative model of the NC model. By using anti-ferroelectric-HZO as gate insulator, for the first time, we successfully observed “effective NC effect (polarization switching)” within sub-V_{th} region. Additionally, we observed that “polarization switching” can be suppressed in sub-V_{th} region due to the small capacitance of depletion layer. Third, in MFMIS-FET with gate leaky MISFET, we experimentally observed steep SS of sub-60mV/decade. The minimum SS value was 20mV/decade and SS < 60mV/decade was for 2 decades of drain current. The steep SS is considered to be the result of voltage amplification, whose physical origin can be attributed to the cooperation of “polarization switching” and “charge injection”. Furthermore, throughout our experiments, it was clearly addressed that, monitoring gate current can be a very effective research approach to understand the device characteristics of steep SS in FeFET.

The results obtained in this thesis give us basic and important information on the characteristics of FeFET with FE:HZO. Therefore, we hope that this work will contribute to the comprehensive understanding of the physical origin of NC effect and phenomena of steep SS in FeFET (including “polarization switching” and “charge injection”), and that shed light on the further researches on the next-generation semiconductor devices for low-power VLSIs.

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Contents

Chapter 1
Introduction

1.1 Background

Recently, untiring progresses of semiconductor devices and VLSI platform, which have been aggressively driven along with the Moore's law [1], are thought to be come up against some fundamental problems. One of the major problems is a significant increase in power consumption (Fig. 1.1 [2]) along the miniaturization of MOSFETs, which results in enormous thermal dissipation and reliability degradation. To reduce the power consumption and realize more energy-efficient MOSFET, lowering the supply voltage (V_{dd}) is the most effective way. However, as shown in Fig. 1.2, in the case of classical MOSFET, lowering V_{dd} while keeping the on-state current (I_{on}) level incurs a striking increase in off-state current (I_{off}), which consequently contributes to the increase in standby power consumption. Therefore, to scale V_{dd} and carry on the Moore's law further, MOSFET with a steeper subthreshold slope (SS) is strongly required (Fig. 1.2). SS is defined as Eq. 1.1 where V_g is gate voltage, Ψ_s is surface potential of channel, I_d is drain current, C_s is capacitance of semiconductor, and C_{ox} is capacitance of total gate insulator [3]. In Eq. 1.1, the term of (ln10)(kT/q) is about 60mV at room temperature, which results in SS > 60mV/decade because both of C_s and C_{ox} are positive.

$$SS = \frac{\partial V_g}{\partial \log_{10} I_d} = \left(\frac{\partial \psi_s}{\partial \log_{10} I_d} \right) \cdot \left(\frac{\partial V_g}{\partial \psi_s} \right) = \ln 10 \frac{kT}{q} \cdot \left(1 + \frac{C_s}{C_{ox}} \right), \quad (1.1)$$

The steep-slope MOSFET is a great solution for reduction of power consumption. Fig. 1.3 shows the calculated energy versus supply voltage (V_{dd}) by varying SS [4]. Energy

minimum in Fig. 1.3 shifts to the lower V_{dd} and lower energy side with lower SS value. This indicates that ultralow-voltage-operating low-power devices can be realized using the steep-slope MOSFET.

To this day, many kinds of steep-slope FETs [5-10] have been proposed to enable SS lower than 60mV/decade and high on-current to off-current ratio (I_{on}/I_{off} ratio), which can consequently contribute to highly energy-efficient transistor. In 2008, negative-capacitance field-effect-transistor (NCFET), which can realize $d\Psi_s/dV_g > 1$ by utilizing the NC effect of ferroelectric (FE) gate insulator ($C_{ox} < 0$), was proposed by Dr. S. Salahuddin and Dr. S. Datta [11]. Fig. 1.4 shows the device structure and the idea of NCFET based on the NC model [11] which uses FE materials [25,26] as a gate insulator. In Fig. 1.4, a region of negative slope in polarization-voltage characteristic corresponds to the NC state. In conventional FE theory [25,26], the NC state is thermodynamically unstable, therefore cannot be realized. Instead of NC state, "polarization switching" occurs in FE materials [25,26] as shown in Fig. 1.4. However, within a framework of NC model proposed by S. Salahuddin *et al.* [11], NC region can be stabilized only by connecting series positive capacitor of semiconductor to FE capacitor.

In 2011, T. S. Böscke *et al.* [12] reported that FE appears in doped hafnium oxide (HfO_2) thin film, which is suitable for realizing CMOS-compatible NCFET. Thanks to this recently explored FE in HfO_2, FE:HfO_2-based NCFET is highly expected as a solution for the ultralow power CMOS technology. The FE:HfO_2-based NCFET has following advantages: (1) high on-current as MOSFET, (2) symmetric operation and use of the same circuit layout with CMOS devices, and (3) CMOS process compatibility. These advantages allow FE:HfO_2 NCFET to be a low-cost and ultralow power device. Now, a growing number of groups are exploring the steep SS in FeFETs using HfO_2 [13-21], for a next-generation low power

consumption transistor.

However, even though NCFETs have been intensively studied and steep SS characteristics have been demonstrated [13-21], the physical origin of the NC effect is not considered to be very clear yet [22-24], and steep SS characteristics in FeFET have not been understood sufficiently. Furthermore, there has not been sufficient number of reports on systematic comparison of experiments and the NC model. Therefore, a systematical study by both of simulations and experiments is now strongly required to clarify the physical origin of the NC effect and to understand steep SS characteristics in FeFET.

1.2 Purpose of This Work

The main purpose of this work is to clarify the physical origin of the NC effect and to understand the phenomena of steep SS in FeFET. To clarify and understand the NC effect and steep SS in FeFET, first of all, simulation-based studies on NCFET and the NC model are conducted. Then, based on the simulation results, experimental exploration of the NC effect and steep SS in FE:$HfZrO_2$-based NCFET is conducted.

1.3 Chapter Organizations

This thesis is organized in 6 chapters.

In chapter 2, based on the NC model [11], static characteristics of FE:HfO_2-based multi-gate NCFET is simulated to understand NC model and to obtain device design points. This simulation work can help us to understand the NC model and NCFET operation. Based on the NC model, design guidelines for steep SS are addressed.

In chapter 3, based on the Landau-Khalatnikov (LK) equation, dynamic characteristics of FE:HfO_2-based NCFET were simulated using the parameters extracted from the experimental

data. Operation speed of FE:HfO_2-based NCFET is surveyed from the simulation results.

In chapter 4, the dynamic model for FE:HfO_2 is developed by incorporate the multiple domain (MD) effect and domain interaction effect into the single domain (SD) model. Various experimental conditions are used to calibrate and validate the model.

In chapter 5, steep SS characteristics in our fabricated FE:$HfZrO_2$-based FETs are experimentally explored. Besides the discussion on the NC model [11], we carefully address that "polarization switching" of FE and "charge injection" into internal gate can be physical origins of the steep SS phenomena in FeFET with $HfZrO_2$. Significant importance of monitoring gate current of FeFET is also addressed.

Finally, chapter 6 is for conclusions of this thesis.

References

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions", IEEE Journal of Solid State Circuits., vol. SC-9, no.5, pp. 256-268, Oct. 1974.

[2] E. Pop, "Energy Dissipation and Transport in Nanoscale Devices", Nano Research, 3, 147, 2010.

[3] Y. Taur and T. H. Ning, "MOSFET Devices", in Fundamentals of Modern VLSI Devices, 2nd ed., ch. 3, pp. 163-166, Cambridge University Press, 2013.

[4] H. Fuketa, T. Yasufuku, S Iida, M. Takamiya, M Nomura, H. Shinohara, and T. Sakurai, "Device-Circuit Interactions in Extremely Low Voltage CMOS Designs", in IEDM Tech. Dig., Washington DC, USA, 2011, pp. 559-562.

[5] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q", in IEDM Tech. Dig., p. 289, 2002.

[6] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "Impact Ionization MOS (I-MOS)−Part I: Device and Circuit Simulations", IEEE Transactions on Electron Devices, 52, 1, p. 69 (2005).

[7] N. Abele, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu, "Suspended-Gate MOSFET: Bringing New MEMS Functionality into Solid-State MOS Transistor", in IEDM Tech. Dig., 2005, pp. 479-481.

[8] K. Akarvardar, C. Eggimann, D. Tsamados, Y. S. Chauhan, G. C. Wan, A. M. Ionescu, R. T.

Howe, and H.-S. Philip, “Analytical Modeling of the Suspended-Gate FET and Design Insights for Low-Power Logic”, IEEE Transactions on Electron Devices, 55, 1, p. 48 (2008).

[9] A. M. Ionescu, H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches”, Nature, Vol. 479, p. 329, 2011.

[10] K. Tomioka, M. Yoshimura, T. Fukui, “Steep-slope Tunnel Field-Effect Transistors using III-V Nanowire/Si Heterojunction”, 2012 IEEE Symposia on VLSI Technology and Circuits, p. 47 (2012).

[11] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices”, Nano Letters, vol. 8 no. 2, pp. 405-410, 2008.

[12] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, “Ferroelectricity in hafnium oxide thin films”, Applied Physics Letters, vol. 99, no. 10, 102903, 2011.

[13] A. Rusu, G. A. Salvatore, D. Jiménez, A. M. Ionescu, “Metal-Ferroelectric-Meta-Oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification”, IEDM Tech. Dig., 2010, p. 395.

[14] H. Ota, T. Ikegami, J. Hattori, K. Fukuda, S. Migita, and A. Toriumi, “Fully Coupled 3-D Device Simulation of Negative Capacitance FinFETs for Sub 10nm Integration”, IEDM Tech. Dig., 2016, p. 318.

[15] H.-P. Lee and P. Su, “Suppressed Fin-LER Induced Variability in Negative Capacitance FinFETs”, IEEE Electron Device Lett. 38, 1492 (2017).

[16] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C.Cheng, C.-C. Chen, Y.-J Wei, Y.-F. Hou, M.-H Liao, M.-H. Lee, M.-C.Chen, J.-M. Sheih, W.-K. yeh, F.-L. Yang, S. Salahuddin, and C. Hu, “Sub-60mV-Swing Negative-Capacitance FinFET without Hysteresis”, in IEDM Tech. Dig., Washington, DC, USA, 2015, pp. 621-623.

[17] M. H. Lee, P.-G. Chen, C. Liu, K-Y. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao, M. Tang, K.-S. Li and M.-C. Chen, “Prospects for Ferroelectric $HfZrO_x$ FETs with Experimentally CET=0.98nm, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, Switch-OFF <0.2V, and Hysteresis-Free Strategies”, in IEDM Tech. Dig., 2015, pp. 616-619.

[18] M. H. Lee, S.-T. Fan, C.-H. Tang, P.-G. Chen, Y.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, S.-N. Liu, M.-H. Liao, C.-A. Jong, K.-S. Li, M.-C. Chen, and C. W. Liu, “Physical Thickness 1.x nm Ferroelectric $HfZrO_x$ Negative Capacitance FETs”, in IEDM Tech. Dig., San Francisco, CA, USA, 2016, pp. 306-309.

[19] J. Jo and C. Shin, “Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/decade Switching”, IEEE Electron Device Lett. 37, 245 (2016).

[20] P. Sharma K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, and S. Datta, VLSI Tech. Symp. Dig., 2017, T12-2.

[21] M. Kobayashi and T. Hiramoto, “Device Design Guideline for Steep Slope Ferroelectric FET Using Negative Capacitance in Sub-0.2V Operation: Operation Speed, Material Requirement and Energy Efficiency”, in VLSI Tech. Symp. Dig., Kyoto, Japan, 2015, pp. 212-213.

[22] C. M. Krowne, S. W. Kirchoefer, W. Chang, J. M. Pond, and L. M. B. Alldredge, “Examination of the Possibility of Negative Capacitance Using Ferroelectric Materials in Solid State Electronic Devices”, Nano Letters, vol. 11, no. 3, pp. 988-992, 2011.

[23] P. Zubko, J. C. Wojdeł, M. Hadjimichael, S. Fernandez-Pena, A. Sené, I. Luk'yanchuk, J. Triscone, and J. Íñiguez, “Negative capacitance in multidomain ferroelectric superlattices”, Nature, vol. 534, pp. 524-528, 2016.

[24] C. M. Krowne, “Evaluation of the differential capacitance for ferroelectric materials using either charge-based or energy-based expressions”, Journal of Advanced Dielectrics, vol. 4, no. 33, 1450024, 2014.

[25] M. E. Lines and A. M. Glass, “Principles and Applications of Ferroelectrics and Related Materials”, Oxford University Press, 1977.

[26] P. Chandra and P. B. Littlewood, “A Landau Primer for Ferroelectrics”, arXiv:cond-mat/0609347, 2006.

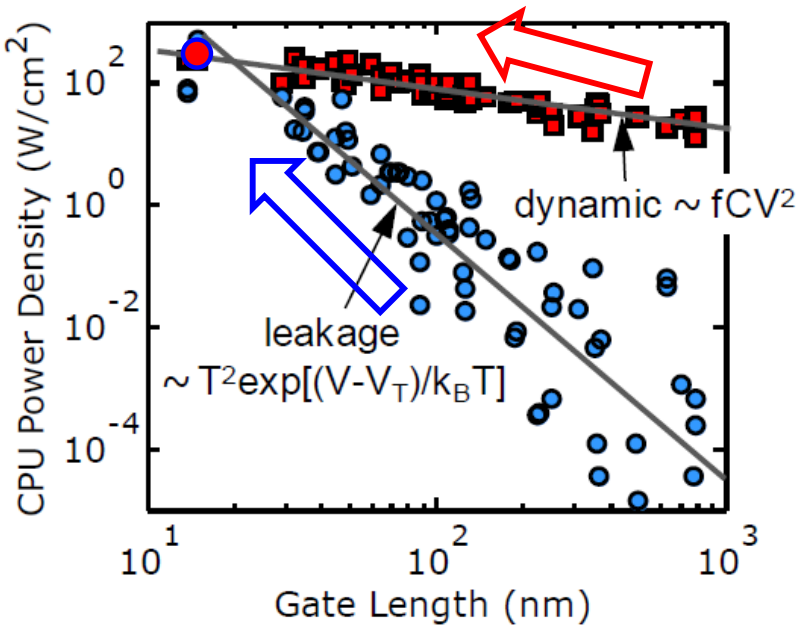


Fig. 1.1. Significant increase in power consumption along miniaturization of MOSFETs [2].

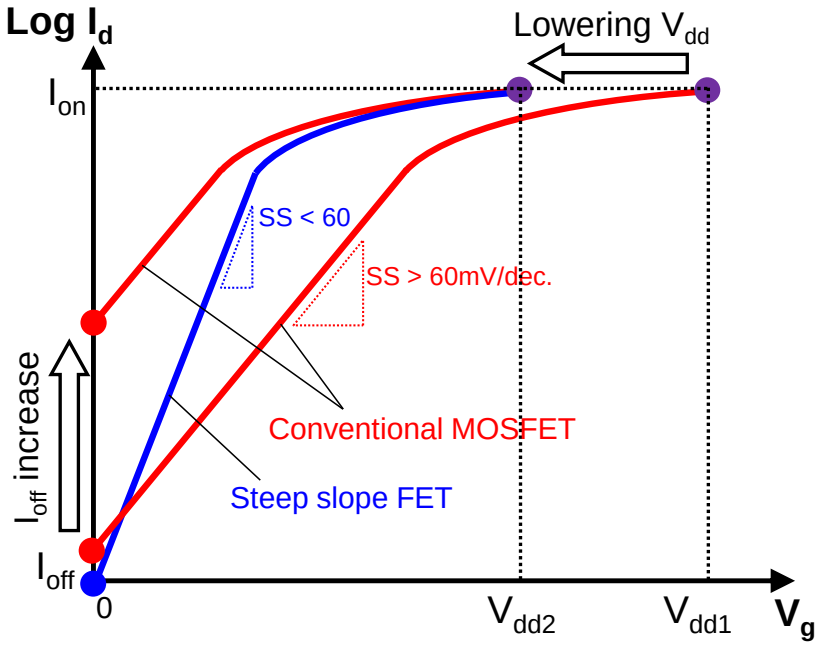


Fig. 1.2. Schematic of I_d-V_g characteristics of a classical MOSFET and steep subthreshold slope FET.

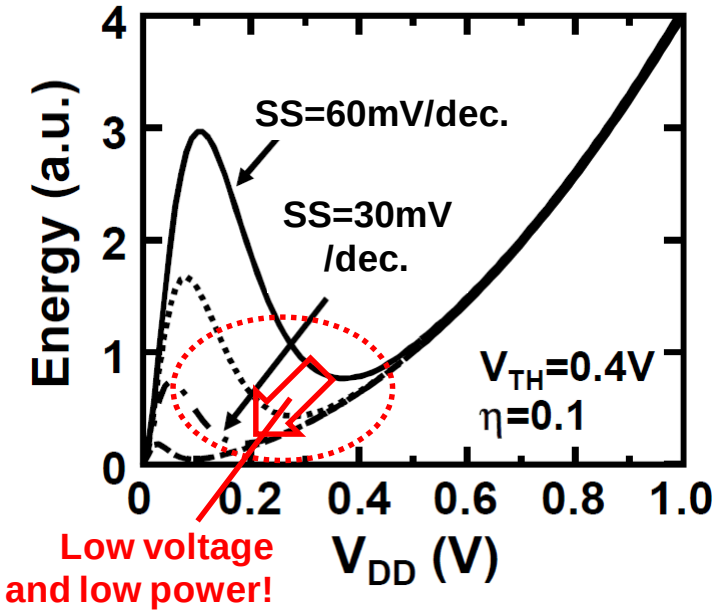


Fig. 1.3. Calculated energy versus supply voltage (V_{dd}) by varying subthreshold slope (SS). Energy minimum shifts to the lower V_{dd} and lower energy side with smaller SS value. Ultralow voltage operating low power devices can be realized using the steep-slope MOSFET [4].

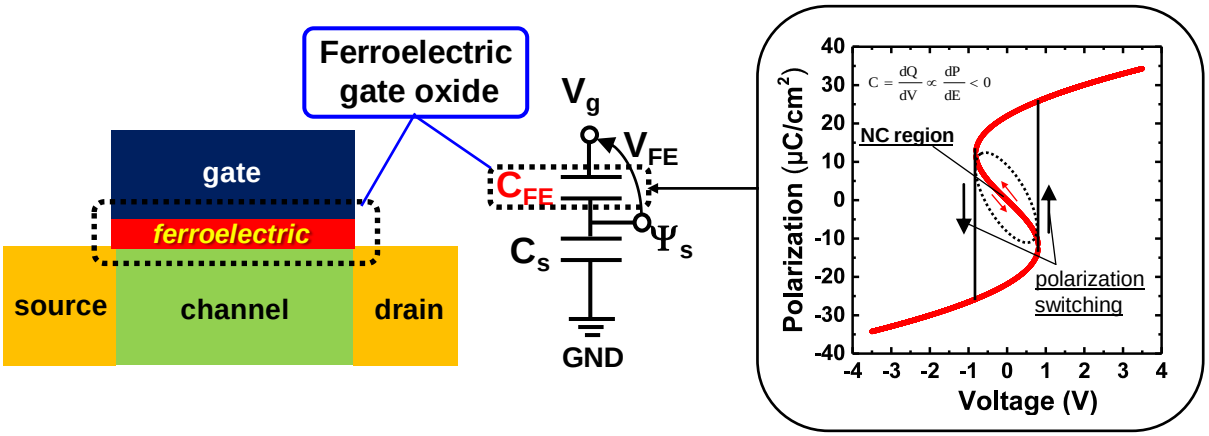


Fig. 1.4. Device structure and the idea of the NCFET [11]. If the NC region is accessible during the device operation, thanks to the negative capacitance of ferroelectric insulator, SS becomes smaller than 60mV/decade.

Chapter 2

Simulation Study on Static Characteristics of FE:HfO_2-based Negative-Capacitance FETs

2.1 Introduction

In this chapter, based on the negative-capacitance (NC) model proposed by S. Salahuddin and S. Datta [1], we investigate a device design and scalability of ferroelectric HfO_2 (FE:HfO_2)-based NCFET using analytic simulation method. Firstly, from chapter 2.2 to 2.8, double-gate NCFET (DG-NCFET) is discussed targeting high aspect ratio FinFET. Energy efficiency improvement in DG-NCFET comparing to classical DG-MOSFET was studied based on the NC model [1]. Then, gate-all-around (GAA) nanowire NCFET (NW-NCFET) is discussed from chapter 2.9 to 2.14, in which NW channel structure is focused on as a replacing structure for Fin channel structure assuming sub-7nm technology node. Energy efficiency improvement in NW-NCFET comparing to classical NW-MOSFET as well as NCFET with DG structure (DG-NCFET) was studied based on the NC model [1].

2.2 Background and Motivation of Study on DG-NCFET

Even though there are some previous simulation-based studies on DG-NCFET [2-4], however, they were performed using conventional FE materials such as PZT or SBT which have been suffered from crucial problems of incompatibility with CMOS process [5]. In this work, however, we choose the ferroelectric HfO_2 thin film (FE:HfO_2) [6-7] as a gate insulator, which is very suitable ferroelectric material for realizing CMOS-compatible NCFET.

Furthermore, the previous simulation studies on DG-NCFET [2-4] did not focus on

energy efficiency and low V_{dd} operation. Therefore, energy efficiency targeting ultralow V_{dd} in DG-NCFET remains unstudied yet. Our previous study on energy efficiency of FE:HfO_2-based bulk Si NCFET [8] should be extended to DG-structured NCFET targeting high aspect ratio FinFET [9].

In order to discuss the gate stack scalability of FE:HfO_2-based NCFET regarding gate length (L_g), we consider a constraint induced by recent gate-last process and impose this process-induced constraint on gate stack thickness. Although thickness of FE:HfO_2 thin film can be very thin [7], the space to fit the FE gate insulator and interfacial insulator will be very limited in the advanced CMOS technology of gate-last process [9-10], because total thickness of gate insulator could be close to the half of L_g as illustrated in Fig. 2.1.

In this work, we investigate the gate stack scalability and energy efficiency of FE:HfO_2-based DG-NCFET focusing on ultralow V_{dd} of sub-0.2V. Based on realistic ferroelectric characteristic of FE:HfO_2, the gate stack thickness is optimized to maximize the I_{on}/I_{off} ratio under gate-last process-induced constraint. Finally, with the optimized gate stack thickness for aggressively scaled L_g, the energy efficiency is benchmarked.

2.3 Device Structure and Model for DG-NCFET

Fig. 2.2 shows the device structure of a DG-NCFET using FE:HfO_2 as a gate insulator with an interfacial insulator. Physical thickness of FE insulator (T_{fe}) and equivalent oxide thickness (EOT) of interfacial insulator (T_{ox}) were set to 7nm and 1nm as nominal, respectively. Nominal width of Fin (T_{si}) was set to 5nm. L_g=200nm was used for long channel device, and then, was scaled down to study scalability.

In this study, to characterize DG-NCFET, an analytic compact model-based simulation [2-3] was carried out. This analytical model can be expressed by combining following two

equations: (1) equations for DG classical MOSFET [11] including Poisson equation, boundary condition of charge density, and current continuity, and, (2) Landau equation [12] for FE material in NCFET model [1-3]. Detailed descriptions on the analytic form for non-doped channel DG-NCFET can be found in Refs. 2-3. However, please note that equations 3 to 7 in Ref. 2 contain errors because $Q = 2\varepsilon_s(d\varphi(t_s/2)/dx)$ was used as the total mobile charge per unit gate area. By using a correct form for the total mobile charge density, $Q = \varepsilon_s(d\varphi(t_s/2)/dx)$, below Eq. 2.1 was obtained as a correct form for equation 3 in Ref. 2. All symbols in below Eq. 2.1 are consistent with them of Ref. 2.

$$\frac{q(V_g - \Delta\varphi - V)}{2kT} - \ln\left(\frac{2}{t_s}\sqrt{\frac{2\varepsilon_s kT}{q^2 n_i}}\right) = \ln(\beta) - \ln(\cos\beta) + a_0(2C_s)\beta\tan\beta + b_0(2C_s)\left(\frac{2kT}{q}\right)^2\beta^3\tan^3\beta + c_0(2C_s)\left(\frac{2kT}{q}\right)^4\beta^5\tan^5\beta \quad (2.1)$$

We used this model to characterize DG-NCFET targeting FinFET with high aspect ratio [9]. Owing to its simplicity, the analytic model-based simulation is an effective approach to investigate the device design guidelines in detail. And, TCAD simulation study on DG-NCFET [4] has shown that the results from this kind of analytic model show good agreement with TCAD numerical simulation. In this model, however, short channel effect, quantum mechanical effect, velocity saturation phenomenon was not considered [11], which allowed us to focus on the intrinsic NC effect on DG-NCFET design. It will be our future work to investigate and incorporate those additional physical effects.

The schematic of a band diagram of multi-gate NCFET is shown in Fig. 2.3 to explain how the $d\Psi_s/dV_g$ larger than unity can be facilitated in NC model [1]. NC of FE layer and positive-capacitance (PC) of interfacial insulator are contacted in series to silicon channel. In

this structure, voltage is divided to each layer which results in V_g - V_{fb} = V_{fe} + V_{ox} + Ψ_s, where V_{fb} is flatband voltage and V_{ox} is voltage drop in interfacial insulator. FE layer presents NC characteristic, so that, FE layer induces opposite polarity of voltage (V_{fe}) to the charge density (Q_{fe}). This indicates that higher negative voltage (V_{fe}) is induced within FE layer when higher positive V_g is applied as illustrated in Fig. 2.3. Owing to this negative V_{fe} within FE layer, Ψ_σ is amplified compared to V_g. Consequently, $d\Psi_s > dV_g$ can be realized in NCFET which contributes to SS < 60mV/decade and higher I_{on}/I_{off} ratio than classical MOSFET.

In this study on DG-NCFET, FE hysteresis characteristic of FE:HfO_2 and/or gate stack thickness were variable parameters to optimize an I_{on}/I_{off} ratio of DG-NCFET. Based on the obtained results, gate stack scalability of FE:HfO_2-based DG-NCFET was discussed. Finally, with the optimized FE characteristic and gate stack thickness, energy efficiency of FE:HfO_2-based DG-NCFET was benchmarked.

Firstly, the I_d-V_g characteristics of DG-NCFET as well as DG classical MOSFET were simulated with remnant polarization (P_r) and/or coercive field (E_c) of FE:HfO_2 as variable parameters, which are determined by the hysteresis characteristic of FE material. Then, we discussed how P_r and/or E_c impact on the I_d-V_g characteristic, and the I_{on}/I_{off} ratio of DG-NCFET. Here, the I_{on}/I_{off} ratio is extracted as a determining factor for energy efficiency [13]. From these results, nominal P_r and E_c were chosen by considering the recent experimental reports on FE:HfO_2. [6-7,14-19]

Secondly, the I_d-V_g characteristics of DG-NCFET as well as DG classical MOSFET were simulated with T_{fe} and/or T_{ox} as variable parameters. Then, we discussed how T_{fe} and/or T_{ox} impact on the I_d-V_g characteristic, and the I_{on}/I_{off} ratio of DG-NCFET. From these results, we searched design window of T_{fe} and/or T_{ox} to achieve high I_{on}/I_{off} ratio. Then, within the obtained

design window, we searched design point of T_{fe} and/or T_{ox} under the gate-last process-induced constraint imposed by the L_g upon T_{fe} and T_{ox}: $T_{fe} + T_{ox} < L_g/2$ as shown in Fig. 2.1. By considering this process-induced constraint regarding T_{fe}, T_{ox}, and L_g, the gate stack scalability of FE:HfO_2-based DG-NCFET was discussed.

Thirdly, with the optimized gate stack thickness for aggressively scaled L_g, energy efficiency of FE:HfO_2-based DG-NCFET was calculated [13], and compared to the DG classical MOSFET.

2.4 Ferroelectric Material Parameters Dependences

Fig. 2.4 shows the I_d-V_g characteristics of DG-NCFET and DG classical MOSFET with (a) P_r and/or (b) E_c of FE:HfO_2 as variable parameters, which determine the hysteresis characteristic of FE material. The gate stack thickness was set to nominal value of T_{fe}=7nm and T_{ox}=EOT=1nm. Drain voltage (V_d) was 0.2V.

In Fig. 2.4, the drain current near the start point of strong inversion region in DG-NCFET was enhanced compared to DG classical MOSFET which results in higher I_{on}. The enhancement of the drain current in DGNCFET is attributed to the NC effect in FE layer ($d\Psi_s/dV_g > 1$) [1]. Additionally, higher I_{on} was achieved with lower P_r (Fig. 2.4(a)) and/or higher E_c (Fig. 2.4(b)). This trend of I_{on}, which is in line with our previous study on the bulk Si NCFET [8], can be explained by considering the NC effect in FE layer [1]. Detailed descriptions on the trend of I_{on} and material requirements based on it can be found in Ref. 8. In brief, with lower P_r and/or higher E_c, NC region of negative V_{fe} ($V_{fe} < 0$) is more accessible near threshold. When the capacitance of FE layer ($C_{fe} < 0$) is defined by $C_{fe} = dQ_{fe} / dV_{fe}$, an absolute value of C_{fe} decreases with lower P_r and/or higher E_c, where Q_{fe} is the charge density (or polarization) in FE layer. Therefore, at a given V_g, an absolute value of V_{fe} increases with

lower P_r and/or higher E_c which results in the larger surface potential bending (Ψ_s), and higher I_{on} as shown in Fig. 2.4.

Fig. 2.5 shows the simulated contour plot of I_{on}/I_{off} ratio of DG-NCFET versus P_r and E_c, where T_{fe}=7nm, T_{ox}=EOT=1nm, and V_{dd}=0.5V. In a wide range of P_r and E_c, higher I_{on}/I_{off} ratio can be achieved in DG-NCFET compared to DG classical MOSFET thanks to the NC effect in FE layer [1]. Lower P_r and/or higher E_c contribute to the higher I_{on}/I_{off} ratio, which has been illustrated in Fig. 2.4. By adjusting P_r and/or E_c, the performance of DG-NCFET can be optimized, however, P_r and E_c should be chosen by considering the experimental reports on FE:HfO_2. The recent experimental reports on FE:HfO_2 [6-7,14-19] have shown that P_r and E_c depend on the doped materials and doping concentration, annealing conditions, and film thicknesses. The distributions of P_r and E_c are among $0 < P_r < 25\mu C/cm^2$ and $0 < E_c <$ 2MV/cm [6,7,14-19]. In this work, we chose P_r=5μC/cm^2 and E_c=1MV/cm as reference values for FE:HfO_2. These chosen reference values are considered to be realistic, because there are experimental data of FE:HfO_2 whose P_r and E_c are close to the reference values [16-19]. Specific ferroelectric materials with the reference P_r and E_c are Al-doped HfO_2 [16], Si-doped HfO_2 [17-18], and Zr-doped HfO_2 [19].

Note that hysteresis region which is not preferred for the logic device application is shown by crosshatching in Fig. 2.5. This hysteresis of I_d-V_g characteristic in NCFET is incurred when capacitance matching between FE layer and semiconductor is poor [20] and snapback Ψ_s-V_g characteristic occurs as illustrated in Ref. 4.

2.5 Gate Stack Thickness Dependences

Fig. 2.6 shows I_d-V_g characteristics of DG-NCFET and DG classical MOSFET where (a) T_{fe} and/or (b) T_{ox}=EOT were variable parameters. P_r=5μC/cm^2 and E_c=1MV/cm were used as

the realistic nominal values as mentioned above. V_d was 0.2V.

Higher drain current can be achieved with thicker T_{fe} and/or thinner T_{ox} in DG-NCFET compared to DG classical MOSFET whose EOT=1nm. To explain these gate stack thickness dependences of drain current, schematic of band diagrams were shown in Fig. 2.7, where only one side of DG-NCFET was shown regarding its symmetry. Based on NC model proposed by Salahuddin [1], at a given V_g, comparing to nominal case (a), higher negative voltage (V_{fe}) is induced with thicker T_{fe} (b), and/or less voltage in the interfacial layer (V_{ox}) drops with thinner T_{ox} (c). As a result, with a thicker T_{fe} (b) and/or thinner T_{ox} (c), surface potentials (Ψ_s) bend more than nominal case (a), which results in higher drain current.

Fig. 2.8 shows the contour plot of I_{on}/I_{off} ratio versus T_{fe} and T_{ox}=EOT, where V_{dd}=0.5V. There exists a wider design window where higher I_{on}/I_{off} ratio can be achieved in DG-NCFET than in DG classical MOSFET. This I_{on}/I_{off} ratio enhancement is attributed to the NC effect of FE layer. Furthermore, thicker T_{fe} contributes to higher I_{on}/I_{off} ratio, which has been illustrated in Fig. 2.6 and Fig. 2.7. By adjusting T_{fe} and T_{ox}, the performance of DG-NCFET can be maximized.

2.6 Gate Stack Scalability under Process-induced Constraint

But, in real device, process-induced constraint regarding T_{fe}, T_{ox} and L_g should be considered under the recent HKMG CMOS process. In a certain technology node of L_g, gate-last process-induced constraint of $T_{fe} + T_{ox} < L_g/2$ should be imposed upon gate stack thickness of T_{fe} and T_{ox} as shown in Fig. 2.1. This indicates that T_{fe} and T_{ox} have to be sufficiently small in order to fit to the dummy gate space for an aggressively scaled L_g.

In order to investigate the gate stack scalability of FE:HfO_2-based DG-NCFET, the boundary of gate-last process-induced constraint of $T_{fe} + T_{ox} < L_g/2$ was shown by dotted line in

Fig. 2.8. Dummy gate can fit to the left side of the boundary, but cannot on the right side. This boundary moves from right to left side when technology node progresses and L_g shrinks. In Fig. 2.8, a design window exists as the process constraint boundary moves from 16nm to 7nm indicated by the arrow. FE:HfO_2-based DG-NCFET has a design point for gate stack under aggressively scaled technology node of sub-10nm L_g.

To investigate the case of even lower V_{dd}, same simulations were conducted at V_{dd}=0.2V, and the result is shown in Fig. 2.9. Even at V_{dd}=0.2V, DG-NCFET has wider design window to achieve higher I_{on}/I_{off} ratio than DG classical MOSFET owing to NC effect of FE layer. Furthermore, there still exist a design point within design window for an aggressively scaled technology node down to L_g=7nm. This result indicates that gate stack of FE:HfO_2-based DG-NCFET for sub-0.2V operation is scalable down to sub-10nm L_g technology node.

2.7 Benchmark of Energy Efficiency

Finally, energy per switching [13], which is referred as energy efficiency, of DG-NCFET with optimized gate stack thickness was calculated and benchmarked. Suppose technology node of sub-10nm L_g, T_{fe} and T_{ox} were optimized to 3nm and 0.3nm, respectively, satisfying process-induced constraint of sub-10nm L_g shown in Figs. 2.8 and 2.9. Energy efficiency of DG-NCFET with this optimized gate stack thickness was estimated and shown in Fig. 2.10. The energy efficiency is calculated by Eq. 2.2, in which ξ is active ratio [13].

$$E \propto V_{dd}^{2}\left(\xi + \frac{I_{off}}{I_{on}}\right) \tag{2.2}$$

By assuming standard logic device, 1/800 was used as a value of ξ. As shown in Fig. 2.10, in case of the ferroelectric FET which operates based on the NC model, DG-NCFET has 2.5x

higher energy efficiency comparing to DG classical MOSFET whose EOT=1nm. This energy efficiency enhancement indicates that DG-NCFET is very beneficial for ultralow voltage operation of sub-0.2V.

2.8 Summary of Study on DG-NCFET

We investigated the gate stack scalability and benchmarked energy efficiency of FE:HfO_2-based DG-NCFET based on the NC model. Regarding gate stack scalability of FE:HfO_2-based DG-NCFET, there was a wide range of design window for T_{fe} and T_{ox} where high I_{on}/I_{off} ratio can be obtained under gate-last process-induced constraint even with sub-10nm L_g. With the optimized gate stack thickness for sub-10nm L_g, DG-NCFET showed 2.5x higher energy efficiency than DG classical MOSFET at ultralow operation voltage of sub-0.2V. These results encourage us to use FE:HfO_2-based DG-NCFET which operates as the NC model for highly energy-efficient computing.

2.9 Background and Motivation of Study on NW-NCFET

In previous chapters, we have discussed on double-gate NCFET (DG-NCFET) based on FE:HfO_2 targeting high aspect ratio FinFET [9]. Beyond 10nm technology node, however, it is highly expected that a novel channel structure of gate-all-around (GAA) nanowire (NW) will be the replacement of Fin channel because of its high short channel effect immunity [21]. Therefore, our study on DG-NCFET [22] should be extended to GAA NW-structured NCFET (NW-NCFET) [23]. In previous chapters of study on DG-NCFET, gate stack scalability issue induced by the gate-last process was discussed. In the case of NW-NCFET, another constraint induced by NW integration is imposed on NW radius and thickness of gate insulator. That is because the sum of NW radius and thickness of gate insulator could be close to the half of

NW pitch as shown in Fig. 2.11(b).

In this work, using FE material which can operate as S-shaped P-V characteristic based on the NC model [1], we focus on the GAA NW-NCFET with CMOS-compatible FE:HfO_2, and investigate its I_{on}/I_{off} ratio enhancement, as a determining factor of energy efficiency [13]. Furthermore, the scalability of NW pitch of FE:HfO_2-based NW-NCFET by thinning the gate insulator and narrowing NW have been investigated from the viewpoint of constraints regarding very limited NW pitch.

2.10 Device Structures and Model for NW-NCFET

Fig. 2.12 shows the device structures of (a) DG-NCFET and (b) NW-NCFET studied here. Gate stack consists of metal-FE:HfO_2-interfacial insulator-semiconductor (MFIS structure). Internal metal plate between FE layer and interfacial insulator is not considered here. Fin width (T_{si}) of DG-NCFET and NW diameter (2R) of NW-NCFET are set to 5nm as nominal. Nominal thickness of interfacial insulator (T_{ox}) is EOT=1nm, and thickness of FE:HfO_2 (T_{fe}) is optimized to obtain the high I_{on}/I_{off} ratio in an each condition. These 2R, T_{si}, T_{ox}, and T_{fe} of device structures are variable parameters in this study. L_g used here is 200nm for long channel device.

All simulations were conducted by an analytic compact model of non-doped long channel NW-NCFET [24-25]. These models are composed by following two parts: (1) equations to describe the classical NW-MOSFET (Poisson equation, boundary condition of charge density, current continuity) [26], and (2) Landau equation [12] to describe the NC characteristic of FE layer [1]. By combining these equations, the characteristics of non-doped channel NCFETs can be expressed in analytic forms whose details are explained in Ref. 24 for NW-NCFET, and Ref.2 for DG-NCFET. The different polarizations in FE layer at the

source and drain side are incorporated in these compact models.

In this model, the details of additional physical effects such as short channel effect, quantum mechanical effect, and velocity saturation phenomenon are not considered. The impacts of parasitic capacitances on NCFET characteristics [27] are not included in these models.

Firstly, we simulated channel size dependences of I_d-V_g characteristics of NW-NCFET as well as classical NW-MOSFET with 2R as a variable parameter. As a reference, the same simulations were conducted for DG-NCFET and DG-MOSFET where T_{si} was a variable parameter. The channel size dependences of the I_{on}, I_{off}, and I_{on}/I_{off} ratio in the NW-FETs and DG-FETs were discussed.

Secondly, the I_{on}/I_{off} ratio enhancement of NW-NCFET was investigated by comparing the I_{on}/I_{off} ratio of NW-NCFET with NW-MOSFET and/or DG-NCFET at same channel size. For fair comparison, NW-FETs were assumed as FET with multiple NWs, so that I_{on} of NW-FETs can match the I_{on} of DG-FETs. Hereafter, 2R and T_{si} were selected to 5nm as channel sizes applicable for beyond FinFET technology node of 10nm. With those aggressively scaled sizes, quantum mechanical effect may need to be included. However, in the scope of this study motivated to investigate the impact of intrinsic geometric scaling on NC effect in NW-NCFET design, we consider not to include quantum mechanical effect for simplicity in the range of 2R=5nm.

Thirdly, the I_{on}/I_{off} ratio was simulated by varying T_{fe} and/or T_{ox}, then we compared the I_{on}/I_{off} ration of NW-NCFET with that of DG-NCFET. Furthermore, the I_{on}/I_{off} ratio was also simulated by varying 2R and/or T_{fe}, then we searched design window of 2R and/or T_{fe} under the NW integration-induced constraint of the very tight NW pitch.

2.11 I_d-V_g Characteristics and Channel Size Dependences

Fig. 2.13 shows the simulated I_d-V_g characteristics of (a) NW-MOSFET, and (b) NW-NCFET with a single NW where 2R was a variable parameter. T_{ox} was fixed to EOT=1nm. Here, T_{fe} was optimized to maximize I_{on}/I_{off} ratio for an each channel size in a range of hysteresis-free operation. As illustrated in chapter 2.4, FE material parameters of remanent polarization (P_r) and coercive field (E_c) were set to 5μC/cm^2 and 1MV/cm, respectively, by considering experimental reports of FE:HfO_2 [6-7,14-19]. Drain voltage (V_d) was 0.5V. NC effect effectively enhances the drain current near the start point of strong inversion region in NW-NCFET compared to NW-MOSFET. And both of I_{on} and I_{off} decrease as 2R decreased.

The SS of NW-FETs is plotted in Fig. 2.14 which is extracted from the I_d-V_g characteristics of Fig. 2.13. In Fig. 2.14(a), the SS of NW-MOSFET has a limit of 60mV/decade within subthreshold region which is attributed to carrier transport dynamics based on thermal diffusion [28]. Fig. 2.14(b) shows, however, the SS of NW-NCFET is lower than 60mV/decade which is attributed to the NC effect. Minimum SS is around 20 to 30mV/decade where drain current level is near start point of strong inversion although SS in deeper subthreshold region is almost 60mV/decade. These features are consistent with the previous studies [8,22,24]. This narrow region for steep SS is attributed to the capacitance mismatching between FE layer and semiconductor within subthreshold region. This capacitance mismatching consequently suppresses NC effect-induced voltage amplification under low amplitude.

As a reference, the same simulations were conducted for DG-MOSFET and DG-NCFET where T_{si} was a variable parameter. The I_d-V_g characteristics were plotted in Figs. 2.15(a) and (b) for DG-MOSFET and DG-NCFET, respectively. As with the case of NW-NCFET, T_{fe} was

optimized to maximize I_{on}/I_{off} ratio for an each T_{si} in a range of hysteresis-free operation. Optimized T_{fe} values for an each T_{si} in DG-NCFET (Fig. 2.15(b)) were in the range of 7 to 8 nm when T_{ox}, P_r and E_c were set to same values with NW-NCFET. Based on the NC model, NC effect enhances the drain current near the start point of strong inversion [1]. I_{on} is almost independent of T_{si} and I_{off} decreases as T_{si} decreased. The SS of DG-FETs were plotted in Fig. 2.16, (a) is for DG-MOSFET, and (b) is for DG-NCFET. SS lower than 60mV/decade around the start point of strong inversion is obtained in DG-NCFET whereas SS in DG-MOSFET has a limit of 60mV/decade.

To investigate channel size dependences of NW-FETs and/or DG-FETs, we plotted (a) I_{on}, (b) I_{off}, and (c) I_{on}/I_{off} ratio versus 2R and/or T_{si} in Fig. 2.17. These channel size dependences can be explained by considering where current flows in on-state and off-state in NW-FETs and/or DG-FETs. Within subthreshold region, a volume (weak) inversion occurs which results in I_{off} proportional to cross sectional area of channel. On the other hand, in strong inversion, a surface inversion occurs which results in I_{on} proportional to the perimeter of the channel. There is transition from the volume inversion state in subthreshold region to the surface inversion state in strong inversion [26,29]. As a result, in the case of NW-FETs, I_{on} is proportional to 2R, and I_{off} to $(2R)^2$, consequently, the I_{on}/I_{off} ratio is proportional to $(2R)^{-1}$ as shown in Figs. 2.17(a), (b), and (c), respectively. In the case of DG-FETs, however, I_{on} is almost independent of T_{si}, and I_{off} is proportional to T_{si}, consequently, the I_{on}/I_{off} ratio is proportional to $(T_{si})^{-1}$ as shown in Figs. 2.17(a), (b), and (c), respectively.

2.12 I_{on}/I_{off} Ratio Enhancement in NW-NCFET

According to Fig. 2.17(c), both of NW-NCFET and DG-NCFET have 5× higher I_{on}/I_{off} ratio than NW-MOSFET and DG-MOSFET at the same 2R and/or T_{si}, respectively.

Furthermore, NW-NCFET has 2x higher I_{on}/I_{off} ratio than DG-NCFET.

To investigate the impact of this I_{on}/I_{off} ratio enhancement in NW-NCFET, we plotted I_d-V_g characteristics of NW-NCFET and DG-NCFET in Fig. 2.18 as well as MOSFETs, where 2R and T_{si} are 5nm, and V_d=0.5V. For fair comparison, assuming NW-FETs with multiple NWs [30] and stacked structure [31-32], drain current of NW-FETs were multiplied by a relevant number of nanowires, so that, I_{on} of NW-FETs can match that of DG-FETs.

Fig. 2.18 shows both of NW-NCFET and DG-NCFET have 5x higher I_{on} than NW-MOSFET and DG-MOSFET, respectively, as mentioned above. This I_{on} enhancement and SS lowering are attributed to the NC effect of FE layer described by NC model.

Fig. 2.18 shows that NW-NCFET has 50% lower I_{off} than DG-NCFET. The reason of this I_{off} reduction in NW-NCFET can be attributed to the cross sectional area of channel where current in the off-state is relatively smaller in NW-FETs than in DG-FETs owing to the GAA NW channel structure of NW-NCFET. This I_{on}/I_{off} ratio enhancement in NW-NCFET indicates that NW-NCFET is beneficial for energy-efficient applications requiring ultralow standby power consumption. Although quantum mechanical effect was not included in the used compact models, previous studies based on quantum mechanical model [33-34], have shown that higher I_{on}/I_{off} ratio can be obtained in NW-MOSFETs comparing to DG-MOSFETs when their channel sizes were 2R=T_{si}=5nm. Furthermore, when considering quantum inversion layer [30] in strong inversion, the peak position of electron concentration from gate oxide/Si interface is closer than 1nm where 2R=T_{si}=5nm [33,35-36]. This suggests that impact of quantum inversion layer on NC effect is negligible. Therefore, it can be said that our classical compact model-based simulation results with 2R=T_{si}=5nm shown in Fig. 2.18 and hereafter can be validated [33-36].

A three-dimensional contour plot of the I_{on}/I_{off} ratio in NW-NCFET versus T_{fe} and/or

T_{ox}=EOT is re-plotted in Fig. 2.19(a). As a reference, a contour plot of the I_{on}/I_{off} ratio in DG-NCFET is plotted in Fig. 2.19(b). NW-NCFET has wider design window where higher I_{on}/I_{off} ratio can be achieved than DG-NCFET as illustrated above.

2.13 Scalability of NW Pitch for NW Integration

In previous chapters, channel size dependences and I_{on}/I_{off} ratio enhancement in NW-NCFET were mainly discussed. In this chapter, we use 2R and/or T_{fe} as variable parameters to investigate the scalability of NW pitch which requires 2R and T_{fe} to be sufficiently small in order to fit to the very tight NW pitch.

Fig. 2.20 shows the contour plot of I_{on}/I_{off} ratio versus 2R and T_{fe} where T_{ox}=EOT=1nm. A wide range of design window was achieved with higher I_{on}/I_{off} ratio in NW-NCFET than in NW-MOSFET; T_{fe}=0nm. Higher I_{on}/I_{off} ratio is achieved when 2R becomes narrow and/or T_{fe} becomes thick. The mechanisms have been explained in previous chapter of 2.11. From Fig. 2.20, it is expected that NW-NCFET performance can be maximized by adjusting 2R and T_{fe} within the design window, if there is no constraint regarding NW pitch.

In real device, however, constraints of $R + T_{fe} + T_{ox} <$ pitch/2 should be considered because this constraint is inevitable for the integration of tight-pitch NWs as illustrated in Fig. 2.11(b). The boundary of this constraint is shown by dotted line in Fig. 2.20. There exists a design window where higher I_{on}/I_{off} ratio can be obtained as the boundary of NW pitch moves from 25nm to 20nm and 15nm indicated by the arrow in Fig. 2.20. This result indicates that GAA NW-NCFET still has a design point even under very tight NW pitch integration of sub-30nm.

This contour plot of the I_{on}/I_{off} ratio in NW-NCFET versus 2R and/or T_{fe} is re-plotted in Fig. 2.21(a) in three-dimensional style. As a reference, the contour plot of the I_{on}/I_{off} ratio in

DG-NCFET is plotted in Fig. 2.21(b). NW-NCFET has wider design window where higher I_{on}/I_{off} ratio can be achieved than DG-NCFET as illustrated in chapter of 2.12.

2.14 Summary for Study on NW-NCFET

In this work, based on the NC model, the I_{on}/I_{off} ratio enhancement and scalability of FE:HfO_2-based NW-NCFET were systematically investigated. NW diameter dependences of I_{on}, I_{off}, and I_{on}/I_{off} ratio in NW-NCFET were studied as well as Fin width dependences in DG-NCFET. Due to NC effect of FE layer which is characterized by the NC model, NW-NCFET had 5x higher I_{on}/I_{off} ratio than classical NW-MOSFET. NW-NCFET had 2x higher I_{on}/I_{off} ratio than DG-NCFET owing to GAA NW channel structure of NW-NCFET. Regarding scalability of NW pitch in FE:HfO_2-based NW-NCFET, there was a wide range of design window for 2R and T_{fe} where high I_{on}/I_{off} ratio can be obtained even under multiple NWs integration-induced constraint with sub-30nm NW pitch. Based on the obtained results, when FE material is assumed to be characterized by the NC model, FE:HfO_2-based NW-NCFET is found to be applicable for sub-10nm L_g technology node and sub-30nm NW pitch integration.

References

[1] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices”, Nano Letters, vol. 8 no. 2, pp. 405-410, 2008.

[2] D. Jiménez, E. Miranda, and A. Godoy, “Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors”, IEEE Trans. Electron Devices, vol. 57, no. 10, pp. 2405-2409, Oct. 2010.

[3] Y. G. Xiao, M. H. Tang, Y. Xiong, J. C. Si, C. P. Cheng, B. Jiang, H. Q. Cai, Z. H. Tang, X. S. Lv, X. C. Gu, Y. C. Zhou, Current Applied Physics, 12, 1591 (2012).

[4] C. Jiang, R. Liang, J. Wang, and J. Xu, “A carrier-based analytical theory for negative capacitance symmetric double-gate field effect transistors and its simulation verification”, J. Phys. D: Appl. Phys., vol. 48, 365103, 2015.

[5] T. Mikolajick, C. Dehm, W. Hartner, I. Kasko, M. J. Kastner, N. Nagel, M. Moert, and C. Mazure, "FeRAM technology for high density applications", Microelectronics Reliability, vol. 41, pp. 947-950, 2001.

[6] J. Müller, T. S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, "Ferroelectricity in Simple Binary ZrO_2 and HfO_2", Nano Letters, vol. 12, no. 8, pp. 4318-4323, 2012.

[7] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwang, "Evolution of phases and ferroelectric properties of thin Hf0.5Zr0.5O2 films according to the thickness and annealing temperature", Applied Physics Letter, 102, 242905, 2013.

[8] M. Kobayashi and T. Hiramoto, "Device Design Guideline for Steep Slope Ferroelectric FET Using Negative Capacitance in Sub-0.2V Operation: Operation Speed, Material Requirement and Energy Efficiency", in VLSI Tech. Symp. Dig., Kyoto, Japan, 2015, pp. 212-213.

[9] C.-H. Lin, B. Greene, S. Narasimha, J. Cai, A. Bryant, C. Radnes, V. Narayanan, B. Linder, H. Ho, A. Aiyar, E. Alptekin, J-J. An, M. Aquilino, R. Bao, V. Basker, N. Breil, M. Brodsky, W. Chang, L. Clevenger, D. Chidambarro, C. Christiansen, D. Conklin, C. DeWan, H. Dong, L. Economikos, B. Engel, S. Fang, D. Ferrer, A. Friedman, A. Gabor, F. Guarin, X. Guan, M. Hasanuzzaman, J. Hong, D. Hoyos, B. Jagannathan, S. Jain, S-J. Jeng, J. Johnson, B. Kannan, Y. Ke, B. Khan, B. Kim, S. Koswatta, A. Kumar, T. Kwon, U. Kwon, L. Lanzerotti, H-K. Lee, W-H. Lee, A. Levesque, W. Li, Z. Li, W. Liu, S. Mahajan, K. McStay, H. Nayfeh, W. Nicoll, G. Northrop, A. Ogino, C. Pei, S. Polvino, R. Ramachandran, Z. Ren, R. Robison, I. Saraf, V. Sardesai, S. Saudari, D. Schepis, C. Sheraw, S. Siddiqui, L. Song, K. Stein, C. Tran, H. Utomo, R. Vega, G. Wang, H. Wang, W. Wang, X. Wang, D. Wehelle-Gamage, E. Woodard, Y. Xu, Y. Yang, N. Zhan, K. Zhao, C. Zhu, K. Boyd, E. Engbrecht, K. Henson, E. Kaste, S. Krishnan, E. Maciejewski, H. Shang, N. Zamdmer, R. Divkaruni, J. Rice, S. Stiffler, and P. Agnello, "High Performance 14nm SOI FinFET CMOS Technology with $0.0174\mu m^2$ embedded DRAM and 15 Levels of Cu Metallization", in IEDM Tech. Dig., San Francisco, CA, USA, 2014, pp. 74-76.

[10] C.-H. Jan, U. Bhattachara, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai., "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications", in IEDM Tech. Dig., San Francisco, CA, USA, 2012, pp. 44-47.

[11] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs", IEEE Electron Device Letters, vol. 25, no. 2, pp. 107-109, Feb. 2004.

[12] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical FET be lowered

below 60 mV/decade?", in IEDM Tech. Dig., San Francisco, CA, USA, 2008.

[13] H. Fuketa, T. Yasufuku, S. Iida, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Device-Circuit Interactions in Extremely Low Voltage CMOS Designs", in IEDM Tech. Dig., Washington, DC, USA, 2011, pp. 559-562.

[14] M. Kobayashi, N. Ueyama, K. Jang, and T. Hiramoto, "Experimental Study on Polarization-Limited Operation Speed of Negative Capacitance FET with Ferroelectric HfO_2", in IEDM Tech. Dig., San Francisco, CA, USA, 2016, pp. 314-317.

[15] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, K. D. Kim, and C. S. Hwang, Applied Physics Lett. 105, 072902 (2014).

[16] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, Adv. Funct. Mater. 22, p. 2412 (2012).

[17] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Applied Physics Lett. 99, 102903 (2011).

[18] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, IEDM Tech. Dig., 2011, p. 547.

[19] T. Shimizu, T. Yokouchi, T. Shiraishi, T. Oikawa, P. S. Sankara Rama Krishnan, and H. Funakubo, Japanese Journal of Applied Physics, 53, 09PA04 (2014).

[20] A. Cano and D. Jiménez, "Multidomain ferroelectricity as a limiting factor for voltage amplification in ferroelectric field-effect-transistors", Applied Physics Letter, 97, 133509, 2010.

[21] S. Bangsaruntip, A. Majumdar, G. M. Cohen, S. U. Engelmann, Y. Zhang, M. Guillorn, L. M. Gignac, S. Mittal, W. S. Granham, E. A. Joseph, D. P. Klaus, J. Chang, E. A. Cartier, and J. W. Sleight, "Gate-all-around silicon nanowire 25-stage CMOS ring oscillators with diameter down to 3nm", in VLSI Tech. symp. Dig., Jun. 2010, pp. 21-22.

[22] K. Jang, T. Saraya, M. Kobayashi, and T. Hiramoto, "On gate stack scalability of double-gate negative-capacitance FET with ferroelectric HfO_2 for energy efficient sub-0.2 V operation", Japanese Journal of Applied Physics, 57, 024201, 2018.

[23] K. Jang, T. Saraya, M. Kobayashi, and T. Hiramoto, "I_{on}/I_{off} ratio enhancement and scalability of gate-all-around nanowire negative-capacitance FET with ferroelectric HfO_2", Solid-State Electronics, Vol. 136, pp. 60-67, 2017.

[24] Y. G. Xiao, Z. J. Chen, M. H. Tang, Z. H. Tang, S. A. Yan, J. C. Li, X. C. Gu, Y. C. Zhou, and X. P. Ouyang, "Simulation of electrical characteristics in negative capacitance surrounding-gate ferroelectric field-effect transistors", Applied Physics Letters, 101, 253511, 2012.

[25] C. Jiang, R. Liang, J. Wang, and J. Xu, "Analytical drain current model for long-channel gate-all-around negative capacitance transistors with a metal-ferroelectric-insulator -semiconductor structure", Japanese Journal of Applied Physics, 55, 024201, 2016.

[26] D. Jiménez, B. Iniguez, J. Sune, L. F. Marsal, J. Pallares, J. Roig, and D. Flores, “Continuous analytic I-V model for surrounding-gate MOSFETs”, IEEE Electron Device Letters, vol. 25, no. 8, pp. 571-573, Jul. 2004.

[27] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, C. Hu, “Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET characteristics”, IEEE Electron Device Letters, vol. 38, no. 1, pp. 142-144, Jan. 2017.

[28] Y. Taur and T. H. Ning, “MOSFET Devices”, in Fundamentals of Modern VLSI Devices, 2nd ed., ch. 3, pp. 163-166, Cambridge University Press, 2013.

[29] Y. Taur, X. Liang, W. Wang, and H. Lu, “A continuous, analytic drain-current model for DG MOSFETs”, IEEE Electron Device Letters, vol. 25, no. 2, pp. 107-109, Feb. 2004

[30] C.-H. Jan, U. Bhattachara, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai., “A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications”, in IEDM Tech. Dig., San Francisco, CA, USA, 2012, pp. 44-47.

[31] C. Dupré, A. Hubert, S. Becu, M. Jublot, V. Maffini-Alvaro, C. Vizioz, F. Aussenac, C. Arvet, S. Barnola, J.-M. Hartmann, G. Garnier, F. Allain, J.-P. Colonna, M. Rivoire, L. Baud, S. Pauliac, V. Loup, T. Chevolleau, P. Rivallin, B. Guillaumot, G. Ghibaudo, O. Faynot, T. Ernst, and S. Deleonibus, “15nm-diameter 3D Stacked Nanowires with Independent Gates Operation: ΦFET”, in IEDM Tech. Dig., 2008, pp. 749-752.

[32] H. Mertens, R. Ritzenthlaer, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuynck, A. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, and A. V-Y Thean, “Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates”, in VLSI Tech. Symp. Dig., Jun. 2016, 15.1.

[33] E. Gnani, S. Reggiani, M. Rudan, and G. Baccarani, “On the Electrostatics of Double-Gate and Cylindrical Nanowire MOSFETs”, Journal of Computational Electronics, 4, pp. 71-74, 2005.

[34] X. Chen and C. M. Tan, “Modeling and analysis of gate-all-around silicon nanowire FET”, Microelectronics Reliability, 54, pp. 1103-1108, 2014.

[35] M. Shoji and S. Horiguchi, “Phonon-limited inversion layer electron mobility in extremely thin Si layer of silicon-on-insulator metal-oxide-semiconductor field-effect transistor”, J. Appl. Phys. 82, pp. 6096-6101, 1997.

[36] Y. Taur, “An Analytical Solution to a Double-Gate MOSFET with Undoped Body”, IEEE Electron Device Letters, vol. 21, no. 5, pp. 245-247, 2000.

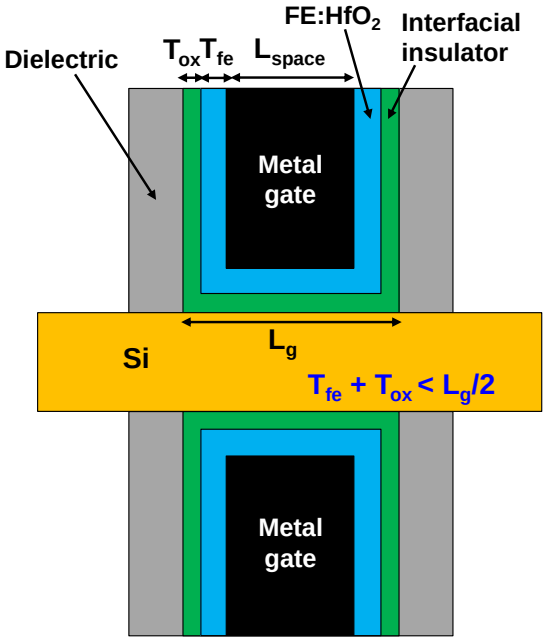


Fig. 2.1. A schematic of the cross-sectional image of FE:HfO_2-based DG-NCFET with gate-last process. To fit the FE gate insulator and interfacial insulator to the structure, a process-induced constraint of $T_{fe} + T_{ox} < L_g/2$ should be considered.

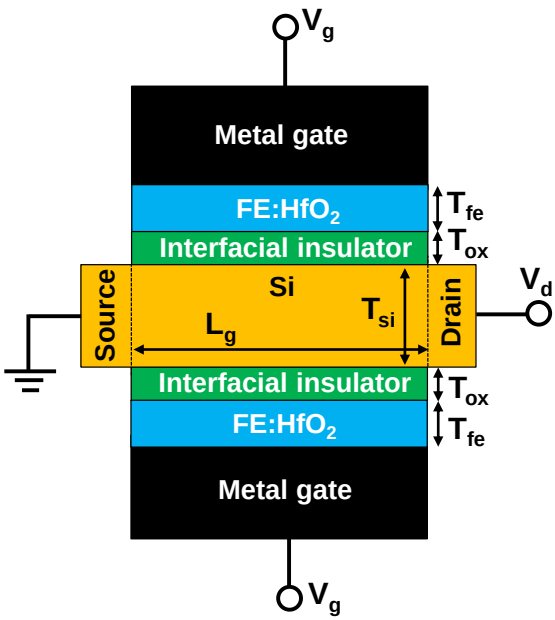


Fig. 2.2. A schematic of DG-NCFET using FE:HfO_2 as a gate insulator with an interfacial insulator.

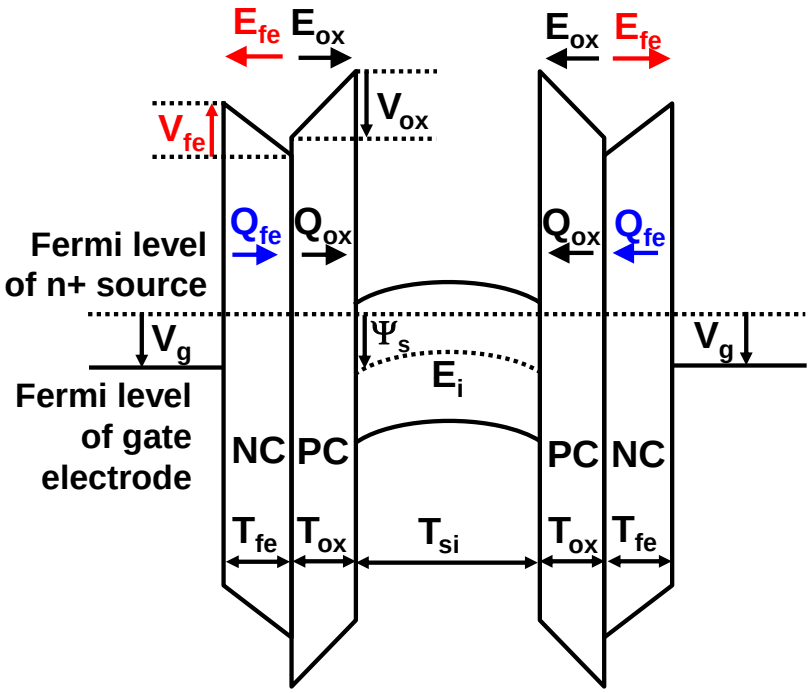


Fig. 2.3. A schematic of band diagram of multi-gate NCFET when positive gate voltage (V_g) is applied. NC effect of FE layer is a source of negative V_{fe} which realizes $d\Psi_s > dV_g$.

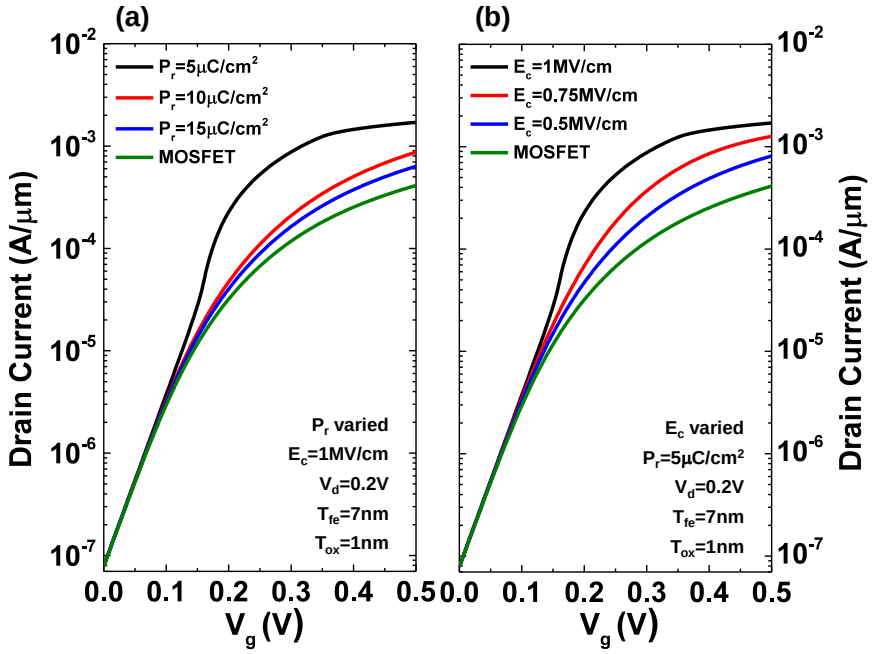


Fig. 2.4. Simulated I_d-V_g characteristics of DG-NCFET where material parameters of FE:HfO_2 were variable parameters. (a) P_r is varied and E_c is fixed, and (b) P_r is fixed and E_c is varied. Simulated I_d-V_g characteristics of DG classical MOSFET (EOT=1nm) were also shown.

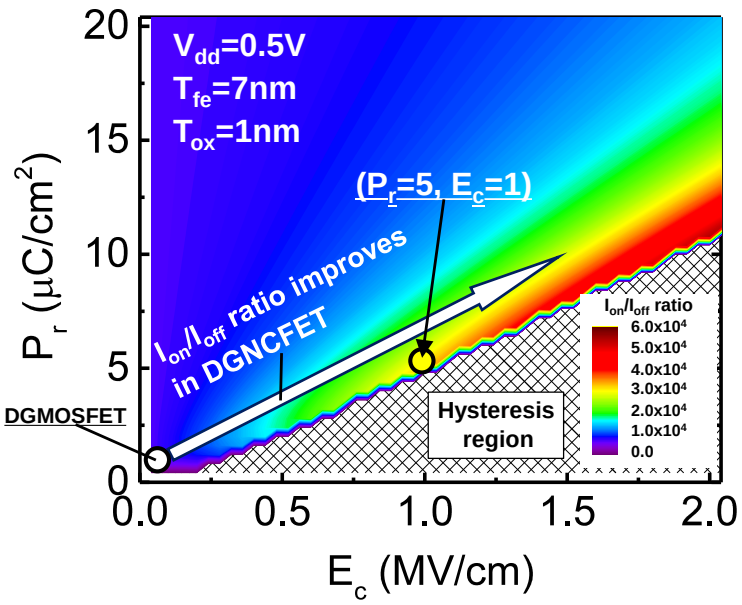


Fig. 2.5. Simulated contour plot of I_{on}/I_{off} ratio versus P_r and E_c of FE gate insulator where T_{fe}=7nm, T_{ox}=EOT=1nm, and V_{dd}=0.5V.

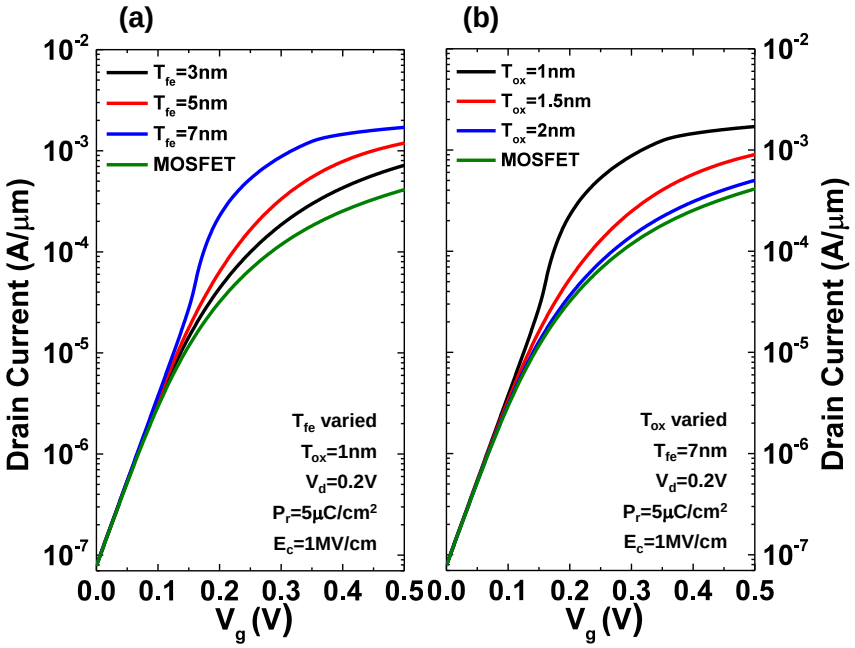


Fig. 2.6. Simulated I_d-V_g characteristics of DG-NCFET where thickness of FE:HfO_2 (T_{fe}) and/or interfacial insulator (T_{ox}) were variable parameters. (a) T_{fe} is varied and T_{ox} is fixed, and (b) T_{ox} is varied and T_{fe} is fixed. Simulated I_d-V_g characteristics of DG classical MOSFET (EOT=1nm) were also shown.

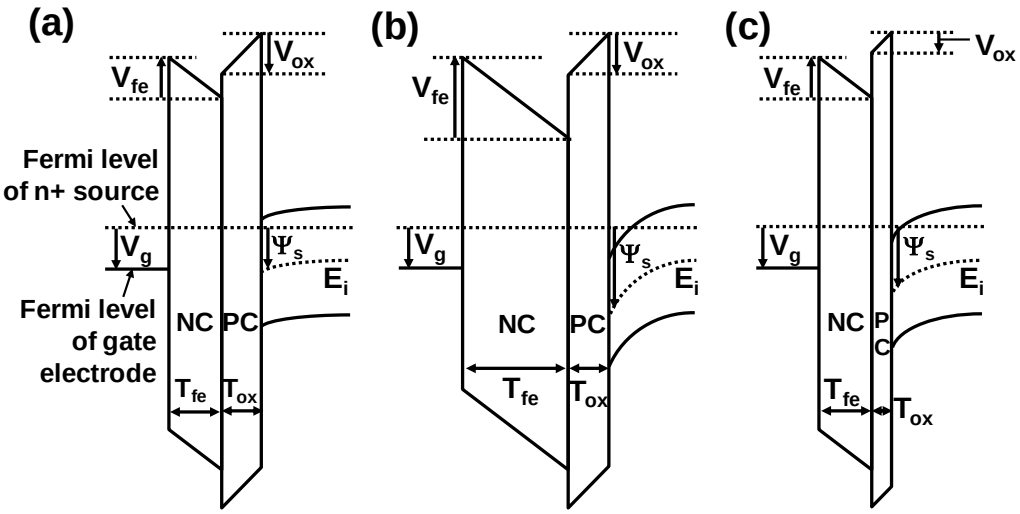


Fig. 2.7. Schematics of the band diagram of DG-NCFET to describe I_d-V_g characteristics in Fig. 2.6. Comparing to (a) nominal case, (b) higher negative voltage (V_{fe}) is induced with thicker T_{fe}, and (c) less voltage drops in the interfacial layer (V_{ox}) with thinner T_{ox}.

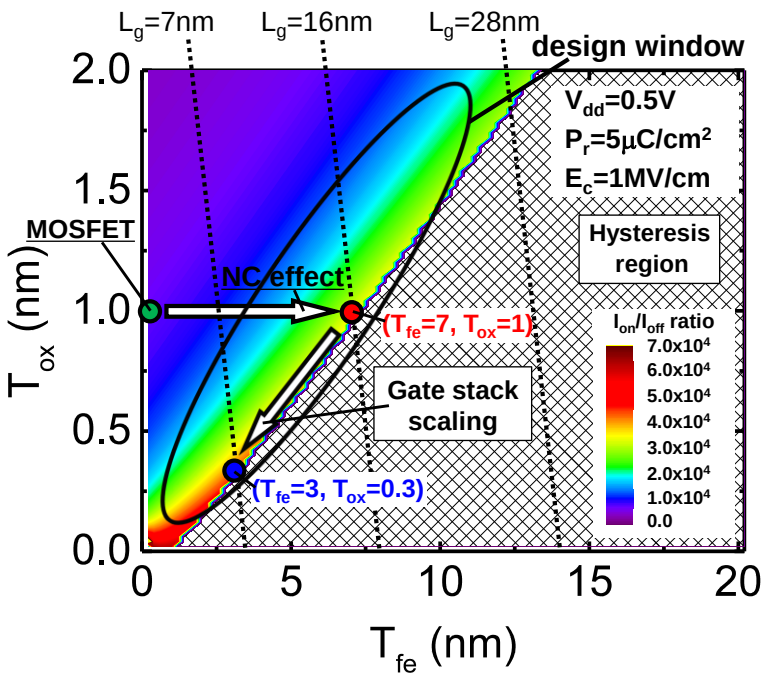


Fig. 2.8. Simulated contour plot of the I_{on}/I_{off} ratio versus T_{fe} and T_{ox}=EOT at V_{dd}=0.5V.

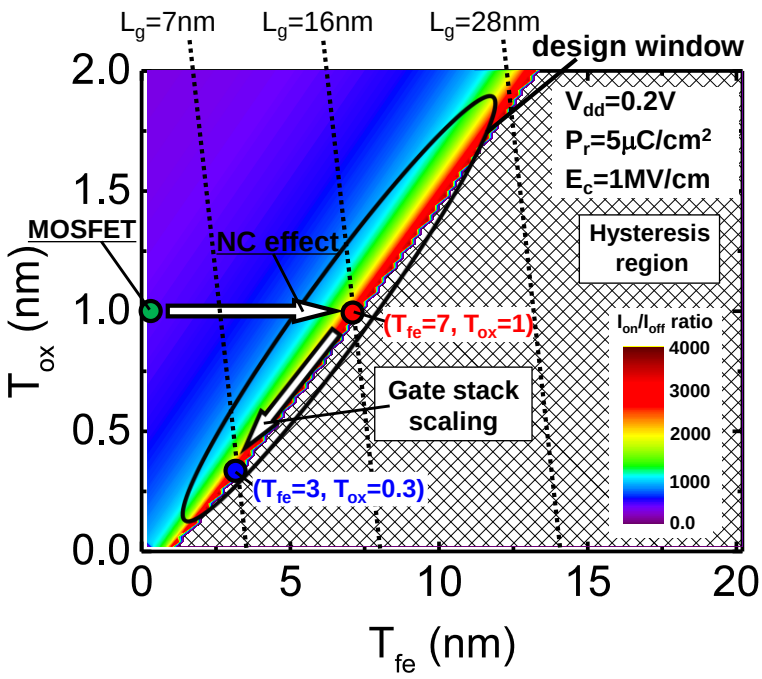


Fig. 2.9. Simulated contour plot of the I_{on}/I_{off} ratio versus T_{fe} and T_{ox}=EOT at V_{dd}=0.2V.

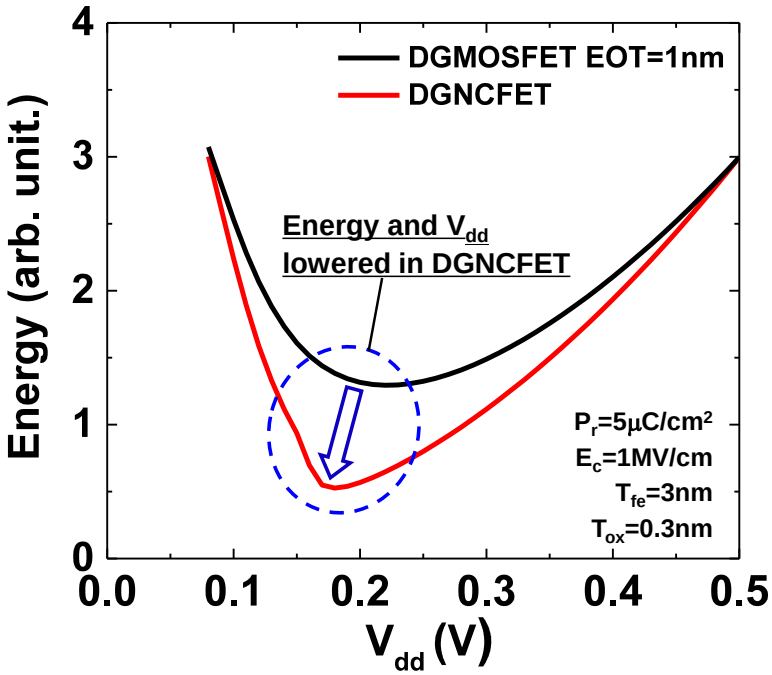


Fig. 2.10. Simulated energy per switching of DG-NCFET with optimized gate stack thickness compared to DG classical MOSFET whose EOT=1nm.

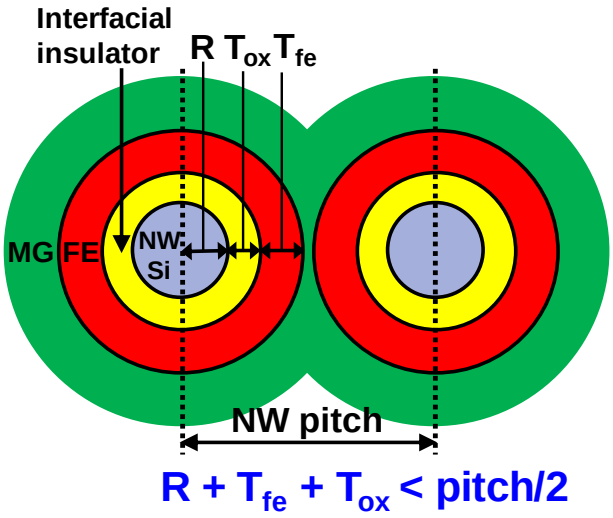


Fig. 2.11. A schematic of the cross-sectional images of multiple NW channels in FE:HfO_2-based NW-NCFET. To fit the gate insulator and NW to the structure of GAA-NW-NCFET, multiple NWs integration-induced constraint of $R+T_{fe}+T_{ox}$ < pitch/2 is considered.

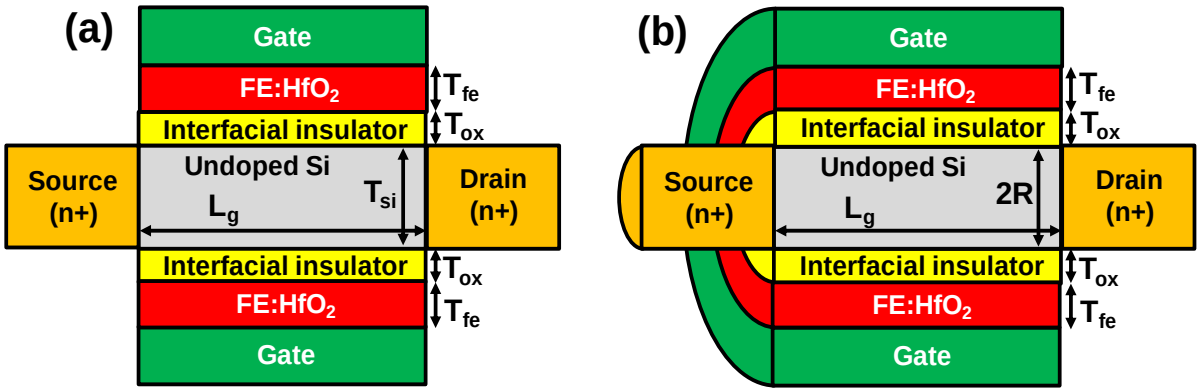


Fig. 2.12. Schematics of multi-gate NCFET using FE:HfO_2 as a gate insulator with an interfacial insulator. (a) is DG-NCFET, and, (b) is GAA NW-NCFET.

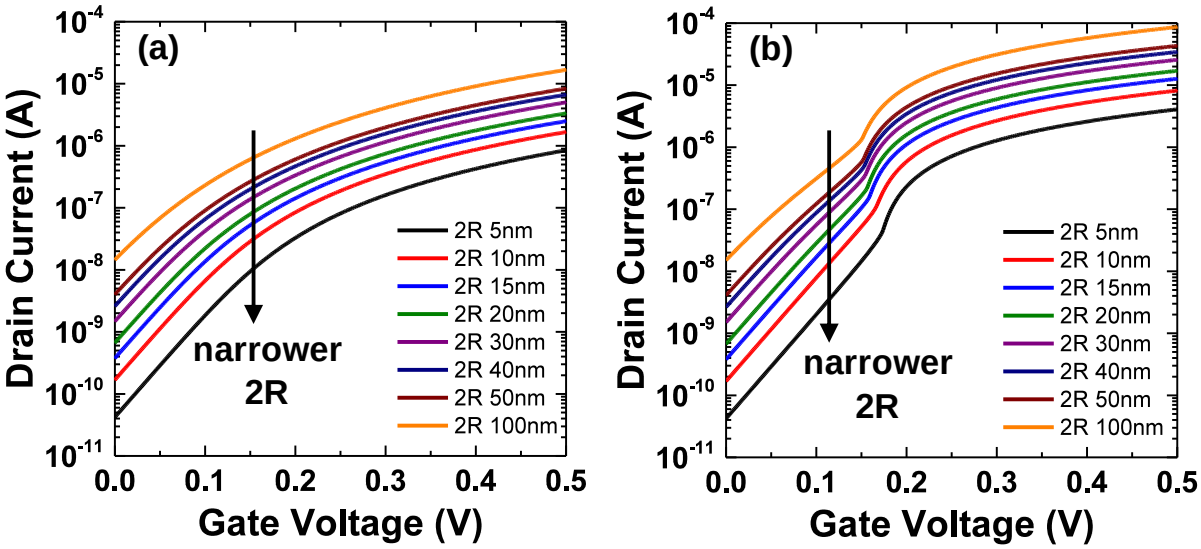


Fig. 2.13. Simulated I_d-V_g characteristics of NW-FETs with single NW where NW diameter (2R) was a variable parameter. T_{ox}=EOT=1nm, V_d=0.5V were used here. (a) is for NW-MOSFET and, (b) is for NW-NCFET with optimum T_{fe} to obtain high I_{on}/I_{off} ratio.

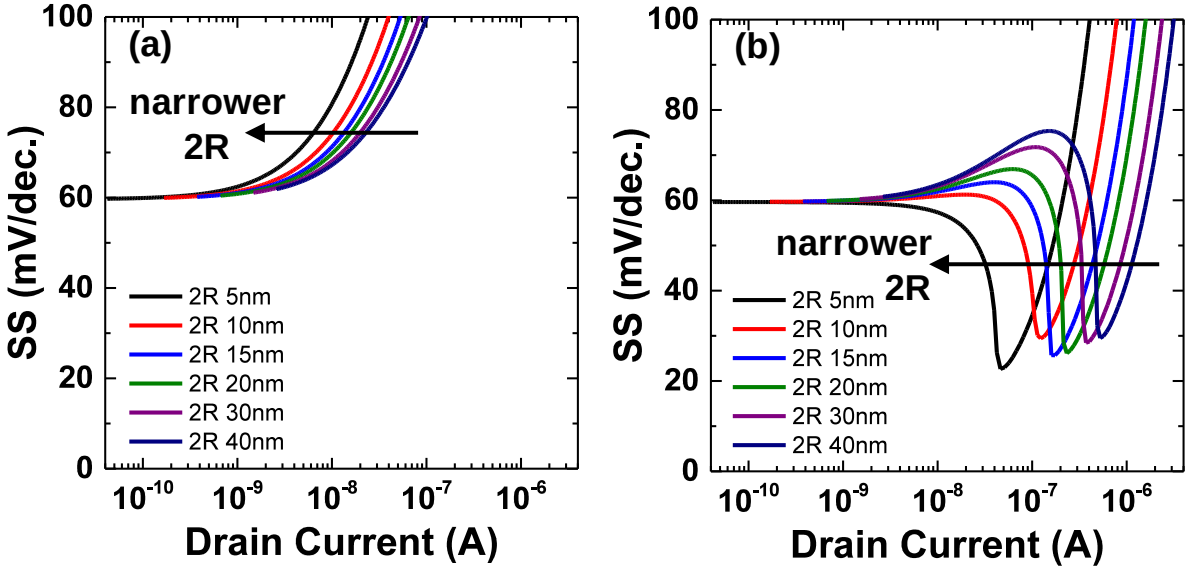


Fig. 2.14. Simulated SS-I_d characteristics of NW-FETs with single NW where NW diameter (2R) was a variable parameter. T_{ox}=EOT=1nm, V_d=0.5V were used here. (a) is for NW-MOSFET and, (b) is for NW-NCFET with an optimum T_{fe} to obtain high I_{on}/I_{off} ratio.

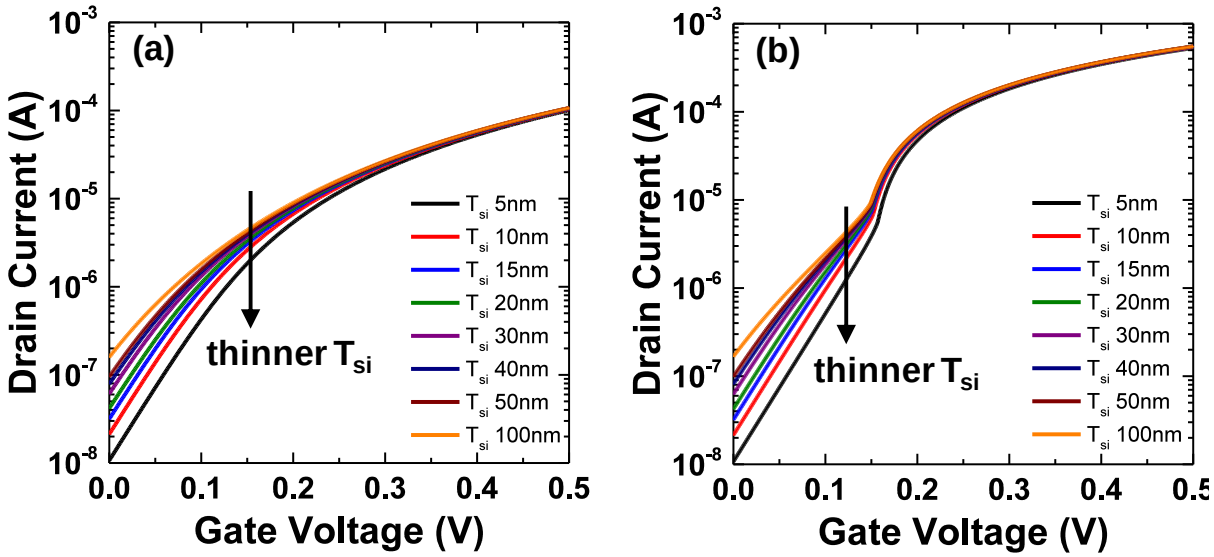


Fig. 2.15. Simulated I_d-V_g characteristics of DG-FETs where fin width (T_{si}) was a variable parameter. T_{ox}=EOT=1nm, V_d=0.5V were used here. (a) is for DG-MOSFET, and (b) is for DG-NCFET with an optimum T_{fe} to obtain high I_{on}/I_{off} ratio.

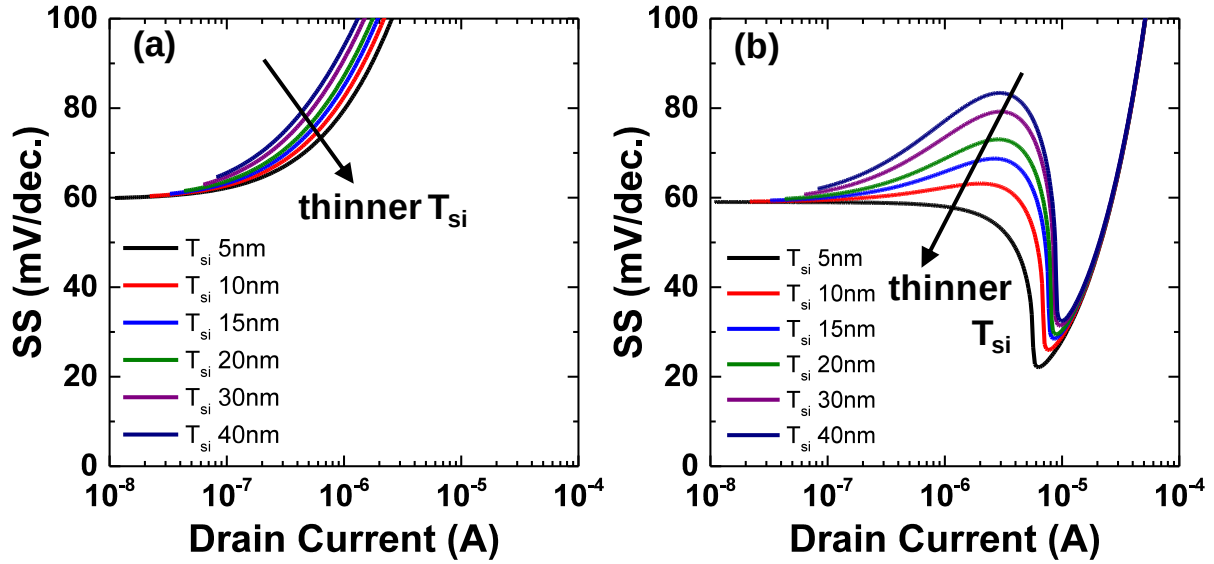


Fig. 2.16. Simulated SS-I_d characteristics of DG-FETs where fin width (T_{si}) was a variable parameter. T_{ox}=EOT=1nm, V_d=0.5V were used here. (a) is for DG-MOSFET, and (b) is for DG-NCFET with an optimum T_{fe} to obtain high I_{on}/I_{off} ratio.

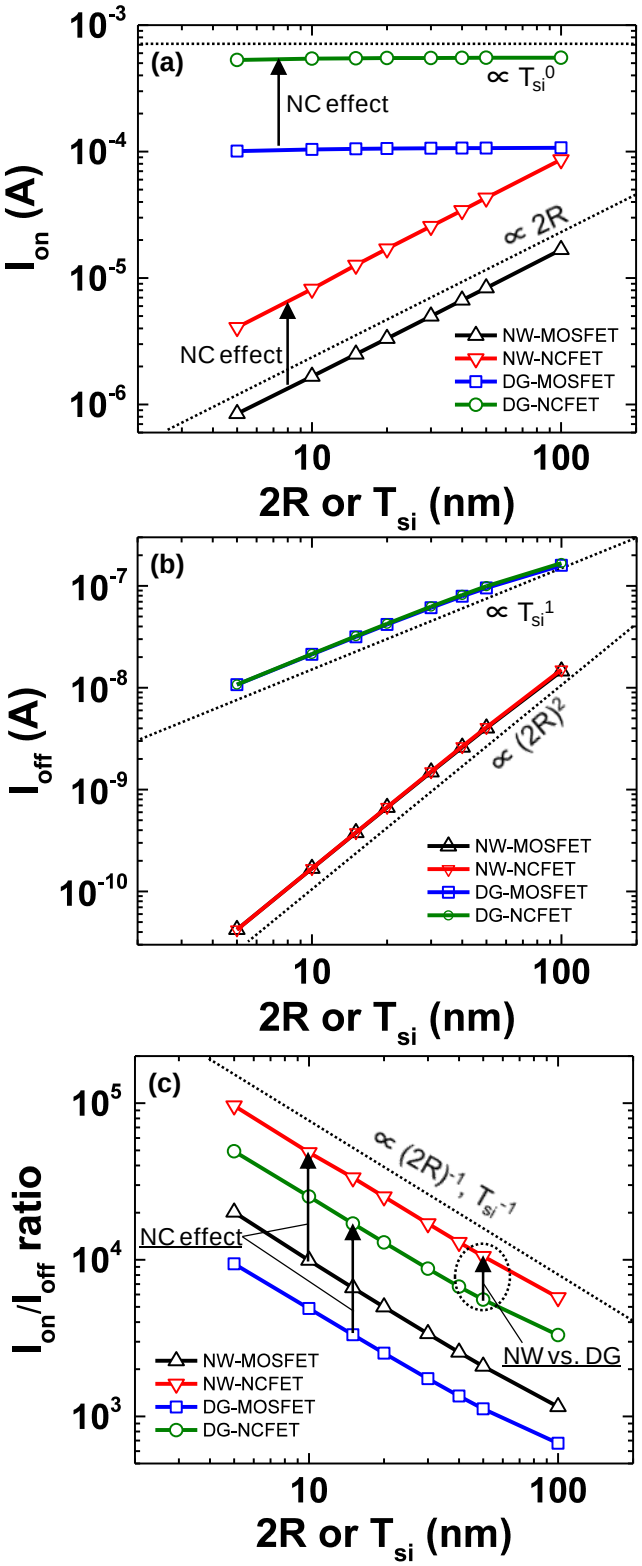


Fig. 2.17. Simulated channel sizes dependences in NW-FETs and DG-FETs. (a) I_{on}, (b) I_{off}, and (c) I_{on}/I_{off} ratio versus 2R and/or T_{si}.

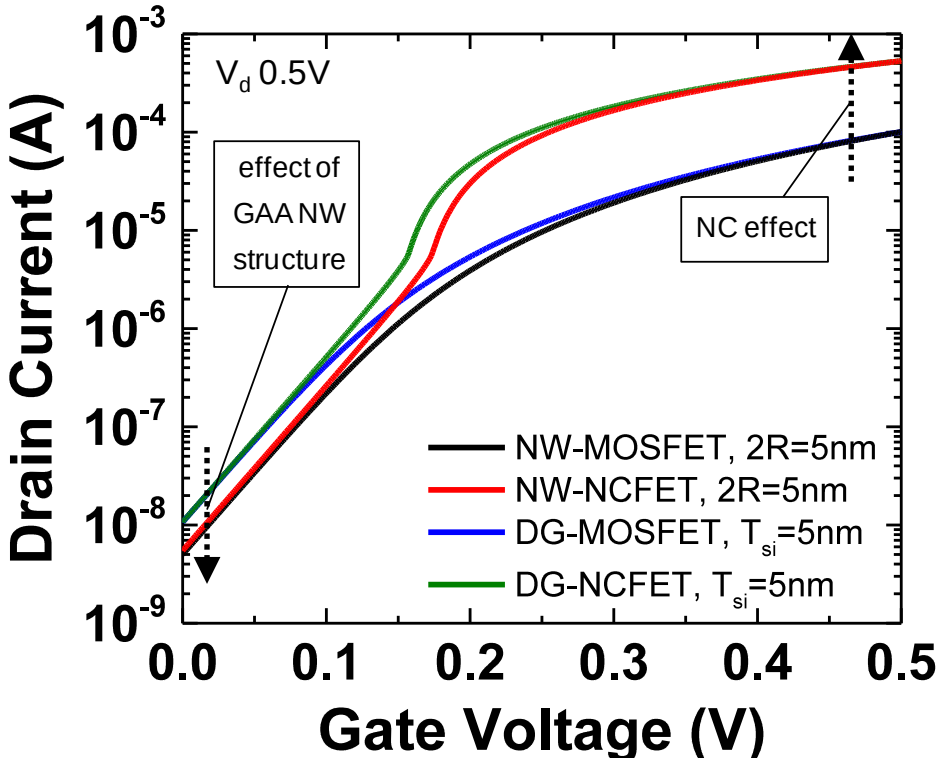


Fig. 2.18. Simulated I_d-V_g characteristics of NW-FETs and DG-FETs where 2R and T_{si} are 5nm, and V_d=0.5V. Drain current of NW-FETs is multiplied to match that of DG-FETs.

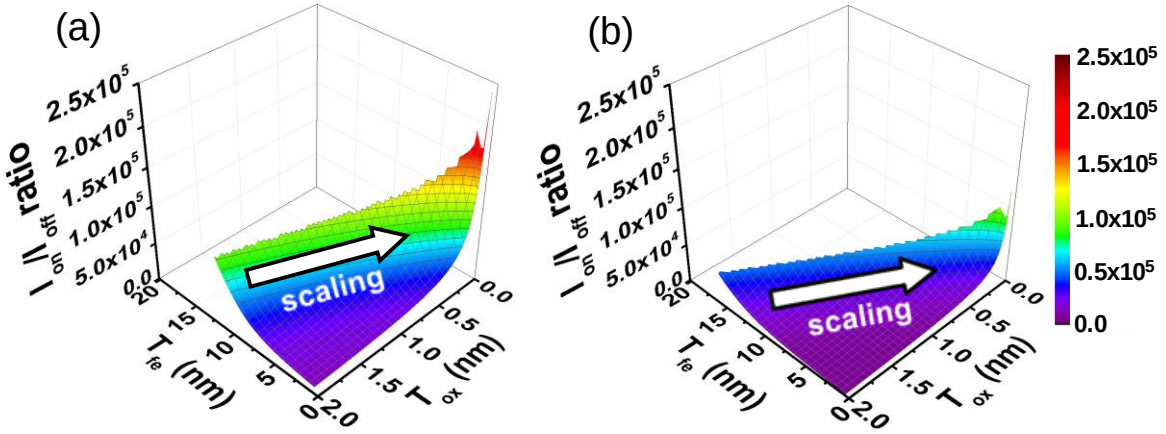


Fig. 2.19. Simulated contour plots of I_{on}/I_{off} ratio versus T_{fe} and T_{ox}=EOT where 2R and T_{si} are 5nm, and V_{dd}=0.5V. (a) is for NW-NCFET, and (b) is for DG-NCFET.

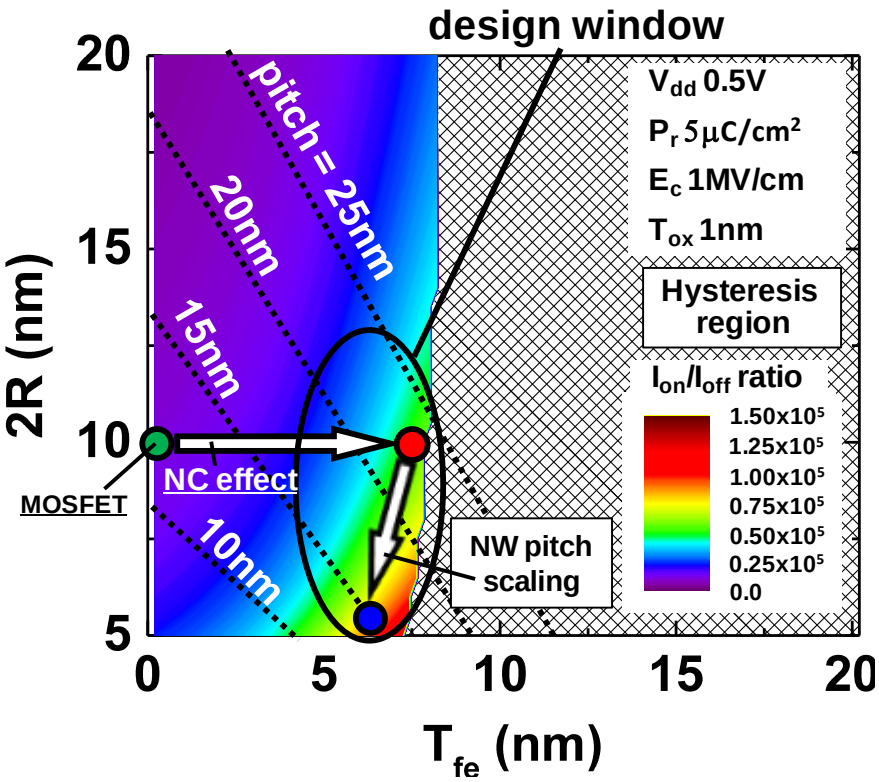


Fig. 2.20. Simulated contour plots of I_{on}/I_{off} ratio of NW-NCFET versus T_{fe} and 2R, where T_{ox}=EOT=1nm, and V_{dd}=0.5V.

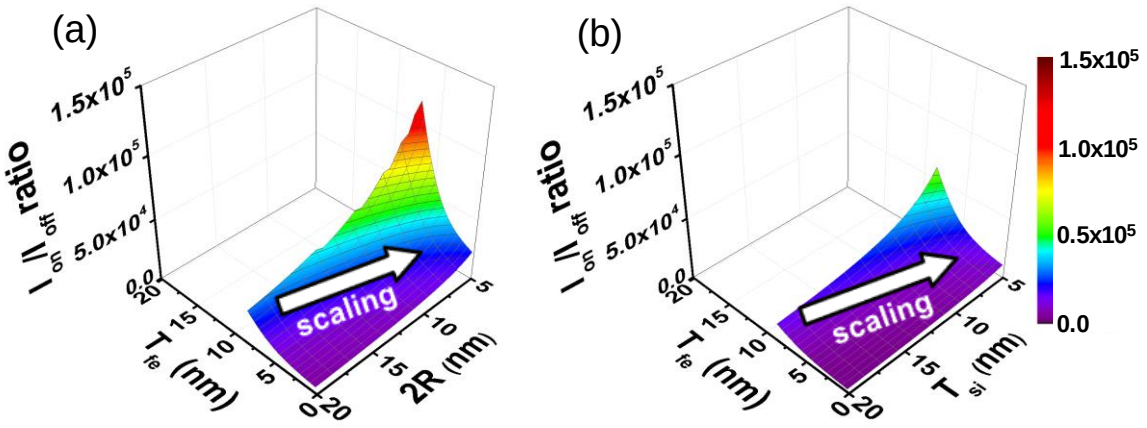


Fig. 2.21. Simulated contour plots of I_{on}/I_{off} ratio versus T_{fe} and channel size (2R or T_{si}) where T_{ox}=EOT=1nm, and V_{dd}=0.5V. (a) is for NW-NCFET, and (b) is for DG-NCFET.

Chapter 3

Simulation Study on Dynamic Characteristics of FE:$HfZrO_2$-based Negative-Capacitance FETs

3.1 Introduction

In previous chapters, base on the NC model proposed by S. Salahuddin [1], we showed device design guidelines of FE:HfO_2 NCFET by simulation. However, our discussion was limited to the static (DC) characteristics. Although FE:HfO_2-based NCFET has many merits to be a good candidate for ultralow power CMOS platform, what remains to be answered is how fast NCFET can operate. The operation speed could be limited by dynamics of polarization in ferroelectric. There have been some reports on the dynamic characteristics of NCFET [2,3]. However, in Refs. 2-3, $Pb(Zr_x, Ti_{1-x})O_3$ (PZT) was used as a FE material, which is not very compatible with CMOS process. Therefore, it can be said that dynamic characteristic and operation speed of FE:HfO_2-based NCFET is not studied sufficiently.

In this chapter, based on the experimental observation of NC phenomena in FE:$HfZrO_2$ capacitor [4], we simulated dynamic characteristics of FE:$HfZrO_2$ NCFET and discussed its operation speed.

NC effect has been experimentally observed from transient responses in FE capacitors by applying voltage pulses to a simple R-C series network with various FE materials: epitaxial PZT [5], epitaxial $BaTiO_3$ [6], polycrystalline doped-HfO_2 [7-8], and spin coated organic material of $P(VDF_{0.75}\text{-}TrFE_{0.25})$ [9]. Same approach was conducted on our fabricated FE:$HZrfO_2$ capacitor by N. Ueyama [4]. With an equivalent circuit model based on the Landau-Khalatnikov theory [10-11], simulation results showed NC response similar to

experimental results. From this LK theory-based simulation, we attempted to extract the material parameters of FE:$HfZrO_2$ capacitor. In this chapter, using the extracted ferroelectric parameters, analytic simulation which incorporates dynamic term of LK theory into the equations in Ref. 12 was conducted to investigate the dynamic characteristics of FE:$HfZrO_2$ NCFET and discussed its operation speed.

3.2 Fabrication and Measurements [4]

We fabricated metal-insulator-metal (MIM) capacitors of Zr-doped ferroelectric HfO_2 (FE:HZO) thin film with top and bottom electrodes of titanium nitride (TiN). Si substrate was cleaned by standard wet clean followed by deposition of bottom electrode by reactive sputtering. After breaking vacuum, 10-nm-thick HZO was deposited by atomic layer deposition (ALD). We chose 30%-Zr-doped HZO, because this composition had a wide process margin for ferroelectricity in our process. Then, top electrodes were deposited by reactive sputtering and shadow mask. The radius for top electrodes was 50μm diameter. Stacked MIM capacitors on Si substrate went through post-metallization-anneal in nitrogen ambient with a rapid thermal anneal process, in which HZO was crystallized. Annealing temperature was 500°C and anneal time was 90s.

To directly observe NC effect in FE:HZO, we measured transient (step) responses of R-C series network which consists of external resistor and FE:HZO capacitor. Fig. 3.1 shows an experimental setup of circuit diagram for transient analysis on R-C series network with FE:HZO capacitor, in which V_{in} and R represent the input voltage amplitude and external resistance, respectively. We applied a step voltage and monitored transient current (I-t characteristic). We calculated the charge (Q_{fe}) and voltage (V_{fe}) across FE:HZO capacitor from monitored I-t characteristic while parasitic components were carefully taken into

account.

3.3 Single Domain Model

For modeling the observed NC effect in FE:HZO capacitor, we developed a dynamic model for FE:HZO capacitor. As a dynamic model for FE capacitor, we used an equivalent circuit model based on the Landau-Khalatnikov (LK) theory [10-11] (LK model). The time evolution of polarization based on the LK theory is described as

$$\rho \frac{dP(t)}{dt} = E(t) - 2\alpha P(t) - 4\beta P^3(t) - 6\gamma P^5(t) \tag{3.1}$$

where, P is polarization, E is electric field across FE, t is time, α, β, and γ are parameters specifying the static characteristics of FE (LK static parameters), and ρ is parameter specifying the dynamic characteristics (LK dynamic parameter). ρ accounts for the resistance of the polarization to switching, therefore, ρ determines the finite time required for polarization switching to occur. Equation (3.1) is assuming uniform polarization, therefore, (3.1) can be applied to the FE capacitor with single ferroelectric domain structure. Based on (3.1), single domain (SD)-based FE capacitor can be modeled by series R-C network consist of an internal resistor (ρ) and a nonlinear capacitor (C_{fe}) characterized by the parameters of α, β, and γ [5,10,11]. This SD-based LK model (SD-LK model) was shown in dotted square line in Fig. 4.2.

3.4 Dynamic Model for Double-Gate NCFET

Parameters of ferroelectric were extracted by fitting simulation results to experimental data. For NCFET modeling, we have newly developed analytical compact model of dynamic

double-gate (DG) NCFET extended from static model in Ref. 12. To study the operation speed of FE:HZO NCFET, we incorporate the time-dependent term (ρ dQ/dt) of LK equation [11] into the boundary condition of equation 2 in Ref. 12, which results in below Eq. 3.2.

$$V_g - \Delta\varphi - V = a_o Q + b_o Q^3 + c_o Q^5 + \rho \frac{dQ}{dt} \tag{3.2}$$

Firstly, by substituting $Q = \varepsilon_s(2kT/q)(2\beta/t_s)\tan\beta$ into Eq. 3.2 [12], time evolution of $\beta_s(t)$ and $\beta_d(t)$ can be solved using Runge-Kutta method at a given V_g (t). Then, assume an MFMIS gate stack structure which has the internal metal plate between FE and interfacial insulator, we used the $\beta_s(t)$ (which corresponds to the charge density at source terminal, Q_s (t)) to calculate the voltage across MFM capacitor, V_{fe} (t). From this V_{fe} (t), by assuming MOSFET is sufficiently faster than polarization switching-limited MFM capacitor, we can obtain the voltage at internal metal plate, V_{mos} (t) which comes from $V_{mos}(t) = V_g(t) - V_{fe}(t)$. With this determined V_{mos} (t), drain current of baseline-MOSFET, I_d (t) can be calculated as conducted in chapter 2.

3.5 Ferroelectricity in $HfZrO_2$ [4]

In this chapter, we characterize electrical properties of fabricated HZO capacitor to confirm ferroelectricity [4]. Fig. 3.3(a) shows measured P-V characteristics of HZO capacitor with various measurement frequencies. Ferroelectric hysteresis characteristics were clearly observed. Remanent polarization (P_r) of 22 $\mu C/cm^2$ and coercive electric field (E_c) of 1 MV/cm were obtained which are consistent with other reports [13-14]. Fig. 3.3(b) shows measured I-V characteristics of the HZO capacitor in response to triangular pulse, in which polarization switching current was clearly distinguished from displacement current. Fig. 3.3(c)

shows measured C-V characteristic of the HZO capacitor with ac frequency of 1kHz. The voltage dependence of capacitance in Fig. 3.3(c) is induced by polarization switching in FE material [15]. Based on the obtained results in Figs. 3.3(a)-(c), we confirmed clear ferroelectricity in our fabricated HZO capacitors (FE:HZO).

3.6 Direct Observation of NC Phenomena [4]

In this chapter, to observe the NC directly, we measure the transient (step) responses of R-C series network with FE:HZO capacitors [4]. Figs. 3.4(a), (b) and (c) show experimental transient current (I-t), transient voltage (V_{fe}-t), and transient charge (Q_{fe}-t) across the FE:HZO capacitor, respectively. V_{in} was -4V → +4V and R was 20kΩ. Responses to positive to negative step voltages were not shown because they were symmetrical with negative to positive cases. The rising time (T_{rise}) of input step voltage was around 3μs. V_{fe}-t characteristic (Fig. 3.4(b)) and Q_{fe}-t characteristic (Fig. 3.4(c)) were calculated from measured I-t characteristic (Fig. 3.4(a)). The parasitic capacitances in the measurement setup were very small, and thus have negligible impacts on the calculated Q_{fe} and V_{fe}. By coupling V_{fe}-t characteristic (Fig. 3.4(b)) and Q_{fe}-t characteristic (Fig. 3.4(c)), Q_{fe}-V_{fe} characteristic was obtained and shown in Fig. 3.4(d).

Transient current (I-t) characteristic (Fig. 3.4(a)) shows the components of displacement current and polarization switching current which confirms ferroelectricity in MIM capacitor. In Figs. 3.4(b) and (c), time period (A-B) in which as voltage increases, charge decreases ($dQ_{fe}/dV_{fe} < 0$) was observed. This is corresponding to the direct observation of negative differential capacitance (referred as NC effect here) in a transient method [5-9]. The region of negative slope in Q_{fe}-V_{fe} characteristic ($dQ_{fe}/dV_{fe} < 0$) (Fig. 4.4(d)) is corresponding to the NC effect directly observed in Ref. 4.

3.7 Analysis of MFM Capacitor and Parameter Extraction

So far, NC was directly observed in FE:HZO capacitor. In this section, we use the SD-LK model to extract LK parameters by fitting simulation results to the experimental results.

Based on SD-LK model (Fig. 3.2(a)), LK static parameters of α, β, and γ were extracted by fitting the simulated P-V characteristic to the measured P-V characteristic as shown in Fig. 3.5. $\alpha=-4.8\times10^{10}$ Vcm/C, $\beta=5.0\times10^{19}$ Vcm^5/C^3, and $\gamma=0$ Vcm^9/C^5 were extracted. Then, SD-LK model-based simulations for the transient response were conducted to extract LK dynamic parameter of ρ.

Now, to extract ρ, circuit simulation was run varying ρ values for fitting. Fig. 3.6 compares measured and simulated I-t curves. Although entire polarization switching current does not match perfectly, transient characteristics related to negative capacitance before polarization switching was well reproduced by simulation. Here ρ was estimated to be 10^3~10^4 Ωcm. To further scrutinize the value of ρ, frequency dependence of P-V curve was also compared to simulated P-V curves, as coercive field (E_c) has frequency dispersion. Fig. 3.7 shows the comparison of relative frequency dependence of E_c of FE capacitor between measurement and simulation. In this work, a value of $\rho=3\text{x}10^3$ Ωcm was extracted as a dynamic LK parameter for FE:HZO.

3.8 Dynamic Characteristics of FE:$HfZrO_2$-based NCFET and Operation Speed

Using the extracted LK parameters above, polarization-limited operation speed of FE:$HfZrO_2$ DG-NCFET was investigated by our newly developed DG-NCFET model based

on Ref. 12. To investigate the operation speed, frequency response of the drain current (I_d) was simulated with 5nm fin thickness by sweeping gate voltage forward and backward and shown in Fig. 3.8. Extracted parameters from our ferroelectric HZO result in ~1MHz frequency operation without too large hysteresis, while maintaining 2x higher on-current than conventional MOSFET. We also simulated by varying ρ values in Fig. 3.9 and found that lower ρ certainly helps to improve operation speed of FE:$HfZrO_2$ NCFET with smaller hysteresis. MHz operation speed is sufficient for IoT applications, therefore, FE:$HfZrO_2$ NCFET can be a good candidate for new low power CMOS platform.

3.9 Summary

In this works, LK theory was used as a time-dependent NC model [1], where FE works as a voltage amplifier. Based on the fabricated and characterized ferroelectric $HfZrO_2$ capacitors [4], FE parameters of LK equation were extracted from P-V, transient I-t and V-t, and frequency dependence of P-V characteristics. Using the extracted parameters and newly developed DGNCFET model, it was revealed that FE:$HfZrO_2$ NCFET can operate at MHz range, which is promising result for ultralow power IoT applications. For faster operation without hysteresis, material engineering on the parameter in dynamic term of $HfZrO_2$, ρ, can be critical.

References

[1] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices”, Nano Lett., Vol. 8, No. 2, p. 405.

[2] Y. Li, K. Yao, and G. S. Samudra, “Effect of Ferroelectric Damping on Dynamic Characteristics of Negative Capacitance Ferroelectric MOSFET”, IEEE Trans. Electron Devices, vol. 63, no. 9, pp. 3636-3641, 2016.

[3] Z. C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T. B. Hook, D. Kienle, S. Gadelrab, P. S. Gudem, and M. Vaidyanathan, “Switching-Speed Limitations of Ferroelectric

Negative-Capacitance FETs", IEEE Trans. Electron Devices, vol. 63, no. 10, pp. 4046-4052, 2016.

[4] N. Ueyama, Master's thesis, The Univ. of Tokyo (2017).

[5] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, "Negative capacitance in a ferroelectric capacitor", Nature Materials, vol. 14, pp. 182-186, 2015.

[6] S. J. Song, Y. J. Kim, M. H. Park, Y. H. Lee, H. J. Kim, T. Moon, K. D. Kim, J.-H. Choi, Z. Chen, A. Jiang, and C. S. Hwang, "Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors", Scientific Reports, vol. 6, 20825, 2016.

[7] M. Hoffmann, M. Pešić, K. Chatterjee, A. I. Khan, S. Salahuddin, S. Slesazeck, U. Schoeder, and T. Mikolajick, "Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2", Adv. Funct. Mater. vol. 26, pp. 8643-8649, 2016.

[8] P. Sharma, J. Zhang, A. K. Saha, S. Gupta, and S. Datta, "Negative Capacitance Transients in Metal-Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-Insulator-Semiconductor (MFIS) Capacitors", in Device Research Conference, 2017.

[9] H. Ku and C. Shin, "Transient Response of Negative Capacitance in P($VDF_{0.75}$-$TrFE_{0.25}$) Organic Ferroelectric Capacitor", Journal of the Electron Devices Society, vol. 5, no. 3, pp. 232-236, 2017.

[10] D. Ricinschi, C. Harnagea, C. Papusoi, L. Mitoseriu, V. Tura, and M. Okuyama, "Analysis of ferroelectric switching in finite media as a Landau-type phase transition", Journal of Physics: Condensed Matter, vol. 10, no. 2, pp. 477-492, 1998.

[11] S. Sivasubramanian, A. Widom, and Y. Srivastava, "Equivalent Circuit and Simulations for the Landau-Khalatnikov Model of Ferroelectric Hysteresis", IEEE Trans. Ultrasonics, Ferroelectrics and Frequency control, vol. 50, no. 8, pp. 950-957, 2003.

[12] D. Jimenez, E. Miranda, and A. Godby, "Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors", IEEE Trans. Electron Devices, Vol. 57, No. 10, p. 2405 (2010).

[13] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwang, "Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature", Appl. Phys. Lett., Vol. 102, p.242905 (2013).

[14] T. Shimizu, T. Yokouchi, T. Oikawa, T. Shiraishi, T. Kiguchi, A. Akama, T. J. Kohno, A. Gruverman, and H. Funakubo, "Contribution of oxygen vacancies to the ferroelectric behavior of $Hf_{0.5}Zr_{0.5}O_2$ thin films", Appl. Phys. Lett., Vol. 106, p.112904 (2015).

[15] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films", Applied Physics Letters, vol. 99, no. 10, 102903, 2011.

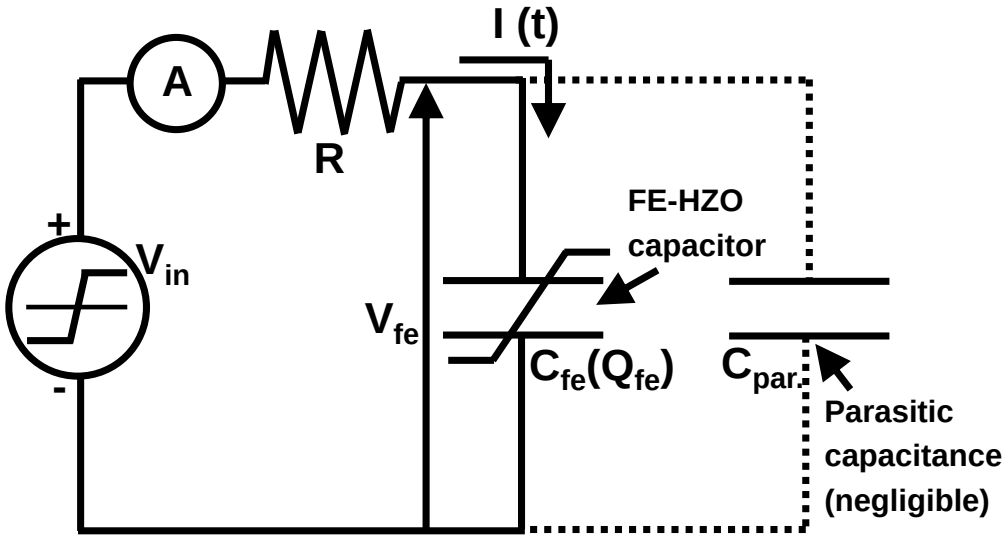


Fig. 3.1. A circuit diagram for transient analysis of FE:HZO capacitor.

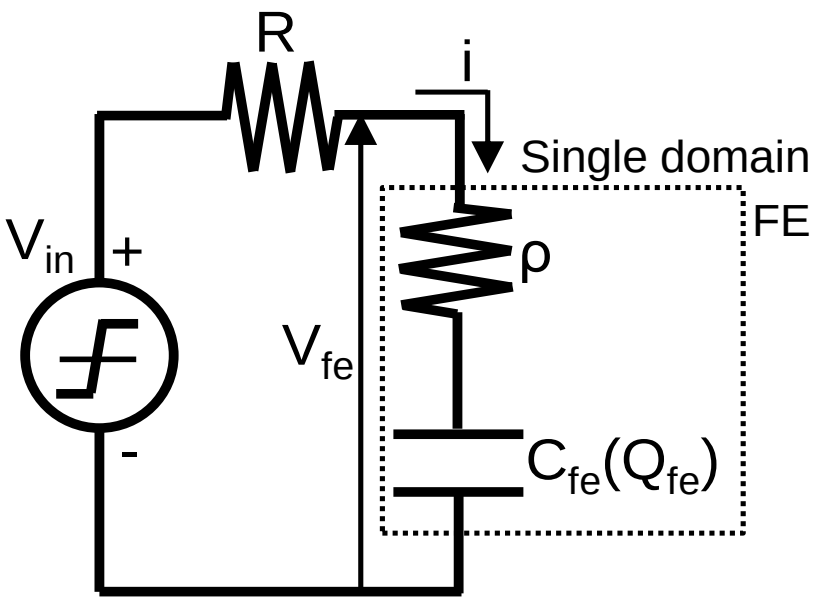


Fig. 3.2. A schematic of the simulated circuit which were used to analyze the experimental results in FE:HZO. SD-LK model-based simulation is modeled by ρ-C_{fe} series component.

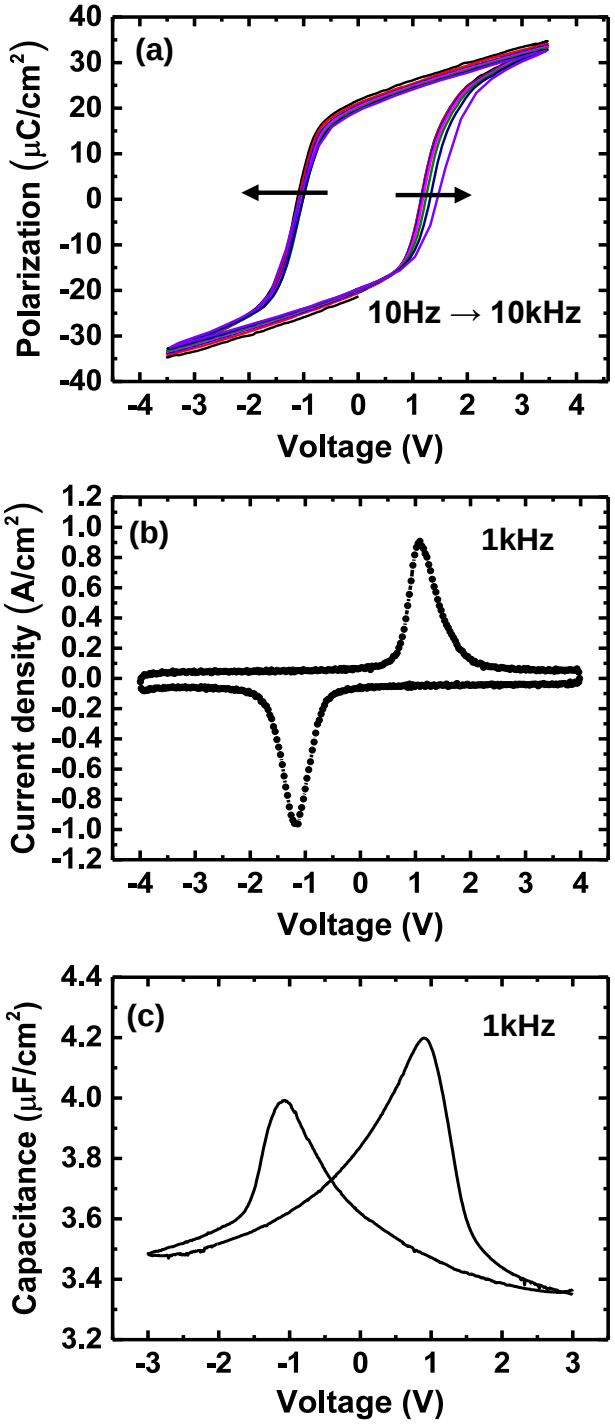


Fig. 3.3. Measurement results for FE:HZO capacitors [4]. (a) P-V characteristics at frequencies of 10Hz to 10kHz. (b) I-V characteristic in response to triangular pulse. (c) C-V characteristics with ac frequency of 1kHz.

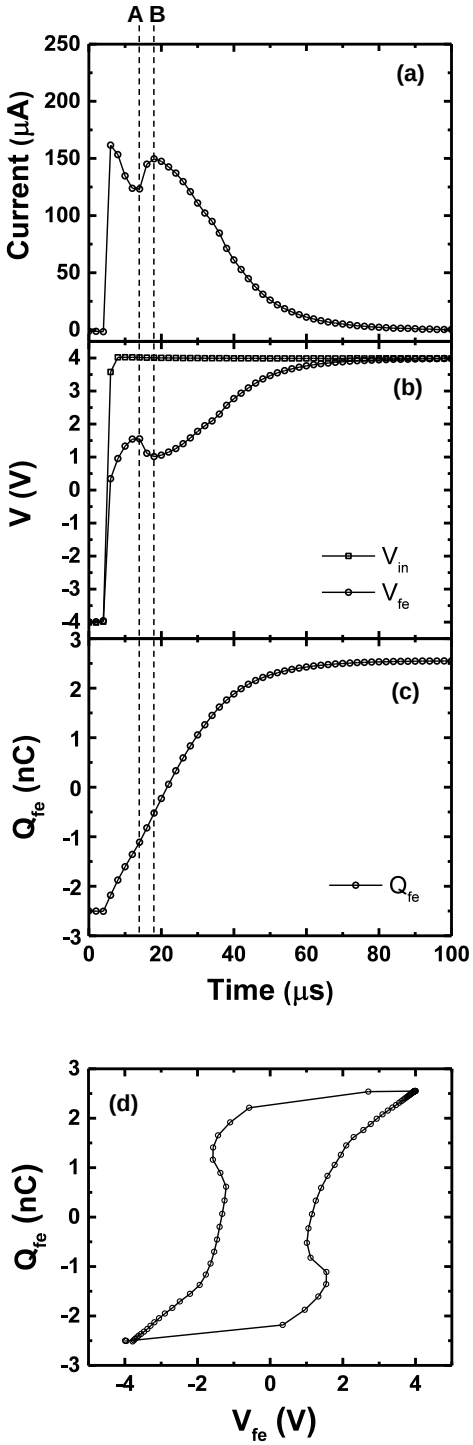


Fig. 3.4. Measured transient characteristics of FE:HZO. Pulse voltage was input from negative to positive [4]. Experimental conditions were V_{in}=-4V → +4V and R=20kΩ. (a) I-t characteristic. (b) V-t characteristics. (c) Q-t characteristic. (d) Q_{fe}-V_{fe} characteristic.

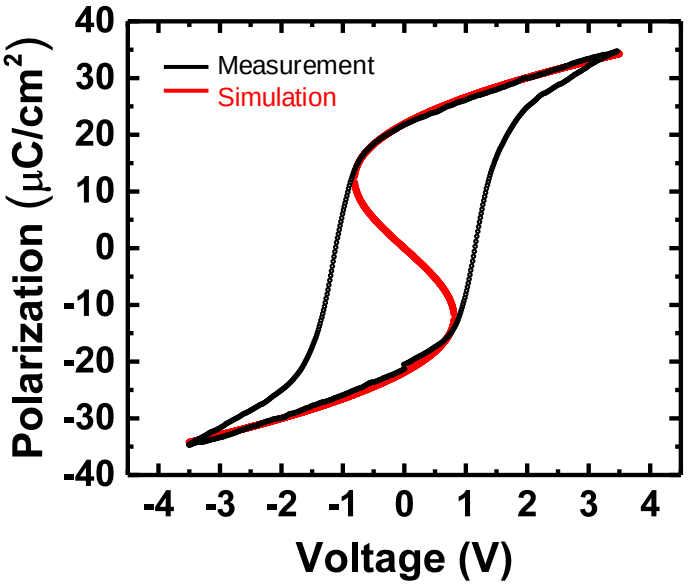


Fig. 3.5. Measured P-V characteristic and fitted simulation result for LK static parameters extraction.

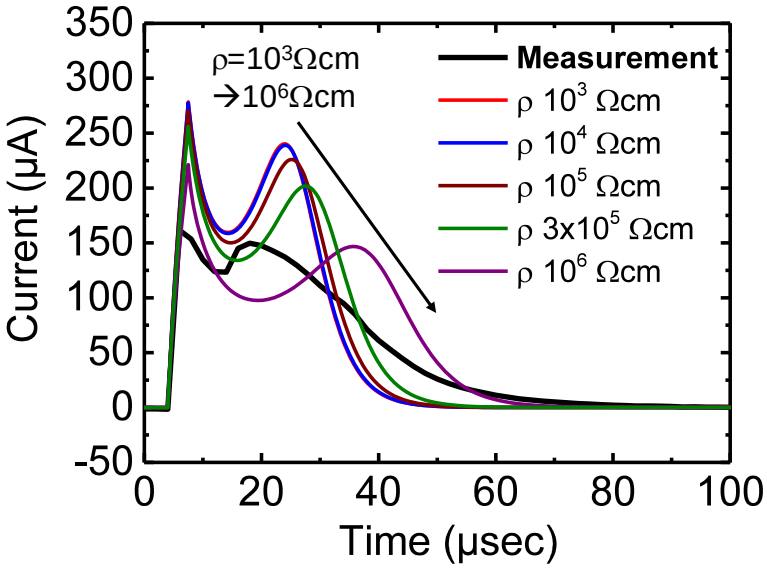


Fig. 3.6. Comparison of measured and simulated I-t characteristics varying ρ value.

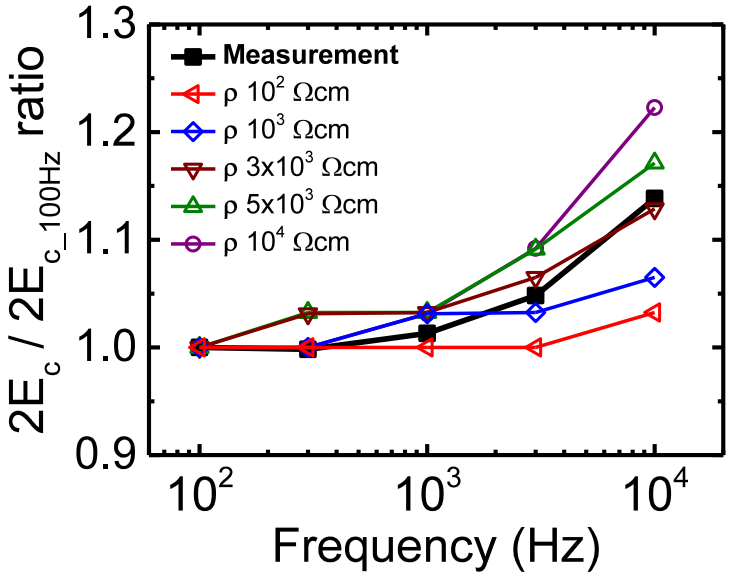


Fig. 3.7. Comparison of measured and simulated I-t characteristics varying ρ value.

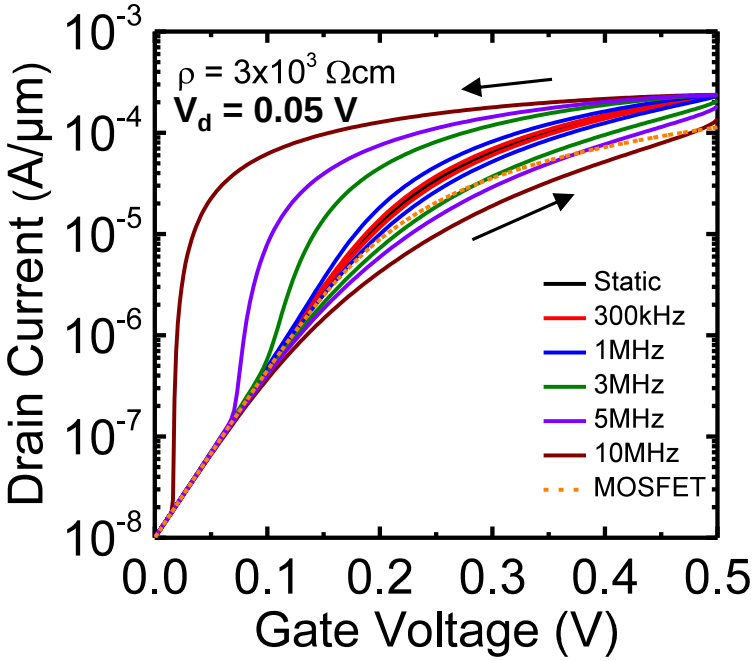


Fig. 3.8. Simulated I_d-V_g characteristics of DG-NCFET by sweeping gate voltage forward and backward at various frequencies. As a value for the dynamic LK parameter, the extracted ρ value of $3x10^3$ Ωcm was used.

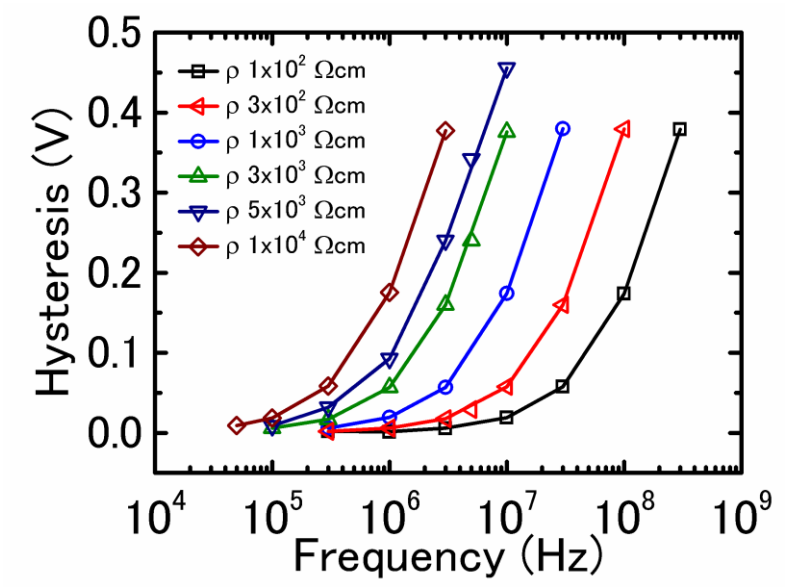


Fig. 3.9. Simulated hysteresis of I_d of DG-NCFET with the extracted ρ and speculated ρ.

Chapter 4

Multi-Domain Model for Negative-Capacitance Phenomena in FE:$HfZrO_2$ capacitor

4.1 Introduction

In chapter 3, the device modeling using extracted parameters from the experimental NC phenomena in FE:$HfZrO_2$ (HZO) capacitor was mainly investigated [1]. Even though simulation results with an equivalent circuit model based on the Landau-Khalatnikov theory can show NC response similar to experimental results, however, single domain model (SD-LK model) were not able to fit the experimental results with high accuracy [1,2].

In this chapter, to develop and validate a new FE model with high accuracy, LK theory-based multi-domain model (MD-LK model) [3] has been applied to the experimental data in chapter 3. There is a previous study on MD-LK model with PZT [4]. In Ref. 4, even if the calibrated MD-LK model was able to fit the experimental NC effect in PZT [2], however, only single input voltage amplitude was demonstrated. Additionally, in previous study on MD-LK model with doped FE:HfO_2 capacitor [5], fitting accuracy of MD-LK model to experimental transient NC effect was not satisfactory, as well as only a single input voltage amplitude was demonstrated. Therefore, it can be said that experimental validation of the compact model as a dynamic FE capacitors (especially FE:HZO) remains unstudied yet. From the viewpoint of developing a reliable (useful) simulation model, developing valid model that can describe the dynamic characteristics of FE:HZO capacitors is crucial for designing the FE:HZO-based NCFET and circuit based on it [4,6-8]. In this chapter, based on the NC effect experimentally observed as illustrated in chapter 3, a compact model for FE:HZO was

validated by applying MD-LK model to experimental NC effect with various experimental conditions.

4.2 Multi-Domain Interaction Model

To capture the MD effect with non-uniform polarization and domain interaction, Eq. 3.1 in chapter 3.3 has to be modified. Assume one-dimensional domain distribution, the time-evolution of polarization in *i*-th domain is described as Eq. 4.1.

$$\rho_i \frac{dP_i(t)}{dt} = E(t) - 2\alpha_i P_i(t) - 4\beta_i P_i^3(t) - 6\gamma_i P_i^5(t) - k\left[\left(P_i(t) - P_{i+1}(t)\right) - \left(P_{i-1}(t) - P_i(t)\right)\right] \quad (4.1)$$

where, P_i is polarization for *i*-th domain, and α_i, β_i, γ_i, and ρ_i are LK parameters for *i*-th domain. *k* is the linear domain interaction parameter that describes the coupling strength between the nearest neighboring domains. Detailed descriptions on the LK theory-based MD model (MD-LK model) can be found in Ref. 3. Based on Eq. 4.1, FE capacitor with MD structure can be modeled by parallel ρ-C_{fe} series components as shown in dotted square line in Fig. 4.1(b). In Fig. 4.1(b), each FE domain corresponds to each series ρ-C_{fe} component. As a linear domain interaction between nearest neighboring domains, the *k*-included fifth term in RHS of Eq. 4.1 was incorporated into the MD-LK model using Verilog-A. As a reference, an equivalent circuit based on SD-LK model which already shown in Fig. 3.2 was repeated in Fig. 4.1(a).

By using these models, we simulated the step responses in R-C networks with FE:HZO capacitors. For model calibration, by adjusting LK parameters, we attempted to fit the simulation results to the experimental results with a default condition of input voltage

amplitude (V_{in}) and external resistor (R). Then, for model validation, we applied the model to the various V_{in} and R, different with a default condition.

4.3 Poor Accuracy with SD-LK Model

Fig. 4.2 shows the SD-LK model-based simulation results for I-t transient characteristics with varied ρ. Even varying ρ in a wide range, SD-LK model-based simulations were not able to fit to the experimental results with high accuracy [1-2]. This discrepancy between the SD-LK model-based simulations and the experiments, consistent with other reports [2,4], is considered to originate in the physical discrepancy between the SD-LK model and the nature of the polycrystalline (multi-domain) FE:HZO thin film [5]. To overcome this discrepancy, we focused on the MD-LK model hereafter [3].

4.4 Model Verification

As a step for model verification, we used MD-LK model with two domains (N=2). This step can help us to understand how the MD-LK model works. Two domains were assumed to have the same LK static parameters (α, β, and γ), but different dynamic parameter (ρ_i); $\rho_1=1\times10^4$ Ωcm and $\rho_2=1\times10^6$ Ωcm. Each domain was assumed to occupy the same area. Fig. 4.3 shows simulated I-t characteristics of MD-LK model of N=2 where domain interaction was neglected; k=0 Vcm/C. The MD-LK model of N=2 has two peaks in its I-t characteristic which are correspond to ρ_1 and ρ_2, respectively. For comparison, I-t characteristics of two separated SD-LK models with the $\rho=\rho_1$ or $\rho=\rho_2$ were also plotted in Fig. 4.3. Fig. 4.4 shows the impacts of increasing domain interaction parameter (k) on the simulated I-t characteristics. With increased *k*, two peaks became closer and finally merged to a peak owing to strong domain interaction effect. Due to the strong interaction between two domains, polarization

switching cannot occur separately anymore.

4.5 Model Calibration

So far, the MD-LK model was verified with simple simulation. In this chapter, we calibrate the LK model by fitting simulation results to the experimental results.

We assumed following assumptions on the model: (1) The film consists of columnar domains which is in accordance with TEM image in [5], and domains are distributed in a one-dimension. (2) The number of domains (N) is five or ten (N=5 or N=10) for simplicity, and each domain has the same area. (3) Each domain has a same LK static parameters (α, β, and γ), however, different dynamic parameter (ρ_i) which results in ρ_i distribution among MD array. (4) Domain interaction exists ($k > 0$), and value of k among whole MD array is the same.

Firstly, based on the above assumption (3), LK static parameters of α, β, and γ were extracted by fitting the simulated P-V characteristic to the measured P-V characteristic as shown in Fig. 3.5. As described in chapter 3.7, α=-4.8×10^{10} Vcm/C, β=5.0×10^{19} Vcm^5/C^3, and γ=0 Vcm^9/C^5 were extracted. Then, for model calibration, ρ_i distribution among MD array and interaction parameter of k were adjusted to fit the simulation results to the experimental results under a default condition of V_{in}=-4V → +4V and R=20kΩ. Fig. 4.5(a) shows MD-LK model-based simulated I-t characteristics and experimental result. From I-t characteristic in Fig. 4.5(a), V_{fe}-t, Q_{fe}-t, and Q_{fe}-V_{fe} characteristics were calculated and shown in Fig. 4.5(b), (c), and (d), respectively. Please note that all solid lines in Fig. 4.5 are simulation results, not as the Fig. 3.4 where only measured results were shown. Figs. 4.5(a)-(d) show that calibrated MD-LK model offers accurate fitting compared to SD-LK model. Adjusted ρ_i values were distributed from 3.0×10^4 Ωcm to 3.0×10^6 Ωcm, and the

average (μ) and standard deviation (σ) were 7.6×10^5 Ωcm and 8.5×10^5 Ωcm, respectively. Value of k was adjusted to be 2.0×10^{11} Vcm/C.

4.6 Model Validation

In this chapter, the MD-LK model was applied to the different V_{in}, and then, different R with a default condition for model validation. Firstly, we applied the MD-LK model to the experimental condition of V_{in} lower than -4V → +4V. LK static parameters (α, β, and γ) for each V_{in} were extracted from the measured P-V characteristics with each V_{in}. The number of domains was set to ten (N=10). Figs. 4.6(a) and (b) show experimental and simulation results for I-t and Q_{fe}-V_{fe} characteristics, respectively, in which V_{in} was varied and R was fixed to 20kΩ. MD-LK model can reproduce experimental results with high accuracy even for V_{in} different from default. However, to reproduce the experimental results for different V_{in}, ρ_i distribution needed slight modifications for each V_{in}. Value of ρ_i was larger for lower V_{in}, which is consistent with the report by A. I. Khan *et al.* (see Supplementary Information in Ref. 2). For V_{in}=-3V → +3V, the μ and σ in ρ_i distribution were 8.8×10^5 Ωcm and 8.3×10^5 Ωcm, respectively. For V_{in}=-2V → +2V, the μ and σ in ρ_i distribution were 1.2×10^6 Ωcm and 1.1×10^6 Ωcm, respectively.

Then, we applied the MD-LK model to the experimental condition of external resistance larger than 20kΩ. Figs. 4.7(a) and (b) show experimental and simulation results for I-t and Q_{fe}-V_{fe} characteristics, respectively, in which R was varied and V_{in} was fixed to -4V → +4V. The number of domains was set to ten (N=10). Similarly to the case of various V_{in}, Figs. 4.7(a) and (b) show that MD-LK model can reproduce experimental results with high accuracy even R different from default. However, to reproduce the experimental results for different R, ρ_i distribution needed slight modifications for each R. Value of ρ_i was smaller for

smaller R. For R=33kΩ, the μ and σ in ρ_i distribution were 1.2×10^6 Ωcm and 1.2×10^6 Ωcm, respectively. For R=51kΩ, the μ and σ in ρ_i distribution were 1.8×10^6 Ωcm and 1.9×10^6 Ωcm, respectively. Fitting parameters for an each condition were summarized in Table. 1.

4.7 Discussions

As described previous chapters, higher V_{in} and smaller R gave rise to smaller ρ_i distribution. These V_{in} and R dependences of ρ_i distribution provided an evidence that LK dynamic parameter (ρ_i) in FE:HZO is not constant but depends on bias condition. There exists a possibility that, in the case of the MD-interacting switching process, a higher V_{in} and/or smaller R can result in more domains to switch at the onset [2]. This increase in the number of fast switching domains can contribute to the smaller ρ_i value. From the viewpoint of modeling, on the other hand, because the LK theory is a phenomenological approach, LK model natively has to be calibrated to an each experimental condition with carefulness to assure the high accuracy. Even though slight modifications on the ρ_i distribution were needed for accurate fitting, it is believed that the validation of MD-LK model is still effective, because modifications on ρ_i values were not far from first calibrated values.

In this work, MD-LK model which was implemented in Verilog-A code and circuit simulator reproduced the experimentally observed NC characteristics in FE:HZO with high accuracy. Of particular note is that MD-LK model can reproduce experimental results well with various input voltage amplitudes as well as various external resistances. Reliable simulation model should give a high accuracy for various input voltages and various external components. Therefore, our approach and obtained results are considered to be valuable for validation of MD-LK model which have never been demonstrated in other reports [2,5,9-11].

From the experiments and model-based analysis, MD-LK model was successfully

validated as a dynamic model for FE:HZO capacitor. Because MD-LK model can be implemented in device or circuit simulations, MD-LK model will be a useful dynamic model for FE:HZO-based devices such as multi-domain NCFET with various experimental conditions. However, we consider that further investigations on the physical validity in our MD-LK model will be necessary from the viewpoint of switching physics in FE:HZO thin film.

4.8 Summary

In this work, we proposed and developed MD-LK model as a compact model for dynamic FE:HZO [12]. With the MD-LK model, fitting accuracy was drastically improved comparing to SD-LK model. MD-LK model successfully reproduced the experimental NC effect in FE:HZO with various input voltage amplitudes and external resistances. MD-LK model was successfully validated as a dynamic model for FE:HZO capacitor. MD-LK model is expected as a useful simulation model for dynamic NCFET with multi-domain FE:HZO [7-8,13].

References

[1] M. Kobayashi, N. Ueyama, K. Jang, and T. Hiramoto, “Experimental Study on Polarization-Limited Operation Speed of Negative Capacitance FET with Ferroelectric HfO_2”, in IEDM Tech. Dig., San Francisco, CA, USA, 2016, pp. 314-317.

[2] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, “Negative capacitance in a ferroelectric capacitor”, Nature Materials, vol. 14, pp. 182-186, 2015.

[3] D. Ricinschi, C. Harnagea, C. Papusoi, L. Mitoseriu, V. Tura, and M. Okuyama, “Analysis of ferroelectric switching in finite media as a Landau-type phase transition”, Journal of Physics: Condensed Matter, vol. 10, no. 2, pp. 477-492, 1998.

[4] Z. C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T. B. Hook, D. Kienle, S. Gadelrab, P. S. Gudem, and M. Vaidyanathan, “Switching-Speed Limitations of

Ferroelectric Negative-Capacitance FETs", IEEE Trans. Electron Devices, vol. 63, no. 10, pp. 4046-4052, 2016.

[5] M. Hoffmann, M. Pešić, K. Chatterjee, A. I. Khan, S. Salahuddin, S. Slesazeck, U. Schoeder, and T. Mikolajick, "Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2", Adv. Funct. Mater. vol. 26, pp. 8643-8649, 2016.

[6] Y. Li, K. Yao, and G. S. Samudra, "Effect of Ferroelectric Damping on Dynamic Characteristics of Negative Capacitance Ferroelectric MOSFET", IEEE Trans. Electron Devices, vol. 63, no. 9, pp. 3636-3641, 2016.

[7] Z. Zhu, H. Zhu, S. Wang, Y. Liu, X. Yin, K. Jia, and C. Zhao, "Negative-Capacitance Characteristics in a Steady-State Ferroelectric Capacitor Made of Parallel Domains", IEEE Electron Device Letters, vol. 38, no. 8, pp. 1176-1179, 2017.

[8] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schoeder, and T. Mikolajick, "Modeling and Design Considerations for Negative Capacitance Field-Effect Transistors", in Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, 2017, pp. 1-4.

[9] S. J. Song, Y. J. Kim, M. H. Park, Y. H. Lee, H. J. Kim, T. Moon, K. D. Kim, J.-H. Choi, Z. Chen, A. Jiang, and C. S. Hwang, "Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors", Scientific Reports, vol. 6, 20825, 2016.

[10] P. Sharma, J. Zhang, A. K. Saha, S. Gupta, and S. Datta, "Negative Capacitance Transients in Metal-Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-Insulator-Semiconductor (MFIS) Capacitors", in Device Research Conference, 2017.

[11] H. Ku and C. Shin, "Transient Response of Negative Capacitance in $P(VDF_{0.75}$-$TrFE_{0.25})$ Organic Ferroelectric Capacitor", Journal of the Electron Devices Society, vol. 5, no. 3, pp. 232-236, 2017.

[12] K. Jang, N. Ueyama, M. Kobayashi, and T. Hiramoto, "Experimental Observation and Simulation Model for Transient Characteristics of Negative-capacitance in Ferroelectric $HfZrO_2$ Capacitor", IEEE Journal of the Electron Devices Society, submitted.

[13] A. Saha, P. Sharma, I. Dabo, S. Datta and S. Gupta, "Ferroelectric Transistor Model based on Self-Consistent Solution of 2D Poisson's, Non-Equilibrium Green's Function and Multi-Domain Landau Khalatnikov Equations", in IEDM Tech. Dig., San Francisco, CA, USA, 2017, pp. 326-329.

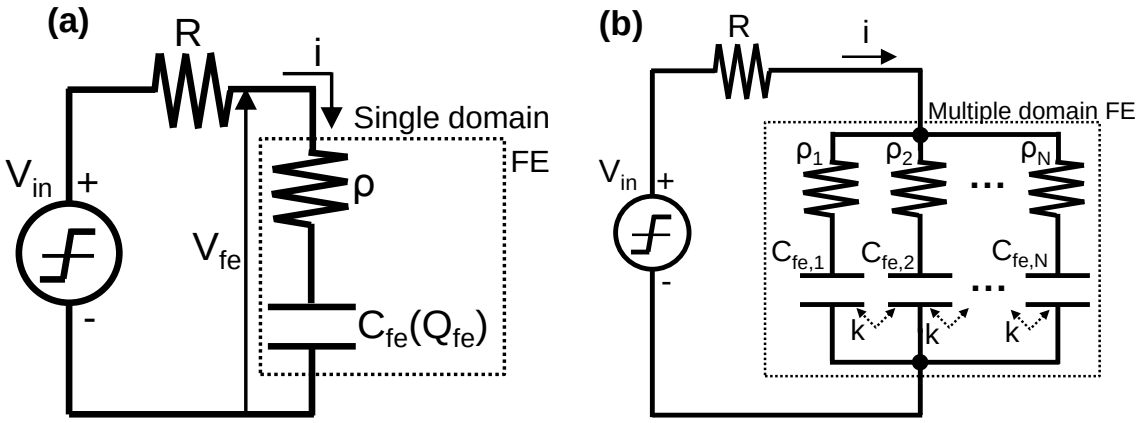


Fig. 4.1. Schematics of the simulated circuit which were used to analyze and reproduce the experimental results in FE:HZO. (a) SD model-based equivalent circuit. (b) MD model-based equivalent circuit where MD effect is expressed by parallel ρ_i-$C_{fe,i}$ series components with linear interaction factor (k).

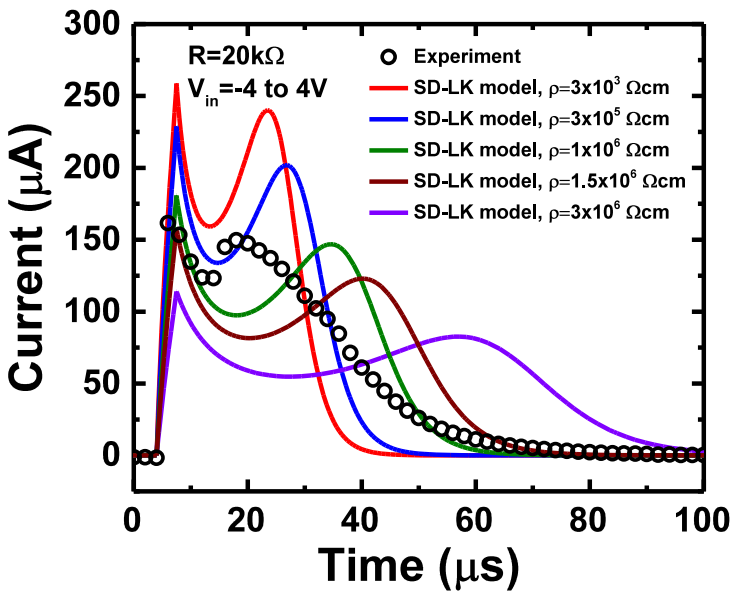


Fig. 4.2. Experimental I-t transient characteristic and SD-LK model-based simulation results with ρ varied. SD-LK model-based simulation cannot fit the experimental result with high accuracy.

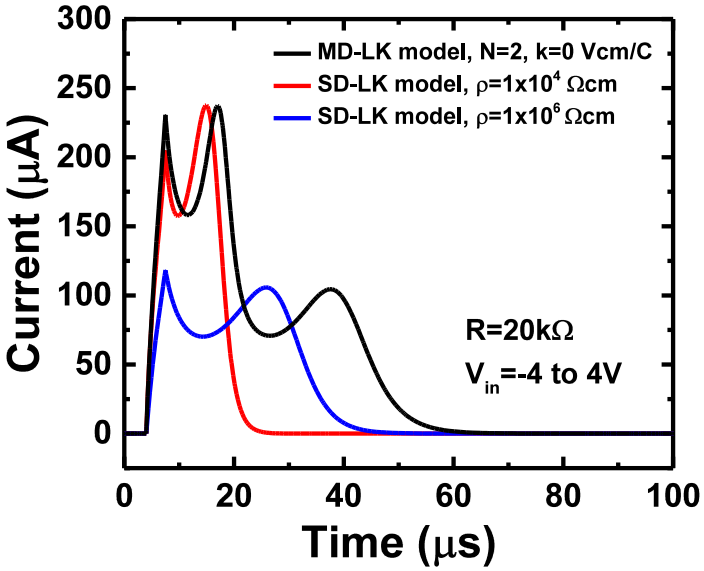


Fig. 4.3. Simulated I-t characteristics of MD-LK model with two domains (N=2) when domain interaction factor k is zero. Two domains have different ρ; ρ_1=1x10^4 Ωcm and ρ_2=1x10^6 Ωcm. For comparison, simulated I-t characteristics of two separated SD whose ρ=ρ_1 and ρ=ρ_2 are also shown.

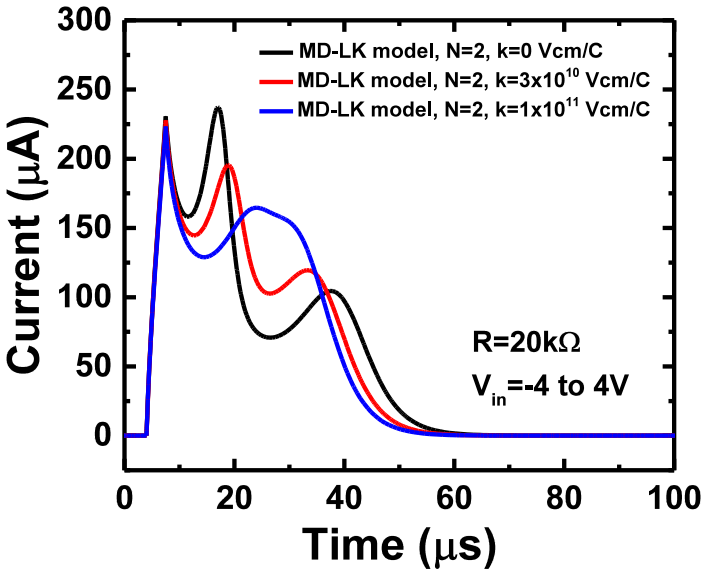


Fig. 4.4. Simulated I-t characteristics of MD-LK model with two domains (N=2) when domain interaction factor k is increased. With a larger value of k, two separated switching peaks become closer and finally merge to a peak.

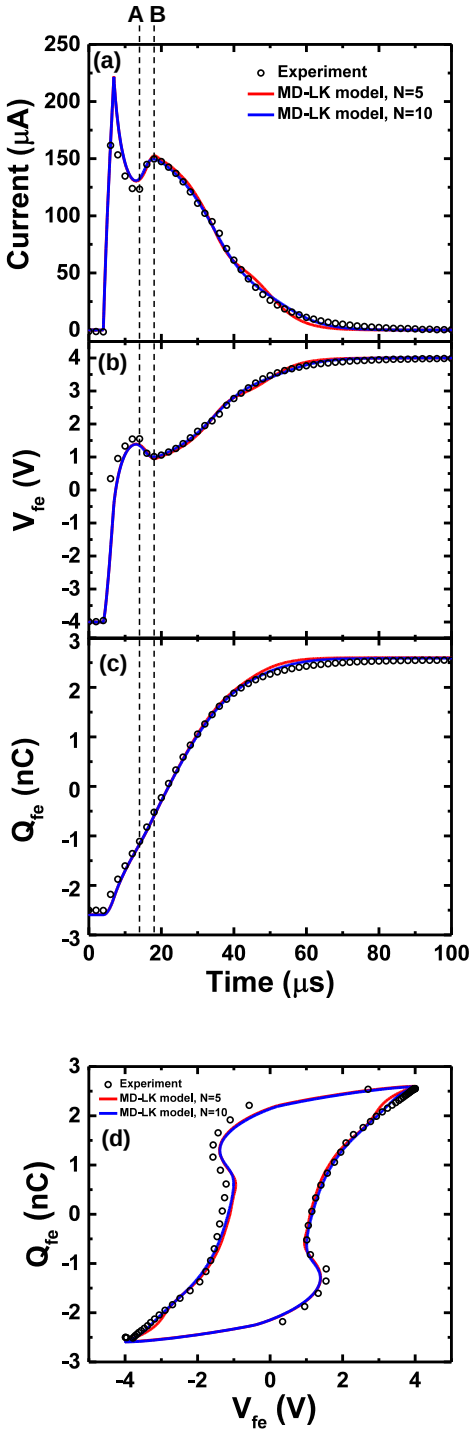


Fig. 4.5. Simulated and experimental transient characteristics with MD-LK model. (a) I-t characteristics. (b) V_{fe}-t characteristics. (c) Q_{fe}-t characteristics. (d) Q_{fe}-V_{fe} characteristics. V_{in} and R were default conditions of V_{in}=-4V → +4V and R=20kΩ. N=5 or N=10 was assumed.

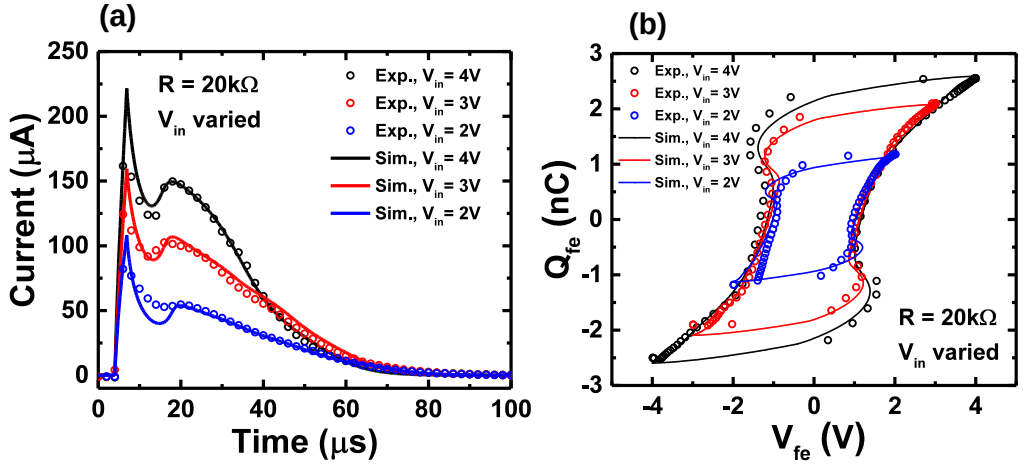


Fig. 4.6. Simulated and experimental transient characteristics with MD-LK model. (a) I-t characteristics. (b) Q_{fe}-V_{fe} characteristics. V_{in} was varied and R was fixed to 20kΩ. N=10 was assumed.

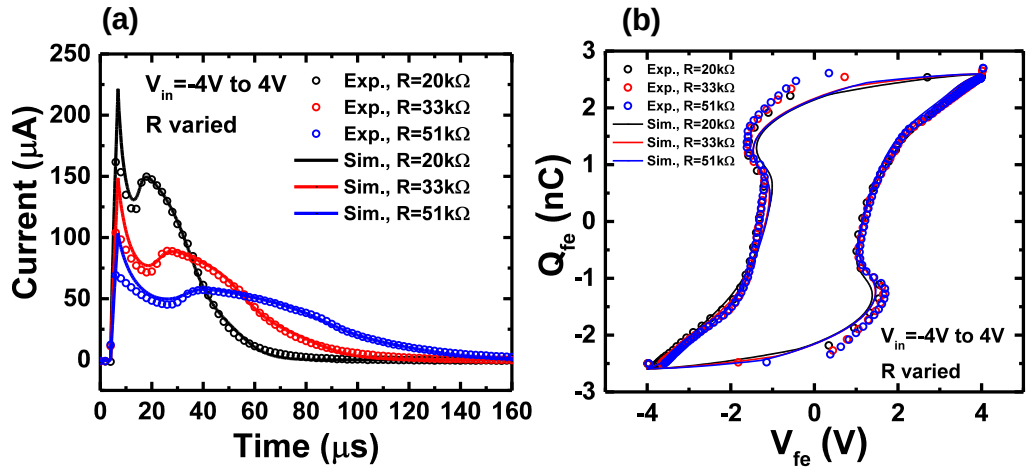


Fig. 4.7. Simulated and experimental transient characteristics with MD-LK model. (a) I-t characteristics. (b) Q_{fe}-V_{fe} characteristics. R was varied and V_{in} was fixed to -4V → +4V. N=10 was assumed.

TABLE I

EXPERIMENTAL CONDITIONS AND FITTING PARAMETERS (N=10)

V_{in} (V)	R (kΩ)	α (Vcm/C)	β (Vcm^5/C^3)	γ (Vcm^9/C^5)	ρ_i (μ) (Ωcm)	ρ_i (σ) (Ωcm)	k (Vcm/C)
-4 → +4	20	-4.8×10^{10}	5.0×10^{19}	0	7.6×10^{5}	8.5×10^{5}	2.0×10^{11}
-3 → +3	20	-5.6×10^{10}	8.1×10^{19}	0	8.8×10^{5}	8.3×10^{5}	2.0×10^{11}
-2 → +2	20	-7.9×10^{10}	2.2×10^{20}	0	1.2×10^{6}	1.1×10^{6}	2.0×10^{11}
-4 → +4	33	-4.8×10^{10}	5.0×10^{19}	0	1.2×10^{6}	1.2×10^{6}	2.0×10^{11}
-4 → +4	51	-4.8×10^{10}	5.0×10^{19}	0	1.8×10^{6}	1.9×10^{6}	2.0×10^{11}

Chapter 5

Experimental Exploration of Steep Subthreshold Slope in FE:$HfZrO_2$-based Negative-Capacitance FETs

5.1 Introduction

In the previous chapters of 2, 3, and 4, based on the NC model [1], simulation-based studies have been conducted on the characteristics of FE:HfO_2-based NCFETs. It has been shown that, with the design points of the device structures and the FE material characteristics, steep SS is expected to be realized in the experiments. For example, thickening FE layer (as well as varying P_r and E_c in FE materials) can significantly contribute to the SS < 60mV/decade based on the NC model [2-3]. However, even though NCFET has been intensively studied and excellent characteristics have been demonstrated, the NC model and experimental device characteristics do not necessarily match nor fully consistent. Furthermore, physical origin of the NC effect and steep SS is not very clear yet. Therefore, a systematical experimental research has been strongly required in the research field of study on NCFET. In this chapter, to clarify the physical origin of the NC effect and to understand the phenomenon of steep SS in FeFET, we fabricated and analyzed ferroelectric FETs (FeFET) by integrating FE:$HfZrO_2$ (HZO) capacitors on the conventional MISFETs, and discussed on the obtained experimental results from our devices.

First, in chapter 5.3, by varying the several parameters of device structures and/or FE material properties, FeFETs were systematically characterized. Then, the discrepancies between our experimental data and the NC model were carefully discussed. Thereafter, we

experimentally explored the steep SS in FeFET. Second, in chapter 5.4, based on the characteristics of nonlinear capacitance (induced by the polarization switching of FE) in FE layer [4,5,6], we fabricated and characterized FeFETs with Zr ratio varied FE:HZO thin films. Third, on our way of experimental exploration of the steep SS in FeFET with FE:HZO, we observed the steep SS of minimum value of 20mV/decade through two decades of drain current in gate leaky FeFETs. These results of steep SS in gate leaky FeFETs were described in chapter 5.5. Finally, through our experiments, we clearly addressed that monitoring gate current (I_g) was effective to understand the device characteristics of FeFETs, because we could trace the polarization switching in FE:HZO from the monitored I_g.

5.2 Device Structure and Fabrication

We fabricated FeFET by integrating a FE:HZO capacitor on a conventional MISFET. Fig. 5.1 shows the device structure of metal-FE-metal-insulator-semiconductor (MFMIS)-type FeFET fabricated in this work. There are mainly two types of gate stack structure in FeFET. Fig. 5.1 is the structure of metal-FE-metal-insulator-semiconductor (MFMIS)-based FeFET which has internal gate between FE and MIS gate. Another structure is the structure of metal-FE-insulator-semiconductor (MFIS)-based FeFET which does not have the internal gate (not shown). There are merits and de-merits in this two devices. In this study, we used the MFMIS-structured FET (MFMIS-FET) by focusing its following merits: (1) Baseline MISFET and MFM capacitor can be fabricated and characterized separately which offers significant merits for device design and analyses. (2) Internal gate of MFMIS-FET allows FE layer to be under the homogeneous electric field along channel. (3) MFMIS-FET can be easily modeled and simulated without considering electric field and polarization distributions along channel in FE layer. These merits of MFMIS-FET offers advantages us to experimentally

explore the physical origin of steep SS in FeFET. Please note that all experimental results of this work were from the MFMIS-FET with internal metal gate. Within framework of NC model [1], there are little differences between the device characteristics of MFMIS and MFIS, when the devices are long channel as in this work. In experiments, the charge and voltage division based on the series capacitance in gate stack is not different between MFMIS and MFIS, because our devices are long channel and drain voltage is not higher than 1V. On the other hands, in experiments, "charge injection" can be different between MFMIS and MFIS as discussed after next section.

In Fig. 5.1, two important physics of FeFETs in this work are shown: "①Polarization switching" and "②Charge injection". Throughout our experiments, these two physics significantly impact on the characteristics of FeFETs, not as NC model [1]. Detailed descriptions can be found in the chapters of 5.3, 5.4, and 5.5. In brief, in this work, we carefully tried to explain the phenomena of steep SS in FeFETs by using these widely accepted physics of "①Polarization switching" and/or "②Charge injection". Please note that, in this work, "②Charge injection" always indicates the charge transfer between "Si channel" and "internal gate" through SiO_2 .In other words, charge injection from "top gate" to "internal gate" [40] is not considered for the relatively thick FE:HZO insulator than SiO_2 dielectric.

Fig. 5.2 shows a process flow of FE:HZO-based MFMIS-FET, in which microscope image of device layout was also shown. First, bulk Si or fully-depleted silicon-on-insulator (FD-SOI)-based single gate MISFET was fabricated by gate last process up to gate stack deposition. Si channel was p-type whose typical doping concentration was 10^{16} cm^{-3}. As a MIS gate insulator, we used thermal SiO_2 whose thickness was designed to be 4 to 5nm to avoid large gate current. As widely known, SiO_2/Si has very low interfacial trap density (D_{it} ~ 10^{11} $cm^{-2}eV^{-1}$), therefore we can expect to obtain good interfacial characteristics in the

baseline MISFET. Then, MFM capacitor was formed by depositing titanium nitride (TiN) (internal gate), HZO, and TiN (top gate) in sequence. TiN was deposited by reactive sputtering. HZO was deposited by atomic-layer-deposition method (ALD). Zr ratio of HZO can be varied by control the pulse cycles of ALD deposition. Final anneal for crystallization of HZO was conducted at 500°C for 60s. To realize capacitance and charge matching between MFM capacitor and baseline MISFET, the area of top gate electrode was varied and typically designed smaller than MIS gate area.

5.3 Comparison of Experiments and NC Model

In previous chapter 2, based on the NC model [1], we investigated how FE material parameters (P_r and E_c) and device structural parameters (T_{fe} and T_{ox}) impact on the characteristics of NCFET. Even though NCFET has been intensively studied and steep SS characteristics have been reported by many groups, however, systematic comparison of the NC model [1] and experimental device characteristics have not been reported yet. Therefore, in this chapter, we verify the NC model whether it can be a useful model for experimental steep SS in FeFET. In other words, by varying several parameters such as area ratio (AR), thickness of FE:HZO (T_{fe}), and remanent polarization (P_r), we confirm that our experimental results can be explained by the NC model well.

In this chapter, monitoring gate current (I_g) was very useful approach to understand the device characteristics of FeFET, because we could trace the polarization switching in FE:HZO from the monitored I_g.

5.3.1 Variable Parameters and Default Condition

Here, we used following three variable experimental parameters. (1) Area ratio (AR)

between top gate and MIS gate area. (2) Thickness of FE:HZO (T_{fe}). (3) Zr ratio in HZO which modifies FE material characteristic, especially remanent polarization (P_r). Default conditions of these three parameters were selected as follows: AR=1:14, T_{fe}=10nm, and Zr ratio of 30%. Baseline MISFETs are long channel devices whose gate length and width were 100μm.

5.3.2 MFM Capacitor and Baseline MISFET

Fig. 5.3 shows FE characteristics of MFM-HZO capacitors with varied Zr ratio of 30%, 20%, and 10% after wake-up (W/U) treatment of 1000 cycles. Typical thickness of FE:HZO was T_{fe}=10nm, and FE:HZO with T_{fe}=6nm was characterized and shown only for Zr ratio of 30%. Diameter of top gate electrode was 30μm. Measuring frequency was 1kHz. Our HZO capacitors showed clear FE P-V hysteresis curves. In the case of 30%-Zr ratio and 10nm-thick FE:HZO, P_r=16μC/cm^2 and E_c=1MV/cm were obtained. Smaller P_r was obtained with lower Zr ratio which is consistent with other previous report [7]. On the other hands, E_c was not much impacted by varying Zr ratio. Please note that transient current responses also showed clear FE characteristics, in which current peaks are induced by “polarization switching”.

Fig. 5.4 shows I_d-V_g characteristic of baseline MISFET (L_g=W_g=100μm), in which monitored I_g was also plotted. Typical SS value was extracted at the drain current level of I_d = W_g / L_g × 10^{-9} A and V_d=0.05V, defined as SS9 here. SS9 of baseline MISFET was 83mV/decade. From the SS9 value, D_{it} was extracted to be 1×10^{12} eV^{-1}cm^{-2}. At the measured V_g sweep range, monitored I_g was very low as noise level (< 5pA). From Figs. 5.3 to 5.4, we confirmed that the characteristics of the separated MFM capacitors and MISFETs were fine.

5.3.3 Simulation Results of Bulk NCFET based on the NC Model

Based on the NC model [1], device characteristics of bulk NCFET were simulated to obtain a device design point for our MFMIS-FET. Here, LK parameters (α, β, and γ) in our Zr ratio-varied HZO thin film were extracted from the P_r and E_c in measured P-V data in Fig 5.3. As a model for baseline MISFET, BSIM4 was used and calibrated to the experimental I_d-V_g characteristics of MISFET shown in Fig 5.4. For the NCFET simulations, SPICE was used as a simulator [8]. This SPICE compact model [8] is based on the MFMIS structure which is a well-used structure for its simplicity on modeling. The characteristics of MISFET are simulated by the BSIM4 model, then, characteristics of NCFET are obtained by coupling Landau equation (described in Verilog-A form) and charge density of MIS gate extracted from SPICE.

Fig. 5.5 shows simulated I_d-V_g characteristics and SS-I_d data of AR-varied NCFETs, in which characteristics of baseline MISFETs were also plotted for comparison. Zr ratio in HZO thin film and T_{fe} were default conditions of 30% and 10nm, respectively. With larger AR (which means smaller top gate with fixed channel size), NC effect effectively impacts on the characteristics of NCFET which results in steeper SS which can be attributed to the voltage division through gate stack as discussed in chapter 2. With larger AR and smaller top gate electrodes, larger negative voltage is induced to FE layer ($|V_{fe}|$) because of small capacitance of FE layer. Please note that, hysteresis was not shown even with AR=1:14 in Fig. 5.5. These results of bulk NCFETs are consistent with our simulation studies on multi-gate NCFET which were described in chapter 2 [2-3]. Here, we focus on the region of $V_g > 0$ because $V_g < 0$ region is leakage dominant which is the out of scope. The $V_g < 0$ region also can be explained by NC model because larger positive voltage is induced in FE with larger AR when $V_g - V_{fb} < 0$, where V_{fb} is flatband voltage.

Fig. 5.6 shows simulated I_d-V_g characteristics and SS-I_d data of T_{fe}-varied NCFETs, in

which characteristics of baseline MISFETs were also plotted for comparison. AR and Zr ratio in HZO thin film were default conditions of 1:14 and 30%, respectively. With thicker T_{fe}, NC effect effectively impacts on the characteristics of NCFET which results in steeper SS. This T_{fe} dependence was already explained by the framework of NC model [1] in previous chapter 2 [2,3]. Based on the NC model [1], with thicker T_{fe}, larger negative voltage is induced to FE layer. Please note that, hysteresis was not shown even with T_{fe}=10nm in Fig. 5.6.

Fig. 5.7 shows simulated I_d-V_g characteristics and SS-I_d data of Zr ratio-varied NCFETs, in which characteristics of baseline MISFETs were also plotted for comparison. AR and T_{fe} were default conditions of 1:14 and 10nm, respectively. Here, Landau parameters were extracted from experimental P-V data with varied Zr ratio in Fig. 5.3. In Fig. 5.3, our experimental results showed that P_r decreases with lowered Zr ratio. In Fig. 5.7, with lower Zr ratio and P_r, NC effect effectively impacts on the characteristics of NCFET which results in steeper SS. This is attributed to the fine capacitance matching in gate stack as described in chapter 2 [2]. With smaller P_r, higher negative voltage ($|V_{fe}|$) is induced in FE layer when the level of charge density is same. Additionally, in the case of Zr ratio of 20% and 10%, very steep jump of drain current was observed, in which an anti-clockwise hysteresis was accompanied. These results are consistent with other simulation studies on NCFETs [9] based on the NC model [1].

In these simulations on bulk NCFET (Figs. 5.5-5.7), we used the parameters from our fabrication and experimental data shown in Figs. 5.3-5.4. Therefore, based on the NC model [1], our experimental MFMIS-FET is expected to offer very steep SS < 60mV/decade when AR, T_{fe}, and Zr ratio are varied and optimized.

5.3.4 Experimental Area Ratio Dependence

First, our fabricated MFMIS-FETs were characterized by varying AR. Zr ratio in HZO thin film and T_{fe} were default conditions of 30% and 10nm, respectively. Fig. 5.8 shows experimental I_d-V_g characteristics and SS-I_d data of MFMIS-FET (L_g=W_g=100μm) with varied AR as 1:1.25 (diameter of top gate=50μm), 1:8 (diameter of top gate=40μm), and 1:14 (diameter of top gate=30μm). The I_d-V_g characteristics and SS-I_d data of MISFET were also plotted for comparison. In the measurement for MFMIS-FETs, internal gate is floated. In Fig. 5.8, hysteresis was observed in the I_d-V_g characteristics which is inconsistent with the simulation results based on the NC model shown in Fig. 5.5. Anti-clockwise hysteresis was observed in MFMIS-FET with AR=1:14 and 1:8, however, clockwise hysteresis with AR=1:1.25.

Hysteresis I_d-V_g characteristics cannot be simply explained by the NC model. Instead, it can be explained by the charge injection between Si channel and internal gate through SiO_2 insulator and conventional P-V hysteresis in FE (spontaneous polarization) shown in Fig. 5.1 [10]. Here, charge injection between top gate and internal gate [40] through FE:HZO is not considered for simplicity. As widely known, hysteresis characteristics in conventional FeFET are determined by the charge injection phenomenon and the spontaneous polarization [10]. For memory applications, finite hysteresis characteristics are preferred. Charge injection into the internal gate (or into the defect state in insulator) is used in the flash memory technologies, and spontaneous polarization (conventional hysteresis P-V curve) is used in the memory technologies of FeRAM including FeFET [10]. From the mechanisms of the charge injection and the spontaneous polarization, AR dependence of memory window in Fig. 5.8 can be simply explained. Charge injection and spontaneous polarization compete each other in shifting V_{th} of MISFET. They shift V_{th} towards opposite direction. With small AR=1:1.25, gate voltage is divided to MIS gate highly which results in charge injection into internal

floating gate to be dominant. This charge injection leads to clockwise hysteresis in I_d-V_g characteristics of nMOSFET which is utilized in floating-gate transistor memory. With higher AR than 1:8, gate voltage can be divided to FE insulator sufficient highly, therefore spontaneous polarization in FE now can impact on surface potential of Si. Spontaneous polarization in FE insulator leads to anti-clockwise hysteresis in I_d-V_g characteristic of nMOSFET as shown in the case of AR=1:8 and 1:14 in Fig. 5.8.

Please note that amount of charge injection is time-dependent, therefore V_{th}-shift can depend on the measurement time. In this work, I_d-V_g measurements was conducted by using "Classical Test Application Test" of I/V sweep in B1500A (supplier: Keysight). Follows are out setting of dc characterization in this work: (1) Integral time: high resolution analog/digital converter of factor 1 (80μsec). (2) Delay time: 0s. (3) V_g step: Typically 50mV. (4) Wait time: factor 1. Under the characterization with much faster measurements than in this work, the impacts of charge injection can be smaller. On the other hands, intrinsic response speed of FE thin films is widely known to be very fast (< 1ns) [31,32], therefore, time delay of FE is not considered here. However, a large area of FE capacitor can incur time delay from its own RC-time constant. In this work, measurement time is much longer than such a time constant, therefore, time delay of FE was not considered.

In Fig. 5.8, SS values of MFMIS-FETs were not steeper than the SS values of MISFETs over all drain current levels. The non-steep SS is inconsistent with the NC model-based simulation shown in Fig. 5.5. This indicates that, in our experiment, capacitance of FE insulator was not negative but positive while transistor is in subthreshold region. We would like to discuss on this in the chapter 5.3.8 of "Discussions on Discrepancies between Experiments and the NC model".

5.3.5 Experimental Thickness of FE:HZO Dependence

Second, our fabricated MFMIS-FETs were characterized by varying T_{fe}. AR and Zr ratio in HZO thin film were default conditions of 1:14 and 30%, respectively. Fig. 5.9 shows experimental I_d-V_g characteristics and SS-I_d data of MFMIS-FET with varied T_{fe}. The I_d-V_g characteristics and SS-I_d data of MISFETs were also plotted for comparison. In our experiments, hysteresis was observed in I_d-V_g characteristics which is inconsistent with the simulation results based on the NC model shown in Fig. 5.6. Anti-clockwise hysteresis was observed in both of T_{fe}=10nm and 6nm. These hysteresis I_d-V_g characteristics can be explained by conventional P-V hysteresis in FE material [10].

Furthermore, in Fig. 5.9, SS values of MFMIS-FETs were not steeper than them of MISFETs over all drain current levels. The non-steep SS is inconsistent with the NC model-based simulation shown in Fig. 5.6. This indicates that, in our experiment, capacitance of FE insulator was not negative but positive while transistor is in sub-V_{th} region. We would like to discuss on this in the chapter 5.3.8 of “Discussions on Discrepancies between Experiments and the NC model”.

5.3.6 FE Material Characteristics (Zr Ratio) Dependence

Third, our fabricated MFMIS-FETs were characterized by varying Zr ratio (P_r). AR and T_{fe} of HZO thin film were default conditions of 1:14 and 10nm, respectively. Fig. 5.10 shows experimental I_d-V_g characteristics and SS-I_d data of MFMIS-FET with varied Zr ratio (P_r). The I_d-V_g characteristics and SS-I_d data of MISFETs were also plotted for comparison. In Fig. 5.10, hysteresis was observed in I_d-V_g characteristics which is inconsistent with the simulation results based on the NC model shown in Fig. 5.7. These hysteresis I_d-V_g characteristics can be explained by conventional P-V hysteresis in FE material and charge injection into internal

gate [10]. From their directions of hysteresis in Fig. 5.10, charge injection is dominant in 30%-Zr ratio, and spontaneous polarization is dominant in 20%- and 10%-Zr ratio. This can be explained by considering that positive capacitance (dielectric constant of paraelectric region) in FE:HZO is higher when P_r is higher [6]. With high P_r, smaller voltage is divided to FE layer (relatively high voltage to MIS capacitor) because of its high capacitance. As a result, charge injection becomes dominant relatively with higher P_r in 30%-Zr HZO, therefore, clockwise hysteresis is observed in I_d-V_g curve. On the other hands, with Zr 10% and lower P_r, owing to its relatively lower positive capacitance, anti-clockwise hysteresis which is induced by FE spontaneous polarization can be dominant.

Furthermore, in Fig. 5.10, SS values of MFMIS-FETs were not steeper than them of MISFETs over all drain current levels. The non-steep SS cannot be simply explained by the NC model as well as inconsistent with the NC model-based simulation results shown in Fig. 5.7. Higher SS value in MFMIS-FET comparing to MISFET indicates that, in our experiment, capacitance of FE insulator was not negative but always positive while transistor is in sub-V_{th} region. We would like to discuss on this in the chapter 5.3.8 of “Discussions on Discrepancies between Experiments and the NC model”.

5.3.7 Current Peaks in Monitored Gate Current by Polarization Switching of FE:HZO

It is worth to note the monitored I_g during I_d-V_g measurements shown in Fig. 5.11. Fig. 5.11 (upper figure) shows that clear transient current responses of FE:HZO can be observed in the monitored I_g during I_d-V_g characterization of MFMIS-FETs [11]. I_g data were obtained by measuring current flow at top gate, while internal gate is electrically floated. In this work, I_d-V_g measurements was conducted by using “Classical Test Application Test” of I/V sweep in B1500A (supplier: Keysight). Follows are out setting of dc characterization in this work: (1)

Integral time: high resolution analog/digital converter of factor 1 (80μsec). (2) Delay time: 0s. (3) V_g step: Typically 50mV. (4) Wait time: factor 1. This indicates that the current peaks of I_g shown in Fig. 5.11 is transient component, therefore current peaks of I_g are dependent on the "time" of measurement. Under a static characterization with much faster measurement, the current peaks of I_g can be small. Furthermore, the monitored I_g at top gate is current component flow through MIS capacitor. In this device process, MISFET was gate leaky than other devices due to process variability, consequently, transient current of polarization switching through MFMIS stack was large in Fig. 5.11 (top). Please note that, in typical, leakage current components through MFM and MIS cannot be equal, as a result, part of charge remains in internal gate ("charge injection"). As discussed after next section, the charge injection significantly impacts on the characteristics of our FeFETs.

Please note that these transient current responses were also observed in separated MFM capacitors with 1kHz triangular input voltage (Fig. 5.11, bottom figure). Therefore, these transient current peaks of I_g can be attributed to the polarization switching of FE:HZO. From these experiments, we clearly addressed that, by monitoring I_g, we can trace the polarization switching of FE:HZO while measuring I_d-V_g characteristics of MFMIS-FETs. In fact, monitored I_g has been reported in some studies on NCFETs [12], however, the significance of it to understand the operation of NCFET has not been addressed yet. Hereafter, monitored I_g data play an importance role in our experimental explorations of steep SS in FeFET.

5.3.8 Discussions on Discrepancies between Experiments and the NC model

So far, our fabricated MFMIS-FETs with FE:HZO capacitors were not steep slope FETs as the NC model [1] shown in Figs. 5.5-5.7. Throughout our systematic experiments, NC effect in FE was not observed, and capacitance of FE:HZO was positive within sub-V_{th} region.

Our experimental results and dependences can be explained by assuming that the capacitance of FE:HZO within sub-V_{th} region was not negative but positive. The evidences and discussions on "the positive capacitance of FE:HZO" are as follows:

First, as mentioned above, hysteresis in experimental I_d-V_g characteristics and several dependences cannot be explained by the "S-shaped non-hysteresis P-V curve" in the NC model [1]. Instead, they can be explained by the simple conventional hysteresis P-V curve and charge injection [10] into internal gate. Second, the non-steep SS values cannot be explained by the negative capacitance values in FE:HZO. Instead, they can be explained by the simple positive capacitance values in FE:HZO.

Here, we would like to discuss on "Why did the NC model and steep SS are frustrated in our devices?" Based on the monitored I_g in Fig. 5.11, our careful consideration is that, the charge injection into internal gate can be the reason [13,18].

Regarding the charge injection issue, monitored I_g in Fig. 5.11 has shown that, current peaks of I_g and I_d, induced by the "polarization switching" of FE:HZO, were observed where transistor is not within sub-V_{th} region but within strong inversion and/or accumulation region. From the viewpoints of charge matching between Si and FE:HZO (i.e., boundary condition of charge density), this indicates that the transition of charge state from accumulation to strong inversion region of MFMIS transistor (from purple circle to red circle in upper figure in Fig. 5.11) matched not the "NC region" around "polarization switching" (from red circle to green circle in bottom figure in Fig. 5.11) but the non-switching paraelectric region of polarization (from purple circle to red circle in bottom figure in Fig. 5.11) in FE:HZO. This interpretation is strongly supported by the positions of the current peaks of I_g (upper) and transient current (bottom) of MFM capacitor in Fig. 5.11.

Then, why does charge transition from accumulation to strong inversion region of

transistor matched not the “NC region” around “polarization switching” (from red circle to green circle in bottom figure in Fig. 5.11) but the non-switching paraelectric region (from purple circle to red circle in bottom figure in Fig. 5.11) in FE:HZO? This can be attributed to the existence of charge injection [13,18] into internal gate, which results in a “charge offset” between Si and FE:HZO, as illustrated in Fig. 5.12 [19]. The “charge offset” can be induced by the charge injection into internal gate while the large positive or negative gate bias is applied to top gate of MFMIS. Fig. 5.12 shows the measured charge-voltage curves (P-V curves) of FE:HZO capacitor and the calculated charge-voltage curves of Si (plotted as load lines with varied V_g) [19]. Here, thickness of interfacial insulator (T_{ox}) of 0nm and area ratio (AR) 1:1 were assumed for simplicity, and doping concentration of p-type Si was $N_a=1\times10^{16}$ cm^{-3}. In the case of no “charge offset” (Fig. 5.12(a)), at $V_g - V_{fb}$=-1V and 0V, the charge state of Si is accumulation, and polarization of FE is not switched yet (correspond to red circle and blue circle). With $V_g - V_{fb} > 0$V, polarization switching occurs in advance (from blue circle to green circle), and then the charge state of Si is transformed from accumulation (blue circle) to the depletion (green circle). This indicates that, without “charge offset” as assumed in the NC model, “NC region” is accessible when transistor is within sub-V_{th} region (depletion region). However, in the case of finite “charge offset” (Fig. 5.12(b)), due to the charge injection and consequent “charge offset” (for example, “charge offset” of 20μC/cm^2 was assumed in Fig. 5.12(b)), with the forward V_g sweep, MFMIS-FET is turned on in advance (from red circle to blue circle and green circle) before the FE:HZO passes through “polarization switching” or enter the “NC region”. This indicates that charge transition of MFMIS-FET from accumulation (red circle) to strong inversion region (green circle) matches not the “NC region” around “polarization switching” but the non-switching region of polarization (i.e., paraelectric component) of FE:HZO as shown in Fig. 5.12(b). As a result, boost of drain current can be

seen not within the sub-V_{th} region but within the strong inversion or accumulation region as shown in upper figure of Fig. 5.11. In our experiments, even though gate leakage in MISFETs are very low, charge injection still incurs this kind of "charge offset" in our MFMIS devices, therefore issue of "charge offset" cannot be avoided. Under the existence of the "charge offset", change of polarization within paraelectric region (ΔQ_{fe}) is large enough to transform the charge state of Si from accumulation to strong inversion region (ΔQ_{si}) as can be seen in Fig. 5.12(b). Consequently, capacitance value of FE:HZO (corresponds to the dQ_{fe}/dV_{fe} in Fig. 5.12(b)) was necessarily always positive when transistor is within sub-V_{th} region. This indicates that, with the finite "charge offset", "NC region" or "polarization switching" is not accessible when transistor is within sub-V_{th} region. Due to the charge injection, only when transistor is within strong inversion or accumulation region, "NC region" or "polarization switching" was accessible in our experiments.

Above discussions are based on the experimental results from our MFMIS structured FeFETs. Here, the issue of "charge injection" into internal gate seems to be incurred by the existence of internal gate. Then, above discussions can be applied to MFIS-FETs? Our consideration is that, even under MFIS structure without internal gate, charge is injected to the interfacial defect state of ferroelectric/dielectric (FE/DE) and/or to the boarder trap state of FE insulator by charge trapping as discussed in Ref. 13. The steep SS can be frustrated by the charge injection into FE/DE [13], therefore our discussion can be partially applied to the MFIS structure.

So far, we discussed why the NC model and steep SS were frustrated in our devices. Based on the monitored I_g (Fig. 5.11) and the charge-voltage curves (Fig. 5.12), our careful consideration is that, the charge injection [13,18] into internal gate is the reason why the capacitance of FE:HZO was always positive within sub-V_{th} region. The charge injection and

consequent “charge offset” have not been considered in the NC model [1] and simulation studies based on it, except Refs. 13 and 18.

Then, it should be addressed that, the phenomena of drain current boost within strong inversion region (and accumulation region) can be attributed to the “NC state” of the NC model [1]? In other words, in our experiments, does FE:HZO pass through the “non-hysteresis S-shaped P-V curve” as the “NC model” [1], or the “conventional hysteresis P-V curve” which accompanies the “polarization switching”? (see a Fig. 1.4) Based on the experimental results in our devices, we consider that our experimentally observed current boosts of drain current and transient gate current can be explained by both of above two explanations (“NC model” or “polarization switching”) on “how does FE work in FeFETs?”.

In fact, this topic has been very highly controversial in the device research community [4,5,6,13,and 15] since the NC model was proposed in 2008 [1]. However, the academic-level discussions on this issue have not been conducted sufficient yet.

My speculations on this topic are as follows: As pointed out by C. M. Krowne *et al*. [4,15], C. S. Hwang *et al*. [5], and H. Ota *et al*. [6], the drain current boost in our FeFETs (and steep SS phenomena by other groups) does not necessarily attributed to the “negative absolute capacitance (NAC)” and “NC state” of NC model [1], when we carefully consider the physical images of that NC model. For discussions on the physical images of “NC state” [1] from various angles, especially its state of energy local maxima and NAC, please refer to Refs. 4,6,15,20-29. Regrettably, a lot of previous experimental reports (except Refs. 16 and 18) on the demonstrations of steep SS in FeFETs have attributed physical origin of observed steep SS phenomena to the “NC model” [1], without clear explanations on its physical images. There have been critical errors in the descriptions on energy landscapes of FE-DE system by the authors who insist NC model. For examples, please refer to Ref. 35 (Fig. 1(a)), Ref. 36 (Fig.

1(a)), Ref. 37 (Fig. 2), Ref. 38 (Fig. 1(c)) and Ref. 33 (pp. 8646, (1)). These have been widely accepted as descriptions of energy landscapes for the "stabilized NC state". However, these [35,36,37] are incorrect because they do not consider electric field in FE and DE. In Refs. 38 and 33, M. Hoffmann *et al.* and A. I. Khan *et al.* indeed considered electric field in FE. However, referring to Fig. 1(c) in Ref. 38, they insist that, "when the applied field is higher than coercive field, energy barrier vanishes and the NC region (defined by the negative curvature of the potential) can be accessed for a certain time during switching [33]". However, there is no negative curvature when the applied field is higher than coercive field as clearly shown in Fig. 1(c) of Ref. 38. When the applied field is higher than coercive field, there is only positive curvature (positive capacitance), consequently, "polarization switching" occurs [39]. In other words, correct physical image corresponding to Fig. 1(c) in Ref. 38 is not the "NC state" [1,33] but the "polarization switching" itself [39]. For the correct energy landscape of "NC state", please, please refer to Fig. 2 of Ref. 4 and related descriptions there.

My speculations is that, instead of such "energy local maxima" and "NAC" [1], the boosts of drain current and gate current in FeFETs can be attributed to the "negative differential capacitance (NDC)" which was also demonstrated in ferroelectric-dielectric (FE-DE) series capacitors (see a negative slope in Q_{fe}-V_{fe} curves of Figs. 2-3 in Ref. 14.). Instead of "NC state" [1], for the NDC phenomena, the "polarization switching" of FE can be a reasonable and physically acceptable explanation [4,5,6]. In conventional FE materials, "polarization switching" accompanies several nonlinearities (i.e., voltage dependences) in their dielectric characteristics (see a Fig. 5.13). The nonlinear capacitance can result in NDC in FE-DE series network while keeping the absolute capacitance positive [4,5,6,and 14]. Detailed descriptions on the nonlinear capacitance of FE can be found in next chapter. In brief, as shown in Fig. 5.11 and Fig. 5.14, at the onset of "polarization switching" and consequent

increase in the positive capacitance of FE (even though they were limited within strong inversion and accumulation in our experimental results), voltage division to FE layer is gradually decreased which results in voltage division to MIS gate to be gradually increased. As pointed out by C. S. Hwang *et al.* [5], this "polarization switching" can result in $dQ_{fe}/dV_{fe} < 0$ which were demonstrated in Figs. 2-3 of Ref. 14 by A. I. Khan *et al.*. In other words, while "polarization switching" process is ongoing, the consequent increase in positive capacitance of FE:HZO (corresponds to the thinned EOT) can contribute to the V_{th}-shift to the negative V_g direction in MFMIS nFETs [6], as a result, drain current boost can be observed as shown in Fig. 5.11 and Fig. 5.14. These discussions are based on the experimental results from the MFMIS structure, however, we consider that these can be applied to the MFIS structure.

5.3.9 Summary

In our experiments, "NDC" and "polarization switching" was observed in our fabricated FE:HZO-based MFMIS-FETs (Fig. 5.1). However, not as simulation results based on NC model [1], the events of the "NDC" and "polarization switching" were not allowed within sub-V_{th} region due to the "charge injection" [13,18] into internal gate, therefore the "steep SS" was not observed. Instead, the events of the "NDC" and "polarization switching" were allowed only within strong inversion and accumulation region due to the "charge injection", therefore the "drain current boost" was observed.

Through our experimental exploration, we clearly addressed that monitoring I_g while I_d-V_g measurement can allow us to trace where polarization switching occurs, for the first time (see a Fig. 5.11). Hereafter, monitoring I_g plays an important role to understand and explore the "NC effect" and steep SS in FE:HZO-based FETs.

5.4 Steep Subthreshold Slope Using Polarization Switching of FE:$HfZrO_2$

In previous chapter, “effective NC effect”, induced by “NDC” and “polarization switching”, was observed in our fabricated FE:HZO-based MFMIS-FETs (Fig. 5.1). However, due to the charge injection, the events of the “effective NC effect” were not allowed within sub-V_{th}, therefore the “steep SS” was not observed. Instead, the events of the “effective NC effect” were allowed only within strong inversion and accumulation region, therefore the “drain current boost” was observed as shown in Figs. 5.11 and 5.14. Then, to realize the steep SS, is it possible to move the events of “polarization switching” from the strong inversion and accumulation region toward the sub-V_{th} region as illustrated in Fig. 5.14? In other words, are there any effective device and material design approaches to overcome the charge injection effect addressed in Fig. 5.12? This chapter includes our experimental exploration for it.

5.4.1 Use of Non-Linear Dielectric (NLD) Properties of FE:HZO for Steep SS

As an alternative physical model of the NC model, nonlinearity of capacitance (i.e., voltage dependences of capacitance in FE) in FE due to the “polarization switching” has been proposed by C. M. Krowne *et al*. [4] in 2011. Then, based on Ref. 4, simulations on the characteristics of FeFET [6] and on the transient responses of series R-C network [5] were reported. Here, following the paper by H. Ota [6], we call this model as nonlinear dielectric model (NLD model) and a transistor designed based on the NLD effect as an NLD-FET. Physical origin of NLD effect is “polarization switching” of FE and nonlinear dielectric properties based on it (Fig. 5.13). The NLD model uses nonlinear dielectric properties of FE:HZO capacitor. Fig. 5.13 shows (a) P-V characteristic, (b) large signal C-V characteristic

(mathematically calculated by dP/dV of (a)), (c) transient I-V response during P-V characterization of (a), and (d) small signal C-V curve of our fabricated FE:HZO capacitor whose Zr ratio was 30% and T_{fe}=10nm. In Fig. 5.13, nonlinear characteristics in FE:HZO are clearly shown, in which a physical origin of the increase/decrease of capacitance and transient current peaks is "polarization switching" of FE:HZO.

In Fig. 5.14, a schematic of idea for the steep SS in NLD-FET was illustrated. If the increase/decrease in positive capacitance of FE insulator (C_{fe}) can be occurred within sub-V_{th} region of MFMIS-FETs during its FE-induced anti-clockwise hysteresis in I_d-V_g measurement, then V_{th} can be gradually shifted which can result in steep SS characteristics [6,14]. There is a simple misunderstanding on the NLD-FETs with FE:HfO_2-based materials. In Ref. 33, M. Hoffmann *et al.* insist that a change of positive capacitance in FE:HfO_2 is not more than one order of magnitude, therefore steep SS and "NDC" cannot be realized. However, NLD-FETs indeed require a large change of capacitance, however, the required change of capacitance is not the small-signal capacitance (Fig. 5.13(d)), but the large signal capacitance (Fig. 5.13(b)) [34]. Small signal C-V measurement is different with the I_d-V_g measurement of FeFETs, therefore, it always underestimates the change of capacitance of FE:HfO_2 for NLD-FETs. As shown in Fig. 5.13(b), with large signal C-V characteristic, change of capacitance is more than one order of magnitude. In MFIS stack, depolarization field due to an imperfect screening of polarization can suppress the change of capacitance and polarization itself, however, depolarization field is not considered in this work on MFMIS stack.

Based on the NLD model, the SS in experimental MFMIS-FET can be steep? Polarization switching of FE can be occurred in sub-V_{th} region? Are there useful design points of device structures and materials based on the NLD model? Even though the physical original of NLD model are supported by conventional FE theory (i.e., electric field-induced

“polarization switching”) [38], experimental studies of steep SS in NLD-FETs have not been reported yet. Therefore our experimental exploration in this chapter can shed light on the steep SS phenomena in FeFETs.

In this chapter, monitoring gate current (I_g) was very useful to understand the device characteristics of FeFET, because we could trace the polarization switching in FE:HZO from the monitored I_g.

5.4.2 Proposal of Using Anti-ferroelectric HZO (AFE:HZO) for Steep SS

A key to realize steep SS in NLD-FET is that, polarization switching of FE insulator has to be occurred within the subthreshold region of Si. In other words, charge (or polarization)-inversion of FE insulator and semiconductor should be simultaneous events in the time and bias. However, already discussed in Figs. 5.11 and 5.12, with clear ferroelectric HZO-based of FE:HZO (Fig. 5.3), polarization switching can be observed only in strong inversion and accumulation region due to the charge injection into internal gate. Even small amount of charge injection can result in large “charge offset” between FE and Si, therefore MFMIS-FETs with clear FE HZO can be elusive. Then, which kinds of device and/or FE material design for MFMIS-FET are effective to use the nonlinear capacitance of FE within sub-V_{th} region? Besides, nonlinear capacitance change in FE:HZO is sufficient for the steep SS < 60mV/decade in NLD-FET?

To answer the above questions by our experiments, we experimentally explored a possibility of steep SS in HZO-based FET based on the NLD model. Purpose of this chapter is to experimentally explore that this alternative physical model of steep SS in FeFET using “polarization switching (nonlinear capacitance)” of FE:HZO can contribute to steep SS. Additionally, we intended to verify the possibility that “polarization switching (nonlinear

capacitance)" in FE:HZO can be physical origins of recent experimental demonstrations of steep slope FeFET by other research groups. However, as addressed above, MFMIS-FETs with clear FE characteristics had a difficulty for the simultaneous charge inversion of FE and Si due to charge injection (Figs. 5.11 and 5.12).

Here, we propose the anti-ferroelectric (AFE) characteristics of HZO (AFE:HZO) with higher Zr ratio as a FE layer. AFE characteristics already have been reported with HfO_2-based materials when doping material or doping concentration is varied [7]. Typically, the P-V curves of AFE materials have two transient current peaks induced by two nonlinear capacitance changes in single voltage sweep. If we can use AFE:HZO insulator, there is a possibility that nonlinearity of capacitance in FE:HZO can be positioned within sub-V_{th} region because the first capacitance change (and current peak) appears near to V_{fe}=0V [7]. Therefore, we designed and fabricated MFMIS-FET with AFE:HZO. Device structures and fabrication process were same with the descriptions in chapter 5.2. Default L_g and W_g were both 100μm. As an AR, 1:8 or 1:32 was used to apply enough voltage to FE layer. To search material design point of AFE:HZO, first, Zr ratio was varied from 0, 10, 20, 30, 50, 60, 70, and 100%. After measuring 70%-Zr ratio MFMIS-FET as a typical case, then, we fabricated MFMIS-FET of Zr ratio 80, 90, 100%, in which stronger AFE characteristics can be expected.

5.4.3 P-V characteristics of Zr ratio-varied HZO

Here, to search for the material design point of AFE:HZO, HZO MFM capacitors with varied Zr ratio were fabricated and characterized as shown in Fig. 5.15, in which Zr ratio was varied from 0, 10, 20, 30, 50, 60, 70, and 100%. From 0% to 100% of Zr ratio, phase transition of paraelectric (Zr 0%) → ferroelectric (Zr 10-50%) → anti-ferroelectric phase (Zr 60-100%) was observed in our experiments. This Zr ratio dependence of HZO is in

accordance with previous report [7].

5.4.4 Two "Polarization Switching" in AFE:HZO-based MFMIS-FET

Fig. 5.16 shows the characteristics of MFMIS-FETs with Zr ratio of 70% as a typical case of AFE:HZO-based MFMIS-FET. AR=1:32 and T_{fe}=10nm were used. In Fig. 5.16(a), HZO with Zr ratio 70% showed clear AFE characteristics where two current peaks and two capacitance changes were observed in single voltage sweep. Fig. 5.16(b) shows I_d-V_g characteristic of baseline MOSFET whose typical SS (SS8 here) value was 110mV/decade. In MFMIS-FETs (Fig. 5.16(c) and (d)), clockwise hysteresis was observed in the I_d-V_g characteristics due to the charge injection. In Fig. 5.16(c) and (d), monitored gate current had two current peaks which can be attributed to the "polarization switching". Furthermore, with these gate current peaks, drain current also had two current peaks at same bias range as expected in NLD model. Thanks to the existence of two current peaks in AFE:HZO, first current peak is closer to the sub-V_{th} region comparing to MFMIS-FET with 30%-Zr ratio in Fig. 5.11. However, in Fig. 5.16, even with AFE:HZO with Zr ratio of 70%, NLD effect (events of polarization switching) was mainly observed over V_{th} region and accumulation regions. It is considered that stronger AFE characteristics can be effective for NLD-FET design.

5.4.5 Suppressed and Split Polarization Switching in Sub-V_{th} region

Fig. 5.17 shows the FE characteristics of the separated HZO capacitors with Zr ratio of 80%, 90% and 100%. Stronger AFE characteristics than Zr 70% were observed in Fig. 5.17, as we expected. Even after 1000 cycle wakeup treatment, AFE characteristics were not significantly degraded nor transited to FE-dominant characteristics.

Fig. 5.18 shows the I_d-V_g characteristics of MFMIS-FET with Zr ratio of 90% and AR=1:8, in which monitored I_g during the I_d-V_g measurement was also plotted. The characteristics of separated baseline MISFET was fine as shown in Fig. 5.16, and gate leakage in baseline MISFET was small as noisy level. In Fig. 5.18, I_d-V_g characteristics of MFMIS-FET (top) have clockwise hysteresis due to charge injection into internal gate. Monitored gate current had two current peaks which are attributed to the polarization switching of AFE:HZO as already shown in 70%-Zr ratio case (Fig. 5.16). With forward gate voltage sweep shown in top figure of Fig. 5.18, first gate current peak appears near V_g=2V and second gate current peak near V_g=5V. These two current peaks can be interpreted as the polarization switching-induced, because so does drain current have two peaks at same bias with the gate current peaks. However, in the extended I_g-V_g graph of MFMIS-FET (bottom), we found an another current peak in negative gate voltage along forward V_g sweep. The current peak in negative V_g is considered to be part of first polarization switching current. In other words, the first current peak was suppressed in around V_g=0V in which transistor enters sub-V_{th} region from accumulation region. With the transition of Si from accumulation to depletion region, capacitance of Si becomes much smaller as capacitance of depletion layer. Then, gate voltage is mainly divided to the depletion layer, as a result, polarization in FE can be suppressed, and current peaks can be split. If polarization switching is suppressed, the increase in capacitance of HZO is also suppressed. In fact, this kind of suppressed and split capacitance increment is not preferred for the steep SS in NLD-FET.

Fig. 5.19 shows the characteristics of MFMIS-FET with Zr ratio of 90% and AR=1:32, in which monitored I_g during the I_d-V_g measurement was also plotted. In MFMIS-FETs, I_d-V_g characteristics (top) had anti-clockwise hysteresis which is attributed to the hysteresis P-V characteristic of AFE:HZO. In MFMIS-FETs, monitored gate current had two current peaks

which are attributed to the polarization switching of AFE:HZO. In forward gate voltage sweep, first gate current peak is near V_g=-2V and second gate current peak is near V_g=+2V. However, in the extended I_g-V_g data of MFMIS-FET (bottom), we found an another current peak near V_g=3.5V along forward V_g sweep. It is considered that this current peak is part of second polarization switching current. The second current peak was suppressed and split in V_g=2~2.5V in which transistor enters sub-V_{th} region from turn-off region. With the transition of Si from accumulation to depletion region, capacitance of Si becomes very small as capacitance of depletion layer. Then, gate voltage was mainly divided to depletion layer, as a result, polarization in FE was suppressed.

Fig. 5.20 shows the I_d-V_g characteristics and extracted SS-I_d characteristics of MFMIS-FET with Zr ratio of 90% and AR=1:32. The results are as follows: (1) The typical SS value in MFMIS-FET was not significantly steep as 60mV/decade. (2) SS values of forward V_g sweep had lower SS value than the backward V_g sweep. (3) Additionally, one SS point in MFMIS-FET had steeper SS value than MISFET. From these results, there is a possibility that NLD effect was realized in our MFMIS-FET with AFE:HZO. Especially, regarding the result of (2), I_g peak was observed only in forward V_g sweep in Fig. 5.20(a), therefore there is a possibility that the NLD effect contributed to the steeper SS of forward V_g sweep. However, we carefully consider that these results cannot be necessarily attributed to the NLD effect and polarization switching. Different SS along V_g sweep direction can be explained by the different of amount of charge injection at positive and negative V_g. Furthermore, there is a possibility that noise from random telegraph noise (RTN) or measurement setup can be another reason for steeper SS than MISFET. In this experiments, by using AFE:HZO capacitor, the use of the FE nonlinearity within sub-V_{th} region was successfully demonstrated for the first time. However, significant steep SS was not observed

due to small capacitance of depletion layer.

Fig. 5.21 shows the characteristics of MFMIS-FET with Zr ratio of 100% and AR=1:32, in which monitored I_g during the I_d-V_g measurement was also plotted. In MFMIS-FETs, I_d-V_g characteristics (top) had anti-clockwise hysteresis which is attributed to the hysteresis P-V characteristic of AFE:HZO. In MFMIS-FETs, monitored gate current (bottom) had two current peaks which are attributed to the polarization switching of AFE:HZO. In forward V_g sweep, first gate current peak appears near V_g=-3.5V and second gate current peak near V_g=2V. However, in the extended I_g-V_g data of MFMIS-FET (bottom), we found the second current peak was suppressed and split along V_g=2.5-3V due to the small capacitance of depletion layer, in which transistor enters sub-V_{th} from turn-off state.

Fig. 5.22 shows the extracted SS-I_d characteristics of MFMIS-FET with Zr ratio of 100% and AR=1:32 from the measured I_d-V_g characteristics in Fig. 5.21. The results are as follows: (1) The typical SS value in MFMIS-FET was not significantly steep as 60mV/decade. (2) SS values of forward V_g sweep had lower SS value than the backward V_g sweep. (3) Additionally, some SS points in MFMIS-FET had steeper SS value than MISFET. From these results, there is a possibility that the NLD effect contributed to the steeper SS of forward V_g sweep. Especially, regarding the result of (2), larger I_g peak was observed in the forward V_g sweep shown in Fig. 5.21. However, we carefully consider that these results cannot be necessarily attributed to the NLD effect and polarization switching. Different SS along V_g sweep direction can be explained by the different of amount of charge injection at positive and negative V_g. Furthermore, there is a possibility that noise from random telegraph noise (RTN) or measurement setup can be another reason for steeper SS than 60mV/decade. In this experiments, by using AFE:HZO capacitor, the use of the FE nonlinearity within sub-V_{th} region was successfully demonstrated for the first time. However, even with 100%-Zr ratio

HZO and AR=1:32, significant steep SS was not observed due to the small capacitance of depletion layer of Si.

It is worth to note that, suppressed and split I_g observed in our experiments (Figs. 5.18-5.21) were very similar to the I_g data in an early experimental demonstration of steep SS in MFMIS-FETs reported by A. M. Ionescu *et al.* in 2010 (see Figs. 5 and 6 in Ref. 30). Furthermore, A. M. Ionescu *et al.* has shown the existence of negative differential capacitance (NDC) region near P=0μC/cm^2 in the P-V curve of FE (see a Fig. 8 in Ref. 30). In Ref. 30, the NDC region is strongly related with voltage amplification and steep SS. Based on these results, our re-interpretation is that, physical origin of steep SS and NDC, clearly demonstrated in Ref. 30, can be attributed to the "polarization switching" as we expected within NLD model (Fig. 5.14). However, the physical origin of steep SS and NDC were not clearly addressed in Ref. 30. We believe that experimentally obtained results in this chapter and Ref. 30 can be an evidence that, part of recent experimental demonstrations of steep SS in FeFETs can be attributed (and explained) to the "polarization switching (Fig. 5.13)" as an physical origin.

Above discussions are based on the experimental results from our MFMIS structured FeFETs. Then, above discussions can be applied to MFIS-FETs? We consider that part of these can be applied to the MFIS structure, because our devices were long channel (L_g=W_g=100μm) and maximum V_d was not very high as 1V. With the long channel devices and not very high V_d, electric field distribution within FE along channel direction is not very significant, therefore voltage division and charge through nonlinear series capacitors (C_{fe}−C_{ox}−C_{dep}) of MFIS structure is not very different from that of MFMIS structure.

5.4.6 Summary

We experimentally explored steep SS in MFMIS-FETs based on the NLD model. Unlike the NC model [1], we could overcome the issue of charge injection within the NLD model [6] by using AFE:HZO.

With AFE:HZO as a gate insulator, for the first time, we successfully demonstrated the "polarization switching" of FE within sub-V_{th} region of Si. There is a possibility that the nonlinearity of FE layer induced by polarization switching impacted on the device characteristics as we designed and expected.

In our experiments, for the first time, we observed that polarization switching was suppressed in sub-V_{th} region due to the small capacitance of depletion layer. This indicates that the small capacitance of depletion layer can be an obstacle for the steep SS in FeFET using polarization switching. It is considered that a precise and experimentally calibrated device model can be helpful for further experimental exploration of steep SS in FeFET using polarization switching [6].

5.5 Steep Subthreshold Slope Using Polarization Switching and Charge Injection

So far, in our experimental exploration of steep SS in FeFET, we have investigated the MFMIS-FETs with FE:HZO (chapter 5.3) or AFE:HZO (chapter 5.4). It has been revealed that, not as NC model [1], "polarization switching in hysteresis P-V curve" and "charge injection" significantly impact on the device characteristics in real FeFETs as illustrated in Fig. 5.1 (chapter 5.3). Furthermore, following an idea of NLD-FET [6], we showed an experimental possibility that, the "polarization switching (Fig. 5.13)" can be an physical origin of the steep SS in FeFETs (chapter 5.4). However, NLD-FET is under a difficulty to obtain significant steep SS due to the "capacitance mismatching" within sub-V_{th}.

In this chapter, we would like to describe our interesting observation that, when above two very important physics ("polarization switching" and "charge injection" in Fig. 5.1) in FeFETs collaborate, it is possible to overcome an issue of "capacitance mismatching" and realize significant steep SS [40]. On our way of experimental exploration of the steep SS in FeFET with FE:HZO, when MISFET has high gate leakage current, we observed the steep SS < 60mV/decade through two decades of drain current. The results and discussions are described below.

In this chapter, as illustrated in previous chapters, monitored gate current (I_g) offered us very important information to understand the device characteristics of FeFET, because we could trace the polarization switching in FE:HZO from the monitored I_g.

5.5.1 Device Structure

Here, we fabricated FeFET with FE:HZO whose gate stack structure is MFMIS as illustrated in previous chapters. FD-SOI was used in this fabrication. Thickness of SOI and BOX were 80nm and 200nm, respectively. Gate length (L_g) and width (W_g) were 50μm and 100μm, respectively. FE:HZO with Zr ratio of 30% was used. Thickness of FE:HZO was fixed to 10nm. As a gate insulator for MISFET, thermal SiO_2 (4.5 nm) was used. To divide large voltage to FE layer, area of top gate electrode was designed smaller than the channel size ($L_g \times W_g$). A typical diameter of top gate electrode was 20μm. The area ratio between top gate electrode and MIS gate channel was 1:16.

5.5.2 Baseline MISFET and MFM Capacitor

First, we characterized MFM capacitor and baseline MISFET separately. Fig. 5.23 shows I_d-V_g characteristic and monitored I_g of MISFET, in which fine transfer characteristics were

confirmed. Please note that the gate leakage of MISFET is high. We are not very clear why this chip had large gate leakage with 4.5nm-thick SiO_2 as gate insulator, however, there is a possibility that mesa structure of FD-SOI can be a reason. Drain current at $V_g < 0$ is considered to flow to gate because I_d and I_g at $V_g < 0$ have same level. The typical SS (SS9) value was 81mV/decade.

Fig. 5.24 shows the P-V characteristics and transient current characteristics of FE:HZO capacitor. Very clean FE characteristics were confirmed in the FE:HZO capacitor.

5.5.3 Experimental Demonstration of Steep SS of Sub-60mV/decade

Then, we characterized MFMIS-FETs. By testing several measurement conditions, with the V_g sweep of V_g=+2V→-2V→+2V, we observed the steep SS < 60mV/decade and minimum SS of 20mV/decade as shown in I_d-V_g characteristic (top) of Fig. 5.25. In Fig. 5.25, clockwise hysteresis was observed due to the large charge injection. Fig. 5.25 shows SS-I_d data (bottom) extracted from I_d-V_g characteristics. Steep SS was observed with forward V_g sweep only.

In Fig. 5.26, the results of Fig. 5.25 were enlarged to clearly show the impacts of steep SS data, in which the results of only forward V_g sweep and V_d=1V in Fig. 5.25 were re-plotted. As clearly shown in Fig. 5.26, compared to the MISFET within MFMIS-FET, drive current was enhanced by 10× at the fixed I_{off} and at the fixed overdrive voltage of 0.5V. Steep SS < 60mV/decade can be achieved in almost 2 decades of drain current. Steeper SS than MISFET can be achieved in almost 4 decades of drain current. We will discuss the physical mechanism after describing the following experimental results.

Such steep SS can be mostly seen with MISFET characteristics in Fig. 5.23, which has gate current in on- and off-state. Please note that gate current is equal to drain current in

off-state. These large gate current results in large charge injection to the internal floating gate, therefore clockwise hysteresis induced by charge injection was seen. However, as already illustrated in previous chapters, with very low gate leakage in MISFET, MFMIS-FET does not show significant steep SS and, instead, shows memory window. Therefore, the physical origin of steep SS in this chapter can be attributed to the dynamics of "polarization switching (spontaneous polarization) of FE:HZO" and "charge injection (charge transfer)". Typical measurement sequence here was, (1) initialize polarization state at positive V_g unless mentioned, (2) sweep V_g in negative direction, and then (3) switch V_g sweep to positive direction.

5.5.4 Driving Force for Steep SS by Polarization Switching of FE:HZO

Fig. 5.27 shows I_d-V_g characteristic of MFMIS-FET by sweeping V_g= +3V → -3V → +3V, in which monitored Ig was also plotted. In Fig. 5.27, there are peaks in I_d and I_g at the same V_g range. As already explained in chapter 5.3, physical origin of these current peaks can be attributed to the "polarization switching" of FE:HZO and consequent "NDC". I_g had current peaks in both of positive and negative gate bias region owing to the polarization switching in FE:HZO, which indicates that MFM capacitor traced major loop of P-V curve. Because of charge injection, I_d-V_g characteristic showed clockwise hysteresis.

Figs. 5.28 and 5.29 show how the subthreshold characteristics and SS are related to the V_g sweep range. Fig. 5.28 shows the measured I_d-V_g characteristics of MFMIS-FET with V_g sweep of V_g= +2V → -3V → +2V. In Fig. 5.28, we observed driving force to turn on the transistor from V_g=-2V to V_g=-2.5V. Fig. 5.29 shows the measured I_d-V_g characteristics of MFMIS-FET with V_g sweep of V_g= +2V → -2V → +2V. In Fig. 5.29, when I_g peak (polarization switching) appears and V_g switches at V_g=-2V at the same time, then the steep

SS was clearly observed as shown in Fig. 5.29. Based on these results, steep SS is considered to be strongly related with the event of “polarization switching”. Because the baseline MISFET is inversion-mode transistor, the drain current after the appearance of steep SS in Fig. 5.29 is not the current in accumulate region. In other words, in Figs. 5.28 and 5.29, there indeed exists the driving force to turn on the transistor in V_g range with the event of “polarization switching”. This indicates that surface potential was amplified in that V_g range (voltage amplification) owing to the driving force induced by “polarization switching” of FE:HZO. Then, does this mean that “polarization switching” is enough for the physical origin of steep SS in this device? The “charge injection” and its amount have to be additionally considered because our MIS device had large gate leakage. Hereafter, we would like to explain the steep SS phenomena by the typical voltage divider of V_g and “charges injection” into internal gate, promoted by “polarization switching” of FE:HZO.

5.5.5 Driving Force for Steep SS by Charge Injection into Internal Gate

Fig. 5.30 shows V_d dependence of I_d-V_g characteristics (top) and extracted SS-I_d data (bottom) of the MFMIS-FET, in which V_g switches at V_g=-2V. Here, for I_d-V_g characteristics and extracted SS-I_d data, the results of only positive V_g sweep were shown, while I_g-V_g characteristics are results of double V_g sweeps. In top figure of Fig. 5.30, as V_d increases, I_g peak at negative V_g shifted to the direction of lower $|V_g|$. This can be explained by considering that, at V_g=+2V, the smaller amount of negative charge can be injected into internal gate with higher the V_d. These decreased negative charge injection into internal gate at positive V_g can result in the FE polarization easy to switch at negative V_g. As a result, FE polarization switches with lower $|V_g|$ with large V_d. In the top figure of Fig. 5.30, as V_d increases, V_{th} of I_d-V_g characteristics of forward V_g sweep shifted to the negative V_g direction. This is a kind of

drain-induced-barrier-lowering (DIBL), however different from the electrostatic DIBL of conventional MISFET due to large charge injection into internal gate at V_g=-2V. This can be explained by considering that, at V_g=-2V, the larger amount of "effective" positive charge is injected into internal gate with higher V_d. These large positive charge injection results in transistor easy to turn on. As a result, transistor turns on with higher $|V_g|$ with large V_d as shown in top figure of Fig. 5.30. Furthermore, in bottom figure of Fig. 5.30, SS-I_d characteristics illustrate that the steeper SS can be achieved with higher V_d. With varied V_d, the conditions of both of "polarization switching" and "charge injection" are changed as shown in the top figure of Fig. 5.30. These different conditions of both of "polarization switching" and "charge injection" with varied V_d are considered to be the reason for the V_d dependence of the SS value. This will be discussed later in Fig. 5.32.

5.5.6 Driving Force for Steep SS by Polarization Switching and Charge Injection

Fig. 5.31 shows V_g step dependences of I_d-V_g characteristics (top) and extracted SS-Id data (bottom) of the MFMIS-FET. Here, I_g-V_g characteristics and monitored I_g (top) are the results of double V_g sweeps, whereas the extracted SS-I_d data (bottom) are the results of only forward V_g sweep. In Fig.5.31, in the case of V_g= +2V → -2V → +2V, steeper SS can be observed with shorter V_g step (longer measurement time). With longer measurement time, larger amount of charge is allowed to be injected to the internal gate during V_g sweep. From Fig. 5.31, it is considered that the amount of charge injection at V_g=-2V strongly impacts on the steep SS. Then, it should be answered that, in our MFMIS-FETs, is there any contribution of "polarization switching" of FE:HZO on steep SS?

We believe that this can be answered from the results of the V_g= +3V → -3V → +3V (green lines) shown in Fig. 5.31. In Fig. 5.31, it is worth to note that steep SS was not

observed at forward V_g sweep in the case of V_g= +3V → -3V → +3V, even though larger charge can be injected into internal gate at V_g=-3V. The non-steep SS can be explained based on the monitored I_g in Fig. 5.31. Because the "polarization switching" process of FE had already finished before V_g reached -3V, voltage amplification cannot be realized with forward V_g sweep in MFMIS-FET . In other words, when transistor enters sub-V_{th} region with forward V_g sweep at V_g=-3V, charge state of FE:HZO was in the non-switching paraelectric region as typical dielectric material.

As shown in Fig. 5.31, in our experiments, without using polarization switching, steep SS and voltage amplification cannot be observed. This indeed indicates that "polarization switching" of FE:HZO is directly involved in our observation of steep SS phenomena, assisted by "charge injection" effect. The steep SS in our MFMIS-FETs with FE:HZO is considered to be the result of the collaboration of the polarization switching and the charge injection.

5.5.7 Discussions on Physical Origin of Steep SS in This Work

Based on the results and discussions above, we would like to discuss a possible physical origin and mechanism of the observed steep SS in our devices. Fig. 5.32 (a) shows the band diagram before the polarization switching at $V_g < 0$ in off-state. In Fig. 5.32 (b), (1) once "polarization switching" occurs, (In this work, we can trace at which V_g range "polarization switching" occurs from monitored the I_g at top gate as shown in Fig. 5.27) (2) negative charges are induced on MIS gate side to balance charge inside the internal gate, which tends to turn off MISFET strongly. Here, when $|V_g|$ is large and V_d is also large enough, (3) electrons escape from internal gate to channel by MIS gate current and consequently more positive charges exist in the internal gate. (From the monitored I_g at top gate, we cannot trace

the “charge injection”. Here, the effect of “charge injection” was introduced as a possible explanation for the steep SS at V_g=-2V.) Here, both of “polarization switching” and “charge injection” are considered to be a driving force to turn on transistor as described in Figs. 5.28 and 5.29. Then, in Fig. 5.32(c), when V_g switches to positive direction, (4) steep SS appears (Figs. 5.29-5.31) due to the typical voltage divider of V_g and positive charge accumulation in internal gate which seems to have long transient time in our measurement time period. The steep SS can be attributed to the voltage amplification: voltage of internal gate (dV_{int}) appears to be larger than gate voltage (dV_g) applied on the top gate ($dV_{int} > dV_g$). This can be interpreted as “effective NC effect” assisted by charge injection as discussed in Ref. 16. Our careful consideration is that, the physical origin of the “effective NC effect” in our experiments can be attributed to the collaboration and coexistence of the “polarization switching” and “charge transfer through gate stack [16]”.

It is considered that, part of recent reports on the steep SS in FeFETs by other groups can be attributed to the “polarization switching assisted by charge injection” as a possible physical origin of steep SS in FeFETs. However, there have been few studies which discuss on the physical effects of charge transfer through gate stack [16,17,18] to address the physics of NCFETs [16,18]. Therefore, it is considered that our experimental work can be valuable information for future research on NCFETs.

In this work, above discussions are based on the experimental results from our MFMIS structured FeFETs. The issue of large charge injection into internal gate is incurred by the existence of internal gate and gate leaky MISFET in our MFMIS-type FeFETs. Then, above discussions can be applied to MFIS-FETs? Our consideration is that, even under MFIS structure without internal gate, when interfacial dielectric is leaky, large amount of charge can be injected to the interfacial defect state of ferroelectric/dielectric (FE/DE) and/or boarder trap

state of FE by a process of charge trapping as discussed in Ref. 13. Therefore, our discussion in this chapter can be partially applied to the MFIS structure. However, not as MFMIS-FETs with internal metal gate, amount of charge injection is strongly depends on the density of trap state of FE/DE in MFIS-FETs, therefore further experimental investigations based on the MFIS-FETs can be valuable.

5.5.8 Summary

In this chapter, the steep SS in FE:HZO-based MFMIS-FETs was demonstrated with the gate leaky MISFET. Minimum SS value was 20mV/decade. SS lower than 60mV/decade was over 2 decades, SS lower than MISFET over 4 decades of drain current. The steep SS can be attributed to the voltage amplification, which is induced by the collaboration of the polarization switching of FE:HZO and charge injection in our devices. It is considered that, in our experiments, “polarization switching” and “charge injection” cooperate to generate the characteristics of steep SS. There is a possibility that physical origin of recent many reports on experimental steep SS in FeFETs can be partially attributed to “polarization switching” assisted by “charge injection”. However, there have been few studies which discuss on the physical effects of charge transfer through gate stack [16,17,18] to clarify the physics of NCFETs [16,18]. Therefore it is considered that our experimental work contains valuable information for future research on NCFETs.

5.6 Summary

We fabricated and characterized MFMIS-FETs (Fig. 5.1) by integrating HZO capacitors on conventional MISFETs both of which are fine capacitor and transistor.

First, based on the NC model, bulk NCFET was designed and characterized. In our

experiments, steep SS was not observed as expected by the NC model. The non-steep SS can be attributed to the “charge injection” into the internal gate.

Second, we experimentally explored the steep SS in MFMIS-FETs based on the NLD model and “polarization switching”. Unlike the NC model, with the NLD model, we could overcome the issue of “charge injection” by using AFE:HZO. With AFE:HZO-based gate insulator, for the first time, we successfully demonstrated the “polarization switching” of FE:HZO within sub-V_{th} region. Additionally, we observed that “polarization switching” can be suppressed in sub-V_{th} region due to the small capacitance of depletion layer, for the first time.

Third, in MFMIS-FETs with gate leaky MISFETs, we observed the steep SS experimentally. The minimum SS value was 20mV/decade and SS < 60mV/decade was observed for 2 decades of drain current. Physical origin of steep SS was carefully discussed. Steep SS is considered to be the result of the voltage amplification which can be attributed to cooperation of “polarization switching” and “charge injection”.

Throughout our experimental explorations of steep SS, we were able to clearly address that how the “charge transfer” through gate stack significantly impacts on the device characteristics of MFMIS structured FeFET. The importance of “charge transfer” has not been sufficiently considered or addressed in NCFET field. We believe that careful considerations on the “charge transfer” (both of effect of charge injection and monitoring gate current) are strongly required for research on NCFET. Especially, we clearly addressed that monitoring gate current is very effective way to understand the device characteristics of FeFET. From the monitored gate current, we could trace the “polarization switching” in FE:HZO. Considering charge transfer through gate stack (both of effect of charge injection and monitoring gate current) will indeed shed light on the further researches on NCFETs.

References

[1] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices", Nano Letter, Vol. 8, No. 2, 2008, pp 405–410.

[2] K. Jang, T. Saraya, M. Kobayashi, and T. Hiramoto, "On gate stack scalability of double-gate negative-capacitance FET with ferroelectric HfO_2 for energy efficient sub-0.2 V operation", Japanese Journal of Applied Physics, 57, 024201, 2018.

[3] K. Jang, T. Saraya, M. Kobayashi, and T. Hiramoto, "I_{on}/I_{off} ratio enhancement and scalability of gate-all-around nanowire negative-capacitance FET with ferroelectric HfO_2", Solid-State Electronics, Vol. 136, pp. 60-67, 2017.

[4] C. M. Krowne, S. W. Kirchoefer, W. Chang, J. M. Pond, and L. M. B. Alldredge, "Examination of the Possibility of Negative Capacitance Using Ferroelectric Materials in Solid State Electronic Devices", Nano Letters, vol. 11, no. 3, pp. 988-992, 2011.

[5] S. J. Song, Y. J. Kim, M. H. Park, Y. H. Lee, H. J. Kim, T. Moon, K. D. Kim, J.-H. Choi, Z. Chen, A. Jiang, and C. S. Hwang, "Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors", Scientific Reports, vol. 6, 20825, 2016.

[6] H. Ota, S. Migita, K. Fukuda, and A. Thorium, "Steep subthreshold swing and energy efficiency in MOSFETs utilizing nonlinear gate dielectric insulators", Japanese Journal of Applied Physics, 55, 04ED02, 2016.

[7] J. Müller, T. S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, "Ferroelectricity in Simple Binary ZrO_2 and HfO_2", Nano Letters, vol. 12, no. 8, pp. 4318-4323, 2012.

[8] M. A. Wahab and M. A. Alam, "A Verilog-A Compact Model for Negative Capacitance FET", version 1.1.0, nanoHUB, 2016. (https://nanohub.org/publications/95/5)

[9] C.-I. Lin, A. I. Khan, S. Salahuddin and C. Hu., "Effect of the variation of Ferroelectric Properties on Negative Capacitance FET Characteristics", IEEE Transactions on Electron Devices, vol. 63, no. 5, pp. 2197, 2016.

[10] E. Yurchuck, J. Muller, S. Muller, J. Paul, M. Pesic, R. Bentum, U. Schroeder, and T. Mikolajick, "Charge-Trapping Phenomena in HfO_2-based FeFET-Type Nonvolatile Memories", IEEE Transactions on Electron Devices, Vol. 63, No. 9, Sep. 2016, pp. 3501-3507.

[11] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. D. Leeuw, "High-performance solution-processed polymer ferroelectric field-effect transistors", Nature Materials, Vol. 4, Mar. 2005, pp. 243-248.

[12] J. Jo and C. Shin, "Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/decade Switching", IEEE Electron Device Letter, Vol. 37, No. 3, 2016, pp. 245-248.

[13] Y. J. Kim, M. H. Park, Y. H. Lee, H. J. Kim, W. Jeon, T. Moon, K. D. Kim, D. S. Jeong, H. Yamada, and C. S. Hwang, "Frustration of Negative Capacitance in $Al_2O_3/BaTiO_3$ Bilayer Structure", Scientific Reports, 6:19039, 2016.

[14] A. I. Khan, M. Hoffmann, K. Chatterjee, Z. Lu, R. Xu, C. Serrao, S. Smith, L. W. Martin, C. C. Hu, R. Ramesh, S. Salahuddin, "Differential voltage amplification from ferroelectric negative capacitance", arXiv:1709.10451, submitted on 29 Sep. 2017.

[15] C. M. Krowne, "Evaluation of the differential capacitance for ferroelectric materials using either charge-based or energy-based expressions", Journal of Advanced Dielectrics, vol. 4, no. 33, 1450024, 2014.

[16] H. W. Then, S. Dasgupta, M. Radosavljevic, L. Chow, B. Chu-Kung, G. Dewey, S. Gardner, X. Gao, J. Kavalieros, N. Mukherjee, M. Metz, M. Oliver, R. Pillarisetty, V. Rao, S. H. Sung, G. Yang, and R. Chau, "Experimental Observation and Physics of "Negative" Capacitance and Steeper than 40mV/decade Subthreshold Swing in $Al_{0.83}In_{0.17}N/AlN/GaN$ MOS-HEMT on SiC Substrate", IEEE International Electron Device Meeting 2013, pp. 691-694

[17] Y.-C. Chiu, C.-H. Cheng, C.-Y. Chang, M.-H. Lee, H.-H. Hsu, and S.-S. Yen, "Low Power 1T DRAM/NVM Versatile Memory Featuring Steep Sub-60-mV/decade Operation, Fast 20-nm Speed, and Robust 80°C-Extrapolated 10^{16} Endurance", VLSI symposium, T185, 2015.

[18] P. Sharma K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, and S. Datta, VLSI Tech. Symp. Dig., 2017, T12-2.

[19] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, Y. Taur, "Modeling and Design of Ferroelectric MOSFETs", IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011, pp. 2401-2405.

[20] C. A. Desoer and E. S. Kuh, "Basic Circuit Theory", McGraw-Hill College, US, *Chapter 2* and *Chapter 19*, 1969.

[21] L. D. Landau and E. M. Lifshitz, "Phase Transitions of the Second Kind and Critical Phenomena", in Statistical Physics, 3rd ed., part 1, vol. 5 (Course of Theoretical Physics), ch. 14, pp. 446-516, Butterworth-Heinemann, 1980.

[22] H. Moriwake, "Ferroelectric Material Research Using First-principles Calculations−Ferroelectricity in $AgNbO_3$−", Journal of the Japan Society of Powder and Powder Metallurgy, Vol. 61, No. 8, pp. 387-391, 2014.：森分　博紀, "第一原理計算の強誘電材料への適用−$AgNbO_3$ における強誘電性の起源の検討−", Journal of the Japan Society of Powder and Powder Metallurgy, Vol. 61, No. 8, pp. 387-391, 2014.

[23] H. Moriwake, C. A. J. Fisher, A. Kuwabara, and T. Hashimoto, "Anisotropic Permittivity of Tetragonal $BaTiO_3$: A First-Principles Study", Japanese Journal of Applied Physics, 50, (2011), 09NE02.

[24] H. Moriwake, A. Kuwabara, C. A. J. Fisher, H. Taniguchi, M. Itoh, and I. Tanaka,

"First-principles calculations of lattice dynamics in $CdTiO_3$ and $CaTiO_3$: Phase stability and ferroelectricity", Physical Review B, 84, 104114 (2011).

[25] M. Stengel, N. A. Spaldin, and D. Vanderbilt, "Electric displacement as the fundamental variable in electronic-structure calculations", Nature physics, Vol. 5, April, 2009, pp. 304-308.

[26] M. Stengel, D. Vanderbilt, and N. A. Spaldin, "Enhancement of ferroelectricity at metal-oxide interfaces", Nature materials, Vol. 8, May, 2009, pp. 392-397

[27] P. Zubko, J. C. Wojdeł, M. Hadjimichael, S. Fernandez-Pena, A. Sené, I. Luk'yanchuk, J. Triscone, and J. Íñiguez, "Negative capacitance in multidomain ferroelectric superlattices", Nature, vol. 534, pp. 524-528, 2016.

[28] V. G. Veselago, "The Electrodynamics of Substances with Simultaneously Negative Values of ε and μ", Soviet Physics Uspekhi, Vol. 10, No. 4, pp. 509-514, 1968.

[29] C. W. Chu, F. Chen, J. Shulman, S. Tsui, Y. Y. Xue, W. Wen, and P. Sheng, "A negative dielectric constant in nano-particle materials under an electric field at very low frequencies", Strongly Correlated Electron Materials: Physics and Nanoengineering, Proceedings of the SPIE, Vol. 5932, pp. 139-148 (2005)

[30] A. Rusu, G. A. Salvatore, D. Jiménez, A. M. Ionescu, "Metal-Ferroelectric-Meta-Oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification", in IEDM Tech. Dig., 2010, p. 395.

[31] J. Li, B. Nagaraj, H. Liang, W. Cao, Chi. H. Lee, and R. Ramesh, "Ultrafast polarization switching in thin-film ferroelectrics", Applied Physics Letters, 84, 7, pp. 1174-1176 (2004).

[32] K. Chatterjee, A. J. Rosner, S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors", IEEE Electron Device Letters, vol. 38, no. 9, pp. 1328-1330 (2017).

[33] M. Hoffmann, M. Pešić, K. Chatterjee, A. I. Khan, S. Salahuddin, S. Slesazeck, U. Schoeder, and T. Mikolajick, "Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2", Adv. Funct. Mater. vol. 26, pp. 8643-8649, 2016.

[34] Masaharu Kobayashi, Nozomu Ueyama, Kyungmin Jang, and Toshiro Hiramoto, "Experimental Demonstration of a Nonvolatile SRAM with Ferroelectric HfO_2 Capacitor for Normally-Off Application", Fig. 7, IEEE Journal of the Electron Devices Society, accepted.

[35] A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Pan, R. Ramesh, and S. Salahuddin, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures", Applied Physics Letters, 99, 113501 (2011).

[36] W. Gao, A. Khan, X. Marti, C. Nelson, C. Serrao, J. Ravichandra, R. Ramesh, and S. Salahuddin, "Room-Temperature Negative Capacitance in a Ferroelectric-Dielectric

Superlattice Heterostructure", Nano Letters, 14, pp. 5814-5819 (2014).

[37] J. Jo, W. Y. Choi, J.-D. Park, J. W. Shim, H.-Y. Yu, and C. Shin, "Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices", Nano Letters, 15, pp. 4553-4556 (2015).

[38] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, "Negative capacitance in a ferroelectric capacitor", Nature Materials, vol. 14, pp. 182-186, 2015.

[39] P. Chandra and P. B. Littlewood, "A Landau Primer for Ferroelectrics", Fig. 5: Schematic picture of hysteresis in an idealized ferroelectric, arXiv:cond-mat/0609347, 2006.

[40] K. Jang, M. Kobayashi, and T. Hiramoto, "Sub-60mV/decade subthreshold slope in metal-ferroelectric-metal-insulator-semiconductor field-effect transistor based on polarization switching of ferroelectric $HfZrO_2$ and charge injection into internal gate (temporary)", to be submitted.

[41] S.-M. Jung, T. Saraya, K. Takeuchi, M. Kobayashi, and T. Hiramoto, "V_{th} Self-Adjusting Tri-Gate Nanowire MOSFET for Stability Improvement of SRAM Cell Operating at 0.1V", IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015.

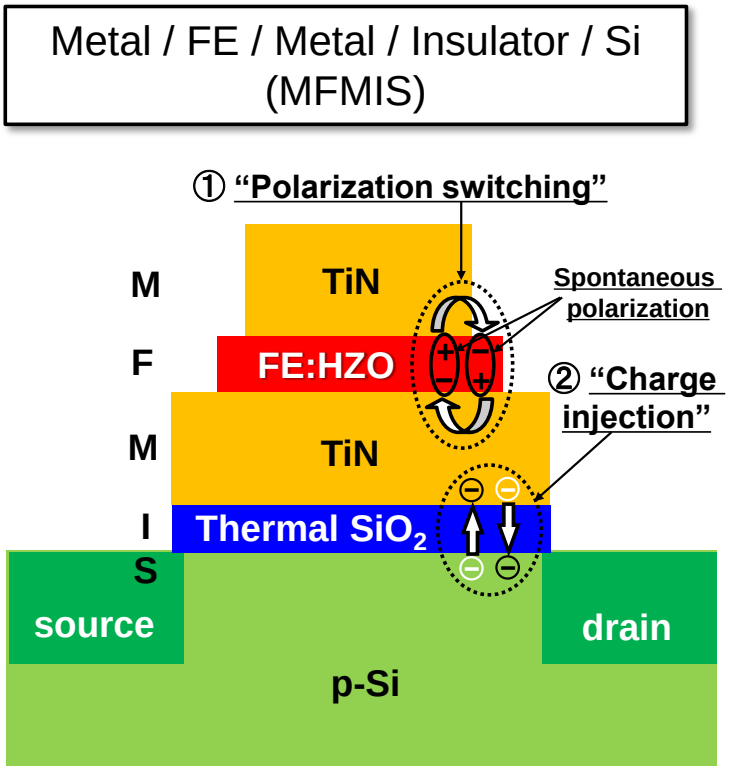


Fig. 5.1. Device structure of metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-type ferroelectric FET fabricated in this work. MFMIS-structured FeFET has internal gate between FE and MIS gate. In this study, we used the MFMIS-FET by focusing on the merits of MFMIS-FET such as MISFET and MFM capacitor can be fabricated and characterized separately. This offers significant advantages for device design and analyses.

In the figure of MFMIS-FET, two important physics of FeFETs in this work are shown: ①Polarization switching and ②Charge injection. Throughout our experiments, these two physics significantly impact on the characteristics of FeFETs, not as NC model [1]. Detailed descriptions can be found in the chapters of 5.3, 5.4, and 5.5. Please note that, in this work, ②Charge injection always indicates the charge transfer between Si channel and internal gate through SiO_2. In other words, charge injection from top gate to internal gate [40] was not considered for the relatively thick FE:HZO insulator than SiO_2.

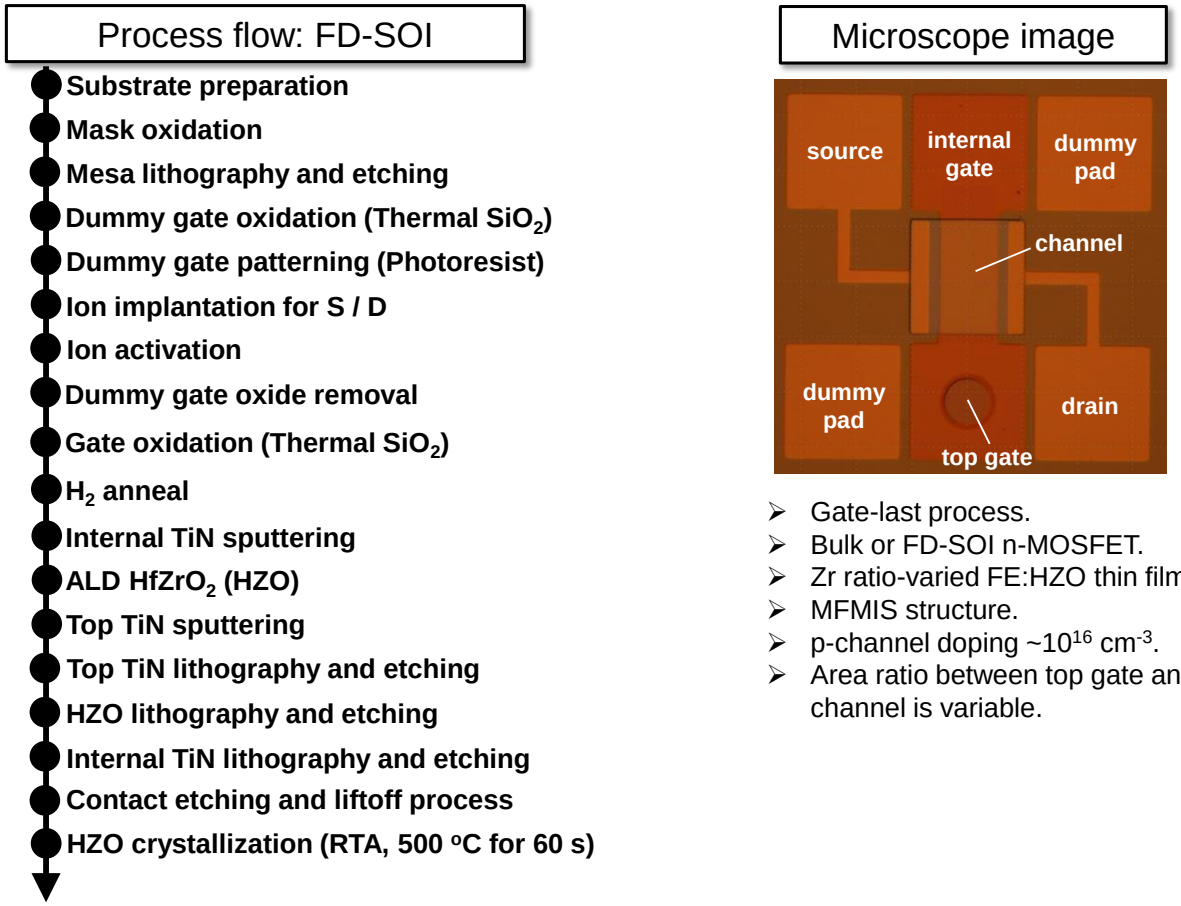


Fig. 5.2. A process flow of FE:HZO-based MFMIS-FET using FD-SOI (left), and microscope top-view image of our device layout (right). In this work, bulk Si-based MFMIS-FET was also fabricated whose process flow is not very different from the above FD-SOI-based MFMIS-FET.

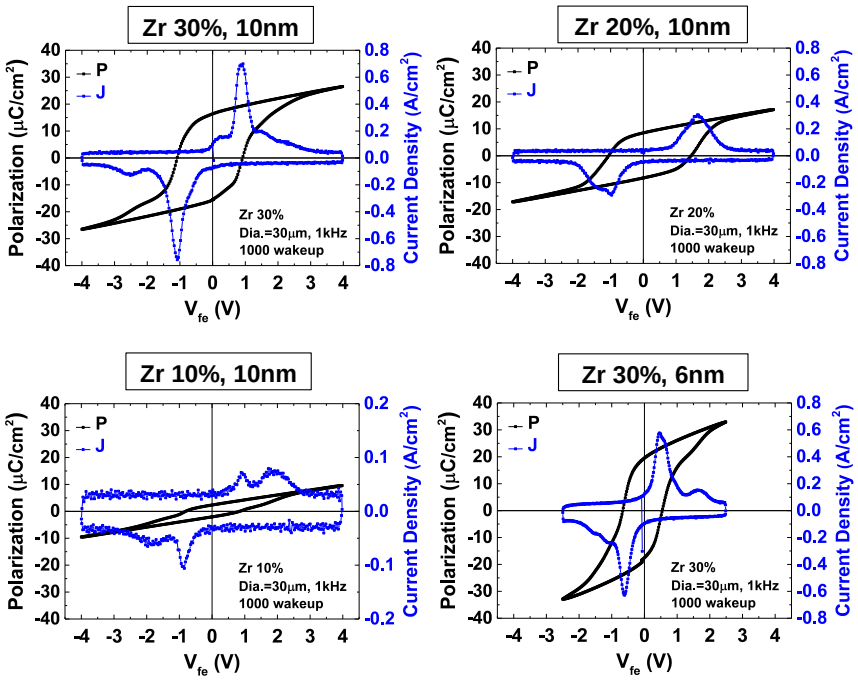


Fig. 5.3. Ferroelectric characteristics of MFM-HZO capacitors with varied Zr ratio of 30%, 20%, and 10% after wake-up (W/U) treatment of 1000 cycles. Typical thickness of FE:HZO was T_{fe}=10nm, and FE:HZO with T_{fe}=6nm was characterized and shown only for Zr ratio of 30%. Black lines show measured P-V curves and blue lines show measured transient current responses. Diameter of circled top gate electrode was 30μm. Measuring frequency was 1kHz.

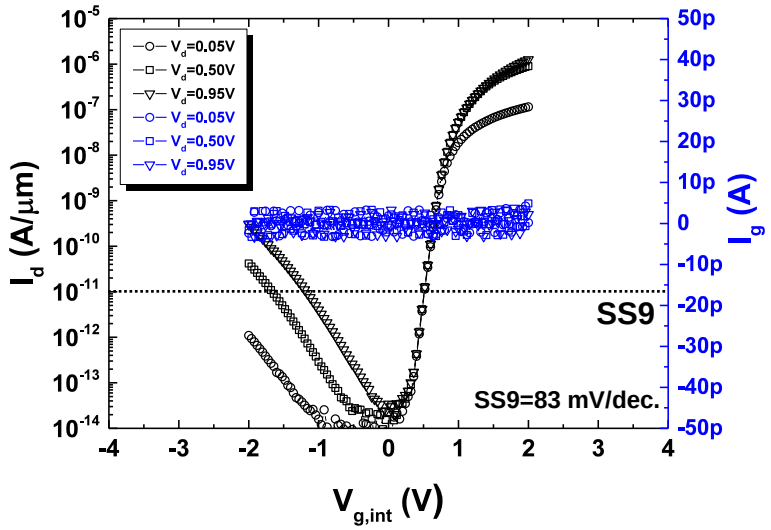


Fig. 5.4. Measured I_d-V_g characteristics of baseline MISFET (L_g=W_g=100μm), in which monitored gate current (I_g) was also plotted. Typical SS value of 83mV/decade was extracted at the drain current level of $I_d = W_g / L_g \times 10^{-9}$ A and V_d=0.05V, defined as SS9 here. At the measured V_g sweep range, monitored I_g was very low as noise level (< 5pA).

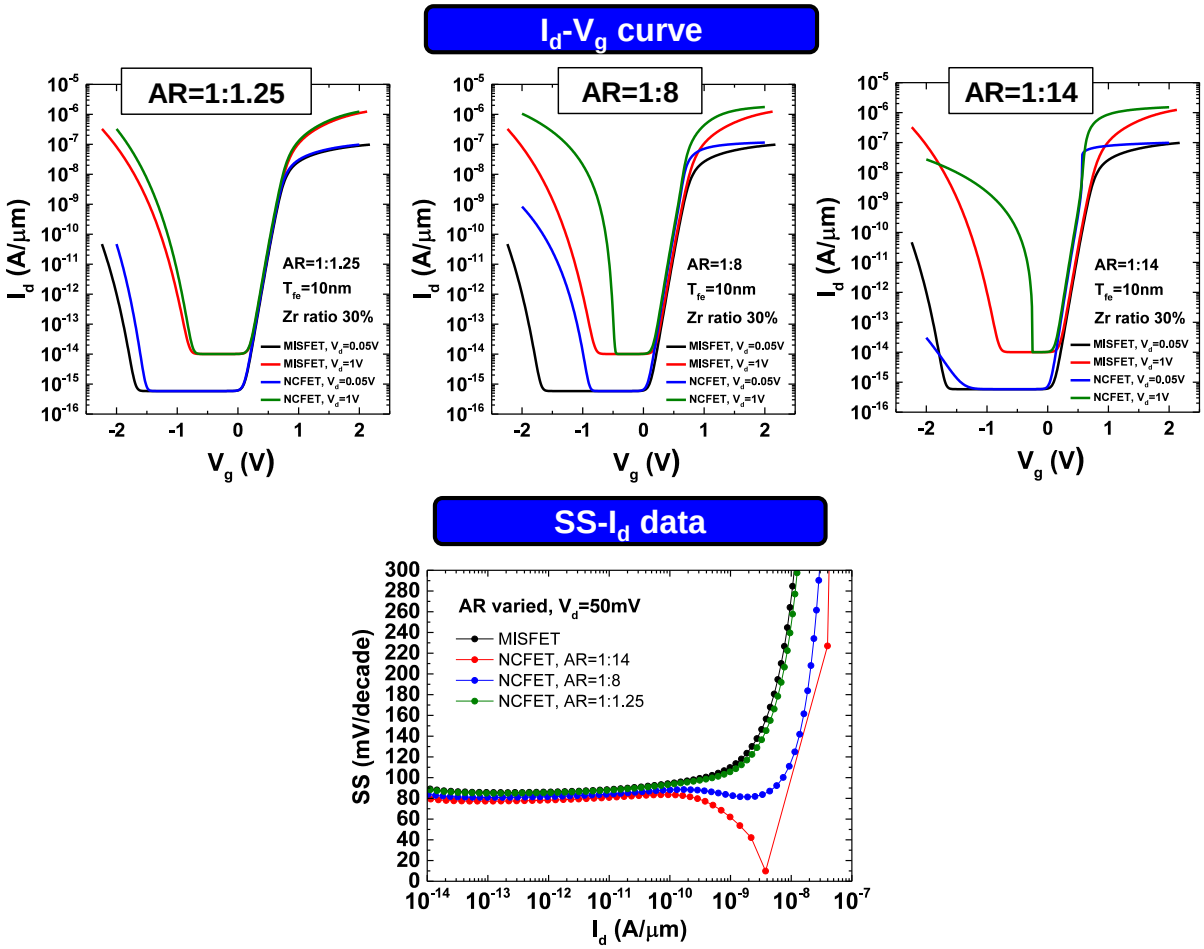


Fig. 5.5. Simulated I_d-V_g characteristics and SS-I_d data of AR-varied NCFETs, in which characteristics of baseline MISFETs were also plotted for comparison. With larger AR, NC effect effectively impacts on the characteristics of NCFET which results in steeper SS.

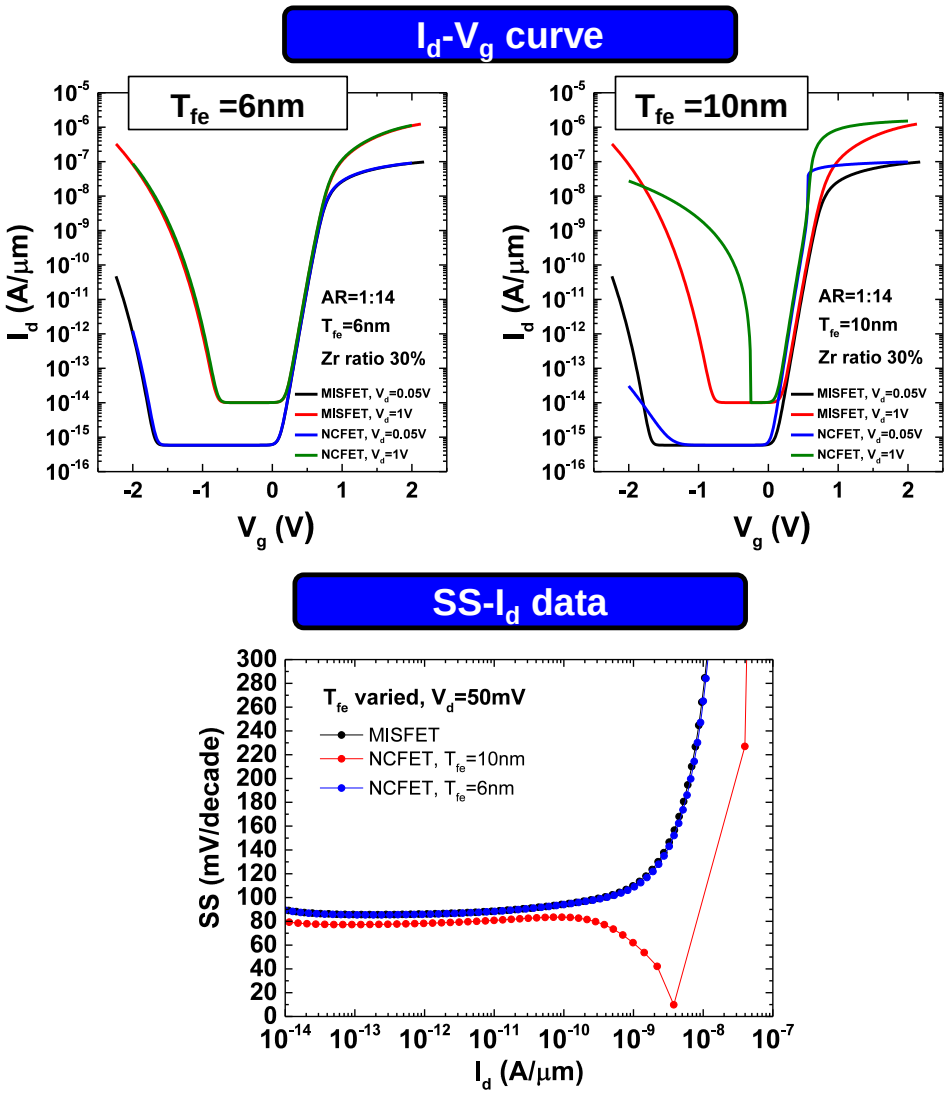


Fig. 5.6. Simulated I_d-V_g characteristics and SS-I_d data of T_{fe}-varied NCFETs, in which characteristics of baseline MISFETs were also plotted for comparison. With thicker T_{fe}, NC effect effectively impacts on the characteristics of NCFET which results in steeper SS.

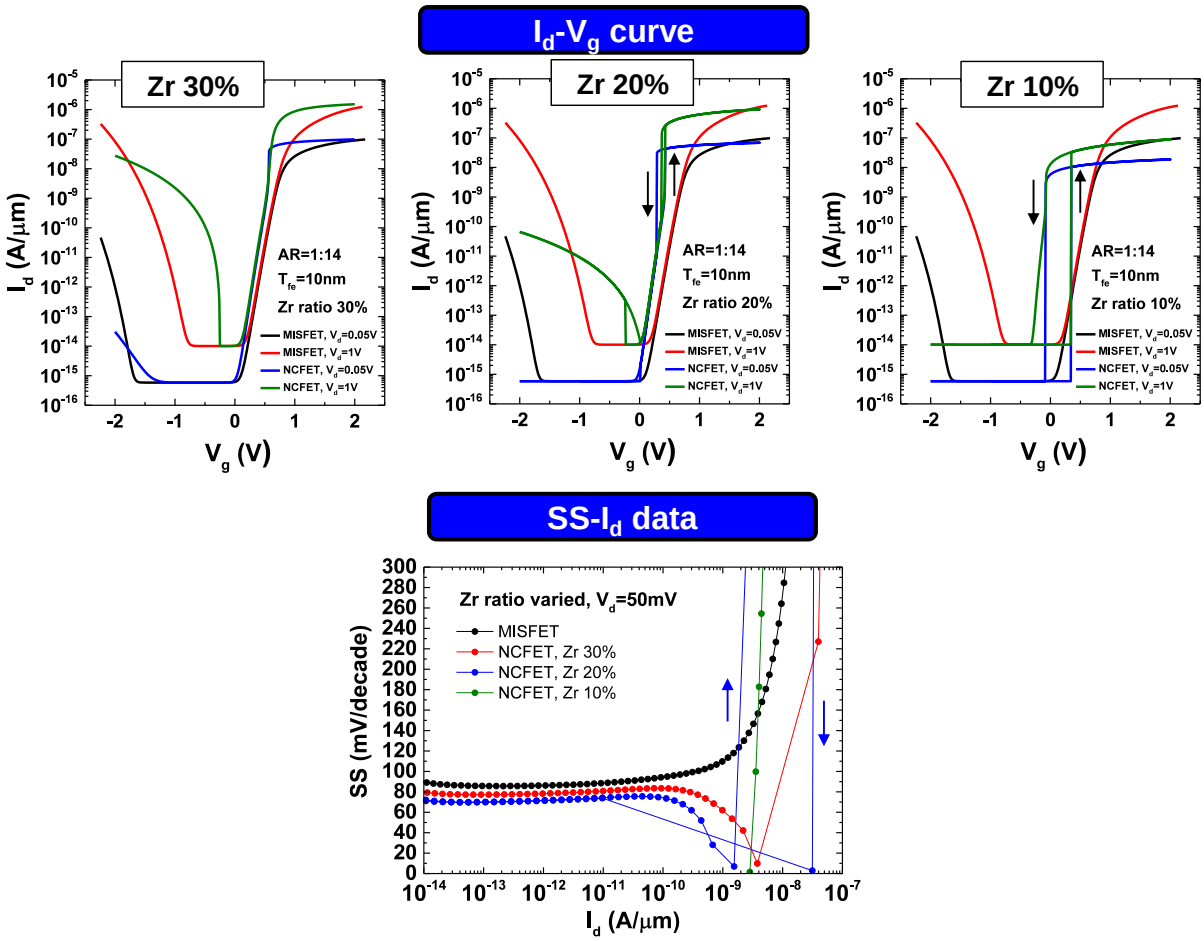


Fig. 5.7. Simulated I_d-V_g characteristics and SS-I_d data of Zr ratio-varied NCFETs, in which characteristics of baseline MISFETs were also plotted for comparison. Here, Landau parameters were extracted from experimental P-V data of Fig. 5.3. With lower Zr ratio and lower P_r, NC effect effectively impacts on the characteristics of NCFET which results in steeper SS.

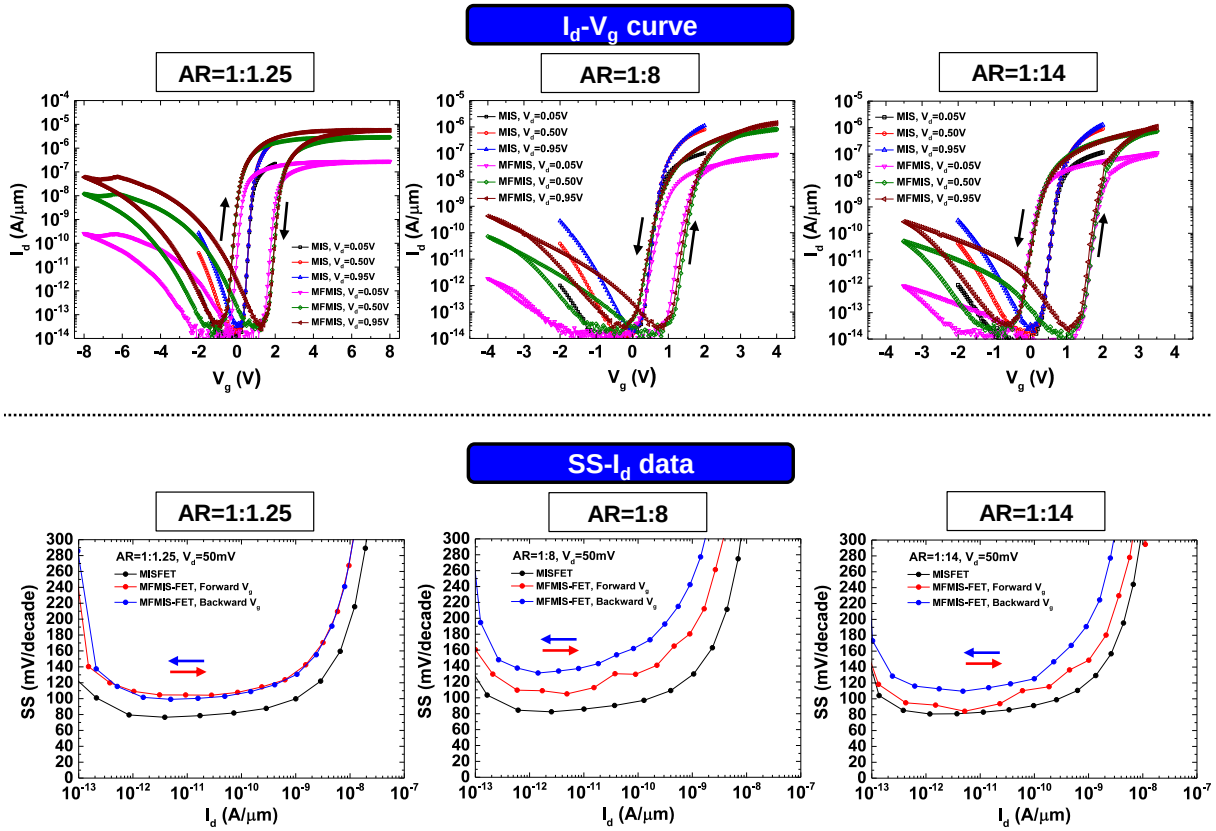


Fig. 5.8. Measured I_d-V_g characteristics and SS-I_d data of AR-varied MFMIS-FETs, in which characteristics of baseline MISFETs were also plotted for comparison. Zr ratio in HZO thin film and T_{fe} were default conditions of 30% and 10nm, respectively. Hysteresis I_d-V_g characteristics and non-steep SS were shown in MFMIS-FETs, which are inconsistent with the simulation results based on the NC model shown in Fig. 5.5.

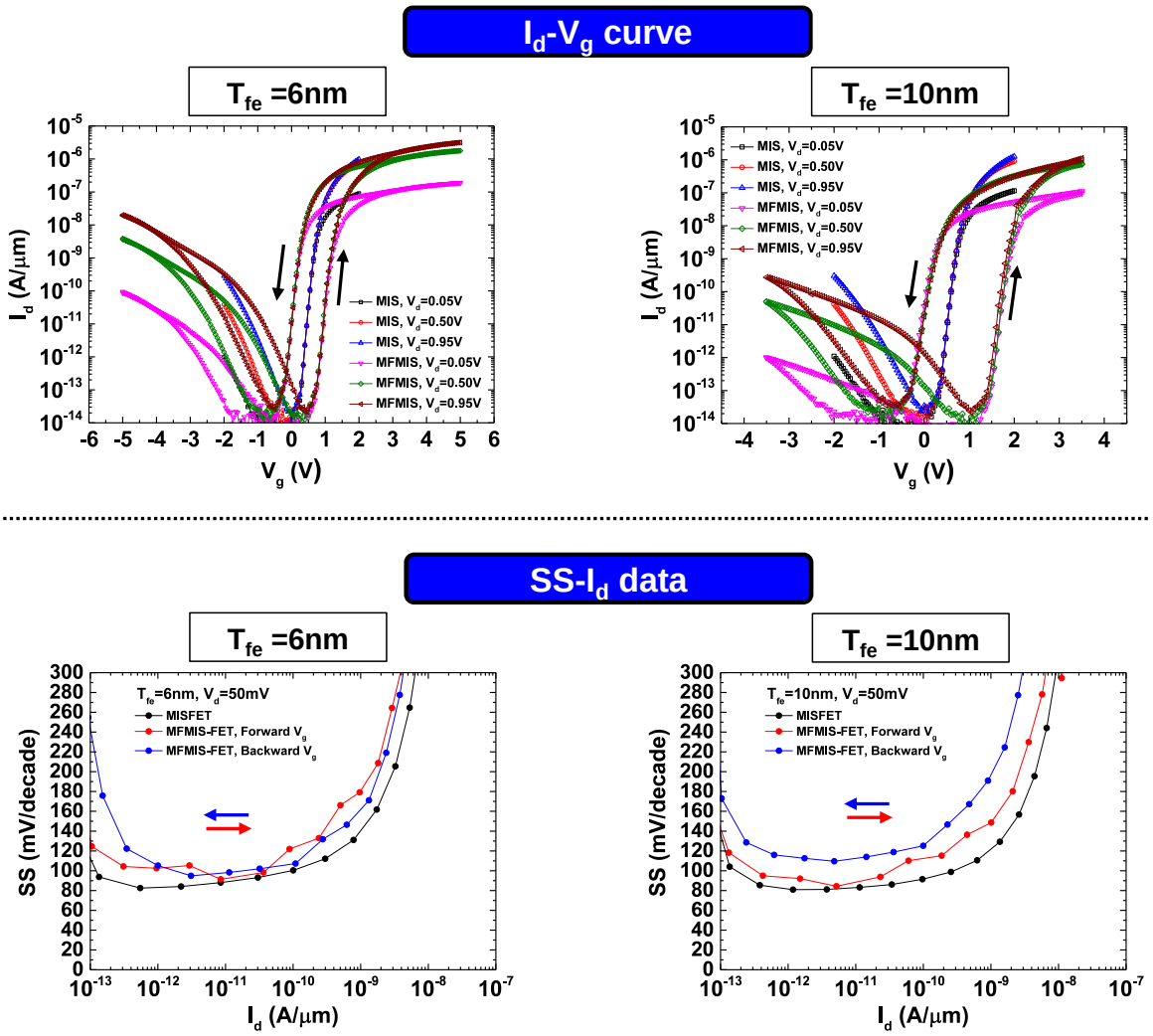


Fig. 5.9. Measured I_d-V_g characteristics and SS-I_d data of T_{fe}-varied MFMIS-FETs, in which characteristics of baseline MISFETs were also plotted for comparison. AR and Zr ratio in HZO thin film were default conditions of 1:14 and 30%, respectively. Hysteresis I_d-V_g characteristics and non-steep SS were shown in MFMIS-FETs, which are inconsistent with the simulation results based on the NC model shown in Fig. 5.6.

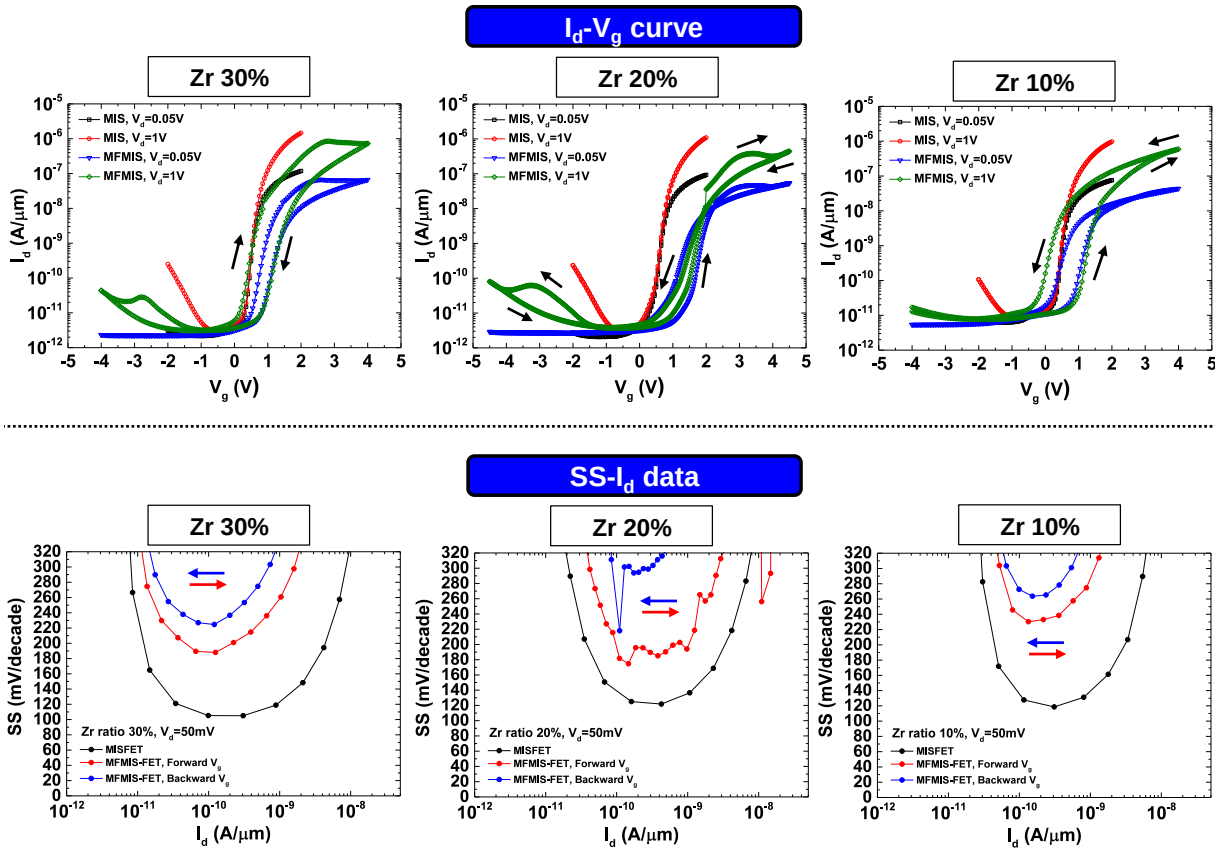


Fig. 5.10. Measured I_d-V_g characteristics and SS-I_d data of Zr ratio-varied MFMIS-FETs, in which characteristics of baseline MISFETs were also plotted for comparison. AR and T_{fe} in HZO thin film were default conditions of 1:14 and 10nm, respectively. Hysteresis I_d-V_g characteristics and non-steep SS were shown in MFMIS-FETs, which are inconsistent with the simulation results based on the NC model shown in Fig. 5.7.

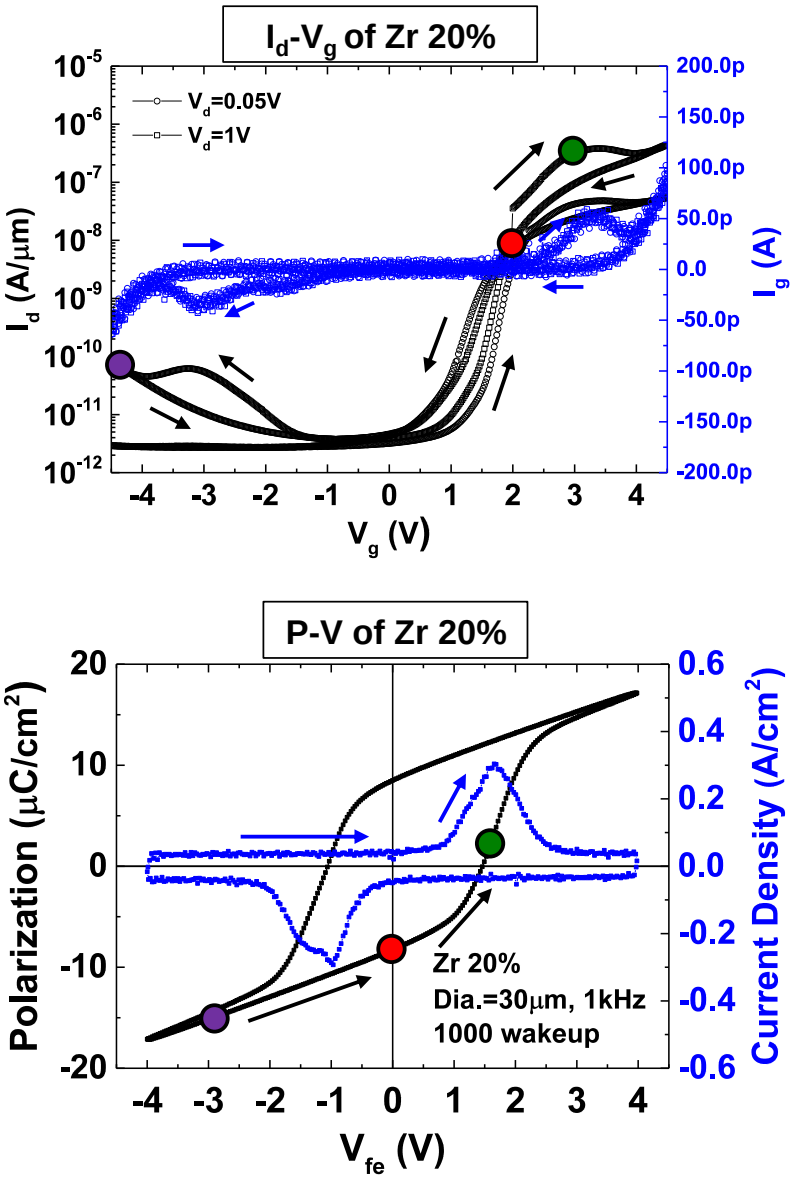


Fig. 5.11. Measured I_d-V_g characteristics of MFMIS-FET with Zr ratio of 20%, in which monitored I_g was also plotted along V_g (top). AR and T_{fe} were default conditions of 1:14 and 10 nm, respectively. Bottom figure is the measured FE properties of FE:HZO capacitor with Zr ratio of 20%. In upper figure, current peaks of I_g (polarization switching) were observed in strong inversion and accumulation region. This indicates that charge from accumulation to V_{th} region of transistor (purple circle to red circle in upper figure) matches not the NC region around polarization switching but the non-switching paraelectric region of FE:HZO (purple circle to red circle in bottom figure).

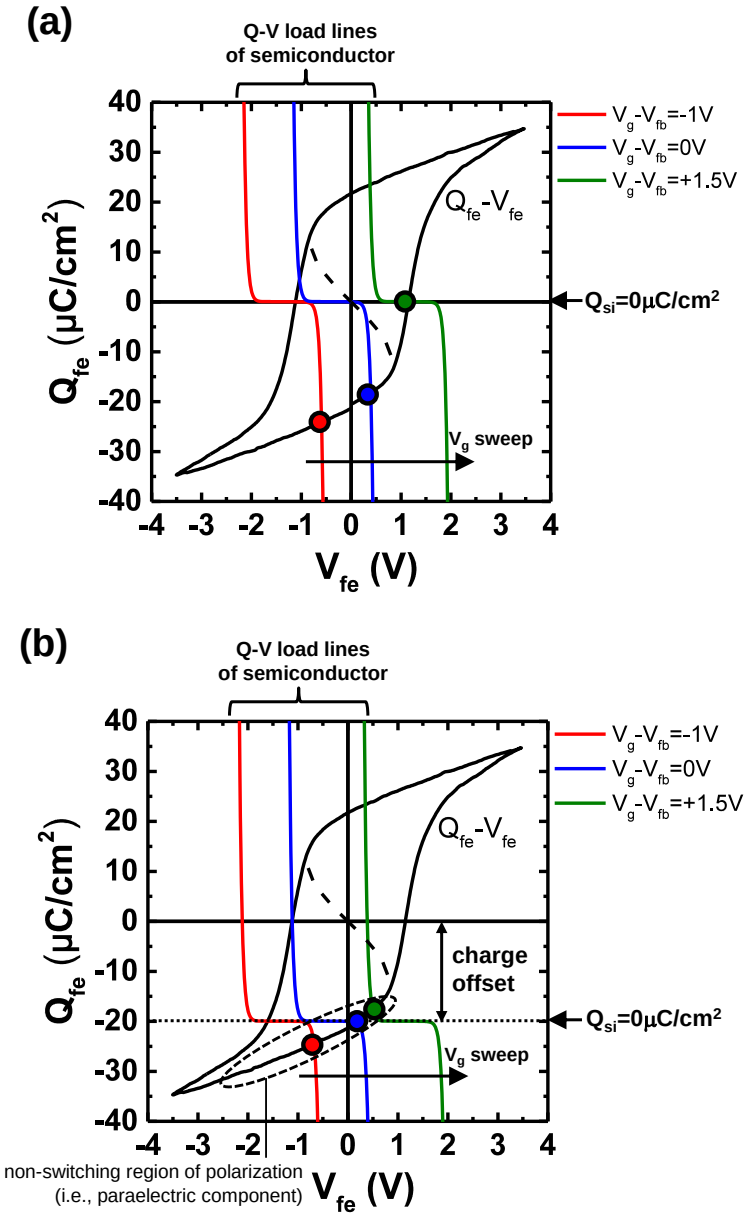


Fig. 5.12. Measured charge-voltage curves of FE:HZO capacitor and calculated charge-voltage curves of Si (plotted as load lines with varied V_g) (a) Without "charge offset". (b) With "charge offset" of 20μC/cm^2. Due to the "charge offset" in (b), when transistor is within sub-V_{th} region, the capacitance of FE:HZO (corresponds to the dQ_{fe}/dV_{fe} in non-switching region of polarization) is always positive.

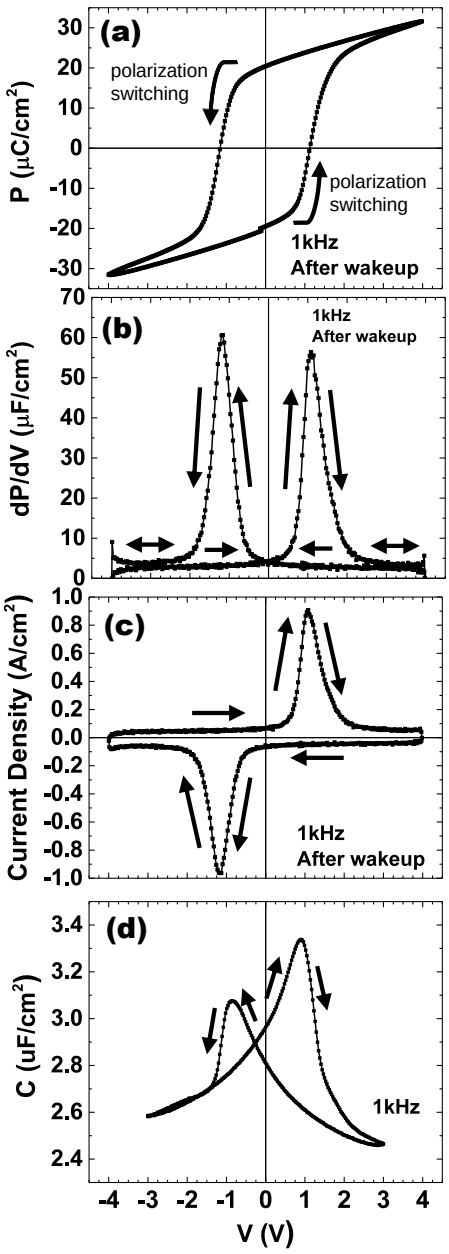


Fig. 5.13. Measured (a) P-V characteristic, (b) large signal C-V characteristic (calculated from dP/dV of (a)), (c) transient I-V response during P-V characterization of (a), (d) small signal C-V characteristic with 1kHz of our fabricated FE:HZO capacitor. Zr ratio was 30% and thickness of FE:HZO was 10nm. A physical origin of these nonlinear dielectric properties is "polarization switching" of FE:HZO.

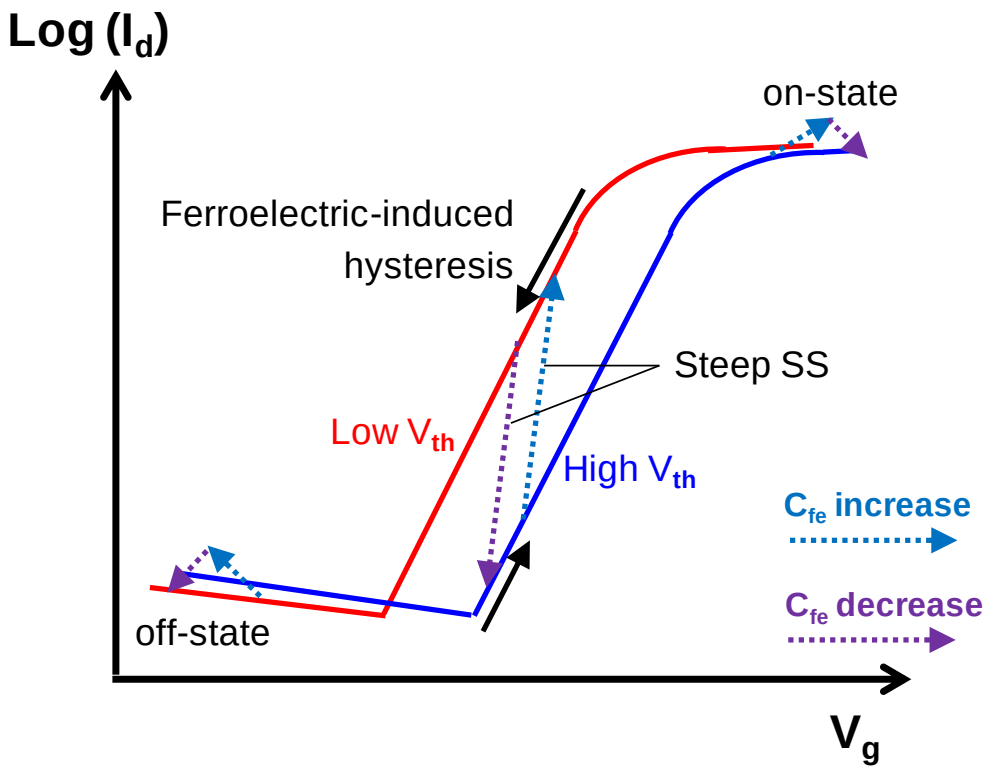


Fig. 5.14. A schematic of idea for the steep SS in NLD-FET using "polarization switching". In our experimental results shown in Fig. 5.10, the increase/decrease in positive capacitance of FE insulator (C_{fe}) induced by polarization switching was obtained in on-state and off-state which results in drain current boost. If the increase/decrease in positive capacitance of FE insulator (C_{fe}) can be occurred within subthreshold region, V_{th} is gradually shifted and steep SS can be obtained.

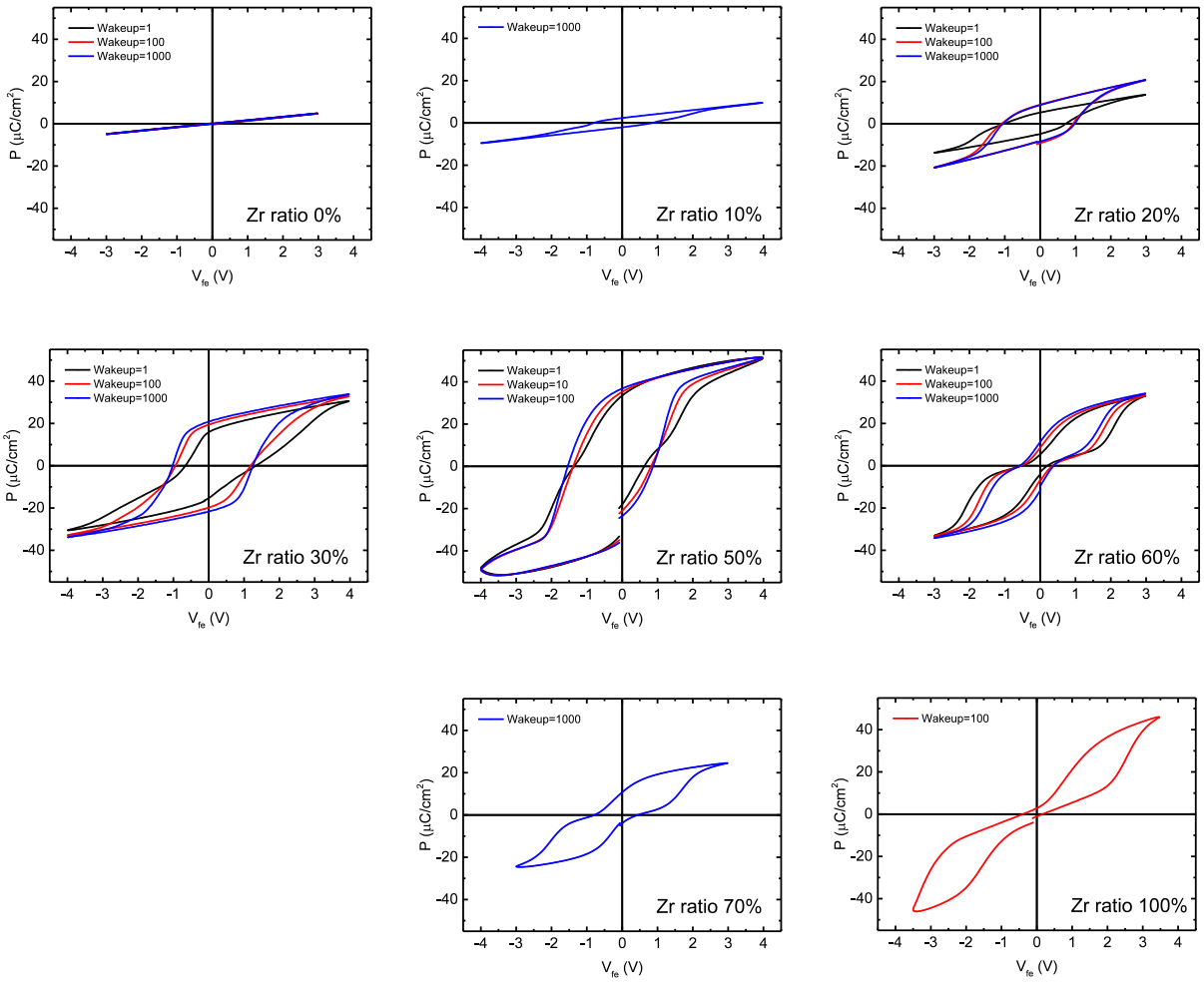


Fig. 5.15. Measured P-V characteristics of HZO capacitors with varied Zr ratio. Zr ratio was varied from 0, 10, 20, 30, 50, 70, and 100% to search material design point of HZO. From 0% to 100% of Zr ratio, transition of paraelectric (Zr 0%) → ferroelectric (Zr 10-50%) → anti-ferroelectric phase (Zr 60-100%) was observed in our experiments [7].

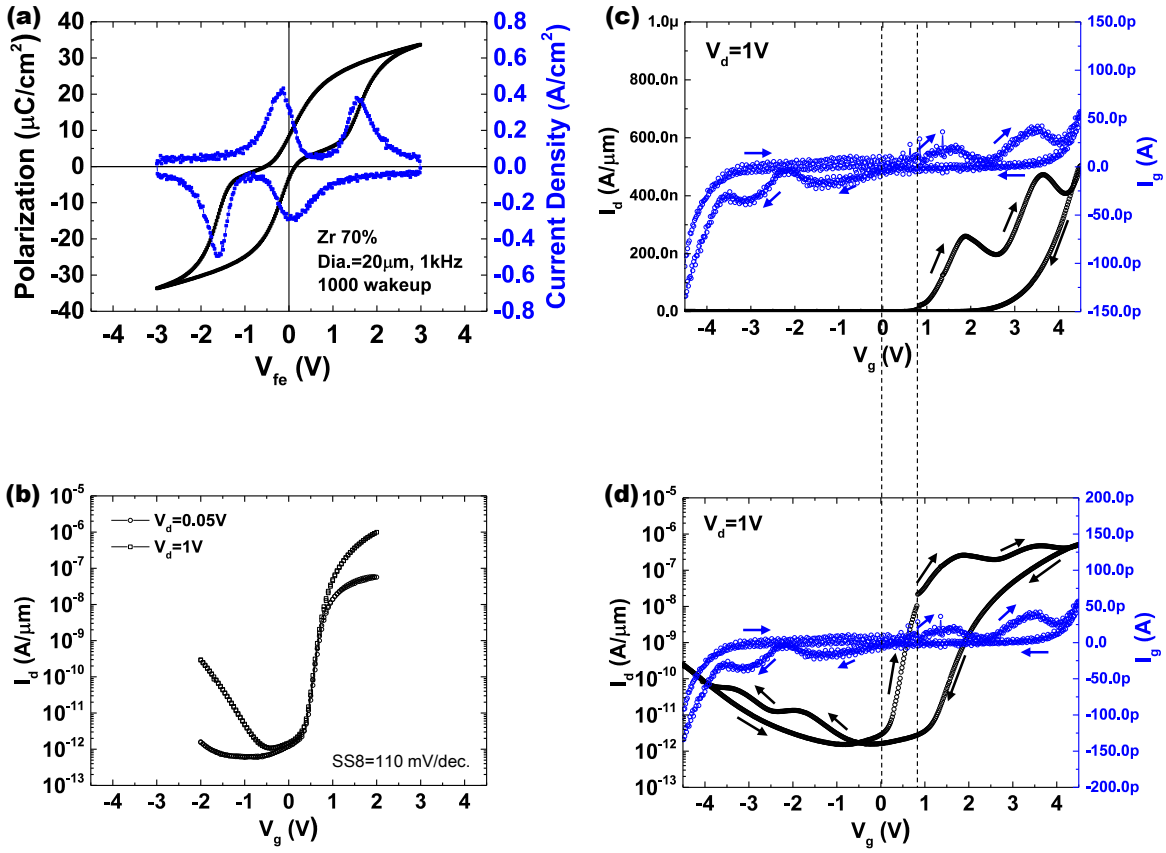


Fig. 5.16. Measured characteristics of MFMIS-FETs with Zr ratio of 70% as a typical case of AFE:HZO-based MFMIS-FET. AR=1:32 and T_{fe}=10nm were used. (a) P-V curve and transient current response of HZO capacitor. Clear AFE characteristics with two current peaks in single voltage sweep were observed. (b) I_d-V_g characteristic of baseline MISFET. (c), (d) I_d-V_g characteristics of MFMIS-FET with monitored I_g. Drain current was plotted in linear scale in (c), and in log scale (d). Clockwise hysteresis was observed in the I_d-V_g characteristics due to the charge injection. Monitored I_g had two current peaks which can be attributed to the "polarization switching". Furthermore, with these gate current peaks, drain current also had two current peaks at same bias range as expected in NLD model. Thanks to the AFE:HZO, first current peak is closer to the sub-V_{th} region comparing to Fig. 5.11. However, even with AFE:HZO with Zr ratio of 70%, NLD effect (events of polarization switching) was mainly observed over V_{th} region and accumulation regions.

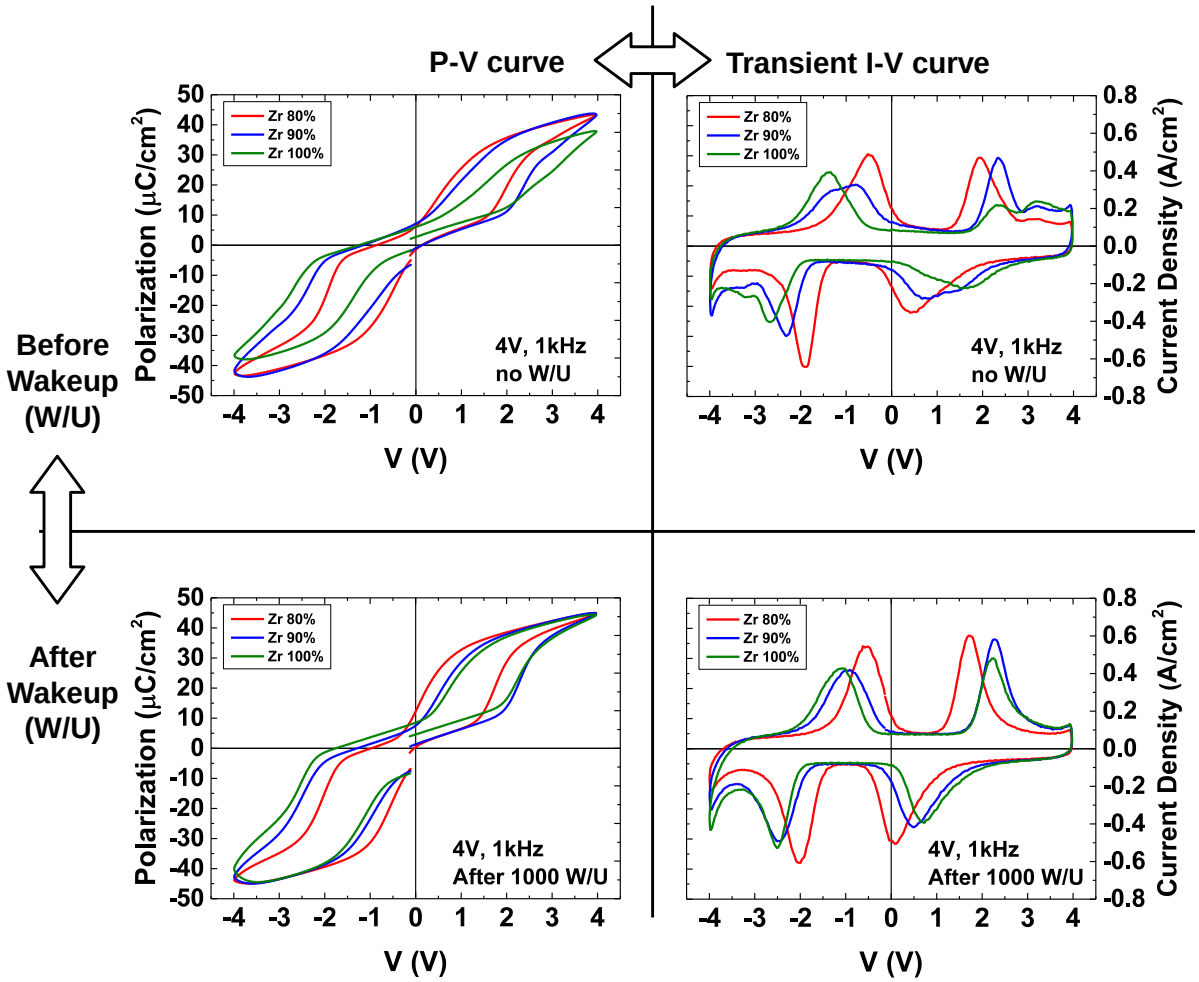


Fig. 5.17. Measured FE characteristics of the separated HZO capacitors with Zr ratio of 80%, 90% and 100%. HZO capacitors showed stronger AFE characteristics comparing to Zr 70%. Even after 1000 cycle wakeup treatments, AFE characteristics were not significantly degraded nor transited to FE-dominant characteristics.

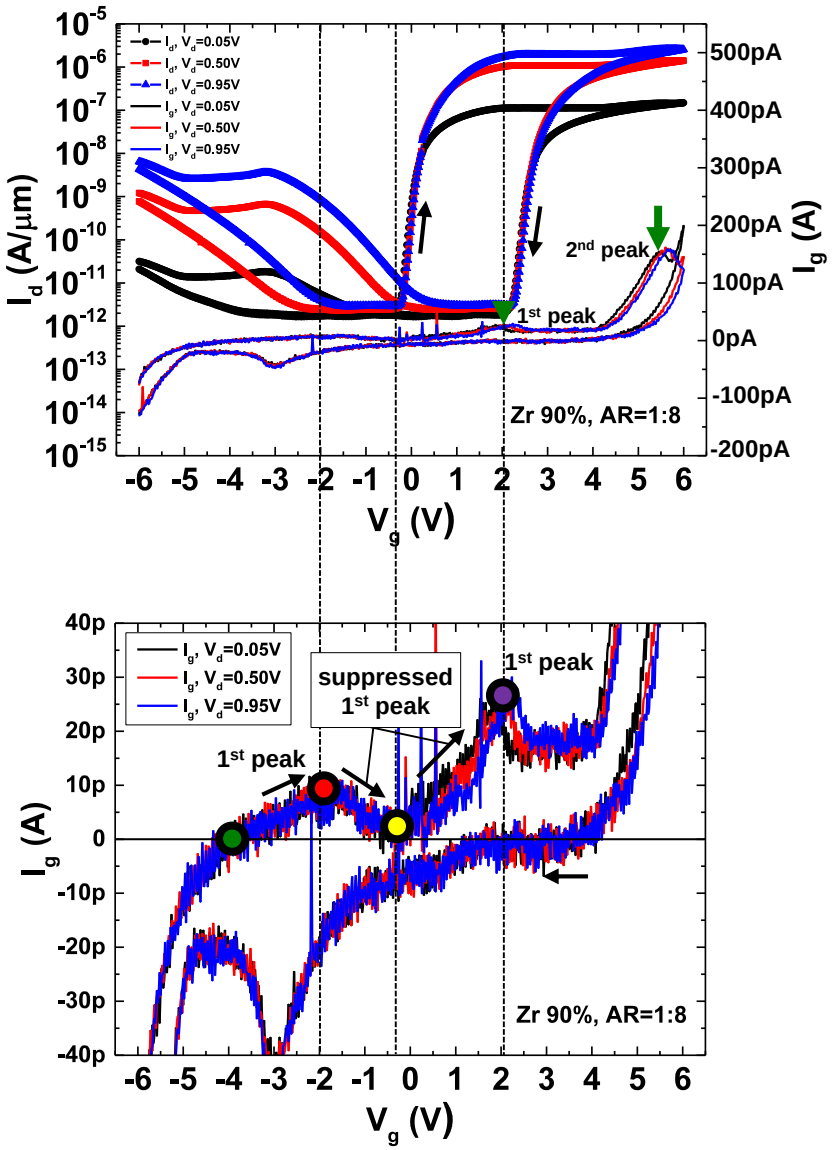


Fig. 5.18. Measured I_d-V_g characteristics of MFMIS-FET with Zr ratio of 90% and AR=1:8, in which monitored I_g was also plotted. Clockwise hysteresis due to charge injection was observed. Both of I_d and I_g had two current peaks induced by the polarization switching of AFE:HZO. In the extended I_g-V_g data (bottom), another current peak was found in negative V_g along forward V_g sweep. The current peak in negative V_g can be a part of first switching current, however considered to be suppressed due to the small capacitance of depletion layer.

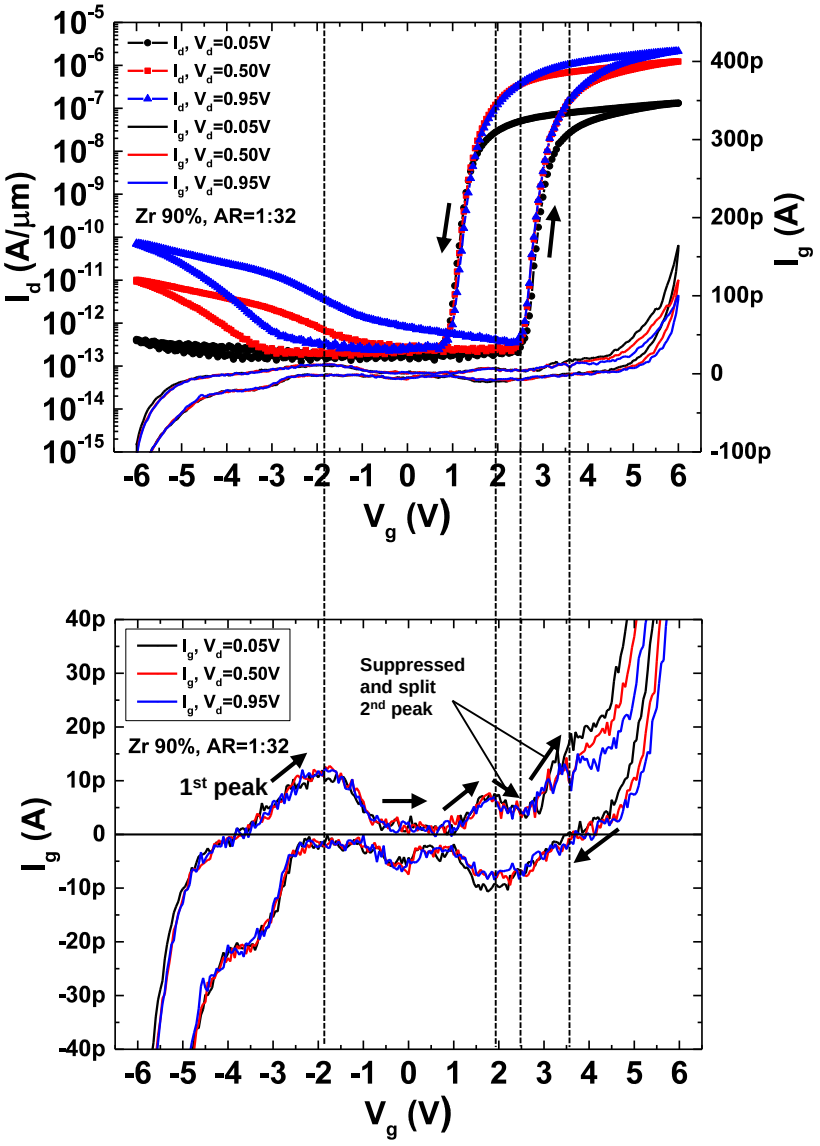


Fig. 5.19. Measured I_d-V_g characteristics of MFMIS-FET with Zr ratio of 90% and AR=1:32, in which monitored I_g was also plotted. Anti-clockwise hysteresis due to FE hysteresis was observed. In the extended I_g-V_g data (bottom), another current peak was found in around V_g=3.5V along forward V_g sweep. The current peak around V_g=3.5V can be a part of second switching current, however considered to be suppressed due to the small capacitance of depletion layer.

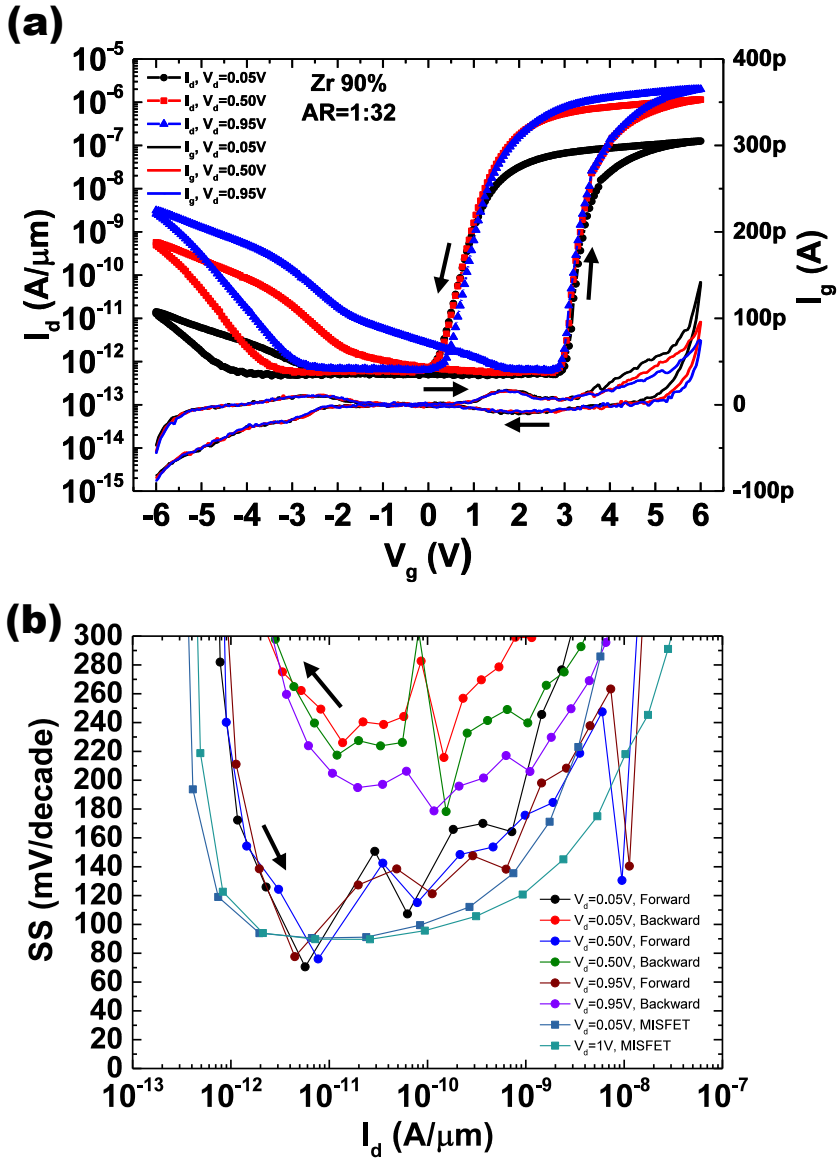


Fig. 5.20. Measured (a) I_d-V_g characteristics with monitored I_g, and (b) extracted SS-I_d data of MFMIS-FET with Zr ratio of 90% and AR=1:32.

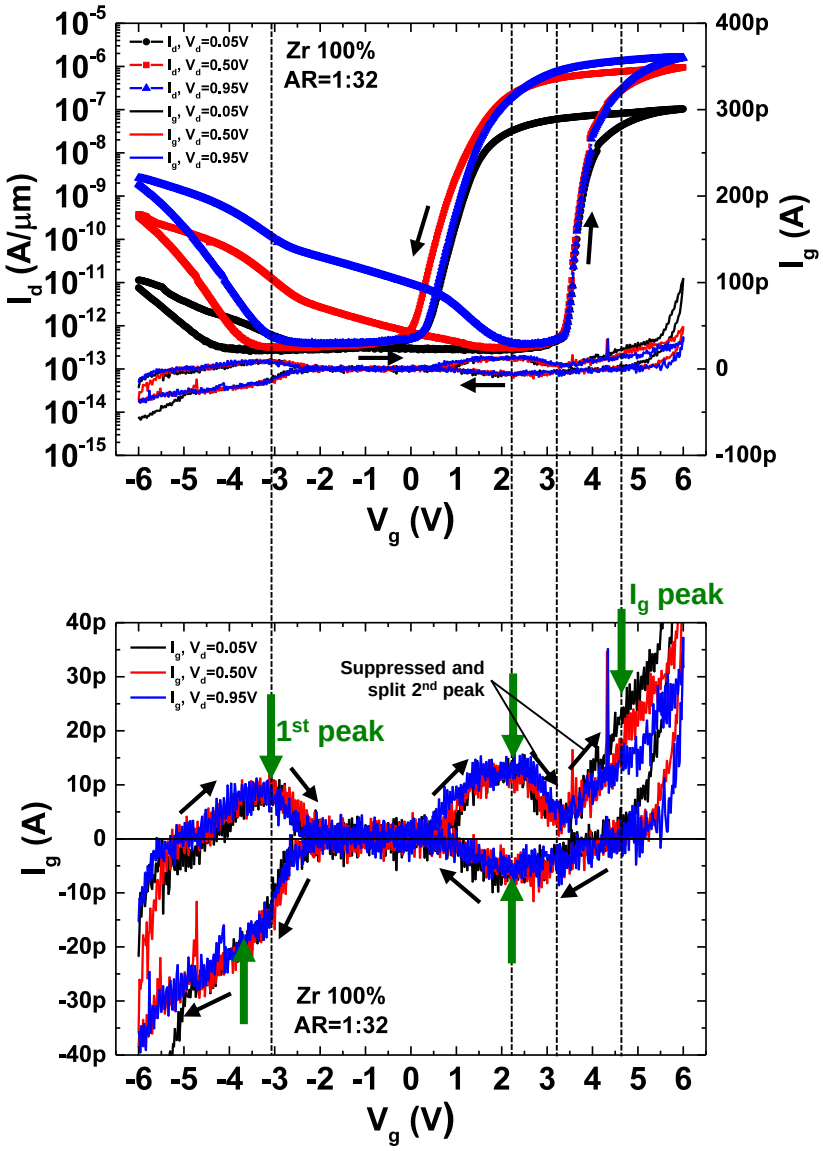


Fig. 5.21. Measured I_d-V_g characteristics (top) of MFMIS-FET with Zr ratio of 100% and AR=1:32, in which monitored I_g was also plotted. Anti-clockwise hysteresis due to FE hysteresis was observed. In the extended I_g-V_g data (bottom), the current peak in positive V_g is considered to be suppressed and separated due to the small capacitance of depletion layer.

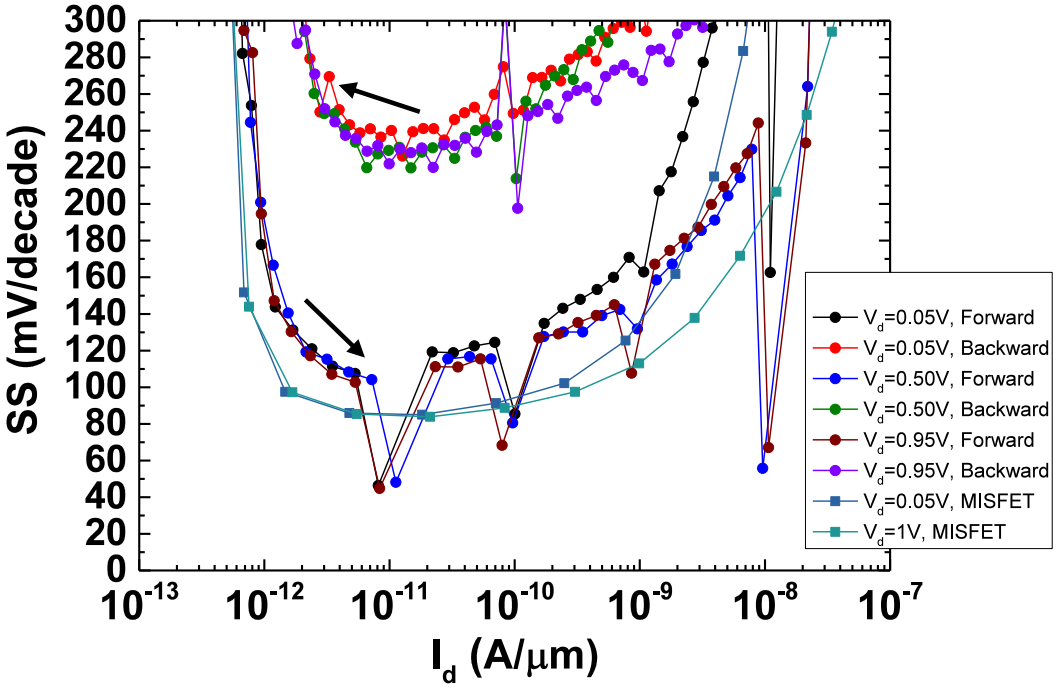


Fig. 5.22. Extracted SS-I_d of MFMIS-FET with Zr ratio of 100% and AR=1:32 from the measured I_d-V_g characteristics in Fig. 5.21.

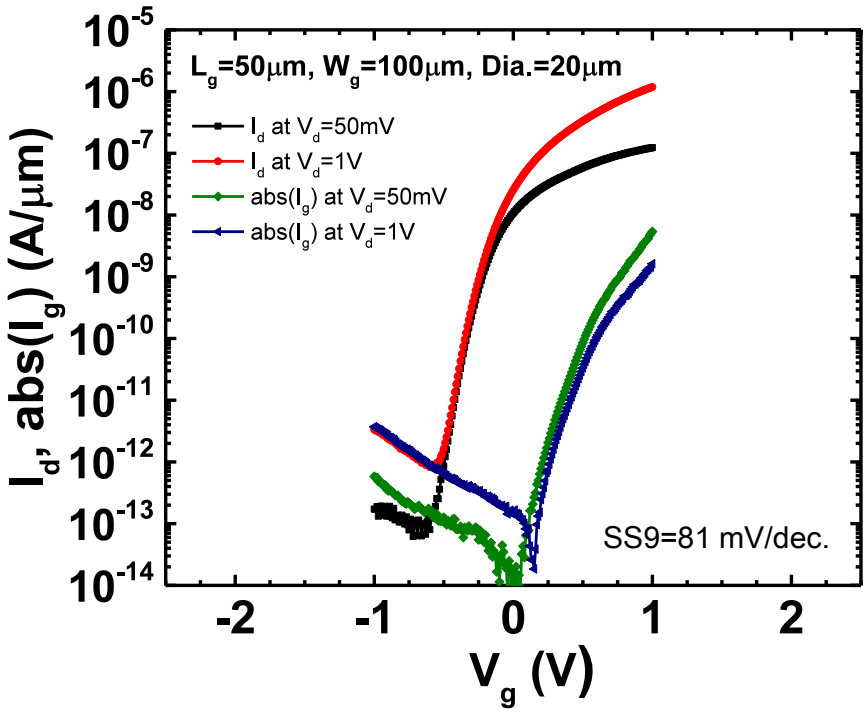


Fig. 5.23. Measured I_d-V_g characteristic of FD-SOI MISFET, in which monitored I_g is also plotted. Please note that MISFET was gate leaky. Typical SS value of 81mV/decade was extracted at the drain current level of $I_d = W_g / L_g \times 10^{-9}$ A and V_d=0.05V, defined as SS9 here.

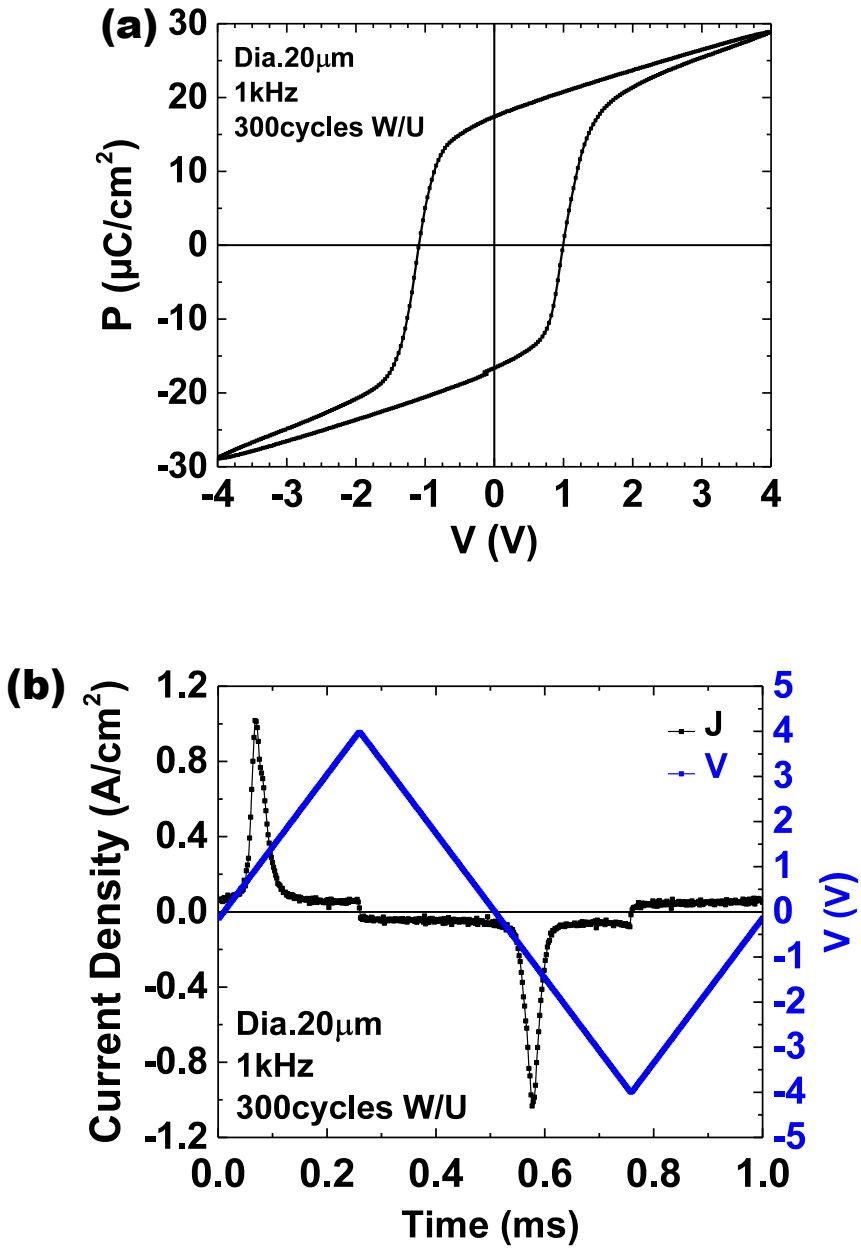


Fig. 5.24. Measured FE characteristics of MFM-HZO capacitors (20μm-diameter pad) with Zr ratio of 30% after wake-up (W/U). (a) P-V characteristic with applied voltage amplitude of 4V (b) Transient current response to applied voltage amplitude of 4V and frequency of 1kHz.

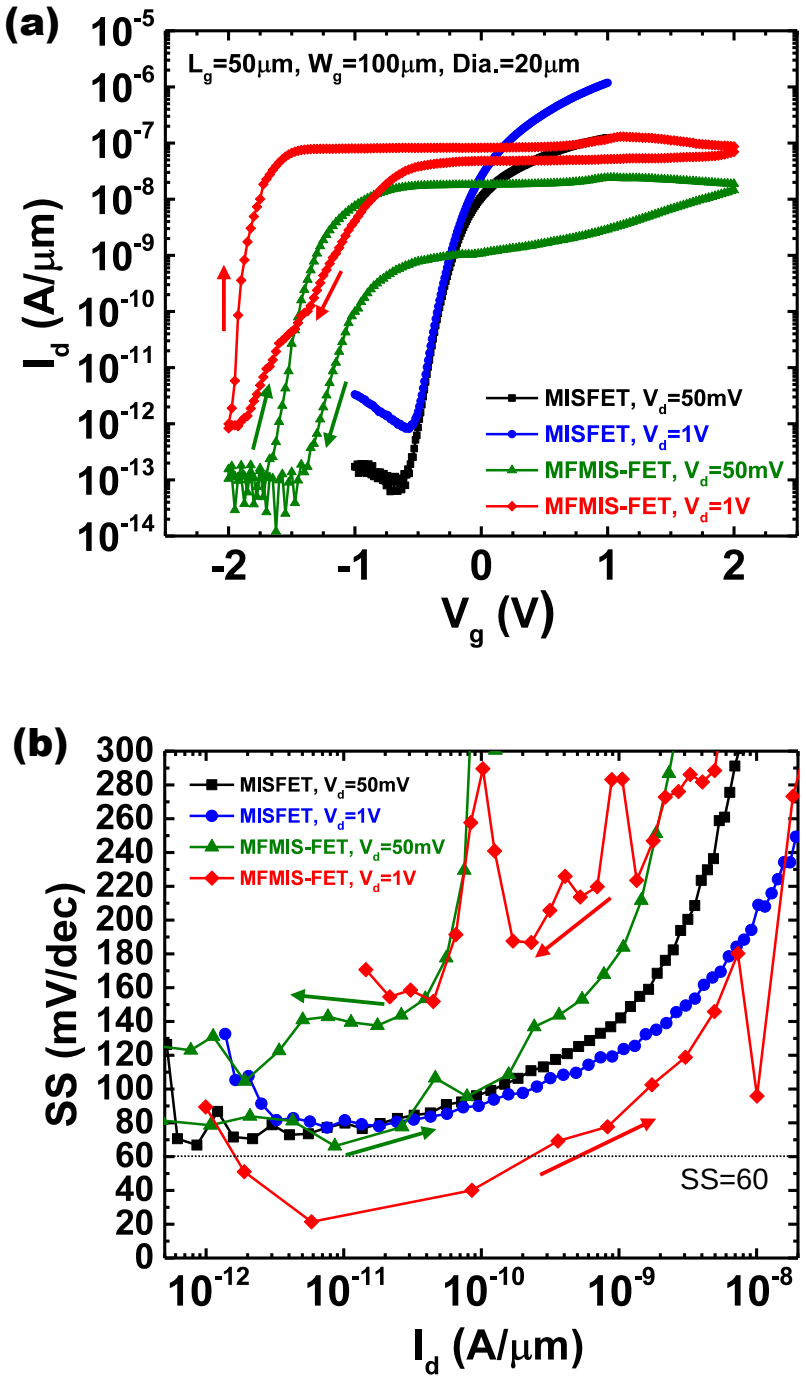
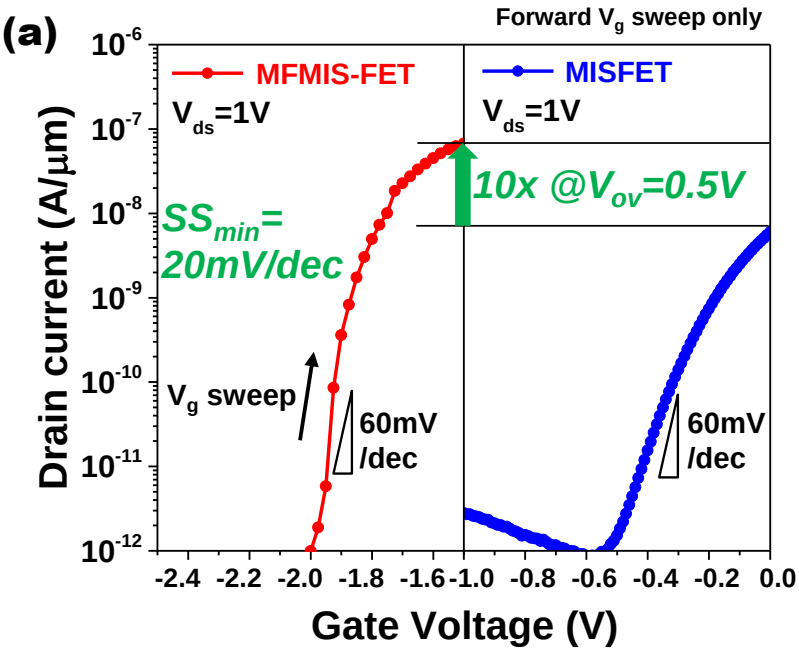


Fig. 5.25. Measured (a) I_d-V_g characteristics with monitored I_g and (b) SS-I_d data of MFMIS-FET with gate leaky MISFET. Zr ratio was 30% and AR was 1:16. Clockwise hysteresis due to the charge injection was observed. The SS < 60mV/decade was observed in forward V_g sweep of MFMIS-FET in 2 decades of drain current. Minimum SS value was 20mV/decade.



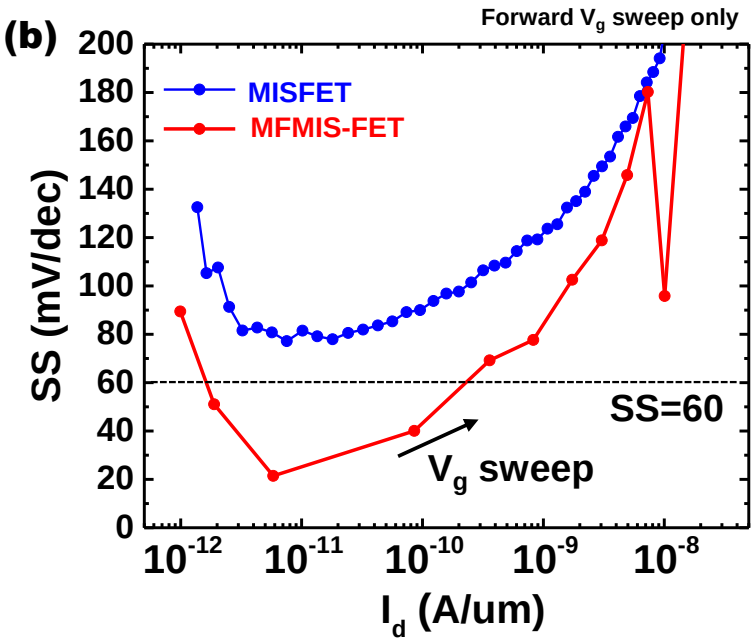


Fig. 5.26. Measured (a) I_d-V_g characteristics with monitored I_g and (b) extracted SS-I_d data of MFMIS-FET with gate leaky MISFET. The results of forward V_g sweep and V_d=1V in Fig. 5.25 were re-plotted here. Minimum SS value was 20mV/decade. The steep SS < 60mV/decade was observed in 2 decades of drain current. Such steeper SS than MISFET was achieved in 4 decades of drain current.

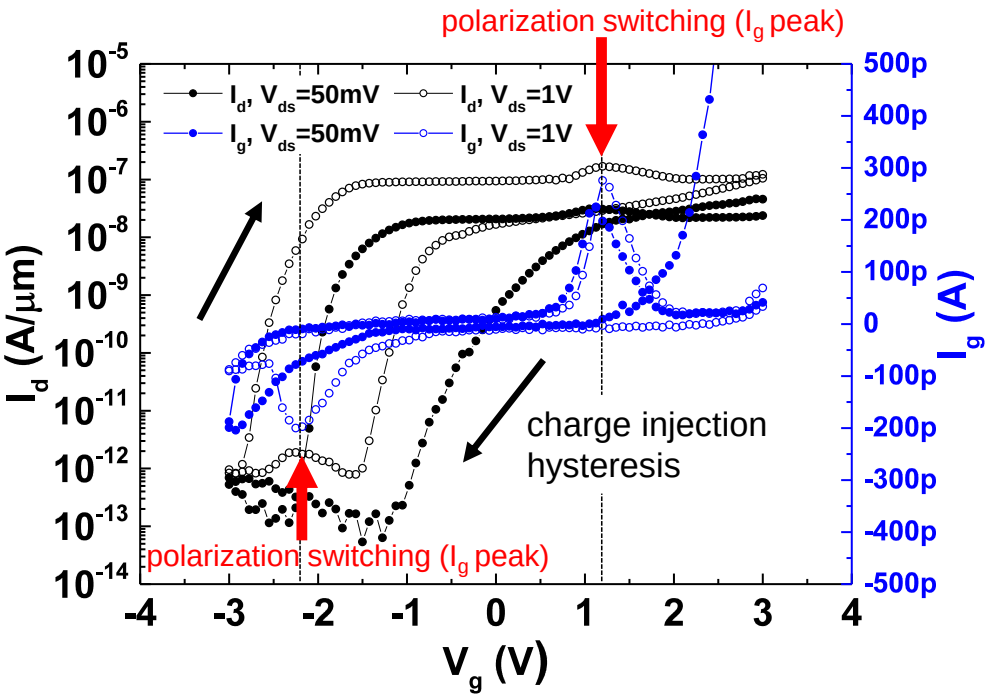


Fig. 5.27. Measured I_d-V_g characteristic of MFMIS-FET by sweeping V_g = +3V → -3V → +3V, in which monitored Ig was also plotted. There are peaks in I_d and I_g at the same V_g range. Physical origin of the current peaks are polarization switching of FE:HZO. I_g had current peaks in positive and negative gate bias region, which indicates that MFM capacitor traced major loop of P-V curve. Because of charge injection, I_d-V_g characteristic showed clockwise hysteresis.

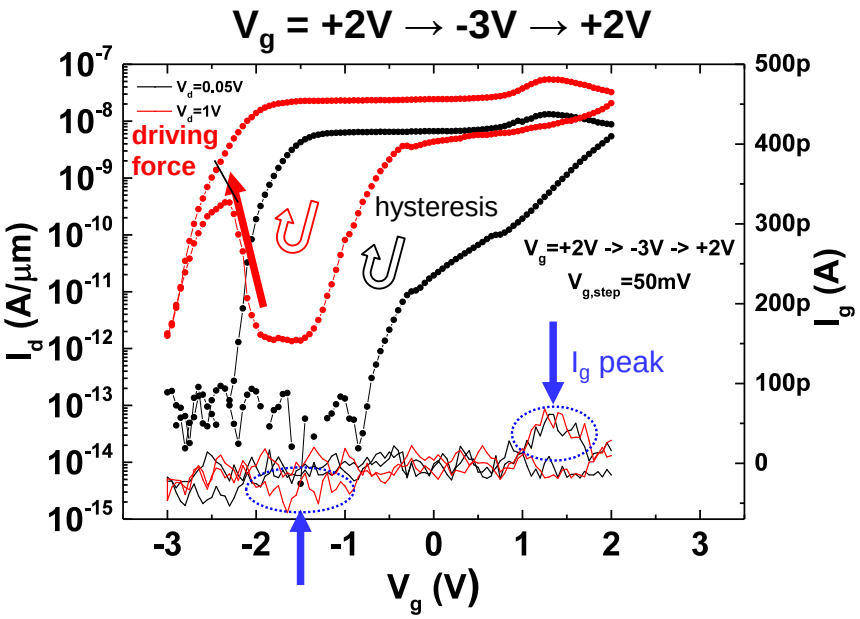


Fig. 5.28. Measured I_d-V_g characteristics of MFMIS-FET with V_g sweep of V_g= +2V → -3V → +2V. We observed driving force to turn on the transistor from V_g=-2V to V_g=-2.5V.

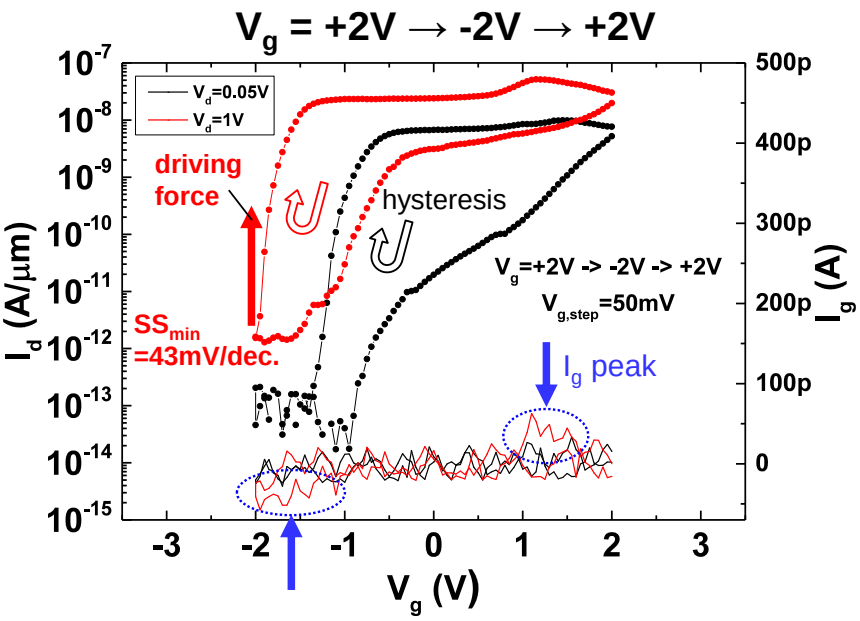


Fig. 5.29. Measured I_d-V_g characteristics of MFMIS-FET with V_g sweep of V_g= +2V → -2V → +2V. When I_g peak (polarization switching) appears and V_g switches at V_g=-2V at the same time, then the steep SS was clearly observed

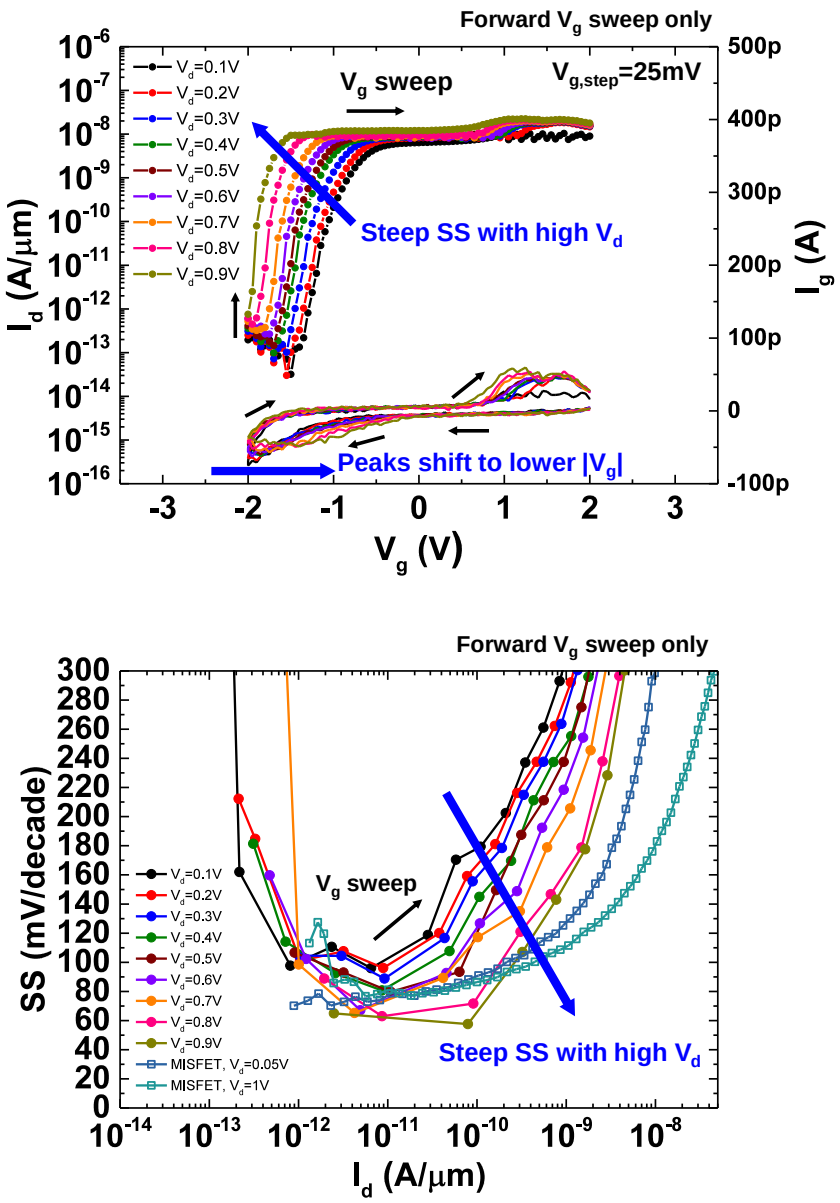


Fig. 5.30. Measured V_d dependence of I_d-V_g characteristics of the MFMIS-FET, in which V_g switches at V_g=-2V (top). Extracted V_d dependences of SS-I_d data from the I_d-V_g characteristics (bottom). Here, for I_d-V_g characteristics and SS-I_d data, the results of only forward V_g sweep were shown, while I_g-V_g characteristics are results of positive and negative V_g sweeps.

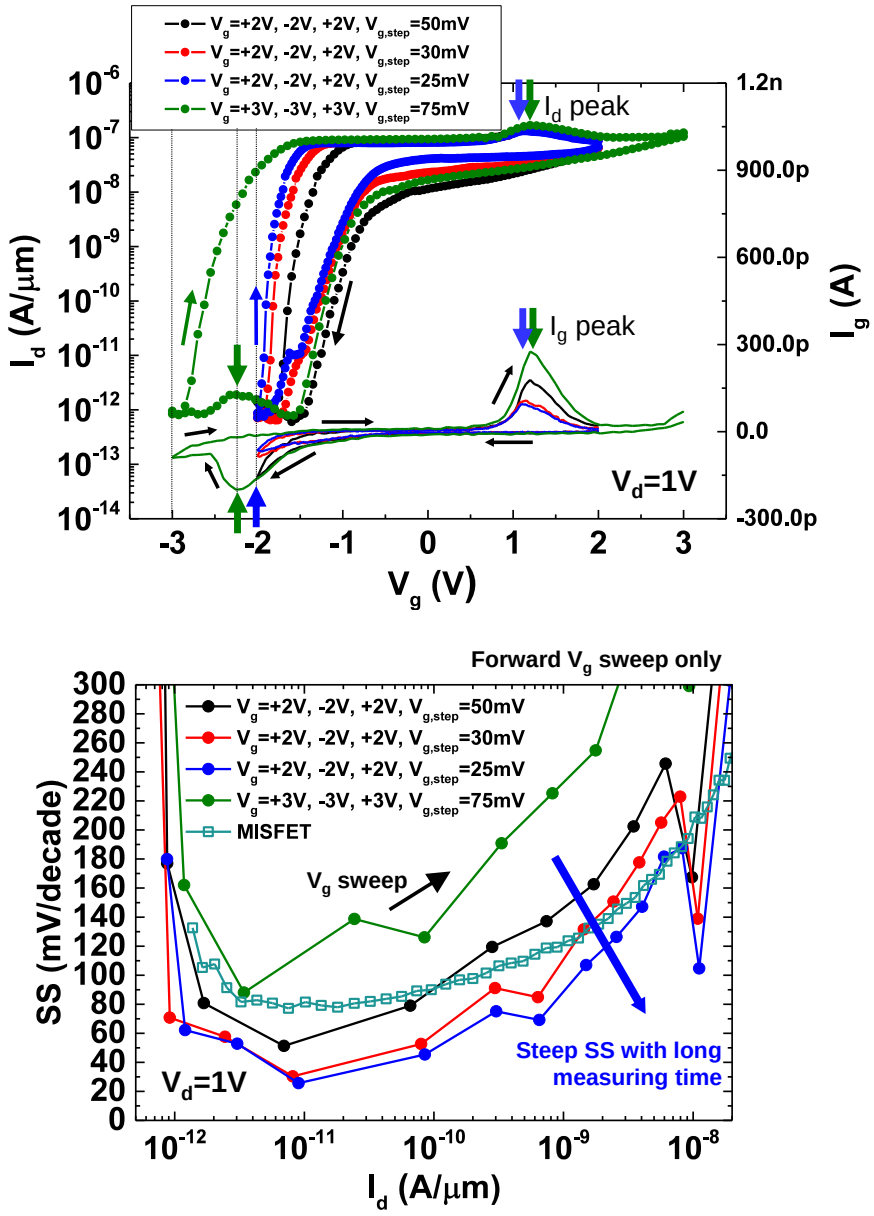


Fig. 5.31. (Top) Measured V_g step dependences of I_d-V_g characteristics of the MFMIS-FET, in which monitored Ig was plotted also. (Bottom) Extracted V_d dependences of SS-I_d data from the I_d-V_g characteristics. Here, I_g-V_g characteristics and monitored I_g are the results of double V_g sweeps, whereas the extracted SS-I_d data are the results of only forward V_g sweep. In the case of V_g= +2V → -2V → +2V, steeper SS can be observed with shorter V_g step. However, steep SS was not observed at forward V_g sweep in the case of V_g= +3V → -3V → +3V, because "polarization switching" process of FE had already finished before V_g reached -3V.

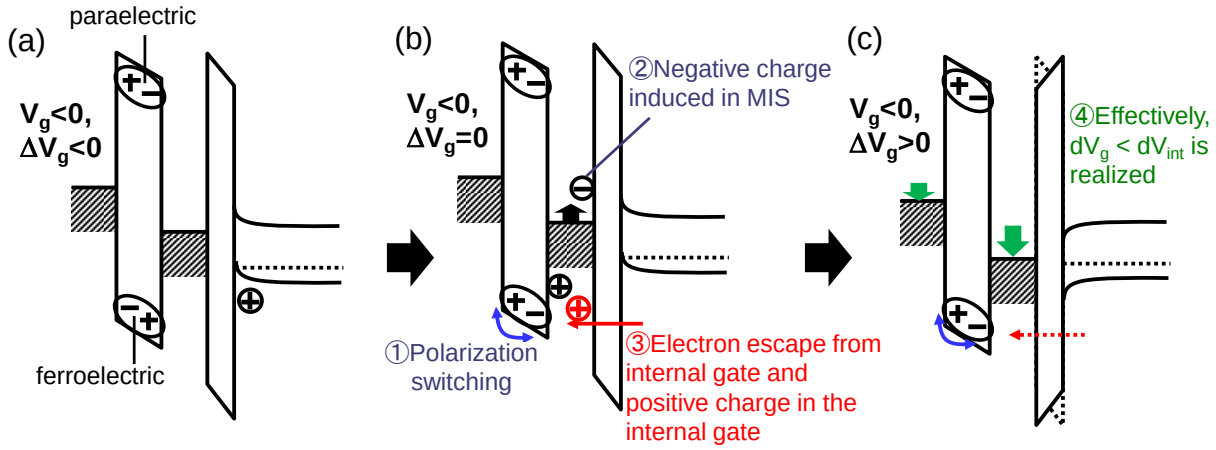


Fig. 5.32. (a) The band diagram before polarization switching at $V_g < 0$ in off-state. (b) Once polarization switching starts, negative charges are induced on MIS gate side to balance the charge inside the internal gate. When $|V_g|$ and V_d is large, "effective positive charges" are also injected to internal gate because electrons escape from internal gate. (c) Then, when V_g switches to the positive direction, the steep SS appears due to the voltage amplification.

Chapter 6
Conclusions

In this thesis, negative-capacitance FETs (NCFETs) using ferroelectric $HfZrO_2$ (FE:HZO) have been studied by both of simulations and experiments. Aiming the low-power VLSI platform, this thesis has been focused on the steep subthreshold slope (SS) in FE:HZO-based NCFETs. Based on the obtained design points for the device structures and/or FE material characteristics, FE:HZO-based NCFETs were fabricated and characterized to clarify the physical origin of the NC effect, and to understand the phenomena of steep SS in FeFETs. The main results obtained in the thesis are summarized as follows.

In chapter 2, device simulation on the static characteristics of multi-gate NCFETs was conducted based on the NC model, in which the design points of device structures and FE properties were obtained. Device design guidance to obtain the steep SS in FE:HZO-based NCFETs was addressed based on the NC model.

In chapter 3, dynamic characteristics and operation speed of FE:HZO-based NCFET were simulated based on the single-domain (SD)-based Landau-Khalatnikov (LK) equation. Our simulation results with SD-LK model revealed that the operation speed of FE:HZO-based NCFET can be limited by the polarization switching of FE:HZO.

In chapter 4, by incorporating the multiple-domain (MD) effect and domain-domain interaction effect into the SD-LK model, the MD-LK was successfully developed and experimentally validated. Experimentally calibrated MD-LK model could reproduce the various experimental transient responses of FE:HZO capacitors with high fitting accuracy.

In chapter 5, to clarify the physical origin of the NC effect and to understand the

phenomena of steep SS in FeFETs, we experimentally explored steep SS in our fabricated FE:HZO-based metal-FE-metal-insulator-semiconductor (MFMIS)-FETs. First, based on the NC model, bulk MFMIS-FETs were designed and characterized systematically. However, in our experiments, steep SS was not observed as expected by the NC model. This can be attributed to the "charge injection" into the internal gate. Second, we experimentally explored the steep SS in MFMIS-FETs based on the nonlinear dielectric (NLD) model and "polarization switching". By using anti-ferroelectric-HZO as gate insulator, for the first time, we successfully observed the "effective NC effect (polarization switching)" within sub-V_{th} region. Additionally, we observed that "polarization switching" can be suppressed in sub-V_{th} region due to the small capacitance of depletion layer. Third, in MFMIS-FET with gate leaky MISFETs, we experimentally observed steep SS of sub-60mV/decade. The minimum SS value was 20mV/decade and SS < 60mV/decade was for 2 decades of drain current. Sub-60mV/decade steep SS in MFMIS-FETs with gate leaky MISFETs is considered to be the result of voltage amplification, whose physical origin can be attributed to the cooperation of "polarization switching" and "charge injection". Furthermore, throughout our experiments, monitoring gate current has offered very useful information to understand the device characteristics of FeFETs.

In conclusion, the results obtained in this thesis show important information on steep SS characteristics in FETs with FE:HZO. Therefore, we hope that this work will contribute to the comprehensive understanding of the physical origin of NC effect and phenomena of steep SS in FeFETs (including "polarization switching" and "charge injection"), and that provide important guidance for the further researches on the next-generation semiconductor devices for low-power VLSIs.

List of Publications

Journal Articles:

[1] Kyungmin Jang, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, "On gate stack scalability of double-gate negative-capacitance FET with ferroelectric HfO_2 for energy efficient sub-0.2 V operation", Japanese Journal of Applied Physics, vol. 57, no. 2, 024201, 2018.

[2] Kyungmin Jang, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, "I_{on}/I_{off} ratio enhancement and scalability of gate-all-around nanowire negative-capacitance FET with ferroelectric HfO_2", Solid-State Electronics, vol. 136, pp. 60-67, Oct. 2017.

[3] Kyungmin Jang, Nozomu Ueyama, Masaharu Kobayashi, and Toshiro Hiramoto, "Experimental Observation and Simulation Model for Transient Characteristics of Negative-capacitance in Ferroelectric $HfZrO_2$ Capacitor", IEEE Journal of the Electron Devices Society, under review.

[4] Kyungmin Jang, Masaharu Kobayashi, and Toshiro Hiramoto, "Sub-60mV/decade subthreshold slope in metal-ferroelectric-metal-insulator-semiconductor field-effect transistor based on polarization switching of ferroelectric $HfZrO_2$ and charge injection into internal gate (temporary)", to be submitted.

[5] Masaharu Kobayashi, Kyungmin Jang, Nozomu Ueyama, and Toshiro Hiramoto, "Negative Capacitance for Boosting Tunnel FET performance", IEEE Transactions on Nanotechnology, vol. 16, no. 2, pp. 253-258, 2017.

[6] Masaharu Kobayashi, Nozomu Ueyama, Kyungmin Jang, and Toshiro Hiramoto, "Experimental Demonstration of a Nonvolatile SRAM with Ferroelectric HfO_2 Capacitor for Normally-Off Application", IEEE Journal of the Electron Devices Society, accepted.

Conference Contributions (International):

[1] Kyungmin Jang, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, "On Gate Stack Scalability of Double-Gate Negative-Capacitance FET with Ferroelectric HfO_2 for Energy-Efficient Sub-0.2V Operation", IEEE Silicon Nanoelectronics Workshop (SNW), pp. 176-177, Honolulu, Hawaii, USA, June 13, 2016.

[2] Kyungmin Jang, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, "I_{on}/I_{off} Ratio Enhancement of Gate-All-Around Nanowire Negative-Capacitance FET with Ferroelectric HfO_2", International Semiconductor Device Research Symposium (ISDRS), FP4-04, Washington, DC, USA, December 9, 2016.

[3] Masaharu Kobayashi, Nozomu Ueyama, Kyungmin Jang, and Toshiro Hiramoto, “Experimental Study on Polarization-Limited Operation Speed of Negative Capacitance FET with Ferroelectric HfO_2”, IEEE International Electron Devices Meeting (IEDM), pp. 314-317, San Francisco, CA, USA, December 6, 2016.

[4] Kyungmin Jang, Nozomu Ueyama, Masaharu Kobayashi, and Toshiro Hiramoto, “Investigations on Dynamic Characteristics of Ferroelectric HfO_2 based on Multi-Domain Interaction Model”, IEEE Silicon Nanoelectronics Workshop (SNW), pp. 15-16, Kyoto, Japan, June 4, 2017.

[5] Masaharu Kobayashi, Kyungmin Jang, Ueyama Nozomu, and Toshiro Hiramoto, “Negative Capacitance as a Performance Booster for Tunnel FET”, IEEE Silicon Nanoelectronics Workshop (SNW), pp. 150-151, Honolulu, Hawaii, USA, June 13, 2016.

Conference Contributions (Domestic):

[1] Jang Kyungmin, 水谷 朋子, 竹内 潔, 更屋 拓哉, 小林 正治, 平本 俊郎, “FD-SOTB nMOSFET における RTN 振幅統計分布の基板バイアス依存性”, 第 76 回応用物理学会秋季学術講演会, 15p-1C-1, 名古屋国際会議場(愛知), 2015 年 9 月 15 日.

[2] Jang Kyungmin, 更屋 拓哉, 小林 正治, 平本 俊郎, “サブ 0.2V の高エネルギー効率動作に向けた強誘電体 HfO_2 ダブルゲート負性容量 FET におけるゲートスタックのスケーラビリティ”, 第 77 回応用物理学会秋季学術講演会, 13p-B13-5, 朱鷺メッセ(新潟), 2016 年 9 月 13 日.

[3] Jang Kyungmin, 上山 望, 小林 正治, 平本 俊郎, “強誘電体 HfO_2 ダブルゲート負性容量 FET の動特性に関する考察”, 第 64 回応用物理学会春季学術講演会, 17p-304-14, パシフィコ横浜(横浜), 2017 年 3 月 17 日.

[4] Jang Kyungmin, 更屋 拓哉, 小林 正治, 平本 俊郎, “強誘電体 HfO_2 を用いた Gate-All-Around ナノワイヤ負性容量 FET における I_{on}/I_{off} 比の向上とそのスケーラビリティ”, 第 64 回応用物理学会春季学術講演会, 17p-304-15, パシフィコ横浜(横浜), 2017 年 3 月 17 日.

[5] Jang Kyungmin, 上山 望, 小林 正治, 平本 俊郎, “強誘電性マルチドメイン相互作用モデルを用いた強誘電体 HfO_2 の動特性に関する考察”, 第 78 回応用物理学会秋季学術講演会, 7p-A204-13, 福岡国際会議場(福岡), 2017 年 9 月 7 日.

[6] 小林 正治, 蔣 京珉, 上山 望, 平本 俊郎, “負性容量によるトンネル FET の性能向上”, 第 77 回応用物理学会秋季学術講演会, 13p-B13-4, 朱鷺メッセ(新潟), 2016 年 9 月 13 日.