博士論文

Power-Law Clock Frequency Control Scheme in CMOS On-Chip DC-DC Converters for Wide Current-Range Applications

（べき乗則周波数制御による広い出力電流範囲に対応したCMOSオンチップDC-DCコンバータ）

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Abstract

With growing development of the Internet-of-Things (IoT), wearable devices, and implantable medical electronics, there is an increasing demand for low-power and energy-efficient large-scale integrated (LSI) circuits. The power consumption of these LSI circuits, however, varies significantly depending on the operating conditions such as the sleep mode or the active mode. As specified by the Bluetooth Low Energy, the load current range can change more than 10^4. In addition, the electronic devices are required operating for a long time without the need to replace the battery because of the material and the labor cost. A DC-DC converter is used to convert the battery input voltage to a well-regulated output voltage for the electronic devices. To prolong the battery lifetime, the DC-DC converter should support more than 10^4 wide output current range with high conversion efficiency. Unlike mobile and laptop applications, however, it shows the LSI circuits in the IoT, wearable electronics, and implantable medical sensors stay in a sleep mode for most of the time and turn into an activate for only a short period of time to transfer data. Therefore, a DC-DC converter achieving high conversion over wide current range, especially in sleep mode, becomes increasingly important to reduce the overall energy consumption. Besides, an on-chip CMOS design technology is attractive to develop low-cost and compact physical dimension LSI circuits and systems.

This thesis is organized with five chapters. The first chapter describes an introduction including the wide-current range applications such as IoT and the contribution of this thesis. The research motivation and the reason why the conversion efficiency of a DC-DC converter is important especially in the sleep mode are also shown in Chapter 1. Two

applications of IoT are employed to calculate the LSI systems energy consumption.

In Chapter 2, a clocked hysteresis control scheme with power-law frequency scaling is newly proposed to improve the conversion efficiency at a light load current and applied to a buck converter design. Compared with a conventional hysteresis control buck converter, the buck converter consumes no DC current in the comparators by replacing a continuously-on comparator by a clocked comparator with power-law frequency scaling. In addition, the clocked hysteresis control maintain a quick wake-up feature because of the inherent hysteresis control. As to the theoretical aspect, expressions for the frequency stability condition, power consumption, and output voltage ripple of the proposed power-law frequency scaling scheme are derived and analyzed. Experimental results show that the buck converter implemented with the power-law frequency scaling scheme achieves higher than 87% and almost flat conversion efficiency over a load current ranging from 500 nA to 20 mA with a 90.4% peak efficiency.

A 2:1 switched-capacitor (SC) DC-DC converter implemented with the proposed power-law frequency scaling scheme is proposed in Chapter 3. This chapter shows that the proposed scheme is also able to improve the conversion efficiency of a SC DC-DC converter in the sleep mode. A prototype is designed and implemented in a standard CMOS 0.18 μm process technology. Experimental results show that the converter achieves higher than 87.5% and almost flat conversion efficiency over a load current range from 600 nA to 150 μA with a 94.9% peak efficiency. The conversion efficiency is higher than 50 % when a load current ranging from 50 nA to 150 μA is applied, and can operate functionally when the load is as low as 10 nA. Compared with a 2:1 switched-

capacitor DC-DC converter using a fixed high frequency clock, the proposed converter improves 33% of conversion efficiency when the load current is 1 μA.

A design of digital low-dropout regulator with the power-law frequency scaling scheme is introduced in Chapter 4. By automatically adjusting the clock frequency of the clock comparator used in a digital LDO, the current efficiency can be improved especially in a light load condition. The target is to optimize the clock frequency and current efficiency with the load conditions to improve the current efficiency under μA order load conditions. A proposed system topology is introduced and simulated in this chapter.

Chapter 5 shows the summary and the conclusion of this thesis.

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I would like to express my sincere gratitude to many people who are related to this dissertation and related to my life in Japan. Especially I am extremely grateful to my supervisors, Prof. Takayasu Sakurai and Prof. Makoto Takamiya, for their dedicated mentorship and many advices about the research. I learned not only a lot of concepts about the research and design, but also thinking and perspective from Prof. Sakurai and Prof. Takamiya. It broadens my knowledge every time I discussed with them.

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Chapter 1: Introduction

1.1 Background

Recently, the development of wide-operating current range applications such as Internet-of-Things (IoTs), implantable electronics, and wearable devices have attracted a lot of attention. Large scale integration (LSI) circuits integrated in the applications are designed to sense activities and environment conditions as data, and transmit the sensed data to the cloud through the internet. After processing and analyzing the data, useful information or features can be extracted and fed back to the LSI circuits at the user ends. It is costly and inconvenient, however, to replace the battery used to power the LSI circuits because of the need for the labor, the material, and the maintenance time. To prolong the battery lifetime, Bluetooth Low Energy (BLE) specifications have been proposed [1.1] for low power communication. It indicates the maximum active current and the sleep current are about 15 mA for data transmission with 10 dBm output power and 1 μA, respectively. Unlike mobile and laptop applications, the LSI circuits stay in a sleep mode for most of the time and wake up to transmit data for only a short period of time. It has been shown by measurement results that the LSI circuits consume much more energy in the sleep mode than the active mode. A smoke detection sensor [1.2] and smart pipeline monitoring system [1.3] in IoT show that more than 95% energy in one periodic operation is consumed by the sleep mode. Table 1.1 shows the distribution of the energy consumption in each operating mode. In accordance with these backgrounds, a DC-DC converter used to convert the battery input voltage to a well-regulated output voltage for the LSI circuit should support more than 10^4 current range with high conversion efficiency.

In addition, high conversion efficiency in the sleep mode becomes more important in order to save the overall energy consumption and prolong the battery lifetime.

Application / Operating mode	Smoke detector in IoT	Smart pipeline monitoring system
Wake-up	1%	1%
Active	2%	4%
Sleep	97%	95%
Total	100%	100%

Table. 1.1. Energy dissipation of each mode in IoT smoke detector and smart pipeline monitoring system

Fig. 1.1 shows a block diagram of a target energy-efficient LSI system for wide-current range applications. The sensors such as smoke, light, and temperature sensors sense environment data according to an event. The data are processed and stored by the processing unit CPU/GPU and the memory, respectively. Information are transmitted to the cloud by the transmitter. Required features extracted by the cloud can be fed back to the LSI system through the receiver and analyzed by the processing unit. A battery is used to power the LSI system for high-reliable operation. Usually, the crystal oscillator can be powered by the battery directly [1.4] [1.5], however, to achieve low-energy operation specified by BLE, other circuits such as CPU/GPU, memory, and other computing functional blocks should be biased at lower voltage level (1.5 ~ 1.6 V). The battery input voltage, however, changes from 2.4 V to 3.3 V depending on the battery electricity.

Therefore, a DC-DC converter is necessary to convert the battery voltage to a stable output voltage and support both the active mode and sleep mode current. In the sleep mode, the DC-DC converter is one of the few circuits aware and dominants the system total energy consumption. The DC-DC converter [1.6] proposed for IoT applications can support an energy harvesting and power management function. The conversion efficiency, however, is lower than 60% when the load current is 1 μA. It is shown by calculation that improving the conversion efficiency from 60% to 80%, the battery lift time can be extended by about 33%. In this thesis, a new clocked hysteresis control scheme with power-law frequency is developed to improve the conversion efficiency at a light load current and to achieve almost flat conversion efficiency over whole load current range. Applying to a buck converter design, 12% - 34% conversion efficiency is improved compared with state-of-the-art buck converters when the load current is 1 μA. Additionally, the buck converter also achieves quick wake-up operation to reduce the wake-up energy consumption, which is important in IoT applications [1.7]. The buck converter is firstly considered because the output can be well-regulated with high conversion efficiency even the input voltage changes over a wide range. In addition, a buck converter usually achieves high conversion efficiency, which is less dependent on the ratio of V_{OUT} and V_{IN}. These properties make buck converter quite suitable for a battery-powered system. Other DC-DC converter topologies including switched-capacitor (SC) DC-DC converter and linear low-dropout (LDO) regulator are also designed and discussed in the latter chapters.

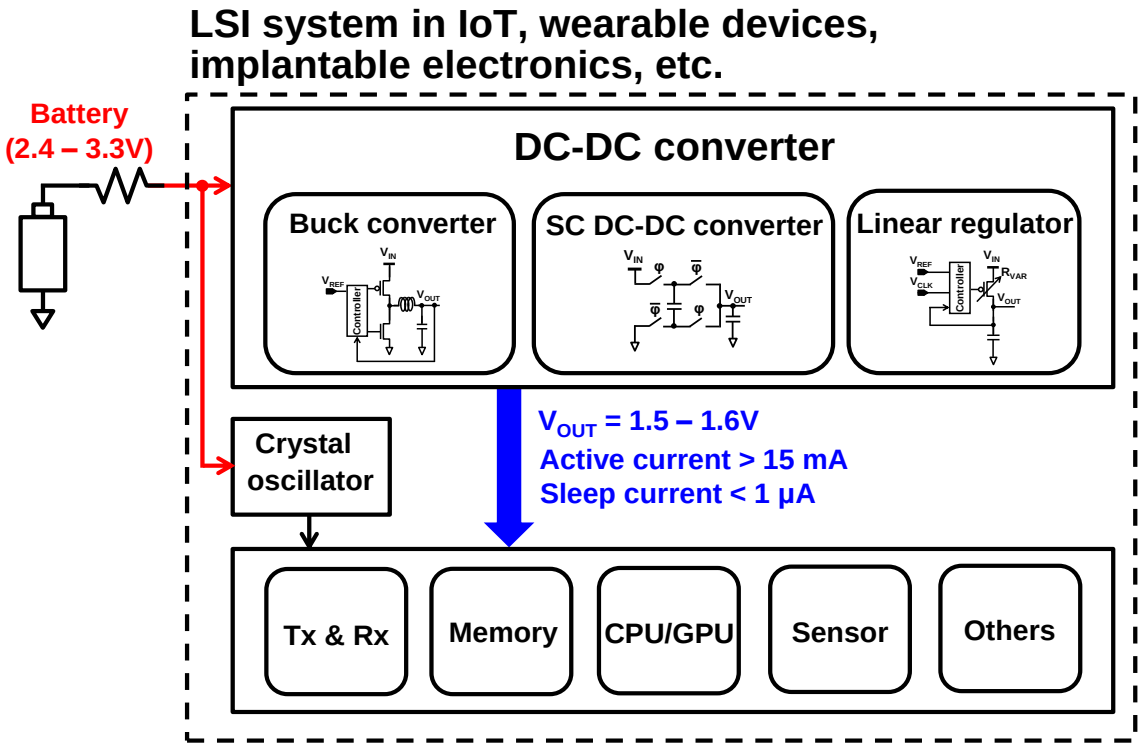

Fig. 1.1. Energy-efficient LSI system for IoT, wearable devices, and implantable electronic.

1.2 Thesis Contribution and Organization

This thesis provides design techniques and theoretical analysis for improving the sleep mode conversion efficiency of a DC-DC converter for wide-current applications. The contribution of this thesis focuses on solving the power consumption limitation caused by the analog circuits in a DC-DC converter, and analyzing the converter properties such as the converter stability, the output voltage ripple, and the output under a fluctuation of the load. The power-law frequency scaling scheme is proposed to optimize the power consumption and the output voltage ripple. Considering all types of DC-DC converters including L (inductive), C (capacitive), and R (resistive), buck converter, SC DC-DC converter, and linear LDO are designed and implemented with the power-law frequency scaling scheme. Almost flat conversion efficiency of the DC-DC converters can be achieved over a wide load current condition. The possible applications are IoT, wearable devices, and implantable electronics. This thesis is organized with 5 chapters, and the organization is illustrated in Fig. 1.2.

Chapter 2 describes the newly proposed clocked hysteresis control scheme with power-law frequency applied to a buck converter. Buck converters can achieve high conversion efficiency and a good adjustability of the output voltage level by controlling the duty cycle. In addition, adapting a hysteresis control, buck converters inherently provide a high output voltage response speed when the load changes [1.8]. Therefore, buck converters are quite suitable for wide-current range applications powered by a battery such as IoT that the load current changes significantly from a sleep mode to an active mode. A buck converter is proposed and designed in this chapter. The improvement

of light load efficiency for a sleep mode and an almost flat conversion efficiency are achieved by scaling the clock frequency dynamically achieved by the power-law frequency scaling. The quite wake-up operation is also achieved by the proposed clocked hysteresis control. The theoretical expressions for the frequency stability, power consumption, and output voltage ripple are derived in this chapter. At the end of this chapter, a prototype design with measurement results is given to verify the proposed control scheme and analysis.

Chapter 3 presents a 2:1 switched-capacitor DC-DC converter implemented with the power-law frequency scaling scheme. By applying the power-law frequency scaling scheme, the continuously-on error amplifier and the high frequency oscillator used in a conventional switched-capacitor DC-DC converter can be removed. As a result, there is no DC power consumed by the error amplifier. The conversion efficiency of the converter can be improved especially in the sleep mode and be flat over a wide load current range. Experimental results show that the converter achieves an almost flat conversion efficiency that is higher than 87.5% over a load current range from 600 nA to 150 μA. In addition, the conversion efficiency in μA order load conditions is improved and the peak efficiency is 94.9% when the load current is 5 μA.

Chapter 4 introduces a design of digital low-dropout (LDO) regulator with the power-law frequency scaling scheme. A system topology is proposed and a simulation is conducted to verify the operation. The power-law frequency scaling scheme is applied to a digital LDO to eliminate the large quiescent current consumed by the clock comparator with high clock frequency. The target of this chapter is to optimize the clock frequency

and current efficiency in a digital LDO with the load conditions for a wide load current range.

Finally, a conclusion of this thesis is presented in Chapter 5.

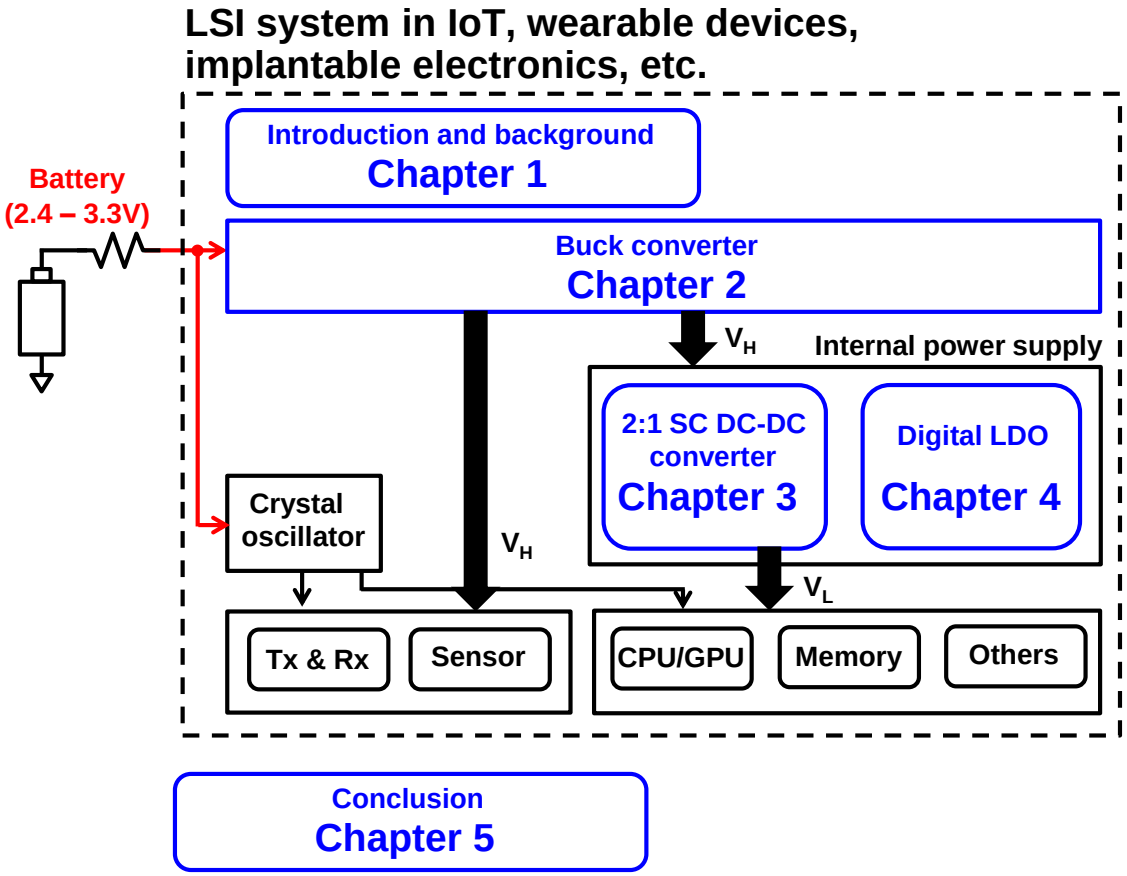

Fig. 1.2. Thesis organization.

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Chapter 2: Clocked Hysteresis Buck Converter with Power-Law Frequency Scaling

2.1 Introduction of Buck Converter

To convert an input with high voltage, such as a battery, to a well-regulated low output voltage provided to LSI systems, a buck converter is an attractive solution because it provides high conversion efficiency, good output voltage adjustability, and large output power density [2.1]. A simplified block diagram of a buck converter is shown in Fig. 2.1 [2.2]. The converter output V_{OUT} is sensed by resistors R_1 and R_2 that generate a feedback voltage V_{FB}. The difference between V_{FB} and V_{ref} is amplified by an error amplifier and used to be compared with a triangular ramp signal V_{RAMP}. The comparator generates a PWM pulse signal to drive power switch Q_1. A square voltage waveform swinging from V_{IN} to about -0.8 V clamped by the diode D_1 is performed at V_1. By controlling the on-time of Q_1, and extracting the DC component of V_1 by a low-pass filter formed by L_O and C_O, a clear DC voltage V_{OUT} can be expressed as:

$$V_{OUT} = D\,V_{IN},\ \mathrm{D} = \frac{T_{ON}}{T} \tag{2.1}$$

where T is the switching period, T_{ON} is the on-time of Q_1, and the switching duty cycle is denoted as D. Therefore, the output voltage can be easily adjusted by controlling the switching duty cycle of Q_1.

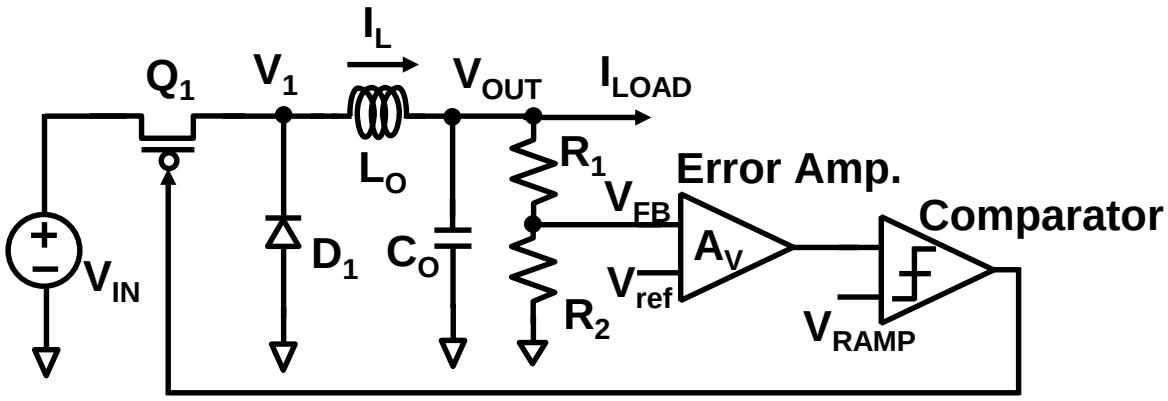


Fig. 2.1. Simplified block diagram of a conventional buck converter.

For wide-current range applications, the buck converter operates in discontinuous conduction mode (DCM) when the load changes from a heavy load (active mode) to a light load (sleep mode). Continuous conduction mode (CCM) and DCM are indicated by the inductor current waveform [2.3] as shown in Fig. 2.2. Because there is no reverse current allowed due to the diode D_1, the inductor current stays around 0 achieving DCM operation. The buck converter starts to operate in DCM when the load current is less than half of the inductor peak current. The boundary of CCM and DCM can be expressed as:

$$I_{LOAD} = \frac{1}{2} I_{L(peak-peak)} = \frac{V_{IN}-V_{OUT}}{2L_O} \mathrm{DT} \quad (2.2)$$

Equation (2.2) indicates the boundary of CCM and DCM is determined by the input and output voltage, inductor value, switching frequency, and load current I_{LOAD}.

In modern integrated buck converters, however, D_1 is replaced by a NMOS transistor to eliminate the -0.8 V voltage drop and improve the conversion efficiency. Zero-current detection (ZCD) circuit is required to achieve DCM operation [2.4] [2.5] to improve the conversion efficiency over a wide-current range. Nevertheless, the minimum output

current of the buck converters with ZCD are limited to 100 μA and 50 μA in [2.4] and [2.5], respectively because the conversion efficiency degrades steeply in μA order. Both converters shown in [2.4] and [2.5] are not suitable for the sleep mode specified by the BLE applications like IoT sensor nodes.

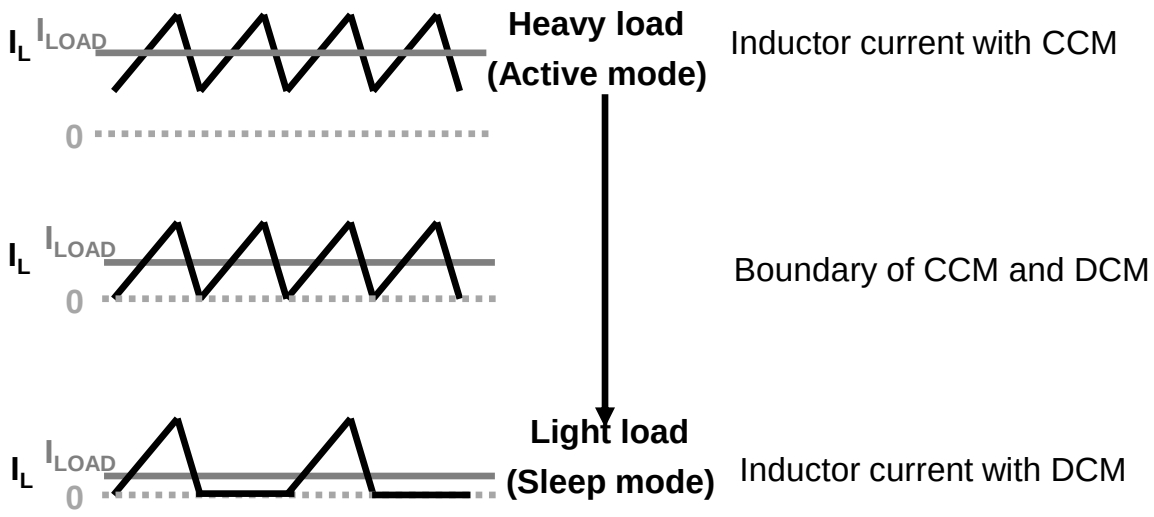
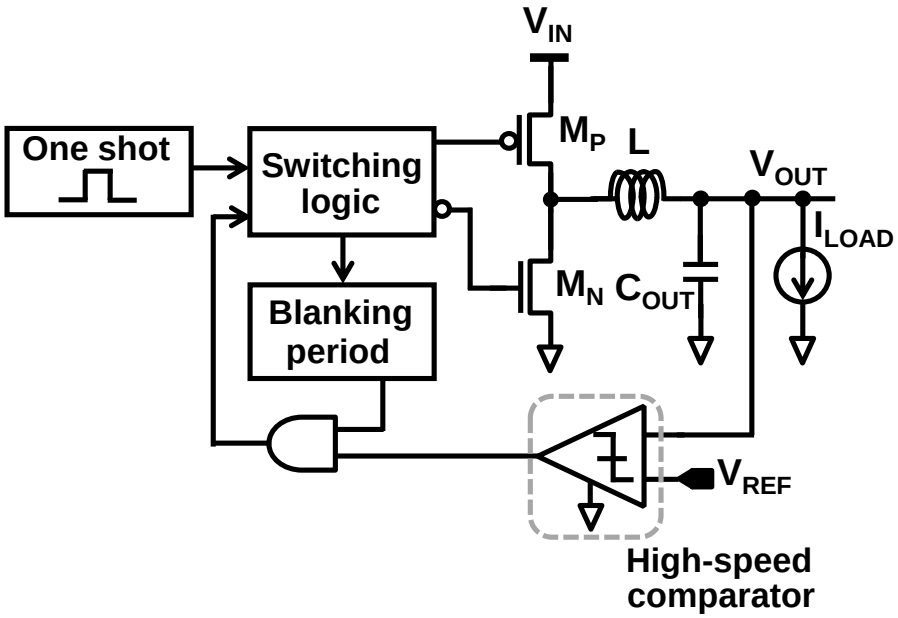


Fig. 2.2. Buck converter inductor current waveform in CCM, DCM, and the boundary.

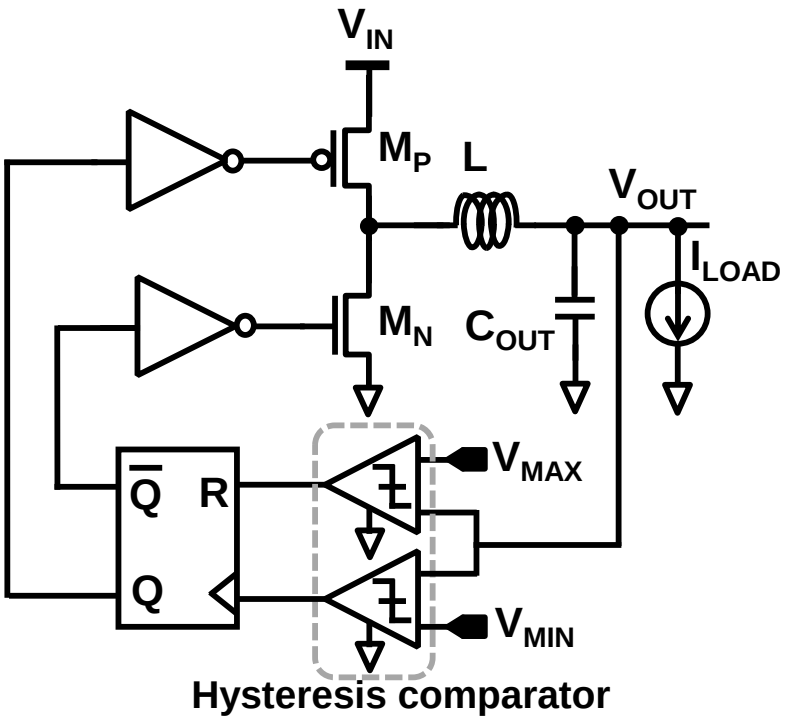
Thus far, several commercial products and publications on buck converters for wide-current range applications have been reported. The conversion efficiency, however, degrades rapidly when the load current decreases to μA order [2.6]. A tri-mode buck converter consisting of a digital pulse-width modulation (DPWM), a pulse-frequency modulation (PFM), and an asynchronized mode (AM) [2.7] improves the conversion efficiency and extends the possible load range down to 100 nA. The conversion efficiency, however, is still lower than 80% when the converter operates in the AM for a 1-μA load. An adaptive application of bias current for analog circuits depending on the loading conditions [2.8] improves the conversion efficiency when the load current is low. The

quiescent current in [2.8] was as low as 110 nA with low output voltage ripple performance. The conversion efficiency, however, was still limited to 78% when the load current was 1 μA. In contrast, the buck converter proposed in [2.9] achieved 87% conversion efficiency at 1 μA, but it did not supply sufficient load current in an active mode and did not support a fast wake-up operation required for IoT, wearable devices, and implantable applications.

Considering there are two basic control schemes for a buck converter operating in the DCM: constant-on-time (COT) control and hysteresis control. The two schemes are shown in Figs. 2.3(a) and (b), respectively. In COT control [2.10], a high-speed comparator is employed to compare the output voltage with a reference voltage, V_{REF}. A pulse signal with a fixed pulse width is applied to the power stage triggered by the comparator output signal. The output voltage is regulated as $V_{OUT} = V_{REF}$, and the voltage error between V_{REF} and V_{OUT} is monitored continuously. On the other hand, hysteresis control uses hysteresis comparators to regulate the output voltage within a designed hysteresis voltage window, an expression indicating the hysteresis behavior is shown in the appendix at the end of this chapter. Hysteresis control inherently provides a high output voltage response speed when I_{LOAD} changes [2.11]. This is preferable, especially when a quick wake-up operation is required to conserve the energy of a system and to reduce the wake-up energy consumption. Both schemes, however, consume DC current because they require continuously-on comparators to monitor the output voltage. A typical circuit schematic of the continuously-on comparator in Figs. 2.3(a) and (b) is shown in Fig. 2.4 [2.12] [2.13].



(a)



(b)

Fig. 2.3. Conventional control schemes for a buck converter operating in DCM. (a) Constant-on-time control. (b) Hysteresis control.

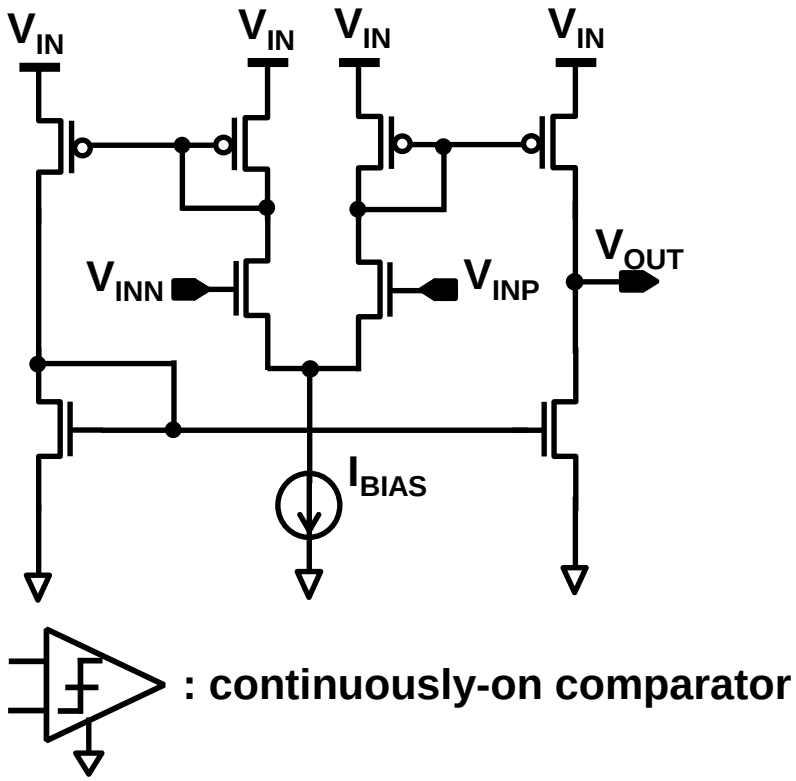
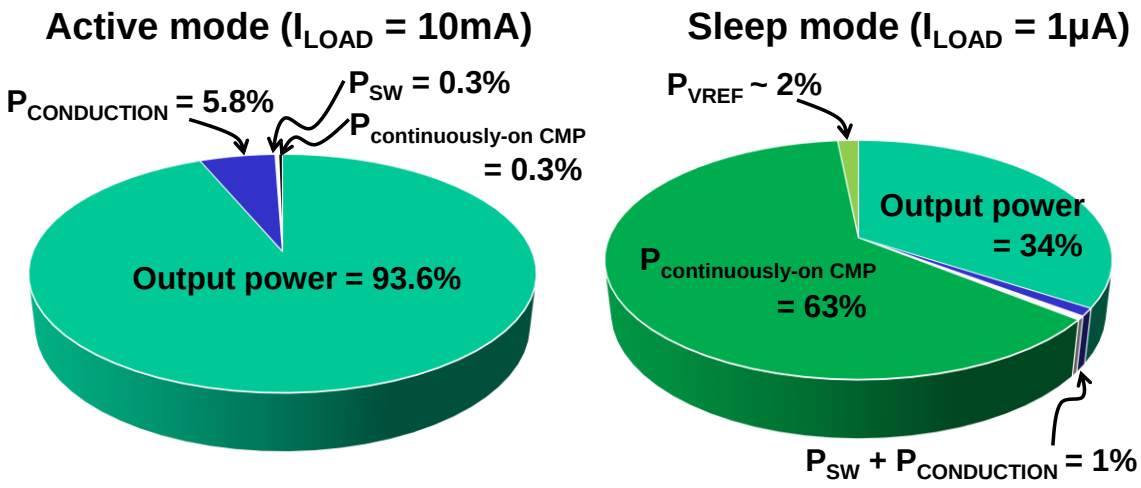


Fig. 2.4. Typical circuit schematic and symbol of continuously-on comparator.

To clarify the power distribution of the typical hysteresis buck converter shown as Fig. 2.3(b), a simulation assuming that V_{IN} is 3 V and V_{OUT} is 1.6 V with a 20-mV hysteresis voltage window and 1-μA bias current is conducted. $P_{CONDUCTION}$ and P_{SW} denote the conduction and switching losses of the converter, respectively. P_{VREF} denotes the power consumption of a reference voltage generator V_{REF}. Fig. 2.5(a) shows the power distribution in a sensor node in an active mode when I_{LOAD} is 10 mA. In a sleep mode where I_{LOAD} is 1 μA, as specified by BLE, the power consumption of the continuously-on comparator accounts for 63% of the total power consumption, limiting the conversion efficiency is only 34%, as shown in Fig. 2.5(b), even though the power consumption of the reference voltage can be reduced to 10-nA order [2.14].



(a) (b)

Fig. 2.5. Simulated power dissipation of typical hysteresis buck converter. (a) Active mode. (b) Sleep mode.

2.2 System Architecture

To improve the conversion efficiency in the sleep mode, a clocked hysteresis control (CHC) buck converter with a power-law frequency scaling scheme is proposed in this paper. Replacing the continuously-on comparator used in conventional hysteresis control by a clocked comparator, as shown in Fig. 2.6 [2.15], the buck converter consumes no DC current in the comparators. The proposed power-law frequency scaling scheme dynamically adjusts the clock frequency for the clocked comparator depending on the load current to stabilize the output voltage. As a result, the comparator power consumption becomes proportional to the load current. The buck converter can achieve almost flat conversion efficiency over the whole load current range specified by BLE while inheriting a quick wake-up response of hysteresis control. Additionally, the buck converter operates in DCM over the whole load current range because the low load current specified by the BLE while using an inductor with small inductance. The operating inductor current is shown in Fig. 2.7. The switching frequency of the inductor current is modulated according to the load current.

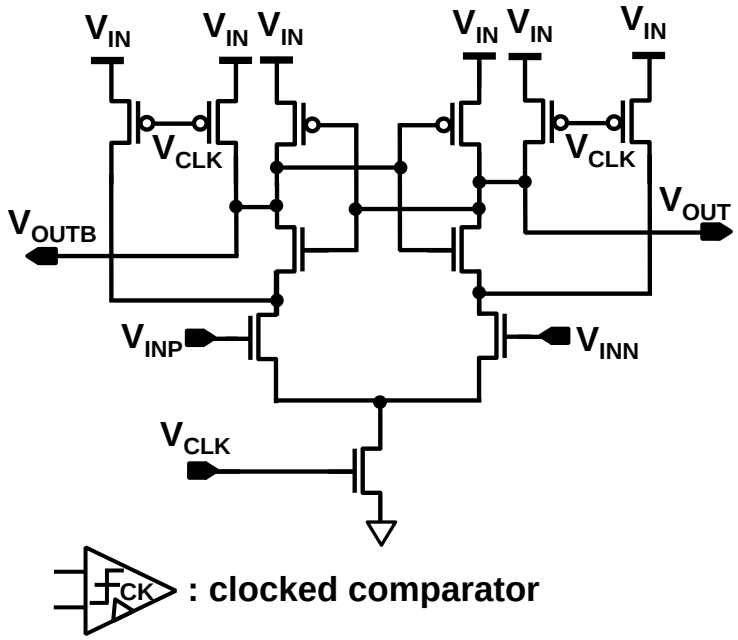


Fig. 2.6. Typical circuit schematic and symbol of clocked comparator.

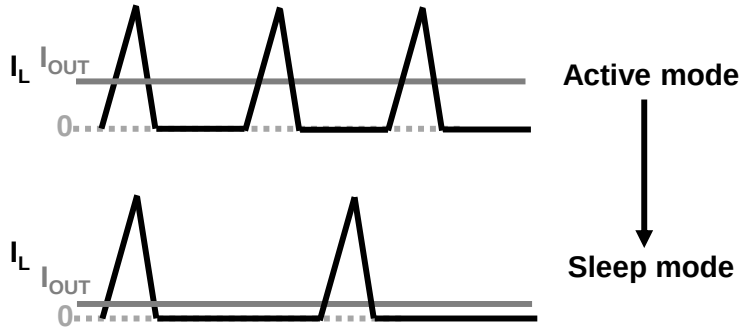


Fig. 2.7. Inductor current waveform of the proposed buck converter operating in DCM.

A system block diagram of the proposed CHC buck converter is shown in Fig. 2.8. The target input voltage ranges from 2.4 V to 3.3 V, allowing it to be a battery-based system. The output voltage is set to be 1.5 V to 1.6 V to power LSI circuits and systems with BLE communication. Compared with the conventional hysteresis buck converter, the continuously-on comparator is replaced by a clocked comparator X_1. Comparators X_2

and X_3 are power-gated comparators whose circuit schematic and symbol are shown in Fig. 2.9. Note that for X_3, a topology consisting of a PMOS input differential pair with an NMOS active load is applied because X_3 compares V_X with ground. Using an enable signal, X_2 and X_3 are turned on in a short period of time in every switching cycle. The bias point of the current mirror and the output are reset to ground and logic "1", respectively, by the enable signal EN. Therefore, no DC current is consumed when the comparators are disabled. X_1 and X_2 are designed to regulate V_{OUT} within a hysteresis voltage window specified by voltage references V_{MAX} and V_{MIN}. The dependence of the output voltage ripple on the hysteresis voltage window will be discussed in Section 2.3. In addition, comparator X_3 is used for zero-current detection (ZCD), preventing reverse inductor current loss. X_3 compares V_X with ground and generates a signal to turn off the NMOS power transistor M_N when the inductor current reaches zero. An analog-type comparator is necessary because X_2 and X_3 should operate sufficiently quickly to reduce the output voltage ripple and to prevent reverse inductor current, respectively. Since there is no need for X_2 and X_3 to be turned on all the time, they are activated for a short time when the enable signal for each comparator is on.

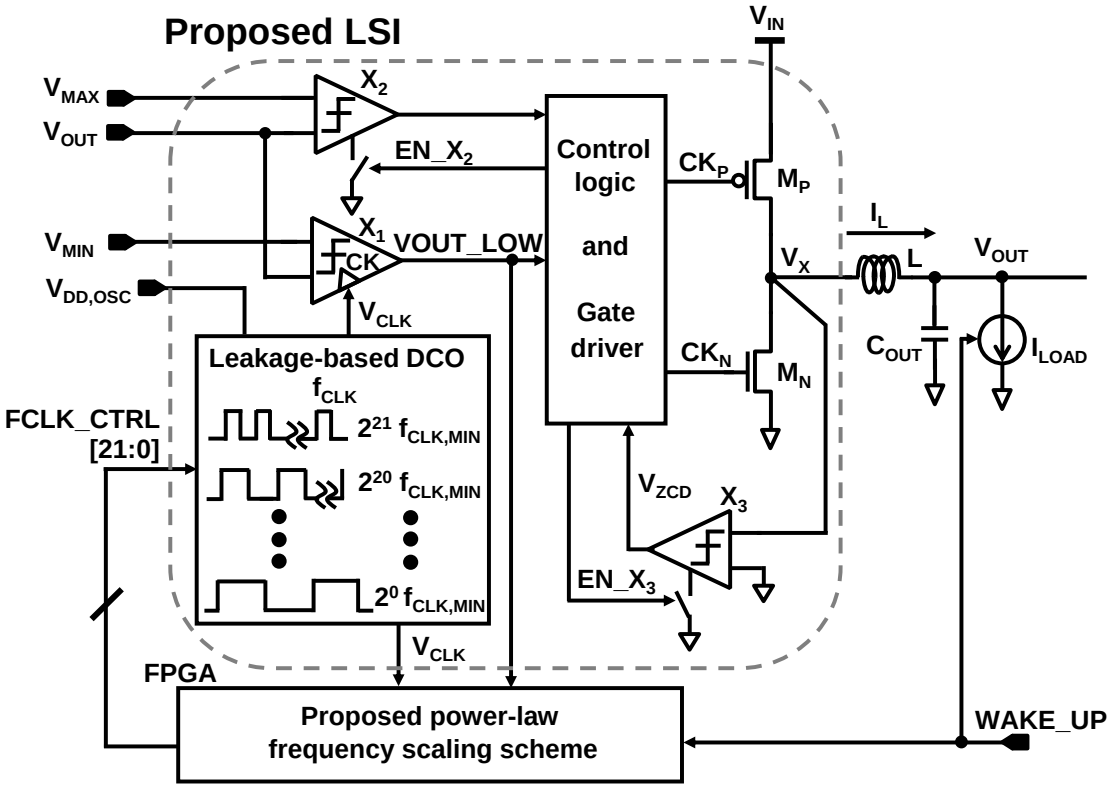


Fig. 2.8. System block diagram of proposed clocked hysteresis control (CHC) buck converter with power-law frequency scaling scheme.

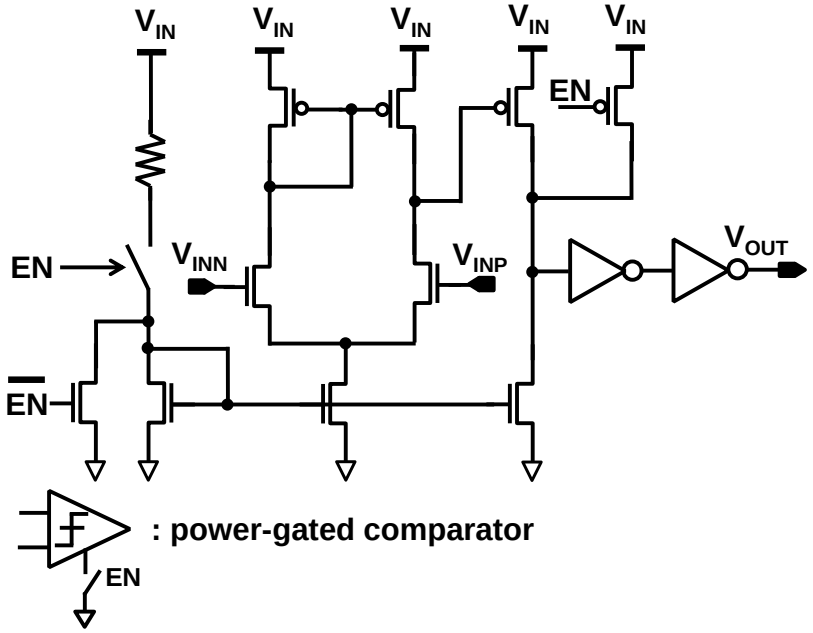


Fig. 2.9. Circuit schematic and symbol of power-gated comparator used in Fig. 2.8.

A leakage-based digitally controlled oscillator (DCO) is implemented to provide a clock signal V_{CLK} to X_1. The frequency of V_{CLK}, f_{CLK}, can be adjusted from $2^0 f_{CLK,MIN}$ to $2^{21} f_{CLK,MIN}$ by 22-bit clock frequency control signals named FCLK_CTRL [21:0], where $f_{CLK,MIN}$ denotes the lowest clock frequency. FCLK_CTRL [21:0] are provided by an FPGA for an experiment but can be easily implemented on a chip. The power-law frequency scaling scheme is implemented by the FPGA. V_{CLK} and the output signal of X_1, VOUT_LOW, are applied to the FPGA to generate FCLK_CTRL. If f_{CLK} is too slow considering the load condition, FCLK_CTRL is increased by 1 bit, making f_{CLK} double. On the other hand, if f_{CLK} is too fast for the load condition, FCLK_CTRL is decreased by 1 bit, making f_{CLK} a half. In later section, the exact meanings of 'too slow' and 'too fast' will be described. Therefore, f_{CLK} is controlled in accordance with the load conditions. Only basic logic elements are used on the FPGA and the clock of the FPGA is also provided by V_{CLK}. By a simple calculation [2.16], the employed gate count on the FPGA is about 700 gates, which consume less than 1 nW when I_{LOAD} is 500 nA, f_{CLK} is 15 Hz, and V_{IN} is 3 V, which is negligible compared with the power loss in a sleep mode.

Fig. 2.10(a) shows the operating timing diagram of the proposed CHC buck converter. When V_{OUT} becomes lower than V_{MIN}, which is detected by X_1, VOUT_LOW is logic "1" and PMOS power transistor M_P is turned on, which conducts an inductor current and charges up the output voltage. At the same time, comparator X_2 is enabled and starts comparing V_{OUT} with V_{MAX}. Once V_{OUT} reaches V_{MAX}, M_P is turned off and NMOS power transistor M_N is turned on. The turn-on signal for M_N is also used to disable X_2 and enable X_3. M_N is turned off when the inductor current reaches zero, which is detected by

the ZCD comparator X_3. X_3 is disabled automatically when M_N is turned off. X_2 and X_3 are turned on during $T_{ON,X2}$ and $T_{ON,X3}$, respectively, in every power stage switching period T_{SW}. Therefore, applying the proposed control scheme, comparators X_1, X_2, and X_3 are all "clocked" and consume no DC power.

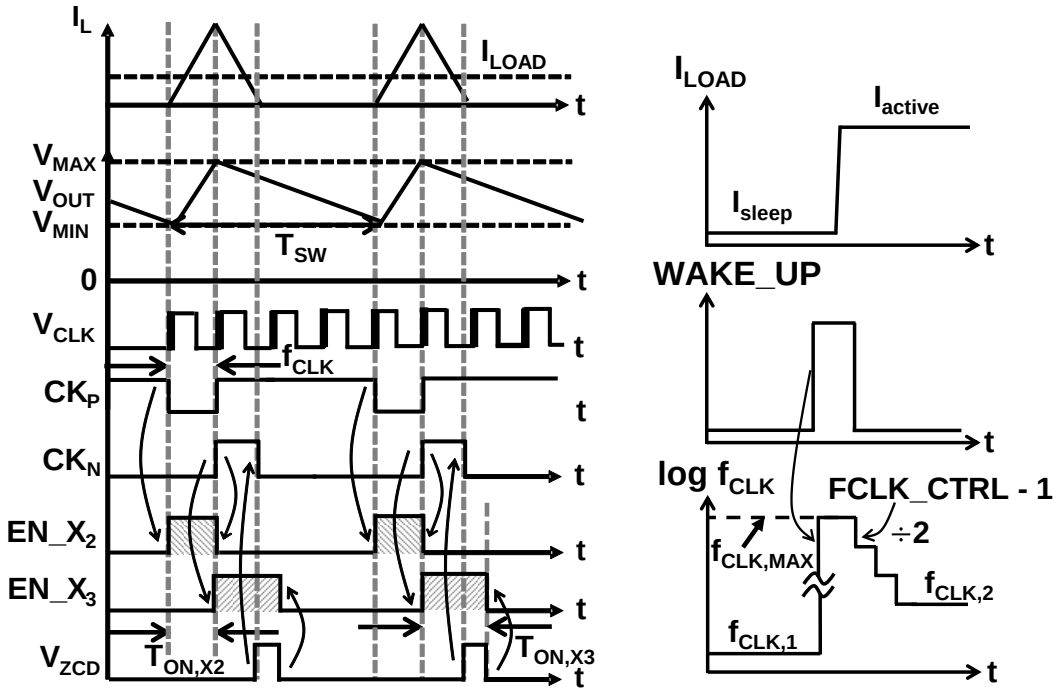


Fig. 2.10. (a) Operating timing diagram and relative control signals in CHC buck converter. (b) Load wake-up operation.

The conduction and switching losses in the buck converter are estimated as follows:

$$P_{conduction} = I_{L,RMS}^2 \cdot (R_{DS,ON} + R_{ESR}) \tag{2.3}$$

$$P_{switching} = \alpha \cdot f_{SW} \cdot C_{TOTAL} \cdot V_{IN}^2 \tag{2.4}$$

where $I_{L,RMS}$ is the root mean square of the inductor current, $R_{DS,ON}$ is the on-resistance of power transistors M_P and M_N, R_{ESR} is the equivalent series resistance of the inductor,

f_{SW} is the switching frequency of the power stage, V_{IN} is the input voltage, C_{TOTAL} is the total capacitance at the gates of M_P and M_N, and α is the average activity factor. In addition, the power consumption of X_2 and X_3 can also be estimated as

$$P_{comp.,X2,3} = \frac{1}{T_{SW}} \int_0^{T_{ON,X2,3}} V_{IN}\, I(t) dt \tag{2.5}$$

where $1/T_{SW}$ is the switching frequency of the power stage f_{SW}, $T_{ON,X2}$ and $T_{ON,X3}$ are the turn-on time of comparators X_2 and X_3, respectively, and I(t) is the current consumed by the comparator. As indicated in (2.3), (2.4), and (2.5), by adopting pulse frequency modulation (PFM) in DCM operation, the conduction loss, switching loss, and power consumption of X_2 and X_3 can be scaled with I_{LOAD} because all of them are proportional to f_{SW}. The power consumption of clocked comparator X_1, however, is proportional to the clock frequency f_{CLK}. An appropriate clock frequency is required to regulate the output voltage while keeping the power consumption of X_1 low. Using a higher clock frequency results in higher power consumption of X_1 and the controller circuits, thus losing the benefit of using the clocked comparator. On the other hand, applying a lower clock frequency induces a large voltage ripple at V_{OUT}. A power-law frequency scaling scheme is proposed to adjust the clock frequency f_{CLK} in the CHC buck converter, making f_{CLK} also proportional to I_{LOAD}. Therefore, the conduction loss and switching loss of the power stage, and the controller power consumption including the comparators are all scaled with I_{LOAD}. Thus, the CHC buck converter can achieve almost flat conversion efficiency over a wide range of loads including a sleep mode.

For the wide load current range applications such as IoT, the buck converter must

support quick wake-up operation when the system operation changes from a sleep mode to an active mode. The wake-up operation of the CHC buck converter is illustrated in Fig. 2.10(b). The load current as the wake-up threshold can be set depending on applications for power and output voltage drop optimization. When the system is woken up, an external wake-up signal WAKE_UP synchronized with a change in I_{LOAD} is applied to the FPGA or a controller on the chip if the logic is implemented on a chip. The current frequency control bits, FCLK_CTRL [21:0], are reset by WAKE_UP, making f_{CLK} change from the current frequency, f_1, to the highest frequency, $f_{CLK,MAX}$, that is, 2^{21} $f_{CLK,MIN}$. Asynchronized logics can be designed so FCLK_CTRL [21:0] can be reset immediately once WAKE_UP is applied. With the proposed frequency scaling scheme, the clock frequency f_{CLK} gets half and half step by step, and automatically settles to a new value, f_2, according to the loading condition. Therefore, the buck converter can achieve fast wake-up operation.

2.3 Theoretical Analysis of Power-Law Frequency Scaling Scheme

A flowchart of the proposed frequency scaling scheme is shown in Fig. 2.11. At the start of the control, the clock frequency f_{CLK} is set to the highest value, $2^{21} f_{CLK,MIN}$, and the V_{OUT} checking counter implemented on the FPGA is reset to 0. If $V_{OUT} > V_{MIN}$ at the clock edge, meaning that VOUT_LOW is logic "0", the counting number n increases by 1, and the process restarts. On the other hand, if $V_{OUT} < V_{MIN}$ at the clock edge, VOUT_LOW is logic "1", making the buck converter start a new switching cycle. At the same time, the counter number n is read out and compared with two preset boundaries, n_1 and n_2, where $n_2 > n_1$. $n \leq n_1$ indicates that the output voltage V_{OUT} crosses V_{MIN} earlier than expected, that is, I_{LOAD} is high but the clock frequency f_{CLK} is too low. M_P should be turned on frequently to transfer energy from V_{IN} to V_{OUT}. Therefore, f_{CLK} is multiplied by m_1 and the algorithm restarts. $n > n_1$ and $n > n_2$, means that f_{CLK} is too high. Clocked comparator X_1 checks V_{OUT} several times and turns on M_P only once. In this case, f_{CLK} is divided by m_2. This process operates continuously, and the V_{OUT} checking counter number n settles to a value larger than n_1 and smaller than n_2, i.e., $n_2 > n > n_1$. In the steady state, an appropriate f_{CLK} is found by the proposed power-law frequency scaling scheme that can stabilize the output voltage of the buck converter, and f_{CLK} is a multiple of the switching frequency f_{SW}. Therefore, the power consumption of X_1 is also proportional to I_{LOAD} because f_{CLK} is proportional to f_{SW}. These three conditions of n including the frequency scaling and the relation between f_{CLK} and I_{LOAD} are summarized in Table 2-1.

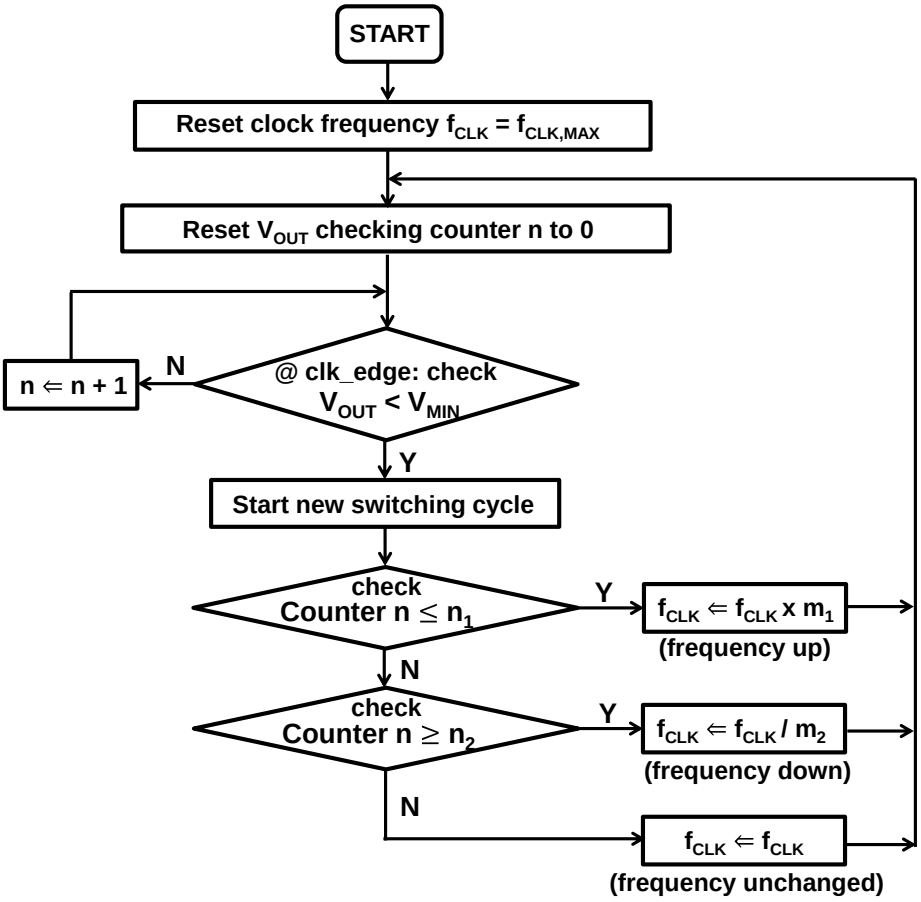
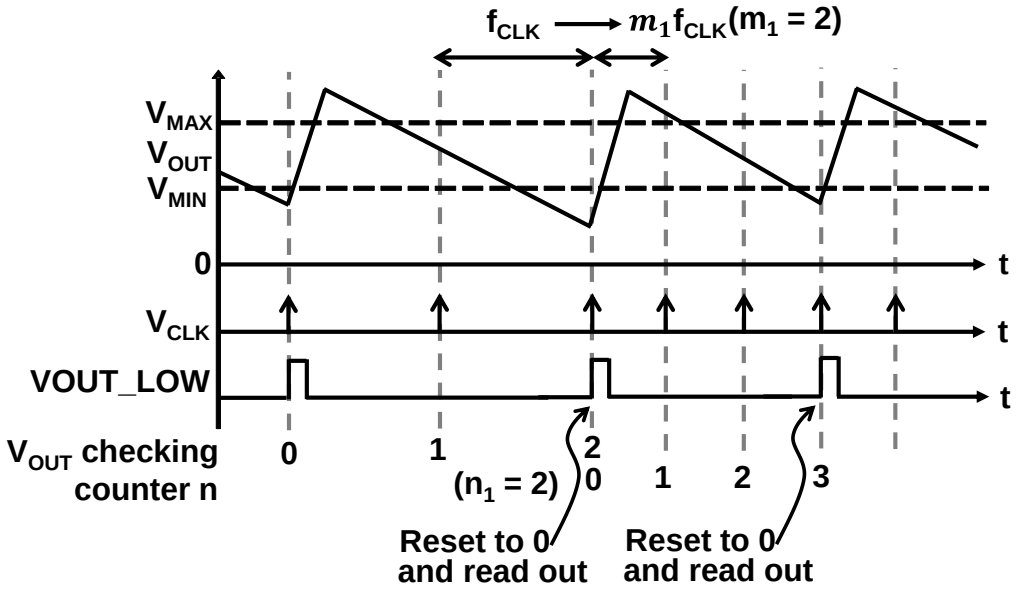


Fig. 2.11. Frequency control flowchart of proposed frequency scaling scheme.

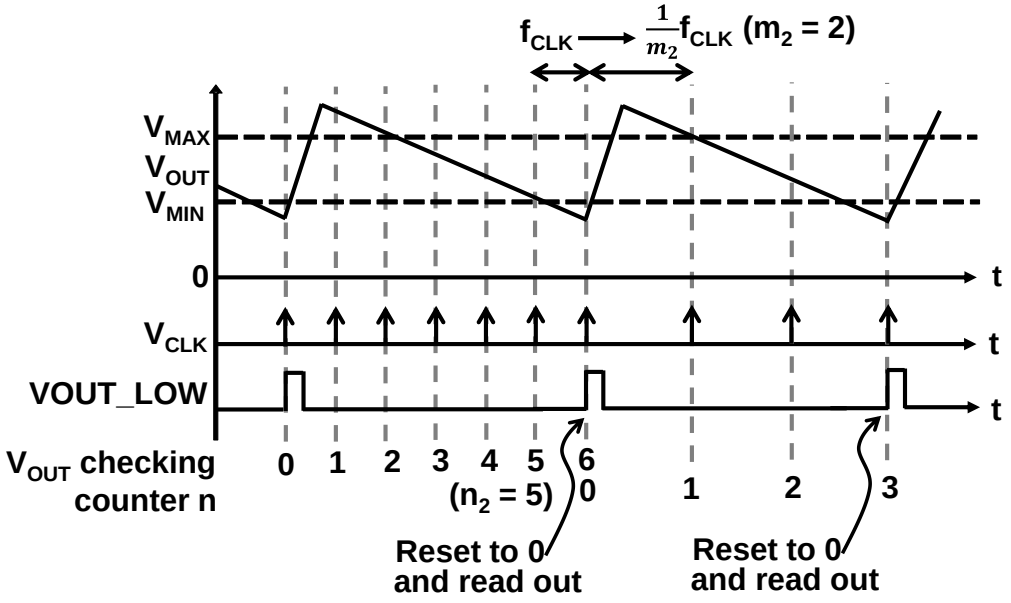
Table 2-1. Frequency Scaling of f_{CLK} and Dependence of f_{CLK} on I_{LOAD} Expressed Using n, n_1, and n_2.

V_{OUT} checking counter n @$V_{OUT} < V_{MIN}$	Current f_{CLK} @ I_{LOAD}	Frequency multiply/divide
$n \leq n_1$	Too low	$\times m_1$
$n_2 > n > n_1$	Appropriate	unchanged
$n \geq n_2$	Too high	$\div m_2$

An example of implementation showing the output waveform, the clock signal, VOUT_LOW, and the V_{OUT} checking counter n in the time domain when $m_1 = m_2 = 2$, $n_1 = 2$, and $n_2 = 5$ is illustrated in Fig. 2.12. In Fig. 2.12(a), V_{OUT} is lower than V_{MIN} when $n = 2 \leq n_1$ in the first switching period. This is the case when the initial f_{CLK} is too low possibly generating a larger output voltage ripple. Thus, f_{CLK} is doubled ($\times m_1$). On the other hand, when the initial f_{CLK} is too high, V_{OUT} is lower than V_{MIN} when $n > n_2$, resulting in the consumption of more power than appropriate, which is the case shown in Fig. 2.12(b). f_{CLK} becomes halved ($\div m_2$) to reduce the power consumption of the comparator. In the following sections, the design parameters that make the CHC buck converter work properly are determined. Then, the frequency stability, the output voltage ripple, and the effect of the load current fluctuation on V_{OUT} are derived theoretically.



(a)



(b)

Fig. 2.12. Implementation example indicates the buck converter output waveform, clock signal, VOUT_LOW, and V_{OUT} checking counter. (a) When the initial f_{CLK} is too slow, f_{CLK} is doubled. (b) When the initial f_{CLK} is too fast, f_{CLK} is halved. The frequency multiply/divide ratio, output voltage ripple, and the dependence of output voltage ripple and the minimum output voltage on the load current are analyzed theoretically in the following subsections.

2.3.1 Frequency Multiply/Divide Ratio Decision

Parameters m_1, m_2, n_1, and n_2 illustrated in Fig. 2.11 should be determined to make the frequency scaling scheme operate properly. As indicated by Fig. 2.11, f_{CLK} can be expressed as

$$f_{CLK} = \frac{{m_1}^q}{{m_2}^p} f_{CLK,MIN} \tag{2.6}$$

$$m_1 = {m_2}^\gamma \tag{2.7}$$

where p and q denote the corresponding decision cycles and m_1, m_2, p, and q are natural numbers. Considering that the frequency scaling scheme may induce harmonics that interfere with other sensitive circuits such as RF blocks on the same chip, the relation between m_1 and m_2 is expressed as (2.6), where γis designed as a natural number, that is, larger than or equal to 1. Therefore, the harmonics generated by the frequency scaling scheme are located at integral multiples of $f_{CLK,MIN}$ in the frequency spectrum. Replacing m_1 in (2.6) by (2.7), f_{CLK} can be expressed as

$$f_{CLK} = {m_2}^N f_{CLK,MIN},\ N = \gamma q - p \tag{2.8}$$

where N is also a natural number. As indicated by (2.7), any natural numbers m_1, m_2, and γ can be chosen for the power-law frequency scaling scheme. A higher m_1 results in a high tracking speed for the I_{LOAD} wake-up operation, but dissipates more power in every frequency transition. On the other hand, a higher m_2 can reduce power consumption during the transient. However, according to the analysis in Section 2.3.3, a higher value of m_2 rapidly reduces the clock frequency, which induces a large output voltage drop and an unacceptable output voltage ripple. Therefore, except 1, the minimum value of a natural number, 2, is chosen for m_2, resulting in frequency scaling of 2^N. Depending on the application, m_2 can be designed to be 8 or higher for a high response speed of load changing. In a sleep mode, however, a minimum value of 2 is designed for m_2 to reduce the power overhead. The combination of (m_1, m_2) = (2, 2) results in double-half frequency scaling [2.18], which is a special case in the proposed power-law frequency scaling scheme.

n_1 and n_2 should be designed to prevent f_{CLK} oscillating between $f_{CLK} \times m_1$ and $f_{CLK} \div m_2$. The constraints on n_1 and n_2 can be represented by

$$n_2 \times \frac{1}{m_2} > n_1 \tag{2.9}$$

$$n_1 \times m_1 < n_2 \tag{2.10}$$

Therefore, f_{CLK} is stable between n_1 and n_2, and its relation with f_{SW} in the steady state can be expressed as

$$f_{CLK} = K \times f_{SW} \tag{2.11}$$

where K is a natural number and a function of n_1 and n_2. f_{CLK} is determined by the power-law frequency scaling scheme according to the load conditions, making the CHC buck converter able to operate stably without f_{CLK} oscillation. Under the same I_{LOAD} condition, choosing a larger value of K results in a higher f_{CLK}. An additional benefit here compared with a conventional hysteresis control is that the switching frequency f_{SW} is fixed to 1/K f_{CLK}. Using the frequency scaling scheme, the power consumption of the clocked comparator can be adjusted to be proportional to I_{LOAD}. The simulated dependence of the power consumption of X_1, X_2, and X_3 on f_{CLK} when K = 3 is shown in Fig. 2.13. Obviously, the power consumption of X_1, X_2, and X_3 can all be scaled with I_{LOAD}.

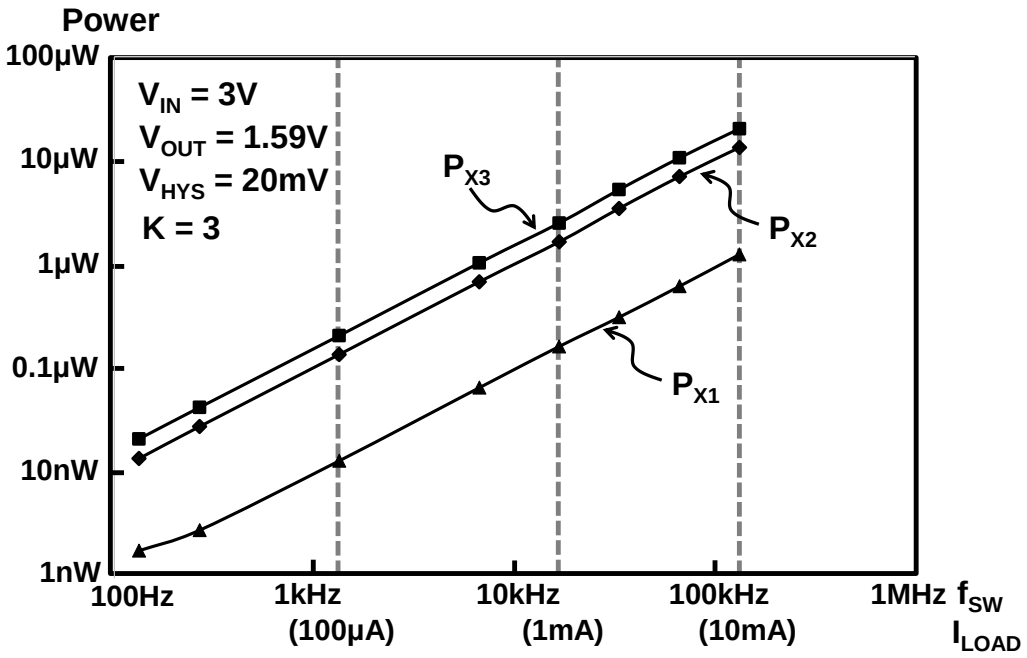


Fig. 2.13. Simulated dependence of power consumption of comparators (X_1, X_2, and X_3) on f_{SW} and I_{LOAD}.

2.3.2 Analysis of Output Voltage Ripple

By applying the proposed power-law frequency scaling scheme in the clocked hysteresis control (CHC), the buck converter employs no continuously-on comparators, resulting in no consumption of DC current by the comparators. The output voltage ripple $V_{OUT,RIPPLE}$, however, is enlarged because comparator X_1 only compares the output voltage with V_{MIN} at the clock edge. In addition, the "real" minimum output voltage level $V_{OUT,MIN}$, which is lower than V_{MIN}, should be analyzed to ensure that the lowest output voltage level is not lower than the specification value. By the proposed theoretical analysis, design guidelines for V_{MAX} and V_{MIN} are provided so that the CHC buck

converter can achieve competitive performance with a conventional buck converter while improving the conversion efficiency in a sleep mode.

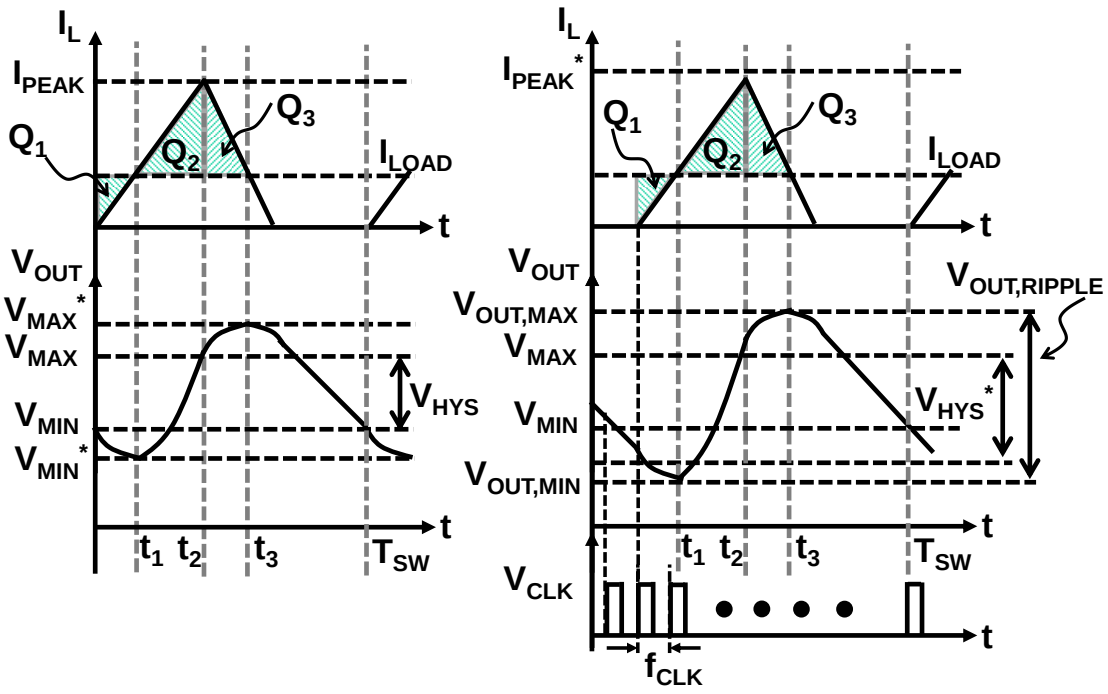
To analyze the voltage ripple of the CHC buck converter, the voltage ripple of conventional hysteresis control is derived first. The inductor current waveform I_L, I_{LOAD}, and V_{OUT} for a conventional hysteresis control buck converter are illustrated in Fig. 2.14(a). I_{PEAK} is the peak inductor current value, $V_{MAX} - V_{MIN}$ is the hysteresis window, denoted as V_{HYS}, and I_{LOAD} is the load current. Because of the time delay between the inductor current and the output voltage, the maximum and minimum output voltages, denoted as V_{MAX}^* and V_{MIN}^*, are higher and lower than V_{MAX} and V_{MIN}, respectively. Therefore, $V_{MAX}^* - V_{MIN}^*$ represents the output voltage ripple. When the output capacitor ESR is neglected for simplicity, the peak inductor can be expressed as [2.18]

$$I_{PEAK} = I_{LOAD} + \sqrt{{I_{LOAD}}^2 + 2C_{OUT}\alpha_1 V_{HYS}} \tag{2.12}$$

where $\alpha_1 = (V_{IN} - V_{OUT})/L$ and $V_{HYS} = V_{MAX} - V_{MIN}$. Using charge balance analysis [2.19] in combination with (2.12), the output voltage ripple can be expressed in terms of only the given specification parameters of the system such as V_{IN}, V_{OUT}, V_{HYS}, L, C_{OUT}, and I_{LOAD}:

$$V_{OUT,RIPPLE} = \frac{1}{2C_{OUT}}\left({I_{LOAD}}^2 + 2C_{OUT}\alpha_1 V_{HYS}\right)\frac{V_{IN}}{V_{OUT}}\frac{1}{\alpha_1} \tag{2.13}$$

A similar equation can also be found in [2.20], although it involves the switching period and cannot refer to the specification parameters directly.



(a) (b)

Fig. 2.14. Inductor current and output voltage waveform. (a) Conventional hysteresis buck converter. (b) Proposed CHC buck converter with clock timing.

For the applications that the maximum I_{LOAD} ranges from mA to 10-mA order, the $2C_{OUT}\alpha_1 V_{HYS}$ term in (2.12) is much larger than ${I_{LOAD}}^2$ term when a μ-F output capacitor and a μ-H inductor are applied. Therefore, (2.13) can be simplified to

$$V_{OUT,RIPPLE}(0) = V_{HYS} \times \frac{V_{IN}}{V_{OUT}} \tag{2.14}$$

Equation (2.14) provides a simple estimation of the output voltage ripple that is only dependent on V_{IN}, V_{OUT}, and V_{HYS}. This equation is defined as the intrinsic output voltage ripple of a hysteresis buck converter, indicating the theoretical minimum output ripple that it can achieve. In addition, the switching period T_{SW} and I_{PEAK} can also be simplified as follows when $\sqrt{2C_{OUT}\alpha_1 V_{HYS}} > I_{LOAD}$

$$T_{SW} = \frac{C_{OUT}}{I_{LOAD}} V_{HYS} \frac{V_{IN}}{V_{OUT}} \tag{2.15}$$

$$I_{PEAK} = \sqrt{2C_{OUT}\alpha_1 V_{HYS}} \tag{2.16}$$

Equation (2.14), (2.15), and (2.16) can be used to calculate the output voltage ripple, switching period, and peak inductor current very simply when the load current is relatively small compared with I_{PEAK}, which is the usual case in IoT applications. The values of T_{SW} and I_{PEAK} calculated by (2.15) and (2.16) compared with simulation results under different I_{LOAD} are shown in Fig. 2.15. Equations (2.15) and (2.16) match the simulation results well and provide a simple means of calculating T_{SW} and I_{PEAK} for a conventional hysteresis buck converter when I_{LOAD} is much lower than I_{PEAK}. In addition, on the basis of (2.14), (2.15), and (2.16), the voltage ripple of the proposed CHC buck converter can be calculated.

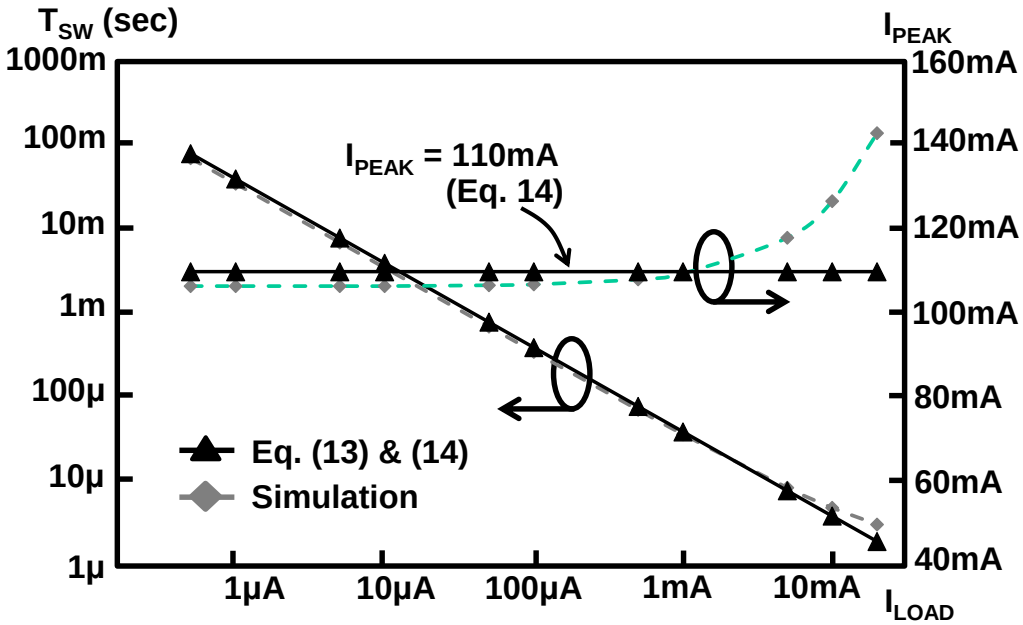
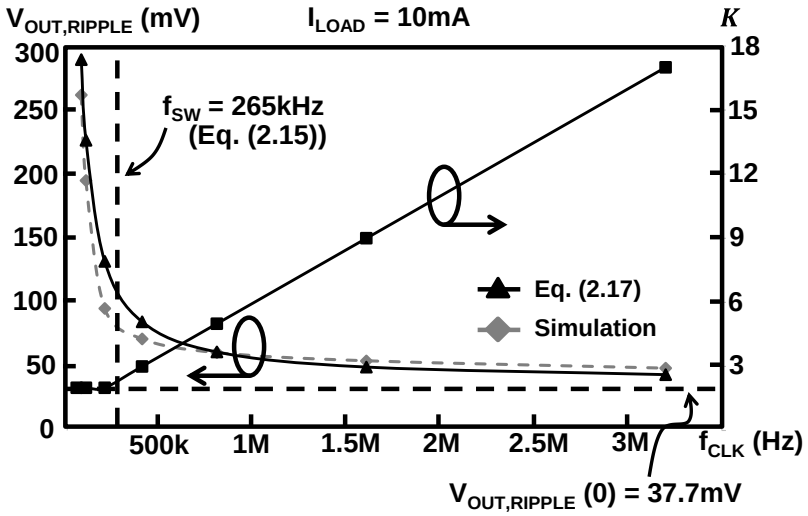


Fig. 2.15. Simulated and calculated T_{SW} and I_{PEAK} by Eqs. (2.15) and (2.16) under different load conditions.

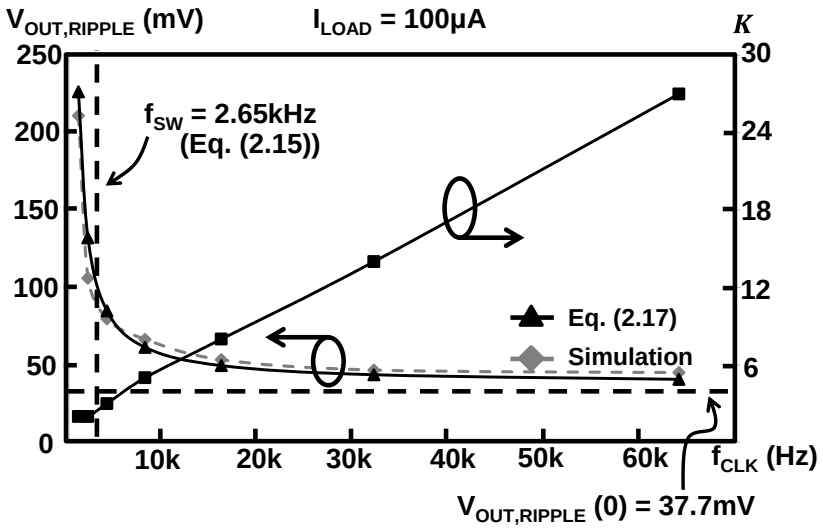
Fig. 2.14(b) shows the inductor current waveform I_L, I_{LOAD}, V_{OUT}, and the clock signal V_{CLK} when CHC is applied. The clocked comparator compares V_{OUT} and V_{MIN} at every clock edge. The effective hysteresis window V_{HYS}^*, however, is enlarged by a limited clock frequency f_{CLK} and K as indicated by (2.11). The worst case of $V_{OUT,RIPPLE}$ is when the clock arrives but V_{OUT} is slightly higher than V_{MIN}. Therefore, V_{HYS}^* is effectively enlarged by a factor of $T_{OSC} \times I_{LOAD}/C_{OUT}$. Therefore, $V_{OUT,RIPPLE}$ can be calculated as

$$V_{OUT,RIPPLE}(CHC) = \frac{V_{IN}}{V_{OUT}}\left(V_{HYS} + \frac{I_{LOAD}}{C_{OUT}}\, T_{CLK}\right) \tag{2.17}$$

The calculated and simulated dependences of $V_{OUT,RIPPLE}$ on f_{CLK}, including the simulated K under V_{IN} = 3 V, V_{OUT} = 1.6 V, V_{HYS} = 20 mV, C_{OUT} = 1 μF, L= 4.7 μH, and I_{LOAD} = 10 mA and 100 μA are shown in Figs. 2.16(a) and (b), respectively. When f_{CLK} is close to the switching frequency f_{SW} calculated by (2.15), the output voltage ripple increases steeply. On the other hand, when a higher f_{CLK} is applied, $V_{OUT,RIPPLE}$ becomes smaller and close to the intrinsic output voltage ripple calculated by (2.14) at the cost of higher power consumption.



(a)



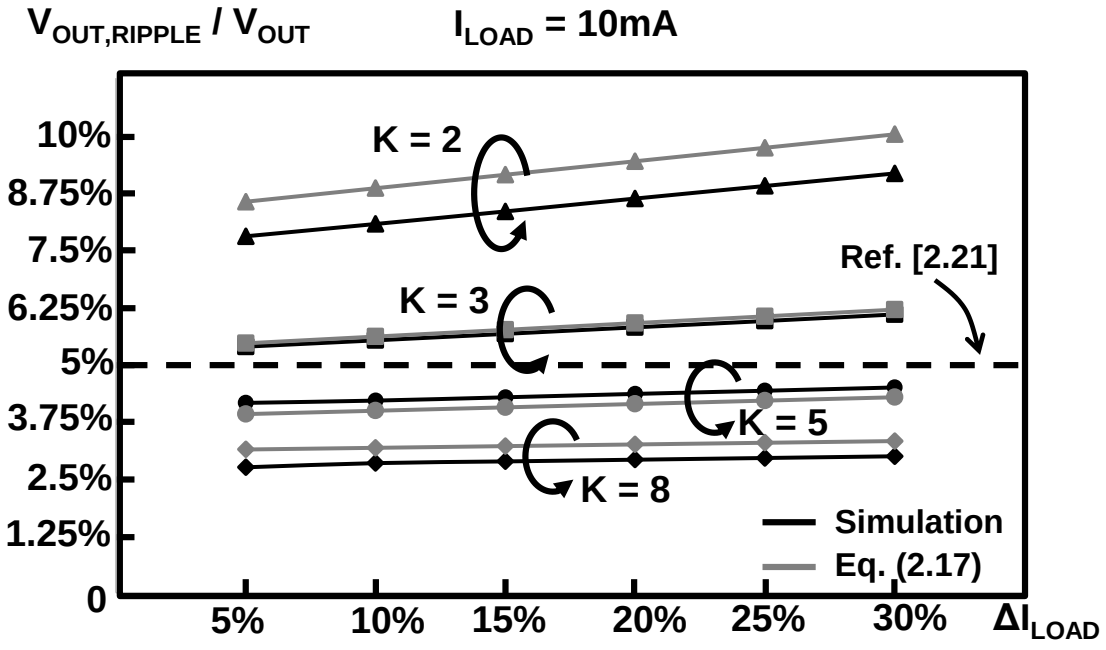
(b)

Fig. 2.16. Simulated and calculated dependence of output voltage ripple on clock frequency f_{CLK}. (a) I_{LOAD} = 10 mA. (b) I_{LOAD} = 100 μA.

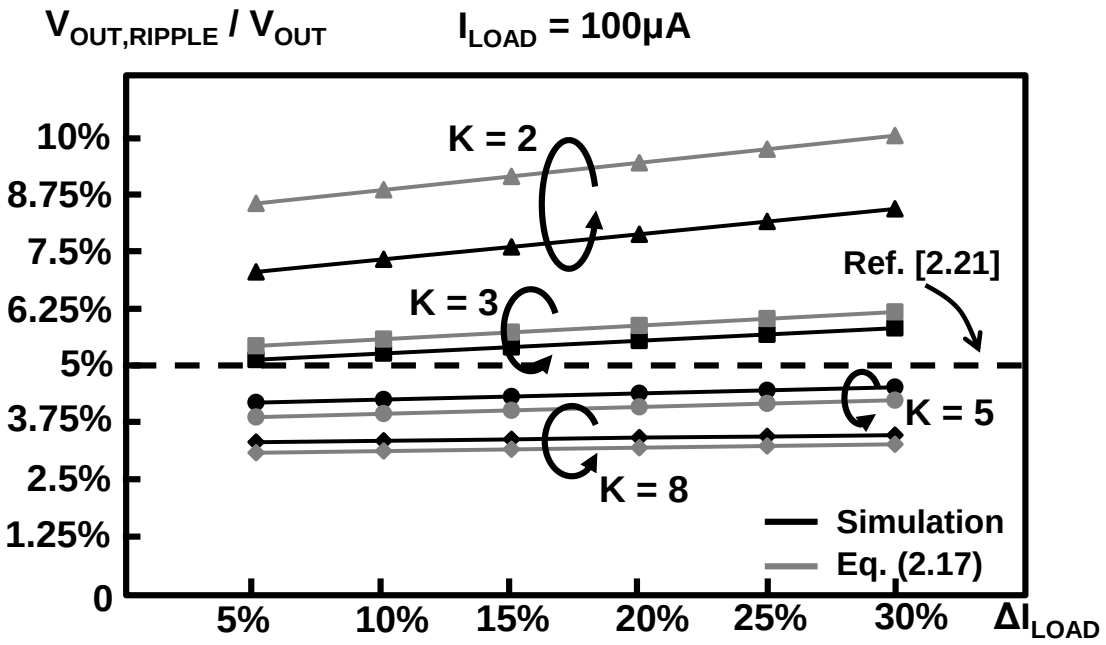
2.3.3 $V_{OUT,RIPPLE}$ and $V_{OUT,MIN}$ under I_{LOAD} Fluctuation

The lowest output voltage level, $V_{OUT,MIN}$, and the maximum voltage ripple, $V_{OUT,RIPPLE}$, of the proposed CHC buck converter under time-dependent I_{LOAD} fluctuation should be calculated. Unlike a conventional buck converter only depending on the output capacitor and the converter loop bandwidth, f_{CLK} and K determine $V_{OUT,MIN}$ and $V_{OUT,RIPPLE}$. Considering that the I_{LOAD} fluctuation is not sufficiently large to change f_{CLK} to $m_1 \times f_{CLK}$, a large value of K is required to keep the minimum output voltage level above the system specifications. Equation (2.17) gives the worst ripple voltage and K is determined by preset numbers n_1 and n_2. Figs. 2.17(a) and (b) show the simulated dependences of the output voltage ripple performance of the proposed CHC buck

converter on K under I_{LOAD} = 10 mA and 100 μA, respectively. The load current is assumed to have a fluctuation of up to 30%. The calculation results obtained from (2.17) and a PFM control with an adaptive on-time buck converter [2.21] are also illustrated in Figs. 2.17(a) and (b) for comparison. The simulation is carried out with V_{IN} = 3 V, V_{OUT} = 1.6 V, V_{HYS} = 20 mV, L = 4.7 μH, and C_{OUT} = 1 μF. A larger value of K indicates that a higher f_{CLK} is applied as shown in Section 2.3.1. When K = 2, the output voltage is easily affected by load fluctuation. In addition, when K = 3, the CHC buck converter achieves competitive voltage ripple performance with the adaptive on-time control buck converter. Applying K = 5, the voltage ripple of the CHC buck converter is lower than that of the conventional one when the I_{LOAD} fluctuation varies from 5% to 30%. Therefore, K = 3 is chosen for low power consumption with acceptable output voltage ripple.



(a)



(b)

Fig. 2.17. Simulated and calculated output voltage ripple for I_{LOAD} with a fluctuation varying from 5% to 30% in a stepped manner with different values of K. (a) I_{LOAD} = 10 mA. (b) I_{LOAD} = 100 μA.

To ensure that the minimum output voltage is higher than the value specified by the system, the lower bound of the voltage hysteresis window, V_{MIN}, should be designed so that is satisfies

$$V_{OUT,MIN}(CHC) = V_{MIN} - \frac{I_{LOAD}}{C_{OUT}} T_{CLK} - \frac{Q_L}{C_{OUT}} \tag{2.18}$$

where Q_L can be expressed as

$$Q_L = \frac{I_{LOAD} \times t_D}{2}, t_D = \frac{I_{LOAD} \times L}{V_{IN} - V_{OUT}} \tag{2.19}$$

and the comparator delay is neglected for simplicity. When I_{LOAD} is 10 mA, V_{IN} = 3 V, and V_{OUT} = 1.6 V, V_{MIN} = 1.57 V gives the CHC buck converter with a minimum output voltage no lower than 3.4% of V_{OUT}, and $V_{OUT,RIPPLE}$ < 6% of V_{OUT} when K = 3.

Therefore, the design parameters $m_1 = m_2 = 2$, $n_1 = 2$, and $n_2 = 5$, resulting in $K = 3$, which is the case shown in Figs. 2.12(a) and (b), are chosen to implement the proposed CHC buck converter

2.4 Circuit Implementation

2.4.1 Leakage-Based Digitally Controlled Oscillator (DCO)

An on-chip digitally controlled oscillator (DCO) is implemented to provide a clock signal to the clocked comparator X_1. The clock frequency is able to be controlled digitally using a factor of 2 and ranges from Hz to MHz order for both active and sleep modes. A circuit schematic of the DCO is shown in Fig. 2.18. As the DCO is the only continuously-on circuit block in the CHC buck converter, the power consumption should be minimized so that it does not limit the sleep mode conversion efficiency. The transistor leakage current is designed as the bias current provided to the current mirror. 4-bit signals A [3:0] are used to control the transistor size of M_P and the leakage current according to PVT variation. A [3:0] can be generated by additional calibrations or implementing a PVT sensors on a chip [2.22] [2.23]. This current is mirrored to charge and discharge the capacitors, generating a saw tooth voltage waveform. A current-starved Schmitt trigger is used as a comparator and output buffer so that there is no need to use an additional reference. Therefore, a square clock waveform can be obtained at the output of the Schmitt trigger. The frequency tuning is separated to control both the transistor multiplier ratio and the number of capacitors. 22-bit thermometer codes, FCLK_CTRL [21:0], are used to adjust the clock frequency monotonically over a frequency tuning range of 10^6. In addition, stacked transistor technology is employed to design M_{N1} to dramatically reduce the transistor area. Therefore, the MSB NMOS transistor multiplier ratio can be reduced to 2048, which can be implemented on a test chip.

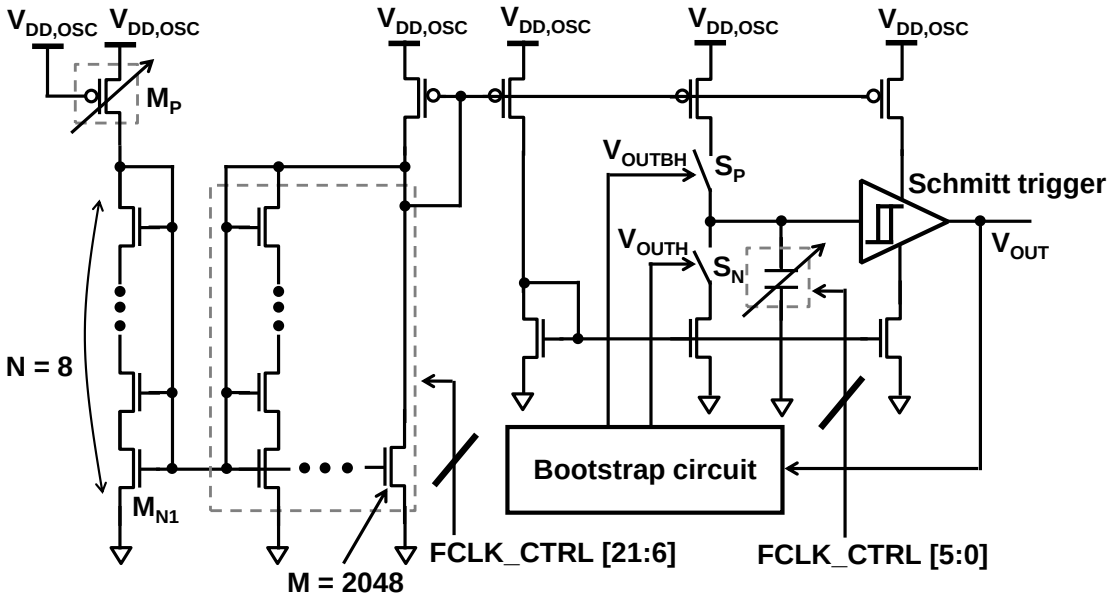


Fig. 2.18. Circuit schematic of the leakage-based DCO.

To reduce the oscillator power consumption, a supply $V_{DD,OSC}$ with a lower voltage is preferred. A bootstrap circuit employing the concept in [2.24] is designed to boost the voltage level of V_{OUT} when the Schmitt trigger is switching. Therefore, switches S_N and S_P can be fully turned on to charge and discharge the capacitor even when $V_{DD,OSC}$ is as low as 0.6 V. An additional low-dropout regulator (LDO) or a switched capacitor (SC) DC-DC converter can be employed to generate this supply voltage. The measurement results show that the DCO consumes only 5.6 nA at 15 Hz and 50.4 μA at 6 MHz when $V_{DD,OSC}$ is 0.6 V. Therefore, it is possible to design the LDO or the SC DC-DC converter [2.25] on a chip with high conversion efficiency and a compact area, although this has not been implemented in the current design.

The frequency scaling scheme applied to the DCO may generate interference that interferes with sensitive circuits on the chip. In the sleep mode, however, the clock

frequency is only 10-Hz order, which is far from the usual RF signal frequency. In addition, there are no RF circuits enabled in the sleep mode. On the other hand, in the active mode, a system clock with a higher frequency, for example, 32 MHz, can be applied as a base frequency for the power-law frequency scaling scheme instead of using the internal leakage-based DCO.

2.4.2 Clocked Comparator and Analog Comparator with Enable Signal

A circuit schematic of clocked comparator X_1 is shown in Fig. 2.6. A clocked comparator with a latch load [2.15] is employed to compare V_{OUT} with V_{MIN}. The output followed by a D flip-flop generates a control signal to turn on the power transistor M_P. The input differential pair is designed with a large transistor width and length to reduce the offset voltage. The 1-sigma simulated and calculated offset voltages [2.26] are less than 2 mV, which does not have a large effect on the voltage hysteresis window.

Fig. 2.9 shows a circuit schematic of the power-gated comparator with an enable signal. Comparator X_2 compares V_{OUT} with V_{MAX}, and is enabled when V_{OUT} is lower than V_{MIN} and turned off when V_{OUT} becomes higher than V_{MAX}. Similarly, a P-type input differential pair with an NMOS active load power-gated comparator is designed for X_3 because the comparator compares the V_X node with the ground. X_3 is turned on when V_{OUT} becomes higher than V_{MAX} and turned off when the inductor current reaches zero. The settling time due to the enable signal in the comparators is not an issue because the bias points in the comparators only need to settle in a time of 100-ns order. To demonstrate the benefit of the proposed CHC, the power distribution of the comparators is simulated. The simulation shows that the power consumptions of X_1, X_2, and X_3 are all lower than 1% of the output power when applying f_{CLK} = 100 Hz under I_{LOAD} = 1 μA.

2.4.3 Voltage Level Shifter Design

The proposed CHC buck converter targets BLE applications for which the input voltage could be a battery with a voltage ranging from 2.4 V to 3.3 V. However, a lower supply voltage is preferred for the leakage-based DCO to reduce the power consumption. A conventional level shifter with a short current reduction topology [2.27] cannot convert a clock signal with a low voltage such as 0.6 V to 3.3 V when the clock frequency is in the MHz order. Fig. 2.19 shows the designed voltage level shifter. An auxiliary bootstrap circuit is designed to boost the amplitude of the input clock signal V_{CLK} to nearly 2 $V_{DD,OSC}$ (~1.2 V), and the voltage level shifter can shift V_{CLKM} to V_{CLKH} functionally. The worst case is when the clock frequency is lowest. In this case, the bootstrap circuit cannot boost the input voltage for a long period. Simulation results show that the voltage level shifter can convert the input signal from 0.6 V to 3.3 V when the frequency ranges from 1 Hz to 5 MHz. The voltage level shifter consumes 380 pW at 1 Hz and 44.5 μW at 5 MHz.

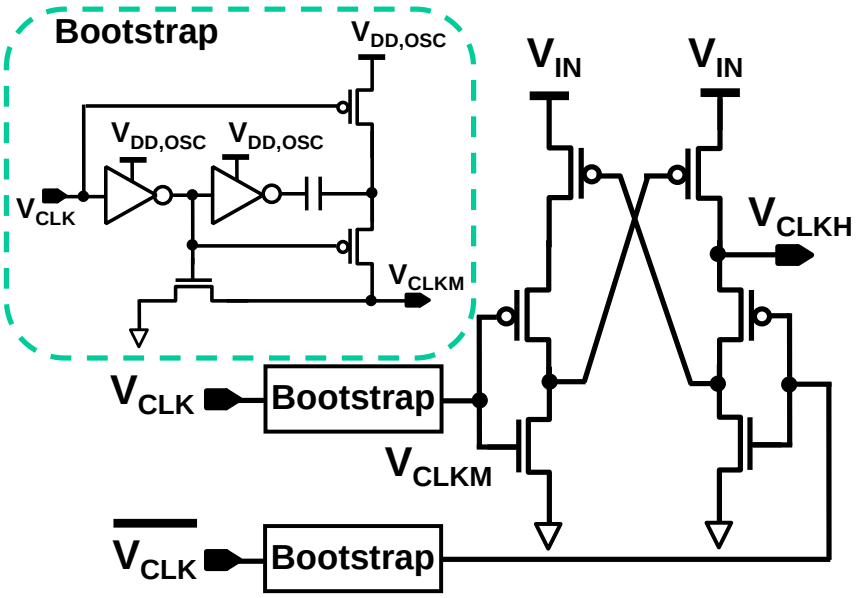


Fig. 2.19. Schematic of the voltage level shifter converting 0.6 V to 3.3V with the frequency of the input signal ranging from 1 Hz to 5 MHz.

2.5 Experimental Results

The proposed CHC buck converter implemented with the double-half frequency scaling scheme (m_1=2, m_2=2) is fabricated by a 0.18 μm standard CMOS process for verification. I/O transistors are used to design buck converter core circuits that should withstand an input voltage of 3.3 V, and switches providing a low leakage current. Fig. 2.20 shows the chip micrograph. The active area including the buck converter core circuits, leakage-based DCO, voltage level shifter, and buffers is 0.71 mm^2. The test chip is measured with a 4.7-μH off-chip inductor and a 1-μF off-chip capacitor, and the frequency scaling scheme is realized using an Altera Cyclone V FPGA. Figs. 16(a) and (b) show the steady-state waveforms of V_{OUT}, V_{CLK}, and VOUT_LOW under V_{IN} = 3 V, V_{MIN} = 1.57 V, and V_{MAX} = 1.59 V when I_{LOAD} = 100 μA and 2 mA, respectively. The voltage hysteresis window V_{HYS} is set to 20 mV for all measurements. The frequency scaling scheme is designed to minimize the power consumption of the comparator and controller. Therefore, n_1 = 2 and n_2 = 5 are used, resulting in K = 3 in (2.11). As shown in Fig. 16, the PMOS power transistor M_P is turned on every three V_{CLK} clock cycles. As discussed in Section 2.3, m_1, m_2, n_1, and n_2 can be changed easily according to the specifications for different applications, such as a high wake-up response speed or a low output voltage ripple. The measurement results show that the output voltage is regulated at 1.6 V with a voltage ripple lower than 100 mV, which is about 6% of the output voltage. Using the frequency scaling scheme, the clock frequency of V_{CLK} automatically settles to 3.57 kHz and 94 kHz when I_{LOAD} = 100 μA and 2 mA, respectively.

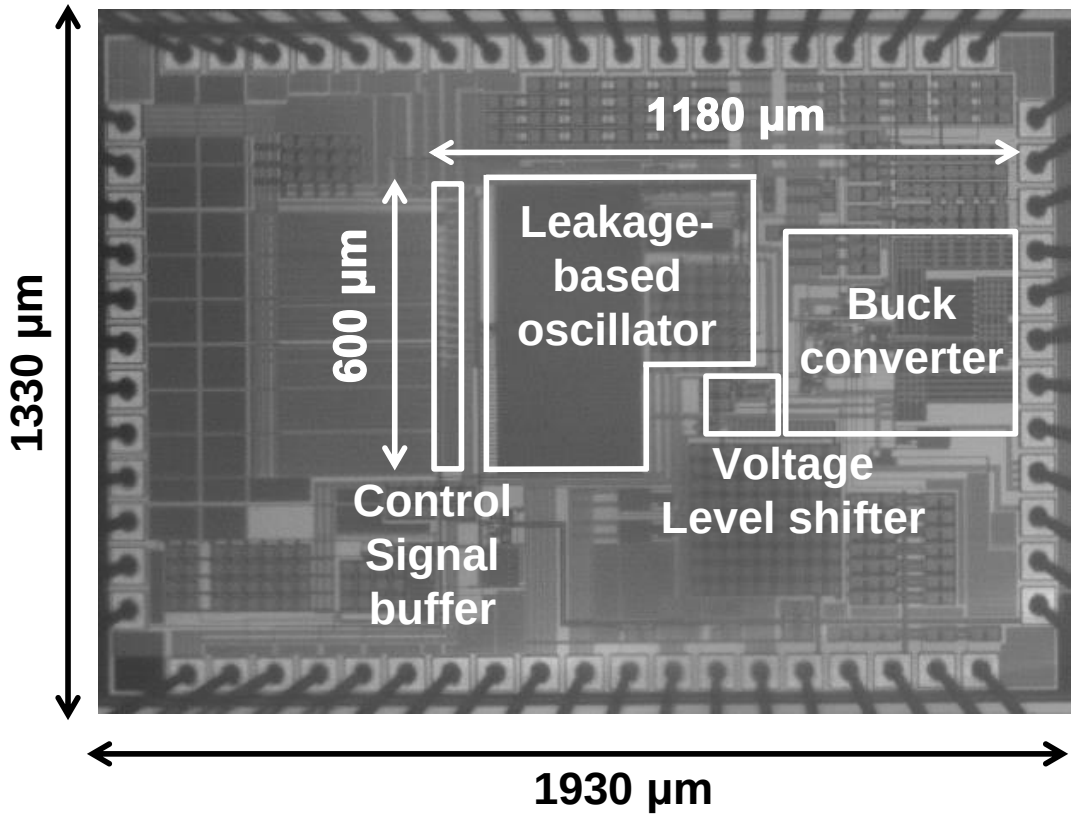
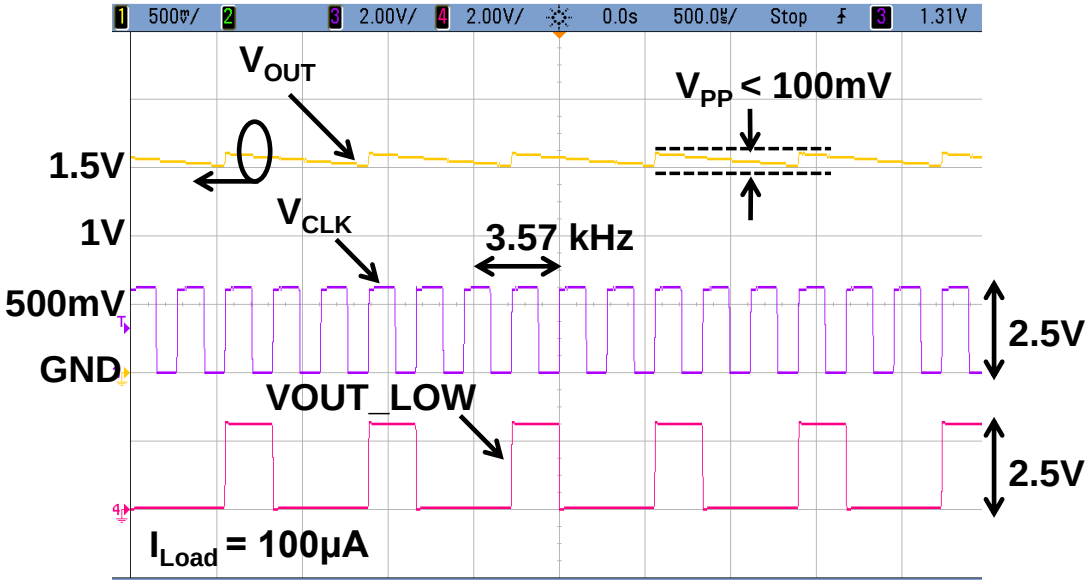
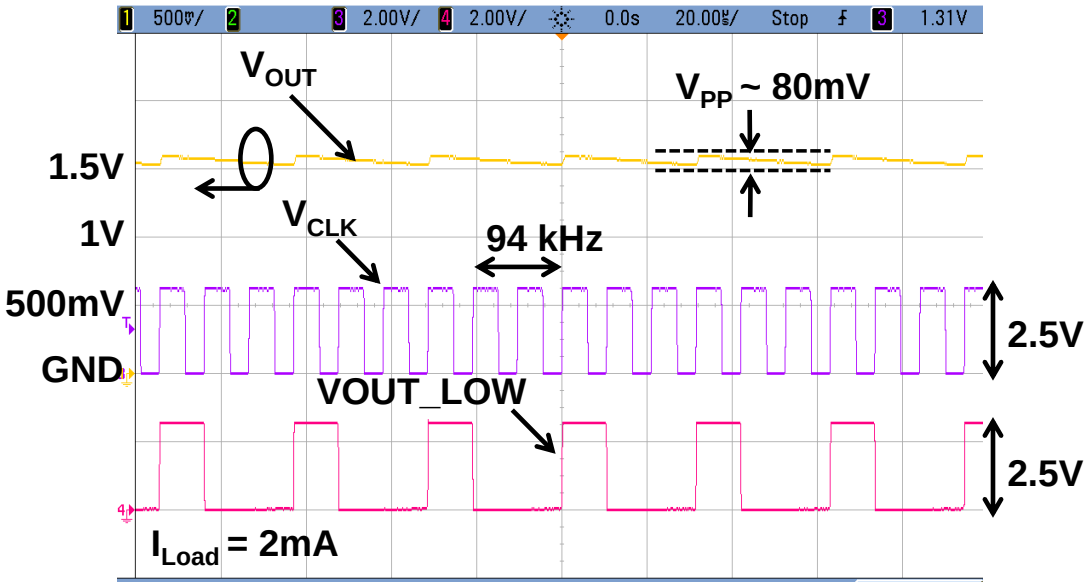


Fig. 2.20. Chip micrograph of the proposed CHC buck converter.



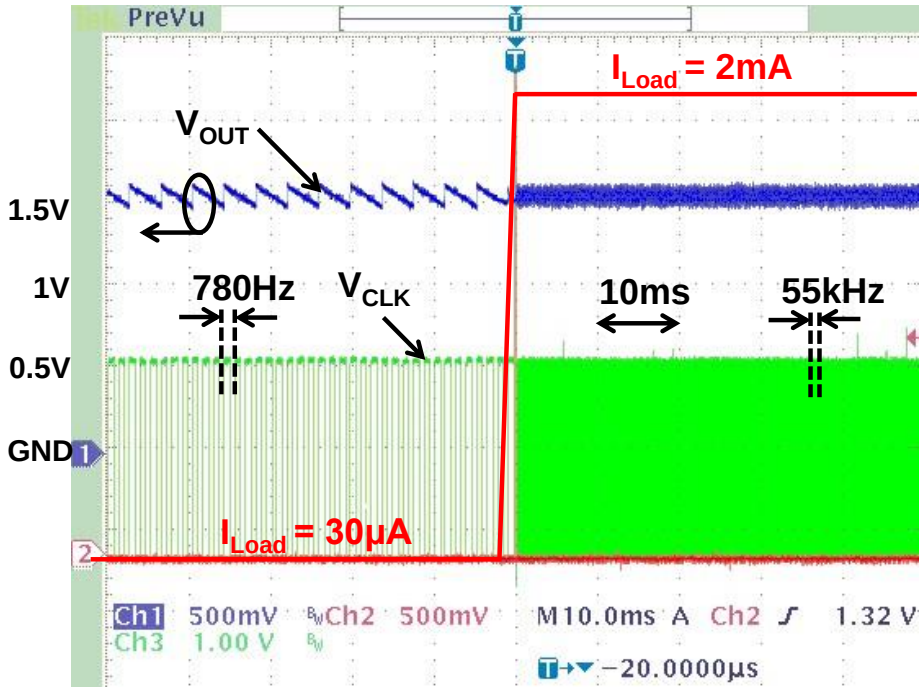
(a)



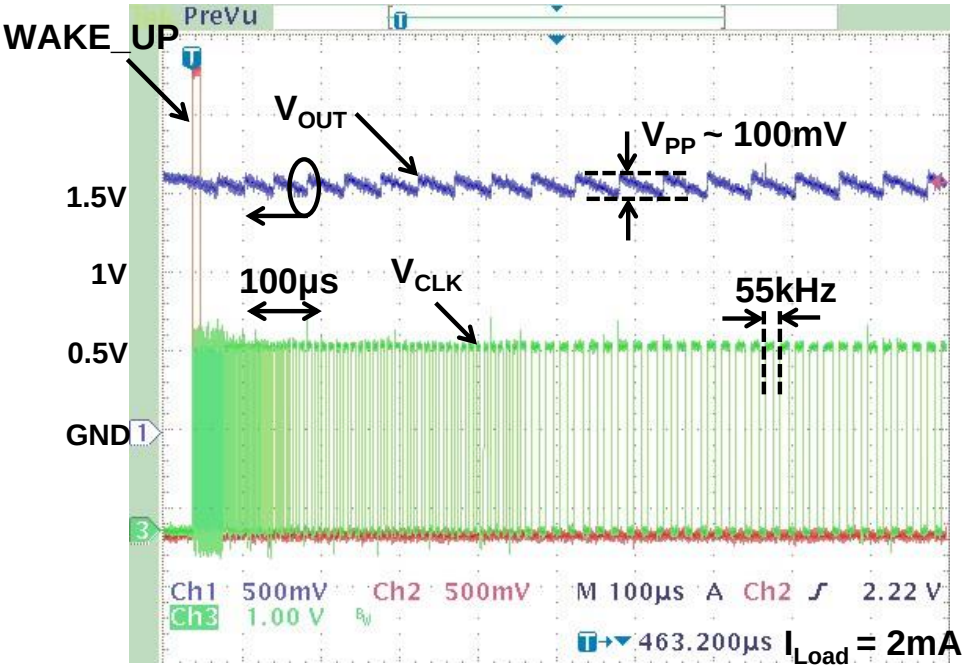
(b)

Fig. 2.21. Measured waveforms of V_{OUT}, V_{CLK}, and VOUT_LOW under different loading conditions. (a) V_{IN} = 3 V, V_{OUT} = 1.6 V, V_{HYS} = 20 mV, and I_{LOAD} = 100 µA. (b) V_{IN} = 3 V, V_{OUT} = 1.6 V, V_{HYS} = 20 mV, and I_{LOAD} = 2 mA.

To verify the load wake-up operation, I_{LOAD} changed from 30µA to 2mA is applied to the output. The signal WAKE_UP resets the clock frequency to the highest value, and the clock frequency is settled in the steady state by the frequency scaling scheme as shown in Fig. 2.22(a). Fig. 2.22(b) shows the detailed waveforms of V_{OUT}, V_{CLK}, and WAKE_UP. The clock frequency changes from 780 Hz to 55 kHz at 2-mA loading without an obvious voltage drop.



(a)



(b)

Fig. 2.22. Measured load wake-up operation when I_{LOAD} is changed from a sleep mode (30 µA) to an active mode (2 mA). (a) Time scale = 10 ms. (b) Time scale = 100 µs.

Fig. 2.23 shows the measured clock frequency and power consumption versus FCLK_CTRL [21:0] for the leakage-based DCO. The clock frequency is controlled by a 22-bit thermometer code with 16 bits in the transistor multiplier ratio and 6 bits in the capacitor bank. Three chips are measured, showing that the frequency can be adjusted monotonically without large frequency and power variations. Upon applying a 0.6 V supply voltage, the DCO consumes 3.5 nW and 32 μW when the clock frequency is 15 Hz and 6.3 MHz, respectively. In addition, the DCO power consumption is also proportional to the loading current because the frequency is mainly controlled by the transistor multiplier ratio in the current mirror. The power distribution of the DCO accounts for less than 1% of the output power of the CHC buck converter when operating in both the sleep and the active modes.

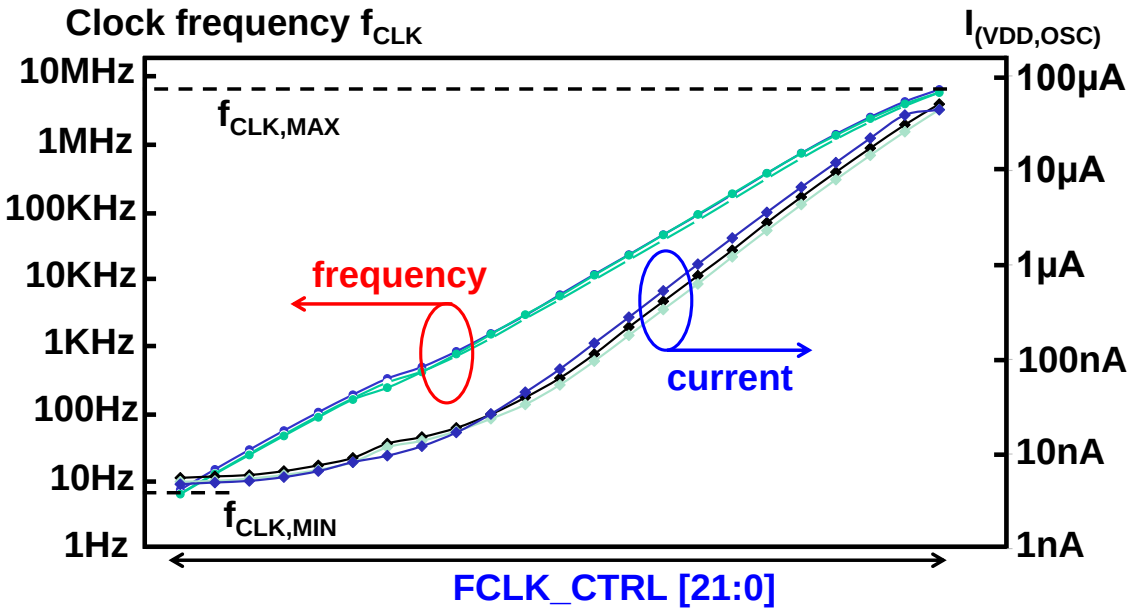


Fig. 2.23. Measured clock frequency and power consumption relationship for proposed DCO in Fig. 2.18 when digital bit of FCLK_CTRL is changed.

The measured dependence of the efficiency and clock frequency f_{CLK} on the load current is shown in Fig. 2.24. The proposed CHC buck converter achieves almost flat conversion efficiency by removing continuously-on comparators and applying the double-half frequency scaling scheme. The frequency scaling scheme is also verified on the Y-axis on the right-hand side of Fig. 2.24. Higher than 87% conversion efficiency is achieved over a load current ranging from 500 nA to 20 mA. When I_{LOAD} = 1 μA, which is defined as the sleep current in BLE, efficiency is improved by 12% - 34% compared with that of state-of-the-art low-power buck converters. A comparison of performance with state-of-the-art buck converters is shown in Table 2-2. The proposed CHC buck converter achieves higher than 87% conversion efficiency over 500 nA to 20 mA with a peak efficiency of 90.4%. In addition, compared with the state-of-the-art buck converters, a higher efficiency at 1 μA is also achieved. The input voltage, output voltage, and loading current are designed for BLE applications. CHC with the double-half frequency scaling scheme was also proposed to remove the continuously-on comparators in the conventional hysteresis buck converter. The frequency scaling scheme is also suitable for other converters that employ continuously-on comparators.

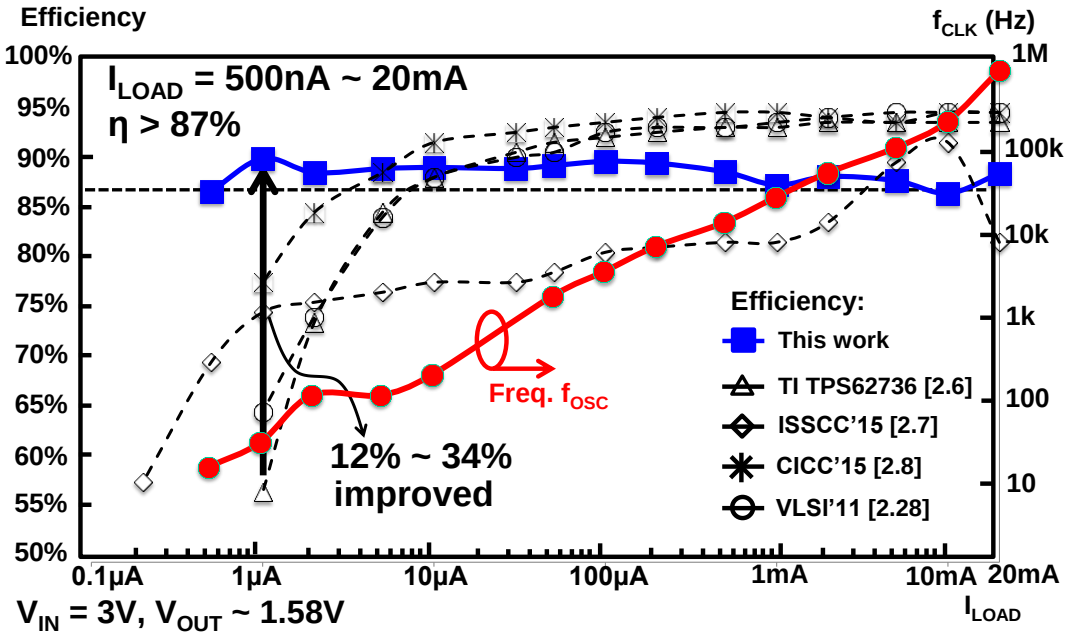


Fig. 2.24. Measured conversion efficiency and clock frequency f_{CLK} versus I_{LOAD} and comparison with state-of-the-art low-power buck converters.

Table 2-2. Performance Summary of the Proposed CHC Buck Converter and Comparison with State-of-the-Art Buck Converters

	ISSCC'15 [2.7]	CICC'15 [2.8]	VLSI'15 [2.9]	VLSI'11 [2.28]	**This work**
Technology	180nm CMOS	350nm CMOS	180nm CMOS	250nm CMOS	**180nm CMOS**
Die size	1.44mm^2	2.88mm^2	2.42mm^2	0.21mm^2	**0.71mm^2 ***
V_{IN} (V)	0.6/1.2	2.2 – 6	3	1.2 – 2.5	**2.4 – 3.3**
V_{OUT} (V)	0.35 – 0.5	2.5	1	1	**1.5 – 1.6**
I_{LOAD}	100nA – 20mA	1µA – 100mA	10nA – 1µA	1µA – 100mA	**500nA – 20mA**
Peak eff. η_{PEAK}	92%	95%	87%	95.2	**90.4%**
η @ I_{LOAD} =1µA	75%	78%	87%	65%	**90.4%**
Inductor value L	4.7µH	2.2µH	47µH	1.5µH	**4.7µH**
Control methodology	PWM, PFM, and AM	Hysteresis control	Constant on-time	Dynamic on/off time	**Clocked hysteresis control**

* Active area

2.6 Summary

A clocked hysteresis control (CHC) buck converter operating in DCM with a power-law frequency scaling scheme is developed to remove the continuously-on comparators used in conventional hysteresis control, resulting in no DC current being consumed by the comparators. The frequency of the clocked comparator is dynamically adjusted in accordance with the load conditions. Therefore, the conduction loss, switching loss, and comparator power consumption in the converter can all be scaled with the load. By applying the proposed topology, the CHC buck converter achieves almost flat conversion efficiency over the entire load current range. The frequency stability, output voltage ripple, and minimum output voltage level of the buck converter when the power-law frequency scaling scheme is applied are analyzed to provide design guidelines for the system. A CHC buck converter with the double-half frequency scaling scheme is implemented to verify the power-law frequency scaling. Experimental results demonstrate that the buck converter achieves conversion efficiency of higher than 87% over I_{LOAD} ranging from 500 nA to 20 mA with a peak value of 90.4%. The conversion efficiency is particularly improved when I_{LOAD} is 1 μA. The I_{LOAD} wake-up operation with the frequency scaling scheme is also verified. The proposed buck converter achieves high conversion efficiency in a sleep mode with a quick wake-up response, making it extremely suitable for IoT sensor node applications.

Appendix: Hysteresis Control for a Buck Converter

Consider a buck converter employs a couple of comparators with references V_{MAX} and V_{MIN} and the circuit schematic is shown in Fig. 2.25. When V_{OUT} goes from a high voltage to a low voltage level, the comparator X_1 comparing V_{OUT} with V_{MIN} is activated first making the output V_Q change from logic "1" to logic "0". At this time, the power switch Q_1 is turned on to charge up the output voltage. Therefore, V_{OUT} is charged up and goes from a low voltage level to a high voltage. Comparator X_2 is enabled at this time and X_1 is disabled. Until V_{OUT} is higher than V_{MAX}, V_Q changes from logic "0" to logic "1". The output voltage waveform with V_{MAX} and V_{MIN} and the dependence of V_Q on V_{OUT} are shown in Fig. 26. From Fig. 26, there is a hysteresis window formed by V_{MAX} and V_{MIN}. Therefore, the control topology performs a hysteresis control for buck converter.

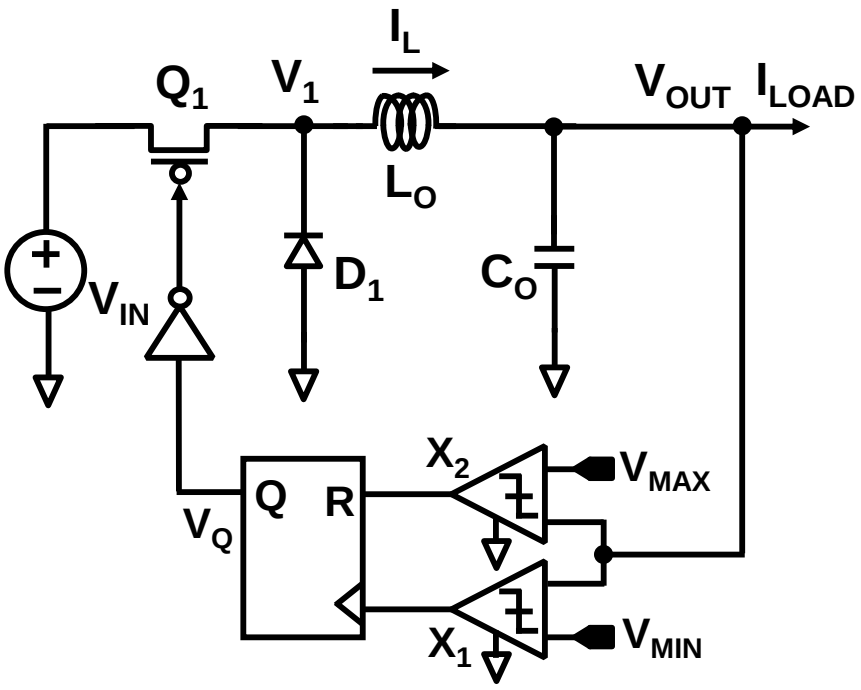


Fig. 2.25. Buck converter using hysteresis control.

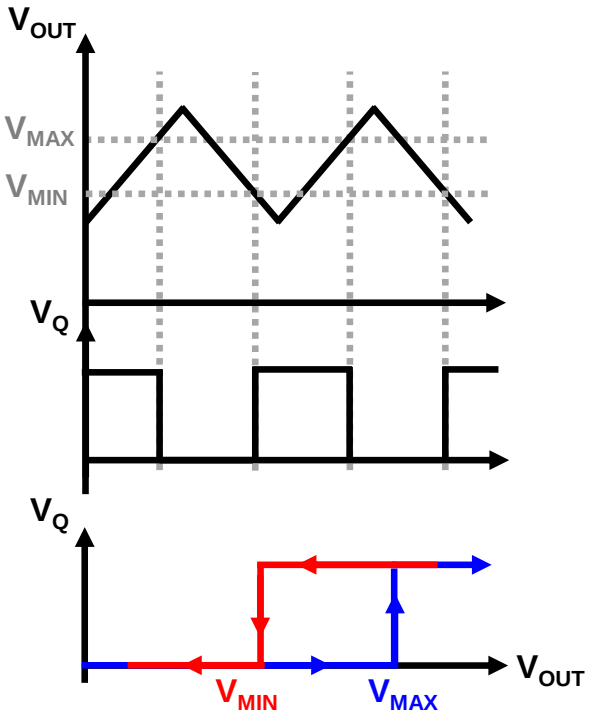


Fig. 2.26. Output voltage waveform with V_{MAX} and V_{MIN}, and the dependence of V_Q on V_{OUT}.

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Chapter 3: Low-Power Wide Current-Range Switched-Capacitor DC-DC Converter

In Chapter 2, clocked hysteresis control scheme with power-law frequency scaling is proposed and applied to a buck converter design for improving the conversion efficiency in the sleep mode. This chapter discusses that the control scheme is also suitable for a capacitive DC-DC converter, usually called switched-capacitor (SC) DC-DC converter. By implementing a clocked comparator with power-law frequency scaling, the continuously-on error amplifier and the high frequency clock in a conventional SC DC-DC converter can be removed. In this chapter, a SC DC-DC with power-law frequency scaling is proposed. A simple 2-to-1 topology is designed so the output voltage of the SC DC-DC converter is regulated at a level of half of the input. Compared with conventional SC DC-DC converters, the clock frequency of the clocked comparator is scaled automatically. Therefore, no continuously-on error amplifier and high frequency clock and clocked comparator are required. The power consumption of the oscillator can also be scaled. The experimental results show that the SC DC-DC converter achieves an almost flat efficiency that is higher than 87.5% over a load current range from 600 nA to 150 μA. In addition, 33% efficiency is improved at the light load specified by BLE compared with a conventional SC DC-DC converter employing a fixed clock frequency. The circuit is implemented in CMOS 180 nm process technology converting a 1.8-V input to a regulated 0.9-V output voltage.

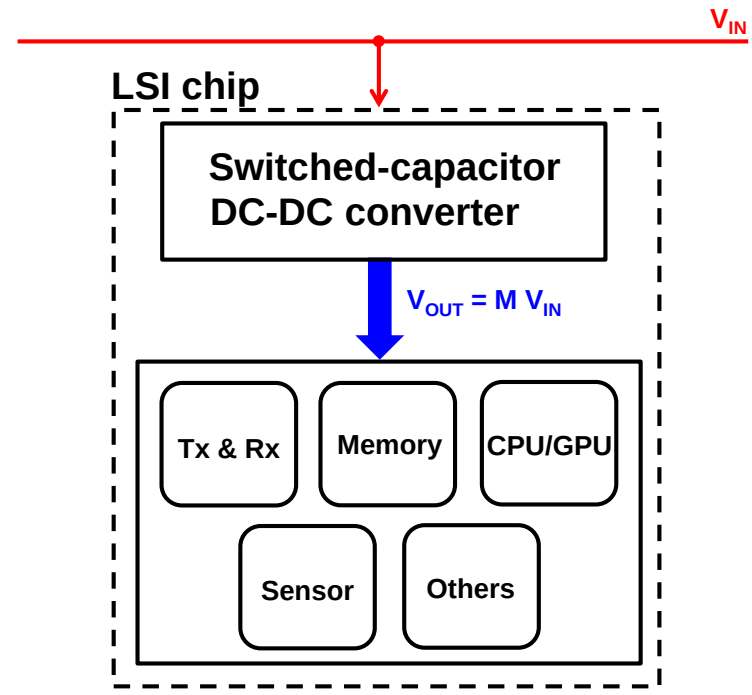
3.1 Introduction and Background of Switched-Capacitor (SC) DC-DC Converter

The interest in switched-capacitor (SC) DC-DC converter becomes growingly increasing over the decades because in many applications such as IoT edge, implantable electronics, and wearable devices require small physical volume. SC DC-DC converter is extremely suitable to implement fully on-chip voltage/power supply and provide multiple voltage domains on a chip. Compared with inductive DC-DC converter such as buck converter, the capacitors in SC DC-DC converter is possible to be integrated in CMOS process technology and fabricated on the same LSI chip. The target LSI systems including SC DC-DC converter for on-chip power management and multiple power domain are shown in Fig. 3.1(a) [3.1] and (b) [3.2], respectively. Fig. 3.1(a) illustrates the LSI system employed a SC DC-DC converter converting an input voltage to an output voltage provided to the chip. The input voltage can be a battery or a global voltage bus generated by other DC-DC converters. On the other hand, fully on-chip SC DC-DC converter can be designed for each power domain to optimize the chip performance as shown in Fig. 3.1 (b). Additionally, compared with a linear low-dropout regulator (LDO), as we will discuss in later chapter, the theoretical conversion efficiency of SC DC-DC converter can be expressed as [3.3]:

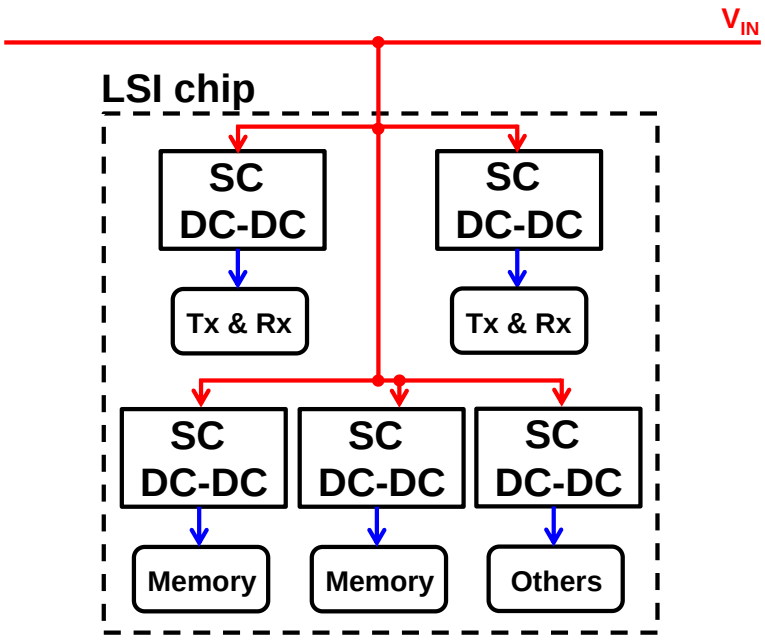
$$\eta_{SC} = \frac{V_{OUT}}{MV_{IN}} \tag{3.1}$$

Where M is a conversion ratio determined by the configuration of the SC DC-DC converter. Therefore, when V_{OUT} is close to $M \times V_{IN}$, the efficiency of a SC DC-DC

converter is much higher than the efficiency of a LDO, which is V_{OUT}/V_{IN}.



(a)



(b)

Fig. 3.1. LSI system with fully integrated SC DC-DC converter. (a) SC DC-DC converter as an on-chip power/voltage supply. (b) On-chip multiple power domains application.

Fig. 3.2(a) and (b) show the simplified circuit schematic of a SC DC-DC that M is 1/2 and M is 2/3, respectively [3.4]. Each switch is turned on according to the switching phase φ_1 and φ_2 illustrated in the timing diagram. By charge conservation, the theoretical output voltage in Fig. 3.2(a) and (b) can be derived as (3.2) and (3.3), respectively.

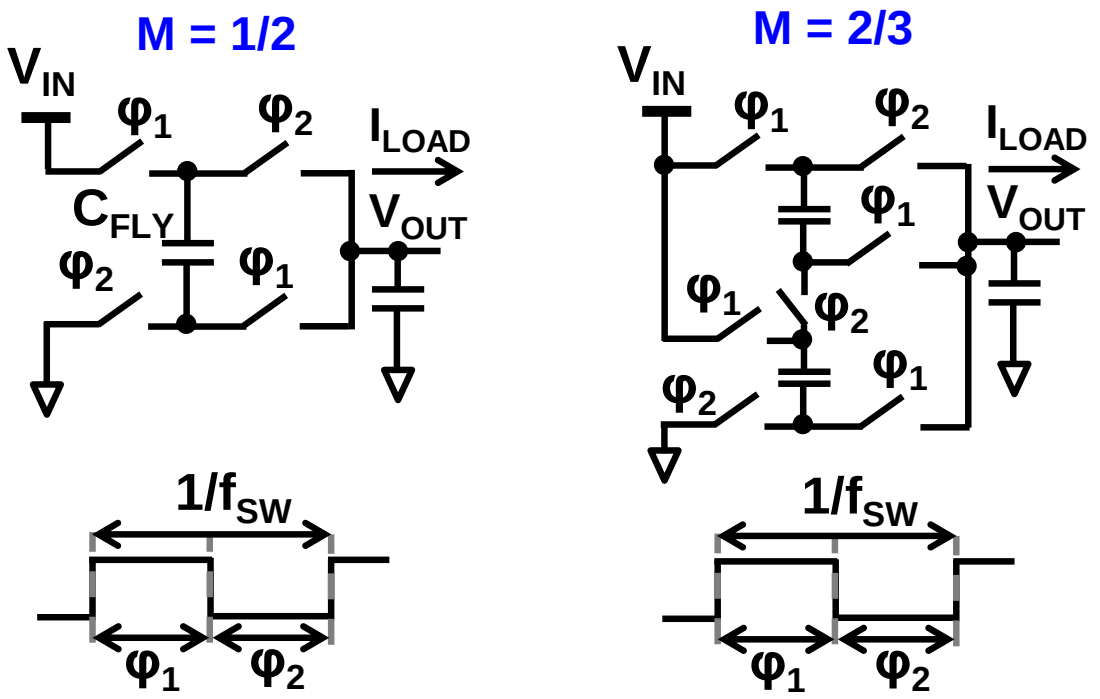
$$V_{OUT} = \frac{1}{2} V_{IN} \tag{3.2}$$

$$V_{OUT} = \frac{2}{3} V_{IN} \tag{3.3}$$

Fig. 3.2(a) can be considered as a 2:1 SC DC-DC converter unit and can be employed to design for generating other conversion ratio. The output voltage and load current waveform of a 2:1 SC DC-DC converter unit are illustrated in Fig. 3.3(a). The ideal output voltage ripple is calculated by:

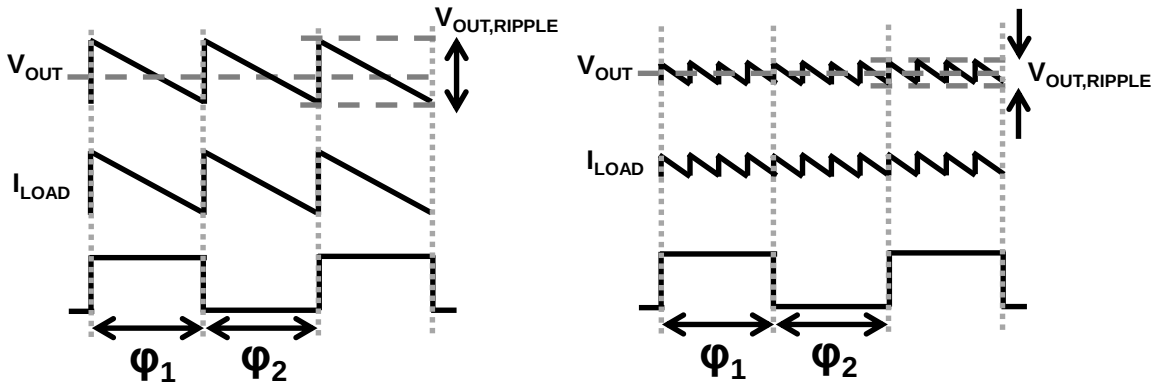
$$V_{OUT,RIPPLE} = \frac{I_{LOAD}}{C_{FLY}} \frac{1}{2f_{SW}} \tag{3.2}$$

where C_{FLY} is the flying capacitor shown in Fig. 3.2(a). To reduce the output voltage ripple, Multi-phase interleaved SC DC-DC converter has been proposed [3.5]. Fig. 3.3(b) shows the output voltage and load current waveform of a 2:1 SC converter with 4-phase interleaved. The output voltage ripple can be significantly reduced by the multi-phase operation.



(a) (b)

Fig. 3.2. Simplified circuit schematic of SC DC-DC converter. (a) M = 1/2. (b) M = 2/3.



(a) (b)

Fig. 3.3. Output voltage and load current waveform of a 2:1 SC converter. (a) Single phase. (b) 4-phase interleaved.

Given these advantages, not only research publications but also industrial fields on SC DC-DC converters for highly integrated applications have been proposed. A fully on-chip SC DC-DC converter implemented in SOI process has been proposed to achieve maximum output power of 0.378 W with a peak efficiency of 81% [3.6]. Without the advantage of SOI deep trench that provides large capacitance, a CMOS SC DC-DC converter designed with on-chip capacitors uses multi-phase operation [3.7] that is able to support output power range from 20 mW to 150 mW with a peak efficiency of 77 %. Topologies combining multiple 2:1 SC converter units and flying capacitors are also proposed for wide input voltage range and multiple conversion ratio applications. In [3.8], a SC DC-DC converter converts an input voltage range from 7.5 V to 13.5 V to an output of 1.5V. The SC DC-DC converter in [3.8] also support a load current from 1 mA to 1 A with a peak efficiency of 92%.

For wide-current range applications including the low-power sleep mode such as IoT and implantable electronics, however, only few publications on SC DC-DC converter have been reported. A SC DC-DC converter achieves 15 conversion ratio with 85% peak efficiency [3.9], however, the conversion efficiency becomes lower than 70% for a 10-μA load. Employing ferroelectric capacitor in a SC DC-DC converter improves the conversion efficiency for low-power applications [3.10]. The conversion efficiency in [3.10] is higher than 90% when the load current ranges from 100 μA to 500 μA. Nevertheless, the efficiency decreases quickly when the load current is lower than 50 μA and becomes 72% at 10 μA. Even through [3.11] claims a SC DC-DC converter is able to support the load range from 20 nW to 500 μW, the peak efficiency is only 60%. In

commercial products, on the other hand, the conversion efficiency drops steeply when the load current is 100 μA or 1 mA [3.12] [3.13].

Instead of developing a fully integrated SC DC-DC converter for multiple power domains applications, the target in this chapter is to develop a SC DC-DC converter that is able to support wide load current range with a high conversion efficiency at a sleep mode. As specified by Bluetooth Low Energy [3.14], the load current of the SC DC-DC converter in the sleep is lower than 1 μA. By applying the proposed power-law frequency scaling scheme discussed in Chapter 2, the efficiency of the SC DC-DC converter is improved significantly at a light load current. In addition, the light load current can be extended to a nA-order range. An almost flat conversion efficiency is achieved and verified by experimental results. The target system diagram is shown in Fig. 3.4 and the proposed SC DC-DC converter is specified by blue lines.

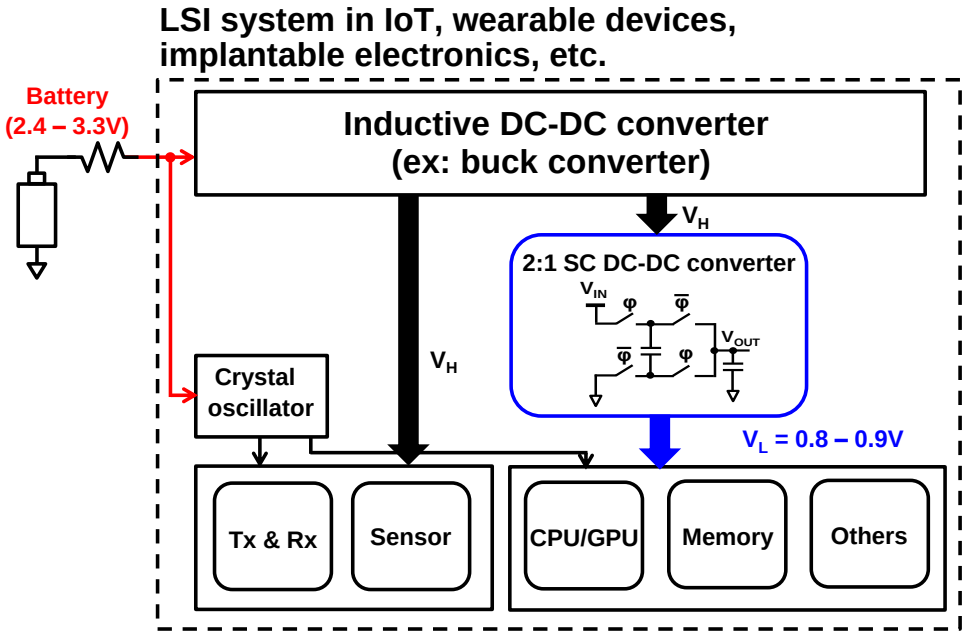


Fig. 3.4. Target energy-efficient LSI system for IoT, wearable devices, and implantable electronic including the SC DC-DC converter.

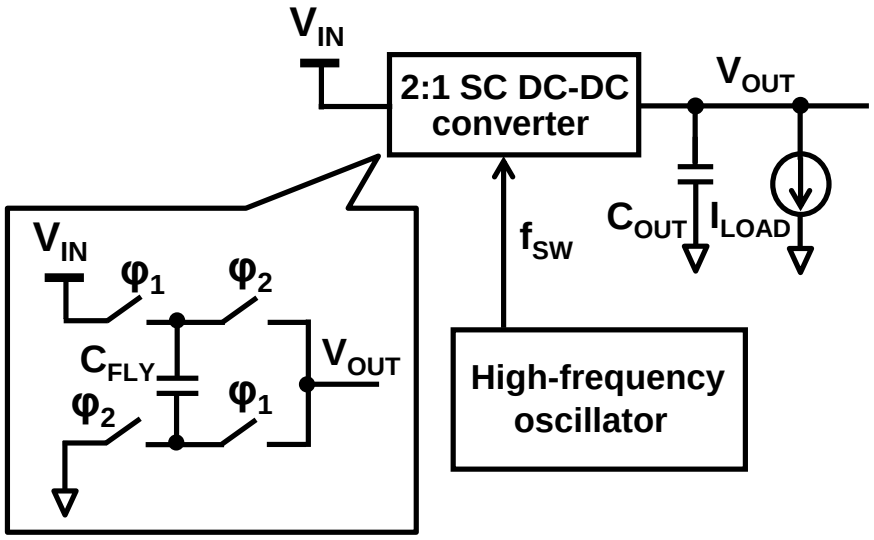
3.2 System Architecture

There are two basic topologies for a 2:1 SC DC-DC converter shown in Fig. 3.5(a) and (b). In Fig. 3.5(a), an oscillator is designed to provide a clock signal to the SC DC-DC converter [3.15]. In this case, the clock frequency is equal to the switching frequency of the SC DC-DC converter, i.e. $f_{CLK} = f_{SW}$. The output voltage is determined by the configuration and is 1/2 V_{IN}. The output voltage ripple and the output voltage level, however, are affected by the load current. A larger load current results in a lower average output voltage. To make the voltage ripple and the output voltage both within the specifications, a clock with high frequency is necessary. On the other hand, a continuously-on error amplifier and a voltage-controlled oscillator (VCO) are employed to perform pulse frequency modulation (PFM) control in Fig. 3.5(b) [3.16]. The error amplifier amplifies a voltage difference between the output and a reference voltage. The voltage difference is used to control the clock frequency generated by the VCO. Therefore, the output voltage can be expressed as:

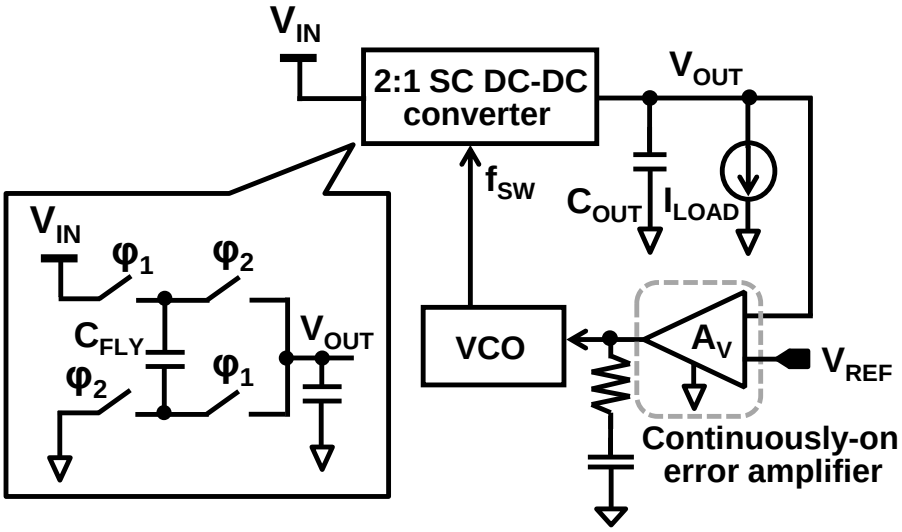
$$V_{OUT} = MV_{IN} - R_{SW}I_{LOAD} \tag{3.3}$$

where R_{SW} is the equivalent resistance of the switch, which is roughly inversely proportional to f_{SW}. In this case, the clock frequency is also equal to the switching frequency of the SC DC-DC converter but can be adjusted according to the load. Therefore, there is no need to use a fixed high frequency clock signal frequency, and the output voltage can be regulated under different load conditions. Both topologies, however, consume large current and decrease the conversion efficiency especially at light load conditions. Large switching power is consumed because of the high frequency oscillator

in Fig. 3.5(a), and large amount of DC current is consumed in Fig. 3.5(b) because of the error amplifier. As discussed in Chapter 2, even a 1-μA bias current is used in the error amplifier, it still occupies 63% of the total power when I_{LOAD} is 1 μA in a sleep mode.



(a)



(b)

Fig.3.5. Typical topologies for SC DC-DC converter. (a) Open-loop control. (b) PFM control.

To avoid using an oscillator with high frequency and avoid employing an error amplifier consuming DC current, power-law frequency scaling scheme proposed in Chapter 2 is applied to a 2:1 SC DC-DC converter to improve the conversion efficiency at light load conditions. Fig. 3.6 shows a system block diagram of the proposed SC DC-DC converter. Compared with the conventional PFM control, the error amplifier and the VCO are replaced by a clock comparator and a digitally controlled oscillator (DCO). The circuit topologies of the clocked comparator and the DCO are discussed in Chapter 2. Power-law frequency scaling scheme is realized by a FPGA for this prototype. Only logic gates on the FPGA are used and the scaling scheme can be implemented on a silicon chip easily. The DCO generates a clock signal V_{CLK} applied to the clock comparator and the FPGA. When V_{OUT} becomes lower than the V_{MIN} and detected by the clock comparator, V_{OUT_LOW} is logic high and is used to trigger a switching signal, V_{SW}, which frequency is denoted by f_{SW}. V_{SW} is used to turn on and turn off the 4 switches in the 2:1 SC DC-DC converter according to the phase φ_1 and φ_2. The frequency of V_{CLK} is controlled by a 22-bit thermometer code signal FCLK_CTRL [21:0] with the power-law frequency scaling scheme. By monitoring the frequency of V_{OUT_LOW}, the clock frequency f_{CLK} is adjusted automatically by FCLK_CTRL [21:0]. If V_{OUT_LOW} only becomes logic high in several clock period, it means the current clock frequency is too fast. The power-law frequency scaling scheme decreases the clock frequency. On the other hand, if V_{OUT_LOW} only becomes logic high in every clock period, it indicates the current clock frequency is too slow. In this situation, the power-law frequency scaling scheme increases the clock frequency. An operating timing diagram in a steady state includes the waveform of V_{CLK},

V_{OUT_LOW}, V_{OUT}, and V_{SW} is shown in Fig. 3.7. Note that compared with the buck converter proposed in Chapter 2, the output voltage of SC DC-DC converter is charged twice in one switching cycle as shown in Fig. 3.7 and also indicated in Fig. 3.3(a).

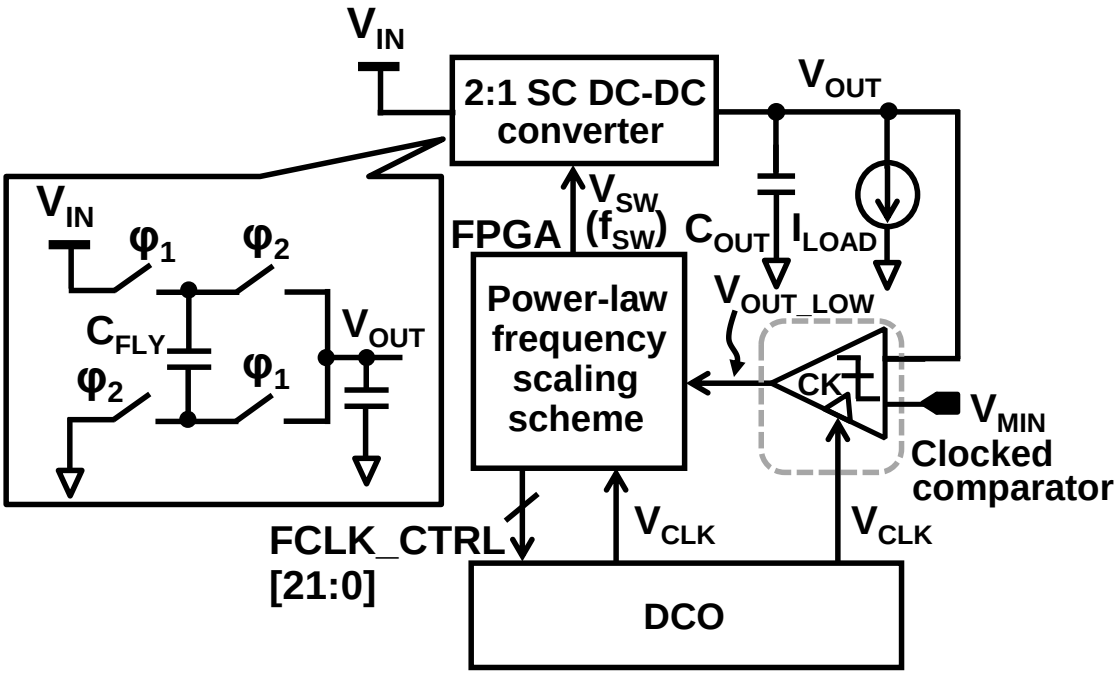


Fig. 3.6. System block diagram of proposed 2:1 SC DC-DC converter.

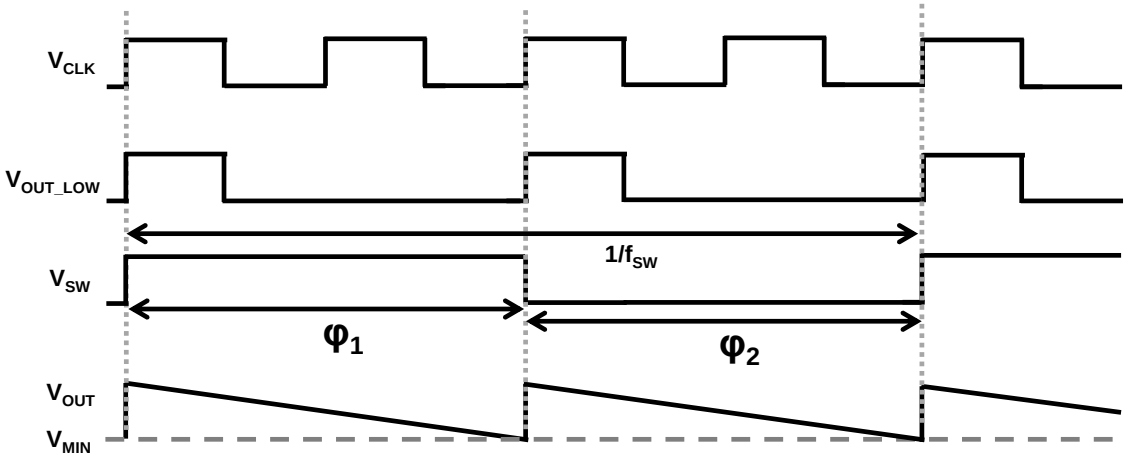


Fig. 3.7. Timing diagram including V_{CLK}, V_{OUT_LOW}, V_{SW}, and V_{OUT} in the SC DC-DC converter.

To simplify the design, the clock frequency increasing ratio and decreasing ratio are both set to 2 in this prototype, i.e. the clock frequency is doubled or halved in accordance with V_{OUT_LOW}, which is function of I_{LOAD}. In addition, as shown in (2.11), in a steady state, $f_{CLK} = K \times f_{SW}$. In a SC DC-DC converter, to make the duty cycle of switching signal V_{SW} 50%, only even numbers can be used for K. In this design, K = 4 is chosen, which is the case as shown in Fig. 3.7.

3.3 Circuit Implementation

Fig. 3.8 shows the circuit schematic of the proposed 2:1 SC DC-DC converter. The leakage-based DCO and voltage level shifter discussed in Chapter 2.4.1 and 2.4.3, respectively, are employed to provide V_{CLK} with a proper voltage level. 22-bit thermometer-coding FCLK_CTRL [21:0] are employed to control the clock frequency. Monotonic frequency tuning is ensured by the thermometer coding. The clock comparator (not shown in Fig. 3.8) discussed in Chapter 2.4.2 and shown in Fig. 2.6 is used to compare V_{OUT} with a reference V_{MIN}. Both PMOS and NMOS transistors are used as the switches to ensure each switch can be fully turned on during φ_1 and φ_2. A non-overlapping signal generation circuit is designed to prevent short current from V_{IN} to V_{OUT} when the switches are switching. An external supply V_{OSC} is used to optimize the power consumption and clock frequency. The leakage-based DCO can also be powered by V_{OUT} directly if a start-up mechanism is applied.

To demonstrate the improvement of the conversion efficiency, a testing structure using a fixed high clock frequency is employed to show the open-loop SC DC-DC converter. The circuit topology is shown in Fig. 3.5(a). The clock frequency is set by the condition that at the maximum load current, V_{OUT} is still higher than $90\% \times M \times V_{IN}$, where M is 1/2 in this case. The measurement results show that the power consumption of the oscillator is 0.816 μW at 167 KHz and 0.24 μW at 43 KHz when V_{OSC} is 0.6V. Obviously, the high frequency oscillator degrades the conversion efficiency in the sleep mode when the I_{LOAD} is 1 μA. The comparison will be shown in the next section.

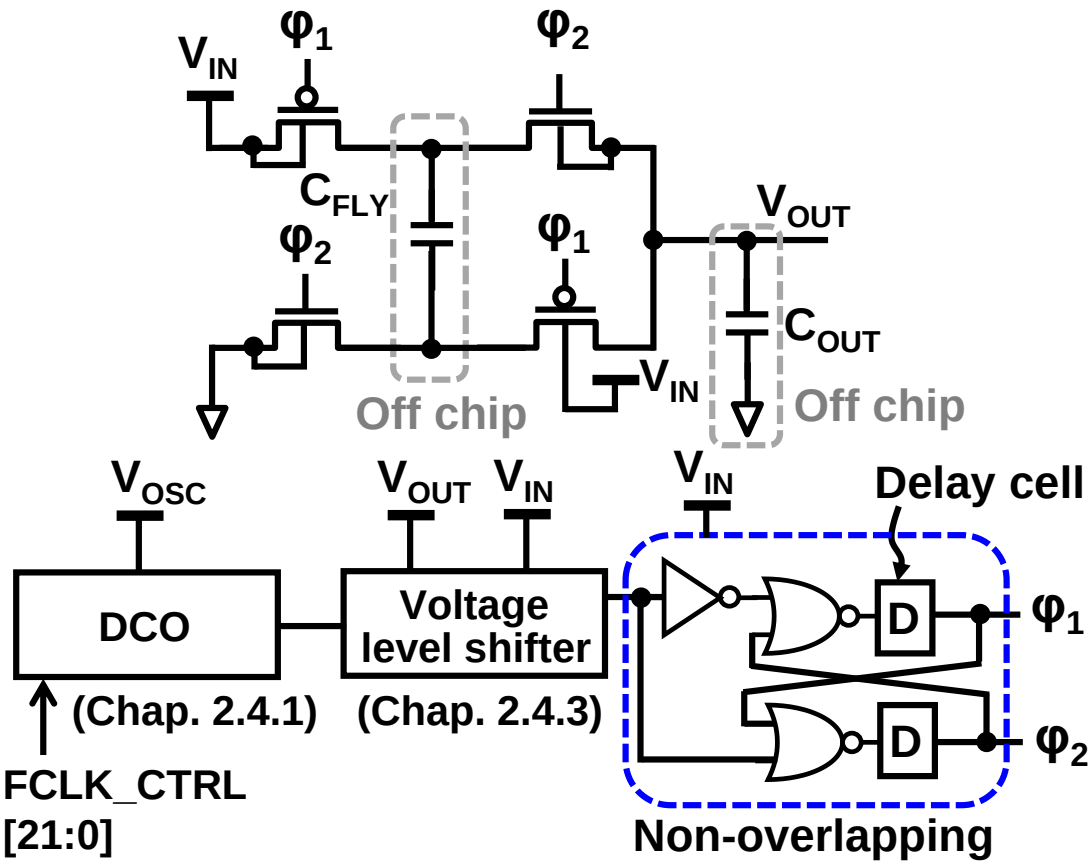


Fig. 3.8. Circuit schematic of SC DC-DC converter including DCO, voltage level shifter, and non-overlapping signal generation.

3.4 Experimental Results

The proposed 2:1 SC DC-DC converter with the power-law frequency scaling scheme is implemented in a 0.18 μm standard CMOS process. The prototype is designed for generating a local supply voltage supporting a load current range from sub-1 μA to hundred μA order. The target input ranges from 1.6 V to 1.8 V that can be generated by a global DC-DC converter. The output voltage is set to be higher than 90% of half V_{IN}. Fig. 3.9 shows the chip micrograph of the proposed SC DC-DC converter. The active area includes four MOSFET switches, digital controller, clocked comparator, and on-chip output capacitor is 0.153 mm^2. Two off-chip capacitors with 100 nF are used as C_{FLY} and C_{OUT} to measure the test chip. The power-law frequency scaling scheme is realized by an Altera Cyclone V FPGA but can be easily implemented and synthesized on a chip. Because the voltage level of the IO pins on the FPGA is 2.5 V, additional voltage level shifters are used to adjust the voltage level applied to the FPGA. The ratio, K between f_{CLK} and f_{SW} as shown in (2.11) is set to 4 in this prototype, i.e. $f_{CLK} = 4 \times f_{SW}$. The measured waveforms of the output voltage, V_{OUT_LOW}, V_{CLK}, and V_{SW} under different load conditions in a steady state are shown in Fig. 3.10 (a) and (b). In Fig. 3.10(a), a 5-μA load current is applied. The clock frequency settles to 833 Hz automatically by the power-law frequency scaling scheme. In Fig. 3.10(b), an 80-μA load current is applied, and the clock frequency settles to 22.7 kHz automatically. In both cases, V_{IN} is 1.8 V, and V_{MIN} is set to 810 mV to ensure V_{OUT} is higher than 90% of half V_{IN}. The peak-to-peak output voltage ripple at I_{LOAD} = 5 μA and I_{LOAD} = 80 μA is about 80 mV and 40 mV, respectively, which is 9.2% and 4.7% of the output voltage.

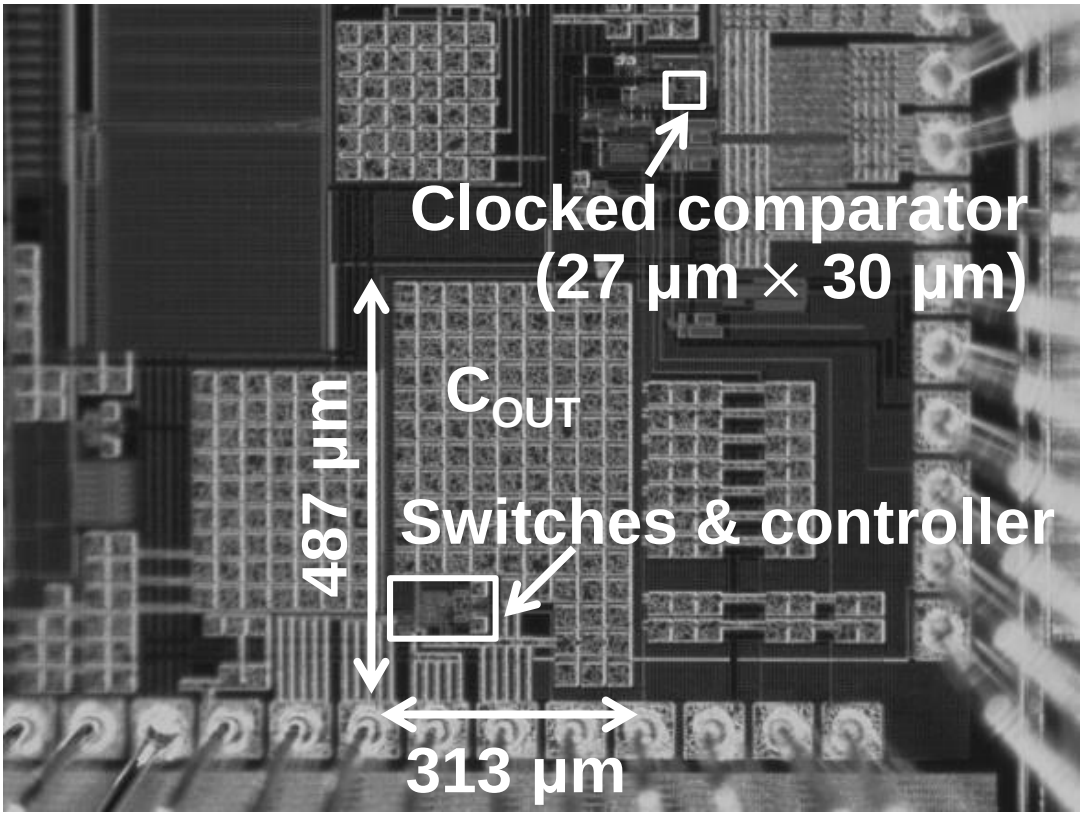
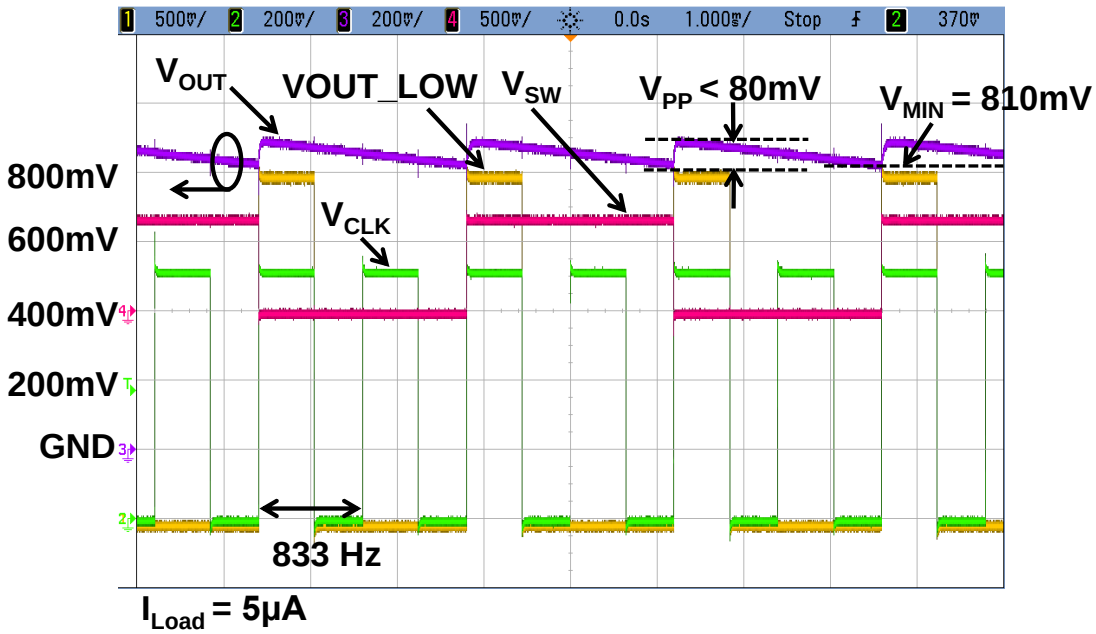
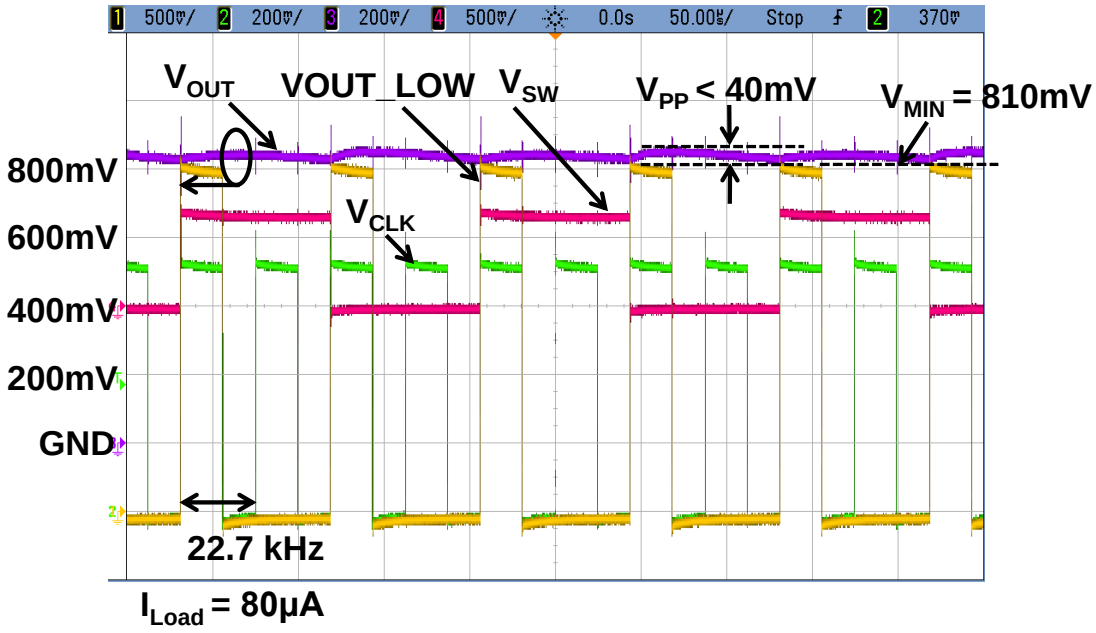


Fig. 3.9. Chip micrograph of proposed SC DC-DC converter.



(a)



(b)

Fig. 3.10. Measured waveforms of V_{OUT}, V_{OUT_LOW}, V_{SW}, and V_{CLK}. (a) V_{IN} = 1.8 V, V_{MIN} = 810 mV, and I_{LOAD} = 5 µA. (b) V_{IN} = 1.8 V, V_{MIN} = 810 mV, and I_{LOAD} = 80 µA.

Fig. 3.11 shows the measured dependences of the conversion efficiency and clock frequency on the load current. The proposed power-law frequency scaling scheme applied to the SC DC-DC converter removes the continuously-on error amplifier and high frequency oscillator in conventional topologies. The converter achieves almost flat and higher than 87.5% conversion efficiency over a load current from 600 nA to 150 µA with a peak of 94.9% when I_{LOAD} = 5 µA. At I_{LOAD} = 1 µA as the sleep current specified by BLE, 91.6% conversion efficiency is achieved, and 33% conversion efficiency is improved compared with the topology using a high frequency oscillator. The converter is able to support a load current as low as 50 nA with a conversion efficiency of 50% and can work functionally when the load is 10 nA. The measured dependences of the average output voltage and clock frequency on the load current are shown in Fig. 3.12. The output

voltage is higher than 90% of $\frac{1}{2}$ V_{IN} in whole operating range from 50 nA to 150 μA, and the minimum output voltage is 0.826 V when a 150-μA load current is applied. When the load current is larger than 100 μA, the on-resistance is dominated by the on-chip MOSFET switches resulting in higher voltage drop at the output. The performance summary table is shown in Table 3.1. The SC DC-DC converter achieves 91.6% conversion efficiency at a 1-μA load and supports a load current range from 10 nA to 150 μA when the proposed power-law frequency scaling scheme is applied. Table 3.2 shows the performance comparison with state-of-the-art SC DC-DC converter. The proposed SC DC-DC converter is able to support a load current down to 50 nA. In addition, the conversion efficiency is higher than 70% when the load current range from 200 nA to 150 μA. Obviously, compared with state-of-the-art SC DC-DC converter, the converter improves the efficiency significantly especially when the load current is lower than 10 μA.

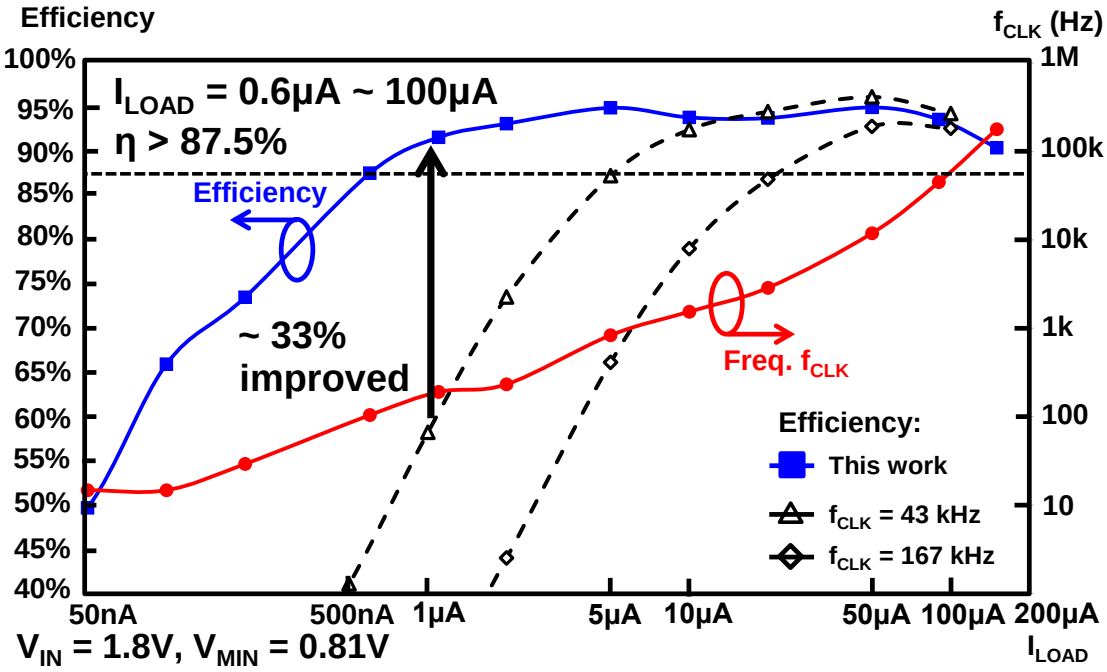


Fig. 3.11. Measured dependences of conversion efficiency and clock frequency f_{CLK} on I_{LOAD} and comparison with open-loop SC DC-DC converters using fixed f_{CLK}.

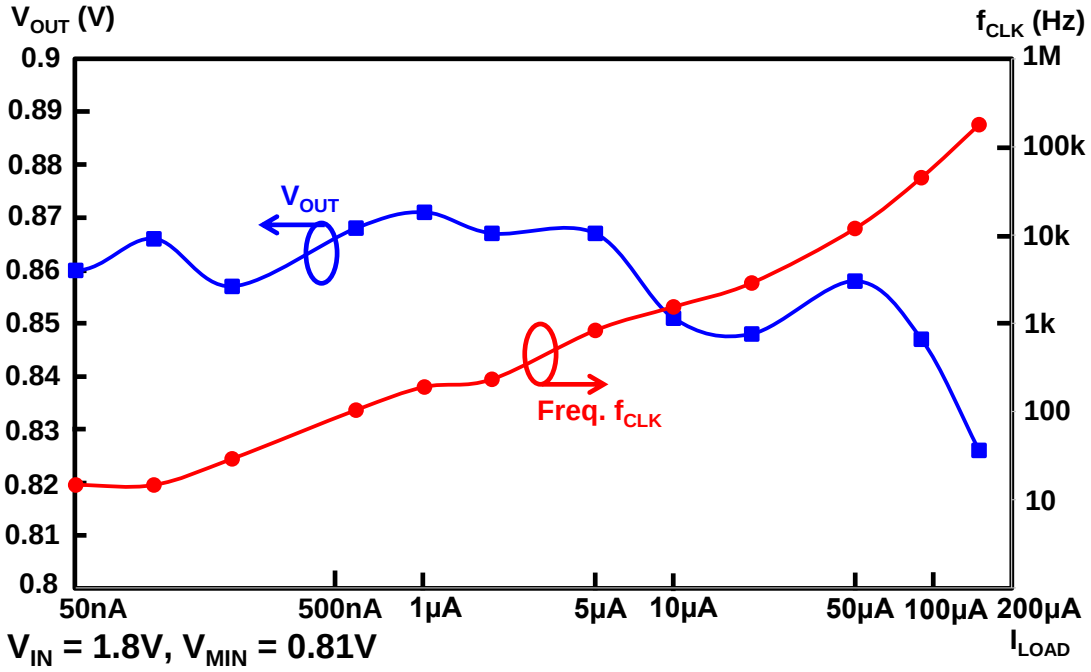


Fig. 3.12. Measured dependences of average output voltage and clock frequency f_{CLK} on I_{LOAD}.

Table. 3.1. Summary of the Performance

	This work
Technology	**180nm CMOS**
Topology	**2:1 switched-capacitor**
Die size	**0.153 mm^2**
V_{IN} (V)	**1.6 – 1.8**
V_{OUT} (V)	**0.8 – 0.9**
I_{LOAD}	**50 nA – 150 µA**
I_{LOAD} (η > 70%)	**200 nA – 150 µA**
Peak eff. η_{PEAK}	**94.9%**
η @ I_{LOAD} =1µA	**91.6%**
Clock frequency	**14.4 Hz – 179 kHz**
Off-chip capacitance	**100 nF × 2**
Control methodology	**Power-law frequency scaling control**

Table 3.2. Summary of Performance Comparison

	ISSCC'14 [3.9]	ISSCC'13 [3.10]	ISSCC'16 [3.11]	**This work**
Technology	180nm CMOS	130nm CMOS	180nm CMOS	**180nm CMOS**
V_{IN} (V)	2.5	1.5	0.9 – 4	**1.6 – 1.8**
V_{OUT} (V)	0.1 – 2.18	0.4 – 1.1	0.6, 1.2, 3.3	**0.8 – 0.9**
I_{LOAD} / P_{LOAD}	10µA – 1mA	20µA – 1mA	20nW – 500µA	**50nA – 150**µA
I_{LOAD} (η > 70%)	20µA – 1mA	20µA – 1mA	N.A.	**200nA – 150**µA
Peak eff. η_{PEAK}	85%	93%	81%	**94.9%**
η @ I_{LOAD} =1µA	~ 50%	N.A.	67%	**91.6%**
Total capacitance	3nF	8nF	N.A.	**100nF × 2**

3.5 Conclusion and Discussion

In this chapter, the proposed power-law frequency scaling scheme is applied to a SC DC-DC converter to improve the conversion efficiency at the sleep mode and achieve wide-current range operation. A 2:1 SC DC-DC converter prototype is designed with the leakage-based DCO and the clocked comparator to verify the operation. By removing the error amplifier and the high frequency oscillator used in the conventional SC DC-DC converter, the converter achieves an almost flat and higher than 87.5% conversion efficiency over a load current range from 600 nA to 150 μA. The peak efficiency is 94.9% when I_{LOAD} = 5 μA. In BLE applications, the converter achieves 91.6% efficiency when I_{LOAD} = 1 μA and achieves higher than 50% efficiency when the load current range from 50 nA to 150 μA. The converter even operates functionally at I_{LOAD} = 10 nA. Therefore, the SC DC-DC converter can be employed to generate a lower voltage on a chip. The power overhead of this converter is 43 nW and 0.23 μW at I_{LOAD} = 50 nA and I_{LOAD} = 5 μA, respectively. The power-law frequency scaling scheme dynamically adjust the clock frequency in accordance with the load current to optimize the power consumption, output voltage ripple, and output voltage level.

When the load current is lower than 200 nA, however, the efficiency is limited by the leakage-based oscillator because the minimum oscillating frequency is 14.4 Hz. Therefore, the power consumption of the clocked comparator, the DCO, and the controller circuit cannot be scaled down with the load. On the other hand, when the load current is larger than 100 μA, the on-resistance is dominated by the on-chip MOSFET switches resulting in higher voltage drop at the output. The control loop delay caused by the FPGA,

external voltage level shifters also induce an additional output voltage drop. Therefore, the average output voltage is slightly lower than the output that employs a fixed high frequency oscillator.

The future work on this research is to optimize the capacitance of the two off-chip capacitors to achieve high power density with competitive performance. In addition, the dependences of the converter power consumption, minimum output voltage level, and output voltage ripple on K mentioned in (2.11) should be analyzed theoretically. The fast wake-up operation should also be verified when the LSI system changes from a sleep mode to an active mode as discussed in Chapter 2.

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Chapter 4: Low-Power Digital Low-Dropout Regulator

In Chapter 2 and Chapter 3, the power-law frequency scaling scheme is applied to a buck converter with clocked hysteresis control and to a 2:1 SC DC-DC converter to improve the conversion efficiency in a sleep mode. By removing continuously-on comparators or error amplifiers in the controller and optimizing the switching frequency, an improved and almost flat conversion efficiency over a sleep mode and an active mode can be achieved. The third type of DC-DC converter, low drop-out (LDO) regulator, which is usually employed to supply a local voltage on a chip, should also support high current efficiency in a sleep mode and an active mode. Digital LDOs have received increased attention because it becomes difficult to design an analog LDO when the supply voltage goes lower especially in an advanced process technology. In this chapter, the design of a digital LDO with the power-law frequency scaling scheme is introduced. The target of this chapter is to propose a topology to improve the current efficiency of a digital LDO when the load current goes down to μA order. At the same time, the LDO should be able to support load current to both a sleep mode and an active mode with a quite wake-up operation.

4.1 Introduction and background of low drop-out regulator

In past decades, analog low drop-out regulator has been widely used in various applications such as sensors, RF/analog circuits, and processors because it can be designed with low quiescent current, small footprint, and low noise. Until 2010, a digital

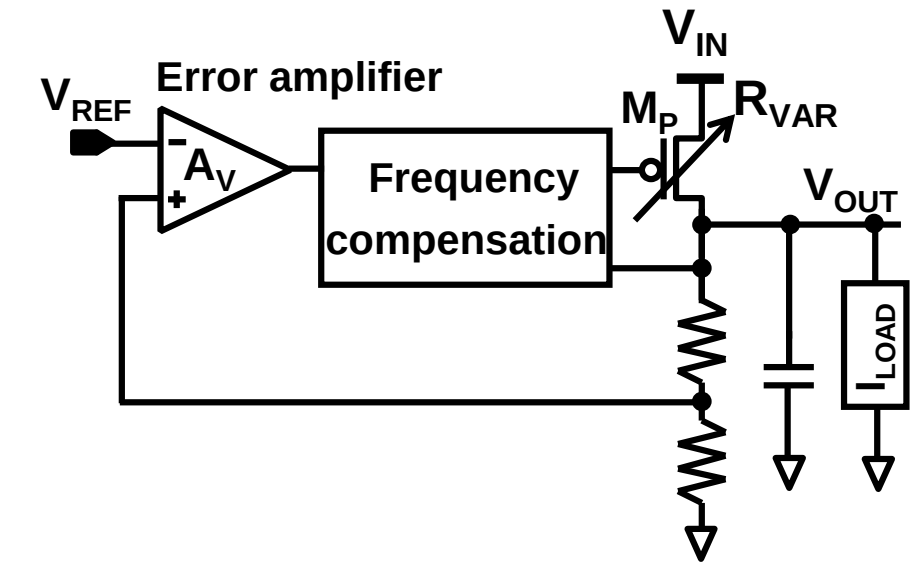
LDO that can operated at a supply voltage as low as 0.5 V was proposed [4.1]. Digital LDOs have received more and more interests in the past years because it can operate at a supply voltage near the threshold voltage of transistors. In addition, the loop compensation can be achieved in digital domain resulting in small chip area. Fig. 4.1(a) and (b) show the typical circuit schematics of an analog and a digital LDO, respectively. In an analog LDO, an error amplifier is used to compare the output voltage with a reference voltage. The voltage difference between V_{OUT} and V_{REF} is amplified and provided to a pass element M_P. The behavior of M_P acts like a variable resistor makes V_{OUT} as:

$$V_{OUT} = V_{IN} - R_{VAR} I_{LOAD} \tag{4.1}$$

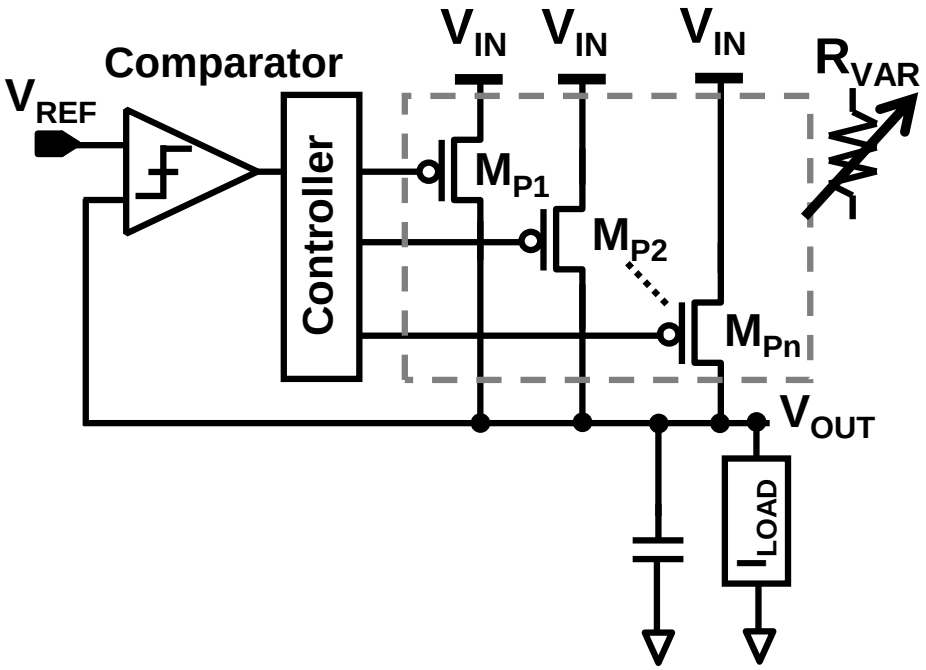
where R_{VAR} is the equivalent resistance of M_P. A frequency compensation is required in an analog LDO to make the negative feedback stable. On the other hand, in a digital LDO, the error amplifier and pass element M_P are replaced by a comparator and a switch array, respectively. The switch array is formed by numbers of transistors, M_{P1} to M_{Pn}. If V_{OUT} is lower than V_{REF}, means R_{VAR} is too large under the load current condition. More transistors in the switch array are turned on to reduce the R_{VAR}. On the other hand, if V_{OUT} is higher than V_{REF}, a part of transistors in the switch array are turned off to increase the R_{VAR}. In steady state, the output voltage can be expressed as:

$$V_{OUT} = V_{IN} - R_{VAR} I_{LOAD} \pm \Delta V \tag{4.2}$$

where ΔV is an error voltage caused by the resolution of the switch array.



(a)



(b)

Fig. 4.1. Circuit schematic of low drop-out regulator. (a) Analog topology. (b) Digital topology.

It has been reported that biasing digital circuits under threshold or near-threshold region achieves energy-efficient operation [4.2]. The analog LDO, however, becomes difficult to design the error amplifier and occupies larger area because of the frequency compensation when the supply voltage goes near the threshold voltage of a transistor. On the other hand, latch-type comparators and digital circuits can operate functionally even when the supply voltage is close or lower than transistor's threshold voltage. Therefore, a digital topology of LDO is much suitable for the applications when the supply voltage is near transistor's threshold voltage.

Recently, many research publications and applications on digital LDO even in industrial fields have been reported. A fully integrated digital LDO for IoT application has been proposed to support a load current range from 50 μA to 3 mA [4.3] with a peak current efficiency of 96.3%. A hybrid digital LDO employing analog-assisted topology [4.4] is proposed to use only 100 pF capacitance and the capacitor is able to be implemented on a chip. Additionally, digital LDO has also been proposed for processor in mobile applications [4.5]. In industrial fields, digital LDOs are also reported to be used in CPU designs [4.6]. For a sleep current that is lower than 1 μA, however, the current efficiency of the reported digital LDOs drops rapidly when the load current is μA order. Even through the digital LDO proposed in [4.7] claims that the load current ranges from 100 nA to 2 mA, the current efficiency is only about 20% when the load is 1 μA.

The controller circuits and the comparator in the previous publication consume high than μA-order current. As shown in [4.1], higher clock frequency is necessary to regulate the output voltage with small voltage error and to achieve a fast load transient response.

The quiescent current, however, increases significantly with the clock frequency. As shown in [4.1], the quiescent current increases from 2.7 μA to 15 μA when the clock frequency changes from 1 MHz to 10 MHz. In this case, the power-law frequency scaling scheme is suitable to dynamically adjust the clock frequency according to the load conditions. Therefore, the control power consumption including the clocked comparator can be scaled, and almost flat current efficiency can be achieved over the load range from μA to mA. In addition, fast wake-up operation from a sleep mode to an active mode can also be achieved if the wake-up mechanism discussed in Chapter 2 is applied.

4.2 System Architecture

The proposed system architecture of a digital LDO with the power-law frequency scaling scheme is shown in Fig. 4.2. An on-chip switch array can be designed according to the load current range and the output voltage resolution. The leakage-based DCO and clock comparator discussed in Chapter 2.4.1 and Chapter 2.4.2, respectively, can be designed on a same chip with the digital LDO. The clock comparator compares V_{OUT} with a reference voltage V_{REF}, and outputs a control signal to the power-law frequency scaling scheme logic. A switching signal V_{SW} used to turn on or turn off the switch transistors in the switch array acts like the VOUT_LOW signal that we discussed in Chapter 2 and Chapter 3. Depending on the load conditions, the clock frequency V_{CLK} can be scaled with the frequency of V_{SW}, which is proportional to the load. Therefore, the power consumption of the control circuits, clock comparator, leakage-based DCO, and the switching loss of the switch array can be scaled with the load conditions. An operation example shown in Fig. 4.3 is used to indicate the digital LDO output waveform, V_{SW}, and V_{CLK} when the power-law frequency scaling scheme is applied and $F_{CLK} = 4 \times F_{SW}$. In addition, a wake-up signal provided by the system can also be used to reset all control bits of FCLK_CTRL to a proper value. Therefore, quick wake-up operation can be achieved without large output voltage drop.

For a load current with a value of lower than 1 μA, a switch with very large resistance becomes necessary. The stack transistor structure [4.7] can be employed to design the switch in the switch array. A switch array includes both coarse and fine switches can be used to support load current for a wide-current range. Fig. 4.4 shows the switch array

include M-bit coarse tuning switches and N-bit fine tuning switches. The output voltage resolution can be improved without losing the fast transient response.

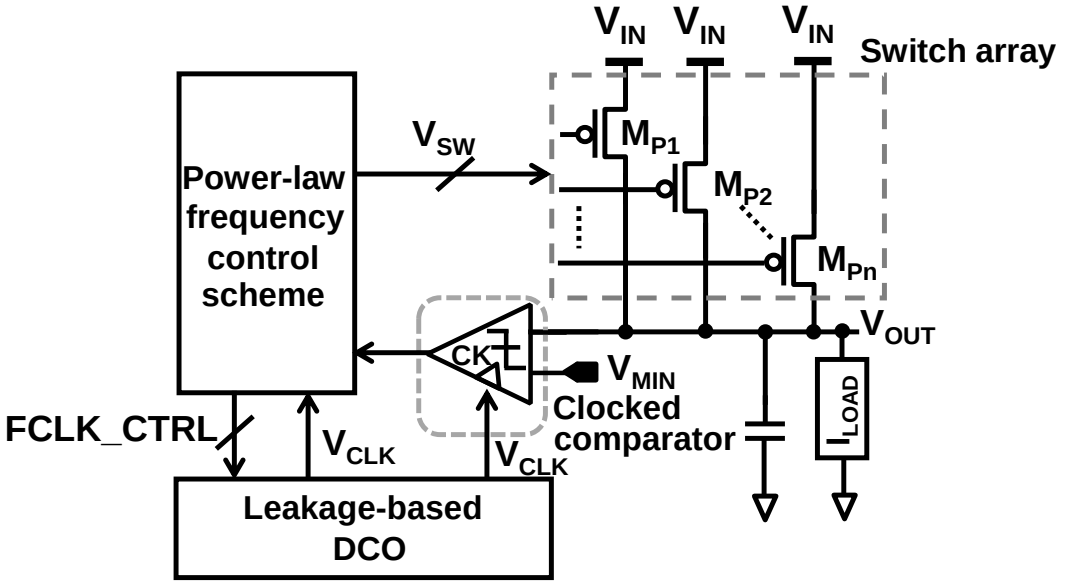
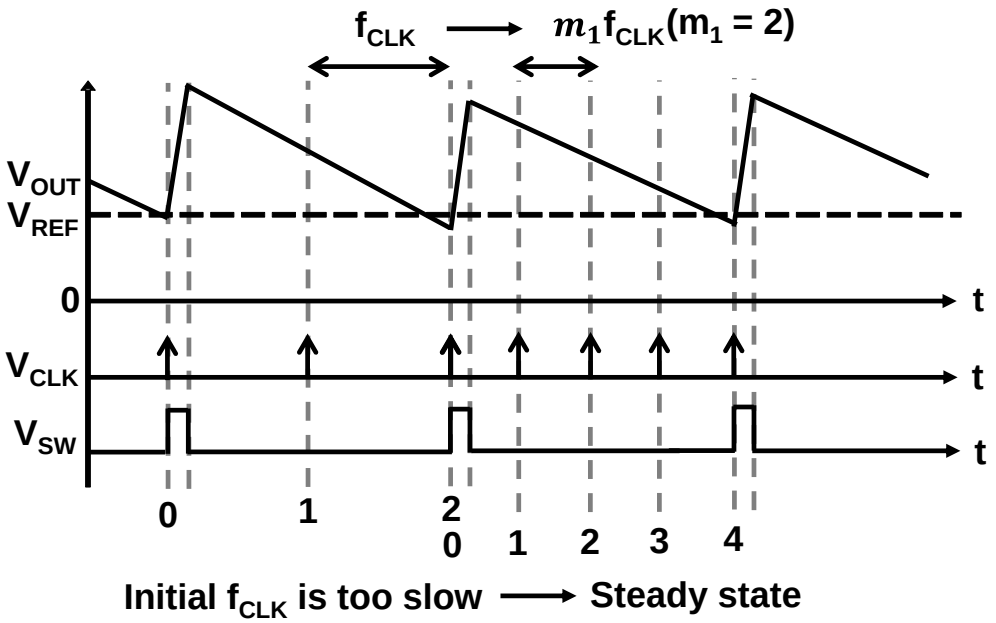
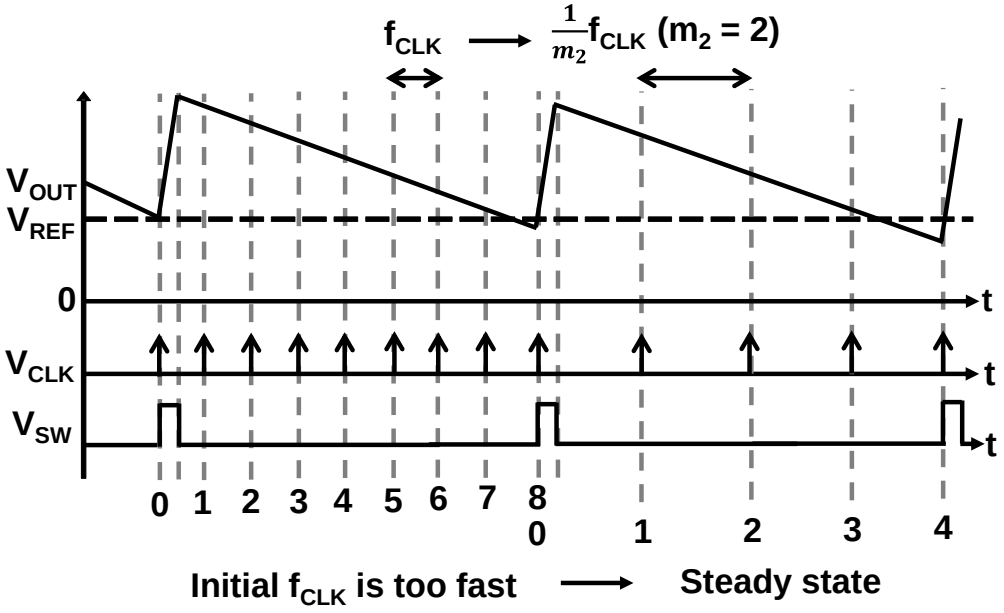


Fig. 4.2. Proposed system architecture of digital LDO with power-law frequency scaling scheme.



(a)



(b)

Fig. 4.3. Operation example of the digital LDO output waveform, clock signal, and V_{SW} when $f_{CLK} = 4 \times f_{SW}$ is designed. (a) The initial f_{CLK} is too slow. (b) The initial f_{CLK} is too fast.

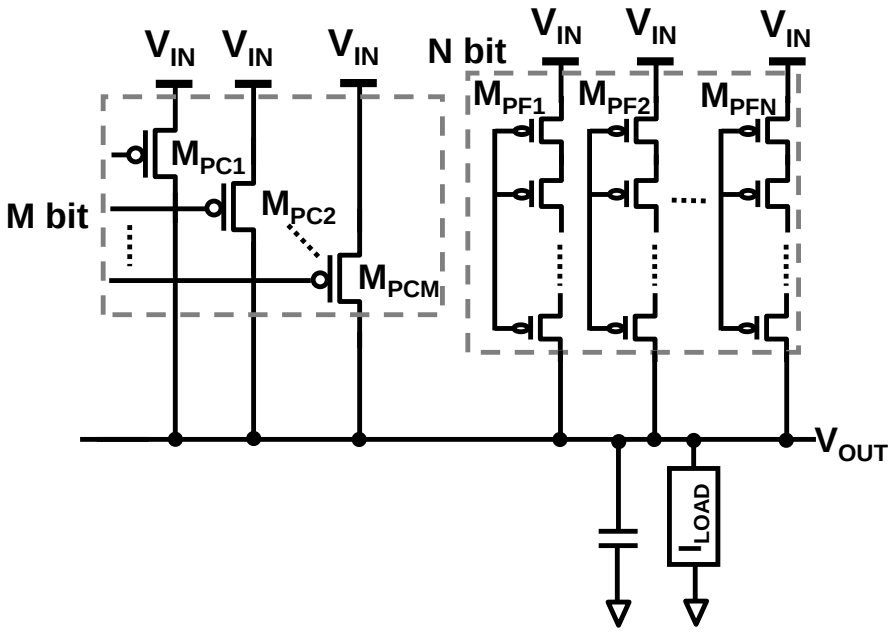


Fig. 4.4. Switch array includes M-bit coarse tuning and N-bit fine tuning.

4.3 Circuit Implementation and Simulation Results

A digital LDO including a switch array and a clocked comparator is designed in a standard CMOS 65nm process technology with 2.5-V IO devices for verification. In this design, the input voltage is set to 0.6 V and the output voltage is 0.5 V, which can be supplied to digital circuits for energy-efficient operation. The switch array shown in Fig. 4.2 is designed and simulated to support a load condition range from 100 nA to 10 mA. In the simulation, the output capacitor is designed as 100 nF, which is possible to be implemented on a chip. IO devices are used to implement the clock comparator to reduce the leakage current in 65nm process technology. To simulate the control current consumption, the gate count of the power-law frequency scaling scheme is about 700 gates synthesized by an external FPGA as shown in Chapter 2. These logic gates can also be implemented on a 65nm CMOS chip easily. Therefore, the gate capacitance of logic gates in these process technology is simulated, and the current consumption is calculated by:

$$I_{CONTROLLER} = \frac{Q}{t} = C_{GATE} V_{IN} f_{CLK} \tag{4.3}$$

Where C_{GATE} indicates the gate capacitance of an IO transistor, and V_{IN} is 0.6 V in this case. The simulated and calculated current consumption of the clocked comparator and the control circuits are shown in Fig. 4.5.

A simulated and calculated current efficiency of a digital LDO with power-law frequency scaling scheme is shown in Fig. 4.6. Current efficiency is used in the LDO design. A conventional digital LDO employing a fixed high frequency (f_{CLK} = 2 MHz) such as [4.1] is used for comparison. When I_{LOAD} is larger than 500 μA, both the proposed

digital LDO and the conventional one can achieve a current efficiency higher than 99%. When I_{LOAD} goes down to μA order, however, the current efficiency of the conventional digital LDO degrades rapidly. Compared with the conventional digital LDO, the simulated current efficiency of the proposed LDO can be improved 61% because the control current consumption can be scaled by the power-law frequency scaling scheme. The dependence of f_{CLK} on the load conditions is also shown in Fig. 4.6. Simulation results show that when I_{LOAD} = 1 μA and f_{CLK} = 4 kHz, the peak-to-peak output voltage ripple is 16.5 mV, which is 3.3% of the output voltage. The simulation results show that the proposed digital LDO with the power-law frequency scaling scheme can improve the current efficiency in μA order load conditions and extend the minimum load current to 10 nA.

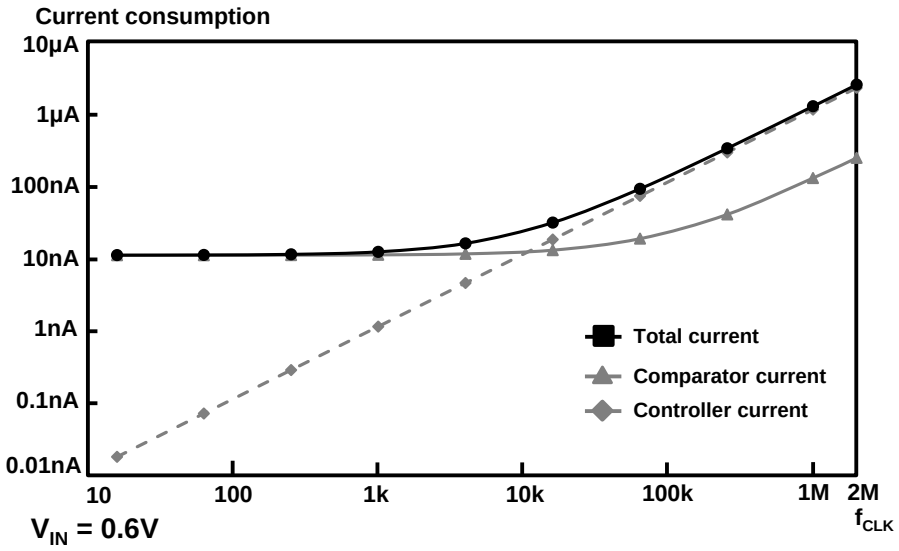


Fig. 4.5. Simulated and calculated current consumption of the clocked comparator and the power-law frequency scaling scheme in the digital LDO.

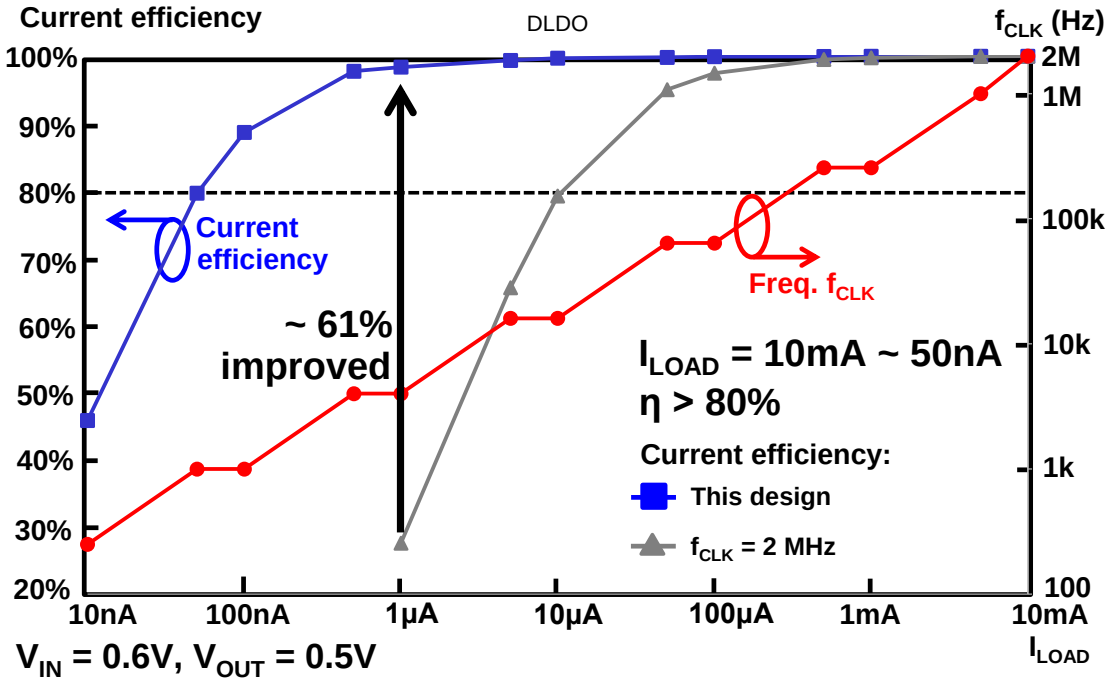


Fig. 4.6. Simulated and calculated dependence of the current efficiency and clock frequency on I_{LOAD}.

4.4 Summary and Discussion

In this chapter, we proposed a design concept of digital LDO with the power-law frequency scaling scheme to improve the current efficiency for light load current conditions and wide-current range applications. The clock frequency of the clock comparator can be optimized in accordance with the load current conditions, output voltage ripple, and converter power consumption. In addition, employing two groups of switch array including coarse and fine tuning can increase the voltage resolution over wide load current range. Therefore, the proposed digital LDO is able to achieve high efficiency in the sleep mode and support both the sleep and the active mode. A simulation is conducted to verify the design of the proposed digital LDO and show that 61% current efficiency is improved compared with a conventional design.

The switch array control signals, however, should be designed sophisticatedly. The output voltage can be expressed as:

$$V_{OUT} = V_{IN} \frac{R_{LOAD}}{R_{VAR}+R_{LOAD}} \tag{4.3}$$

where R_{VAR} is controlled by the switch array and R_{LOAD} is the equivalent resistance of the load. The output voltage, however, is neither determined by the hysteresis window nor by the converter configuration. The charging behavior of the output voltage in a digital LDO is different from a hysteresis buck converter and a SC DC-DC converter. Therefore, the future work includes not only the clock frequency optimization but also the analysis of the output voltage ripple and the loop stability. In addition, the oscillator power consumption is not included when calculate the current efficiency. The proposed leakage-based DCO in Chapter 2 still consumes relatively high current when the load goes to nA

order. A much more low-power digitally controlled oscillator should be designed and implemented in 65nm process technology to avoid degrading the current efficiency.

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Chapter 5: Conclusion

Conversion efficiency and load current range are the most important factors in a DC-DC converter. For the wide-current range applications including a sleep mode and an active mode such as IoT, implantable electronics, and wearable devices, DC-DC converter with high conversion efficiency becomes much more important in order to prolong the battery lifetime. Previous publications and research on DC-DC converter cannot support high conversion efficiency in both sleep and active modes especially when the load goes down to μA order. This thesis proposed a novel power-law frequency scaling scheme that is suitable for inductive, capacitive, and resistive DC-DC converters. The frequency scaling scheme is applied to a newly proposed clocked hysteresis control buck converter, a 2:1 SC DC-DC converter, and a digital LDO.

In Chapter 1, the research background of wide-current range applications are introduced. Energy consumption calculated according to BLE specifications. To clearly indicate the reason why the conversion efficiency in a sleep mode becomes much more important, two real applications used in IoT are introduced.

In Chapter 2, at first, we investigated the conventional control schemes for a buck converter operating in discontinuous conduction mode for Bluetooth Low Energy specifications. To eliminate the DC current consumed by the continuously-on comparator, a clocked hysteresis control is introduced for a hysteresis buck converter. Additionally, a power-law frequency scaling scheme is proposed to scale the conduction loss, switching loss, and comparator power in the converter with the load conditions. Therefore, an almost flat conversion efficiency is achieved and the conversion efficiency

in μA-order load conditions is also improved. As to the theoretical aspect, expressions for the frequency stability conditions, power consumption, and output ripple are derived and analyzed. A clocked hysteresis control buck converter with the double-half frequency scaling scheme is designed and implemented to verify the theorem and analysis. Experimental results demonstrate that the buck converter achieves conversion efficiency of higher than 87% over I_{LOAD} ranging from 500 nA to 20 mA with a peak value of 90.4%. Compared with state-of-the-art low-power and wide-current range buck converters, 12% ~ 34% conversion efficiency is improved when I_{LOAD} is 1 μA. The I_{LOAD} wake-up operation with the frequency scaling scheme is also verified. Therefore, the proposed buck converter achieves both high conversion efficiency in a sleep mode and quick wake-up operation, making it extremely suitable for energy-efficient and wide-current range applications.

In Chapter 3, we introduce the concepts and research background of switched-capacitor (SC) DC-DC converter firstly. Recent publications show the conversion efficiency of the SC DC-DC converters become lower than 70% when the load current is lower than 10 μA. Moreover, the conversion efficiency of all SC DC-DC converters degrade steeply in μA order. By analysis, the high-frequency oscillator and/or the continuously-on error amplifier in the SC DC-DC converter consume a large amount of power. Therefore, a 2:1 SC DC-DC converter prototype is implemented with the power-law frequency control scheme to improve the conversion efficiency over a wide load condition. The converter achieves an almost flat and higher than 87.5% conversion efficiency over a load current range from 600 nA to 150 μA. The peak efficiency is 94.9%

when I_{LOAD} = 5 μA. Compared with using a fixed, high frequency oscillator, conversion efficiency is improved by 33% when I_{LOAD} = 1 μA. The converter can also support a load current range from 50 nA to 150 μA that can extend the sleep mode range to nA order. The future work of the SC DC-DC converter is to optimize the power density and analyze the output voltage ripple versus conversion efficiency theoretically.

In Chapter 4, digital LDO with the power-law frequency scaling scheme is introduced. The load current range of the digital LDOs proposed recently is limited to about 10-μA order load condition because the quiescent current consumed by the controller and the clock comparator limits the current efficiency. High frequency clock is necessary for the clock comparator and controller loop to stabilize the output voltage with fast response speed. As shown in [4.1], the current consumption of a digital LDO strongly depends on the clock frequency. A digital LDO with the power-law frequency scaling scheme is designed and simulated to optimize the clock frequency according to the load conditions. A simulation result is used to demonstrate the operation functionally. Compared with a conventional digital LDO using a fixed and high frequency clock, 61% current efficiency is improved. In addition, wide load current range operation can be achieved by separating the switch array into a coarse-tuning and a fine-tuning group. As a result, the proposed digital LDO can achieve high current efficiency at light load conditions and support wide load current range operation.

Conversion efficiency in a sleep mode for electronic devices that stay in a sleep mode for most of the time will become more and more important in the future in order to prolong the battery lifetime. In a sleep mode, however, the DC-DC converter converting input

voltage to a stable output voltage provided to other functional circuits consumes large amount of power and limits the conversion efficiency. This thesis proposed a power-law frequency scaling scheme that can be applied to inductive, capacitive, and resistive DC-DC converters to improve the sleep mode efficiency and to support wide-current range applications. In addition, a clocked hysteresis control is proposed for buck converters that can achieve fast wake-up operation when the load changes from a sleep to an active mode.

Related Publications

Journals:

[1] C.-S. Wu, M. Takamiya, and T. Sakurai, “Clocked Hysteresis Control Scheme with Power -Law Frequency Scaling in Buck Converter to Improve Light-Load Efficiency for IoT Sensor Nodes,” submitted to *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* in Sep. 2017, finished minor revision and resubmitted in Dec. 2017.

International Conferences:

[1] C.-S. Wu, M. Takamiya, and T. Sakurai, “Buck Converter with Higher Than 87% Efficiency over 500nA to 20mA Load Current Range for IoT Sensor Nodes by Clocked Hysteresis Control,” *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, Texas, USA, pp. 1-4, Apr. 2017.

Domestic Conferences/Workshops:

[1] 呉　仲祥，高宮　真，桜井貴康，"Wide Load Range Buck Converter Using Clocked Hysteresis Control for IoT Sensor Nodes,"電子情報通信学会，LSIとシステムのワークショップ，ポスターセッション 学生部門，59，東京，2017年5月.

Other Publications

Journals:

[1] C.-S. Wu, H.-H. Lee, P.-H. Chen, and W. Hwang, “Digital Buck Converter with Switching Loss Reduction Scheme for Light Load Efficiency Enhancement,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 25, issue 2, pp. 783-787, Feb. 2017.

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[1] C.-S. Wu, K.-C. Lin, Y.-P. Kuo, P.-H. Chen, Y.-H. Chu, and W. Hwang, “An All-Digital Power Management Unit with 90% Power Efficiency and ns-order Voltage Transition Time for DVS Operation in Low Power Sensing SoC Applications,” *IEEE International Symposium on Circuits and System (ISCAS)*, Lisbon, Portugal, pp.1370-1373, May 2015.

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