# 論 文 の 内 容 の 要 旨

論文題目　Power-Law Clock Frequency Control Scheme in CMOS On-Chip DC-DC Converters for Wide Current-Range Applications
（べき乗則周波数制御による広い出力電流範囲に対応したCMOSオンチップDC-DCコンバータ）

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With growing development of the Internet-of-Things (IoT), wearable devices, and implantable medical electronics, there is an increasing demand for low-power and energy-efficient large-scale integrated (LSI) circuits. The power consumption of these LSI circuits, however, varies significantly depending on the operating conditions such as the sleep mode or the active mode. As specified by the Bluetooth Low Energy, the load current range can change more than $10^4$. In addition, the electronic devices are required operating for a long time without the need to replace the battery because of the material and the labor cost. A DC-DC converter is used to convert the battery input voltage to a well-regulated output voltage for the electronic devices. To prolong the battery lifetime, the DC-DC converter should support more than $10^4$ wide output current range with high conversion efficiency. Unlike mobile and laptop applications, however, it shows the LSI circuits in the IoT, wearable electronics, and implantable medical sensors stay in a sleep mode for most of the time and turn into an activate for only a short period of time to transfer data. Therefore, a DC-DC converter achieving high conversion over wide current range, especially in sleep mode, becomes increasingly important to reduce the overall energy consumption. Besides, an on-chip CMOS design technology is attractive to develop low-cost and compact physical dimension LSI circuits and systems.

This thesis is organized with five chapters. The first chapter describes an introduction including the wide-current range applications such as IoT and the contribution of this thesis. The research motivation and the reason why the conversion efficiency of a DC-DC converter is important especially in the sleep mode are also shown in Chapter 1. Two applications of IoT are employed to calculate the LSI systems energy consumption.

In Chapter 2, a clocked hysteresis control scheme with power-law frequency scaling is newly proposed to improve the conversion efficiency at a light load current and applied to a buck converter design. Compared with a conventional hysteresis control buck converter, the buck converter consumes no DC current in the comparators by replacing a continuously-on comparator by a clocked comparator with power-law frequency scaling. In addition, the clocked hysteresis control maintain a quick wake-up feature because of the inherent hysteresis control. As to the theoretical aspect, expressions for the frequency stability condition, power consumption, and output voltage ripple of the proposed power-law frequency scaling scheme are derived and analyzed. Experimental results show that the buck converter implemented with the power-law frequency scaling scheme achieves higher than 87% and almost flat conversion efficiency over a load current ranging from 500 nA to 20 mA with a 90.4% peak efficiency.

A 2:1 switched-capacitor (SC) DC-DC converter implemented with the proposed power-law frequency scaling scheme is proposed in Chapter 3. This chapter shows that the proposed scheme is also able to improve the conversion efficiency of a SC DC-DC converter in the sleep mode. A prototype is designed and implemented in a standard CMOS 0.18 μm process technology. Experimental results show that the converter achieves higher than 87.5% and almost flat conversion efficiency over a load current range from 600 nA to 150 μA with a 94.9% peak efficiency. The conversion efficiency is higher than 50 % when a load current ranging from 50 nA to 150 μA is applied, and can operate functionally when the load is as low as 10 nA. Compared with a 2:1

switched-capacitor DC-DC converter using a fixed high frequency clock, the proposed converter improves 33% of conversion efficiency when the load current is 1 μA.

A design of digital low-dropout regulator with the power-law frequency scaling scheme is introduced in Chapter 4. By automatically adjusting the clock frequency of the clock comparator used in a digital LDO, the current efficiency can be improved especially in a light load condition. The target is to optimize the clock frequency and current efficiency with the load conditions to improve the current efficiency under μA order load conditions. A proposed system topology is introduced and simulated in this chapter.

Chapter 5 shows the summary and the conclusion of this thesis.