博士論文

Study on SPAD Imagers with Quick Readout Circuits

(高速読み出し SPAD イメージャに関する研究)

平成 29 年 12 月 1 日提出

指導教員　浅田邦博　教授

東京大学大学院工学系研究科

電気系工学専攻

37-157091

楊　驍

Xiao Yang

Study on SPAD Imagers with Quick Readout Circuits

(高速読み出しSPADイメージャに関する研究)

A Dissertation

Submitted to the Department of

Electrical Engineering and Information Systems,

The University of Tokyo

in Partial Fulfillment of the Requirements

for the Degree of Doctor of Philosophy

Supervisor: Professor Kunihiro Asada

楊　驍

Xiao Yang

Dept. of Electrical Engineering and Information Systems

The University of Tokyo

December 2017

Abstract

This thesis focuses on the design of a SPAD in the standard CMOS process, and the design of SPAD imagers. The basic principle and key parameters of a SPAD are introduced in Chapter 2. Then, structures and experimental results about the designed several types of SPADs are presented in Chapter 3. From Chapter 4 to Chapter 5, a new sensor architecture with high readout efficient and 3 SPAD imagers utilizing the proposed architecture are shown. In Chapter 6, a SPAD imager with real-time event discriminator is introduced.

Chapter 2 provides an introduction about basic principles and features of SPAD in order to understand the required constraints in designing CMOS SPAD. The breakdown voltage, dark counts rate (DCR) , and photon detection efficiency (PDE) are introduced. According to the introduction, the breakdown voltage of a SPAD should be greater than 15 V in order to suppress the influence of band to band tunneling, and s suitable guard ring is necessary for preventing premature breakdown due to edge effect. Furthermore, an analysis on the influence of DCR and PDE is introduce, and the desirable DCR for the SPAD imager is about 10 kHz.

Chapter 3 focuses on designing and testing about SPADs fabricated by the available standard CMOS process. The detail about the design of SPADs used for the SPAD imagers in this work are presented in this chapter. The structures of three types of CMOS SPADs are reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process in order to find a suitable structure of SPADs are introduced. According to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V. A suitable SPAD of Pwell/DeepNwell with PolyGate around the active region, low DCR with purely avalanche breakdown, and planer breakdown region were confirmed by the experimental results. Then, a test circuit for after-pulsing probability measurement is presented. The experimental results

demonstrates the efficiency of hold-off time about reducing the influence of after-pulsing, and the after-pulsing probability can be decreased to lower than 1% with a 20 ns hold-off time.

This chapter targets on the efficient readout architecture for SPAD imagers. Since the breakdown SPAD pixels are sparse in many applications, an architecture that only extracts the address of breakdown pixels can achieve a higher readout efficiency. A breakdown pixel extraction (BPE) readout architecture is proposed based on the binary feature of SPADs. The design and behavior of BPE architecture are introduced at first, and the design of a 15×15 SPAD imager to verify the functionality of the proposed architecture is presented. Then, a detail design about the imager with 31×31 pixels utilizing background readout method is shown. This imager adds an additional 1-b memory in each pixel to store the value of the previous frame, and to realize the background readout. This method can minimized T_{dead} to 3 cycles under dark conditions or under sparse breakdown pixels. Furthermore, another BPE based 31×31 SPAD imager with event discriminator is proposed for minimizing T_{dead} and event detecting. This imager counts the value of $Max(_{BD,i})$ of each frames at first, and the readout procedure only starts when $Max(_{BD,i})$ became larger than a threshold value.

Chapter 5 presents the experimental results including the functionality, DCR distribution, PDE and dead time about the three designed imagers in Chapter 4. For the first designed sensor with 15×15 SPAD array, the functionality of BPE readout method is experimentally demonstrated firstly. Then, the DCR distribution is measured, and the median value, mean value, are 10 kHz, 20 kHz, respectively. Based on the measured DCR, an analysis about the temporal aperture ratio (TAR) is show. For the second imager that contains 31×31 SPAD array with background readout method based on BPE architecture, the ability of random event detection has been shown by pulsed laser imaging at first. Then, measurements about the DCR distributions of the images with different SPAD sizes are presented. Furthermore, an analysis about the requirements that can minimize T_{dead} is presented, and TAR as function of T_{win} has been shown comparing with the first imager. A 40% improvement of TAR is shown based on the calculated results. Finally, Photon detection efficiency of designed SPAD is measured. For the third imager that employs an event discriminator based on BPE architecture, the functionality of this sensor is measured using the same method as the previous one.

Then, an analysis about the setting of threshold value is shown.

Chapter 6 shows the design a 32×32 SPAD imager with the real time current logic event discriminator together with the experimental results. This imager employs a current logic to monitor the number of breakdown pixels in real time, and a free-running with variable hold-off time active quenching circuit is proposed to achieve zero T_{dead}. The ability of random event distinction is shown through the experimental results.

Acknowledgements

I would like to thank all the teachers, colleagues, friends, and family that have supported me throughout the duration of my thesis work.

I would like to express my special appreciation and thanks to my dissertation supervisor, Professor Kunihiro Asada, for the continuous support of my Ph.D study and related research, for his enduring guidance, keen insight, encouragement throughout my graduate studies. His considerable advices and fruitful discussions lead my research to the right direction. I fell very fortunate to have taken him as my supervisor, and the precious experiences in these years will be irreplaceable assets in my life.

I would also like to thank Professor Toru Nakura and Professor TeTsuya Iizuka for their constructive support and help, and give me many meaningful advices and discussions on my research. I am also very grateful to Professor Makoto Ikeda, who gives me a comfortable research environment and many advices that encourage me a lot in my laboratory life.

I am deeply grateful to Dr. Hongbo Zhu, who is currently in Sony semiconductor solutions for his valuable advices in the start-up phase of my research. I am also thankful to Dr. Nguyen Ngoc Mai Khanh for his support and advices on chip measurements.

I would also thank to all the current and past members in Asada, Ikeda, Nakura and Iizuka laboratory for their helpful advices, encouragement, comfortable research circumstances and pleasant time: in particular, Mr. Hiroki Yabe, who is currently in SanDisk Corp, for his support and advice about CAD and image sensor design; Dr. Toshiyuki Kikkawa and Dr. Parit Kanjanavirojkul, for their friendly talk and many essential advices on my laboratory life; Mr. Kai Xu for having many meaningful discussions on scintillation detectors as well as a plenty of pleasant time with me.

I would like to acknowledge my dissertation committee, Professor Yoshio Mita, Professor Makoto Takamiya, and Professor Toshihiko yamasaki, for their extremely valuable sugges-

tions and comments.

I with to thank all the members of VLSI Design and Education Center (VDEC), the University of Tokyo, for their support in CAD environment and VLSI process technologies. The CAD tools and process technologies used in this study has been provided by Synopsys, Inc. Cadence Design Systems, Inc, and Rohm Corp. through VDEC.

I also wish to thank the Yamaoka Scholarship Foundation for the financial support.

Finally, I would like to express my appreciation to my parents Fengkui Yang and Di Ma, and to my wife Huiting Wang, for their constant support and encouragement throughout my life.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

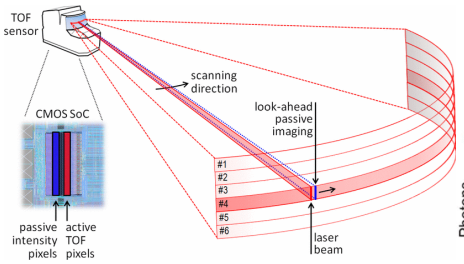
1.1 Background

Recently, single photon detectors are employed in a wide variety of applications in science and technology because of its high sensitivity and fine time resolution. These applications include time-of-flight (ToF) 3D sensors [1, 2, 3, 4, 5, 6], scintillation detectors [7, 8, 9, 10], fluorescence lifetime imaging microscopy (FLIM) [11, 12, 13, 14], Raman spectroscopy (RS) [15, 16, 17], and ultra-fast imaging [18, 19, 20] as shown in Fig. 1.1.

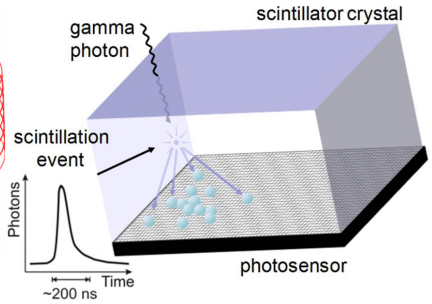
These applications requires to detect the incident photons in a high response speed, and photomultiplier tubes (PMT) have been utilized as the photon detectors before [21]. A PMT contains a photo-cathode, several electron multipliers, and an anode. Incident photons is converted into electrons through the photo-cathode, and these electrons are multiplied by the electron multipliers. Then, a larger number of electrons reach the anode and generate a current pulse. The PMT can detect very weak light with high resolution, so that it can satisfy the requirements for the applications mentioned above.

However, the drawbacks of the conventional PMTs are also obviously. Even though position sensitive PMT (PS-PMTs) has been developed to improve the spatial resolution, it is limited by its large size. PMTs are unable to be operated under high magnetic field, and sensitive to electromagnetic disturbances. Moreover, PMTs are fragile, high cost, and require very high supply voltages (2 to 3 kV) [22]. Therefore, a solid-state, low cost, low power, and high sensitive single photon detector is desirable.

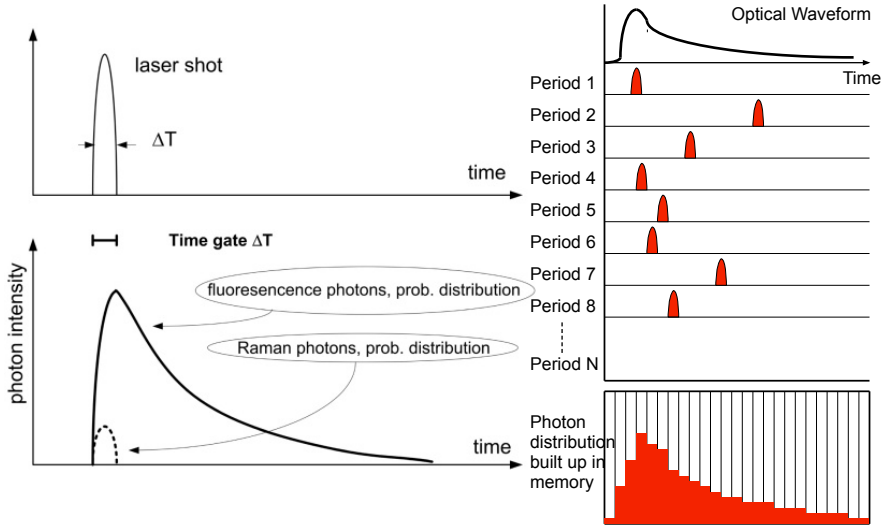
Single photon avalanche diodes (SPAD) imager fabricated by a standard CMOS process



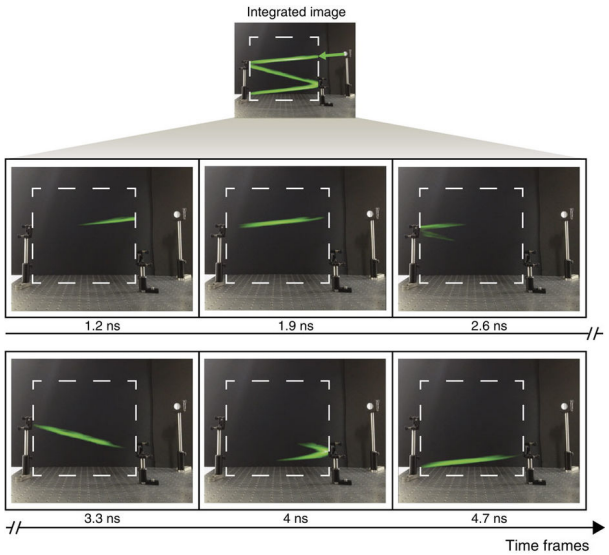
(a) ToF 3D sensor[6]



(b) scintillation detectors [9]



(c) Time-corelated single photon counting for FLIM and RS [11, 16].



(d) Ultra-fast imaging [18].

Figure 1.1 Applications based on single photon detectors.

can satisfy all the requirements including ultra-high sensitivity, fine time resolution, high spatial resolution, low power supply and low cost. CMOS SPAD imagers have been developed recently, and show promising results in the applications mentioned above.

1.2 Research Objectives and Thesis Organization

This thesis focuses on the design of a SPAD in the standard CMOS process, and the design of SPAD imagers. The basic principle and key parameters of a SPAD are introduced in Chapter 2. Then, structures and experimental results about the designed several types of SPADs are presented in Chapter 3. From Chapter 4 to Chapter 5, a new sensor architecture with high readout efficient and 3 SPAD imagers utilizing the proposed architecture are shown. In Chapter 6, a SPAD imager with real-time event discriminator is introduced.

Chapter 2 provides an introduction about basic principles and features of SPAD in order to understand the required constraints in designing CMOS SPAD. The breakdown voltage, dark counts rate (DCR) , and photon detection efficiency (PDE) are introduced. According to the introduction, the breakdown voltage of a SPAD should be greater than 15 V in order to suppress the influence of band to band tunneling, and s suitable guard ring is necessary for preventing premature breakdown due to edge effect. Furthermore, an analysis on the influence of DCR and PDE is introduce, and the desirable DCR for the SPAD imager is about 10 kHz.

Chapter 3 focuses on designing and testing about SPADs fabricated by the available standard CMOS process. The detail about the design of SPADs used for the SPAD imagers in this work are presented in this chapter. The structures of three types of CMOS SPADs are reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process in order to find a suitable structure of SPADs are introduced. According to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V. A suitable SPAD of Pwell/DeepNwell with PolyGate around the active region, low DCR with purely avalanche breakdown, and planer breakdown region were confirmed by the experimental results. Then,

a test circuit for after-pulsing probability measurement is presented. The experimental results demonstrates the efficiency of hold-off time about reducing the influence of after-pulsing, and the after-pulsing probability can be decreased to lower than 1% with a 20 ns hold-off time.

Chapter 4 targets on the efficient readout architecture for SPAD imagers. Since the breakdown SPAD pixels are sparse in many application, an architecture that only extracts the address of breakdown pixels can achieve a higher readout efficiency. A breakdown pixel extraction (BPE) readout architecture is proposed based on the binary feature of SPADs. The design and behavior of BPE architecture has been introduced at first, and the design of a 15×15 SPAD imager to verify the functionality of the proposed architecture is presented. Then, a detail design about the imager with 31×31 pixels utilizing background readout method is shown. This imager adds an additional 1-b memory in each pixel to store the value of the previous frame, and to realize the background readout. This method can minimized T_{dead} to 3 cycles under dark conditions or under sparse breakdown pixels. Furthermore, another BPE based 31×31 SPAD imager with event discriminator is proposed for minimizing T_{dead} and event detecting. This imager counts the value of $Max(_{BD,i})$ of each frames at first, and the readout procedure only starts when $Max(_{BD,i})$ became larger than a threshold value.

Chapter 5 presents the experimental results including the functionality, DCR distribution, PDE and dead time about the three designed imagers in Chapter 4. For the first designed sensor with 15×15 SPAD array, the functionality of BPE readout method is experimentally demonstrated firstly. Then, the DCR distribution is measured, and the median value, mean value, are 10 kHz, 20 kHz, respectively. Based on the measured DCR, an analysis about the temporal aperture ratio (TAR) is show. For the second imager that contains 31×31 SPAD array with background readout method based on BPE architecture, the ability of random event detection has been shown by pulsed laser imaging at first. Then, measurements about the DCR distributions of the images with different SPAD sizes are presented. Furthermore, an analysis about the requirements that can minimize T_{dead} is presented, and TAR as function of T_{win} has been shown comparing with the first imager. A 40% improvement of TAR is shown based on the calculated results. Finally, Photon detection efficiency of designed SPAD is measured. For the third imager that employs an event discriminator based on BPE architec-

ture, the functionality of this sensor is measured using the same method as the previous one. Then, an analysis about the setting of threshold value is shown.

Chapter 6 shows the design a 32×32 SPAD imager with the real time current logic event discriminator together with the experimental results. This imager employs a current logic to monitor the number of breakdown pixels in real time, and a free-running with variable hold-off time active quenching circuit is proposed to achieve zero T_{dead}. The ability of random event distinction is shown through the experimental results.

Finally, Chapter 7 gives conclusions of this thesis.

Chapter 2

Principles and features of SPAD

This chapter aims to provide an introduction about basic principle of SPAD in order to understand the required constraints in designing CMOS SPAD. Several key parameters of SPAD including the breakdown voltage, dark counts rate (DCR) , and photon detection efficiency (PDE) are introduced. Then, an analysis on the influence of DCR and PDE is shown, and the desirable characteristics of a SPAD are presented.

2.1 Basic Principle of SPAD

Single photon avalanche diode (SPAD) is a PN diode which is reversely biased above the breakdown voltage (V_{BD}), and usually equipped with a quenching circuit as shown in Fig. 2.1(a) [23, 24]. Under this condition, if there is no carrier in depletion region, the SPAD remains in a stable state and only a extremely small current is flowing through the SPAD as shown in Fig. 2.1(1).

Once there is a primary carrier being triggered by incident photons or some other noise sources [25], the depletion region's electric field is so high that the energy of accelerated carrier is large enough to generate additional carriers by impact ionization avalanche [26, 27]. The newly generated carriers can cause more carriers so that the avalanche breakdown procedure is triggered and a large current flows through the quenching resistor R_Q. At the same time, the cathode's voltage falls down below V_{BD} immediately to quench the avalanche breakdown procedure as shown in Fig. 2.1(3). Then, the SPAD is recharged to its over-bias voltage (V_{EX}) and returns to the stable state.

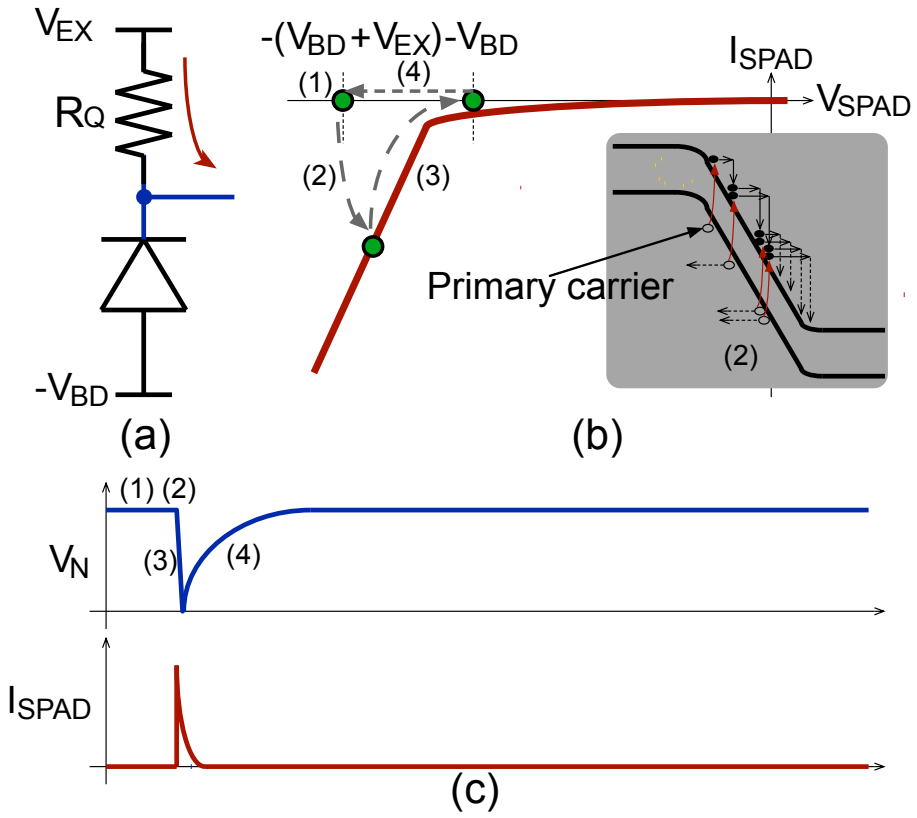


Figure 2.1 Operation procedure of SPAD: (a) SPAD with passive quenching circuit; (b) SPAD I-V characteristics; (c) SPAD output waveform.

As a result, the SPAD generates an easily measurable sharp pulse when breakdown happens, and even a single incident photon may trigger the avalanche breakdown immediately. Therefore, SPAD is capable of capturing incident photons that are generated closely in time, and is a photon detector with ultra-high sensitivity and fine time resolution.

Furthermore, SPADs was firstly fabricated by a standard CMOS process in 2003[28], which opened the way to SPAD arrays with low fabrication cost and the integration of on-chip signal processing circuits for high functional imaging systems. As a results, SPAD becomes a potential candidate for replacing PMT and EM-CCD in applications such as time-of-flight (ToF) 3D sensors [1, 2, 3, 4, 5, 6], scintillation detectors [7, 8, 9, 10], fluorescence lifetime imaging microscopy (FLIM) [11, 12, 13, 14], Raman spectroscopy (RS) [15, 16, 17], ultra-fast imaging [18, 19, 20], etc.

2.1.1 Breakdown Voltage

The breakdown voltage of a SPAD is determined by its structure and doping profile of the PN diode, and there are mainly two kinds of breakdown mechanisms: avalanche breakdown and tunneling breakdown [26].

Avalanche breakdown

When the reversely biased voltage is so large that the electric field in depletion region is higher than a threshold value, the carriers can gain enough energy to excite electron-hole pairs by impact ionization. The number of electron-hole pairs excited by a carrier traveled in a certain distance is α, which is called as ionization rate and is strongly dependent on the electric field [29, 30]. Assuming that the electronic current at the beginning of the depletion region is I_{n0}, this current at position $x = W$ is multiplied to $I_n(W) = M_n I_{n0}$ by the impact ionization, where M_n is multiplication factor. For the hole current I_p, it reaches its largest value at $x = 0$. Therefore, the incremental electronic current value at position x is:

$$dI_n(x) = I_n(x)\alpha_n dx + I_p(x)\alpha_p dx \tag{2.1}$$

And the total current I is constant, which is:

$$I = I_n(x) + I_p(x) \tag{2.2}$$

So that,

$$\frac{dI_n(x)}{dx} + (\alpha_p - \alpha_n)I_n(x) = \alpha_p I \tag{2.3}$$

On the condition that $\alpha_n = \alpha_p = \alpha$,

$$I_n(W) - I_n(0) = I\int_0^W \alpha dx \tag{2.4}$$

Since that $I_n(W) = M_n I_{n0} \approx I$, and $I_n(0) = I_{n0}$,

$$1 - \frac{1}{M_n} = \int_0^W \alpha dx \tag{2.5}$$

The avalanche breakdown voltage is defined as the voltage that M_n becomes infinity, where,

$$1 = \int_0^W \alpha dx \tag{2.6}$$

Since the value of α is strongly dependent to the electric filed, the avalanche breakdown happens when the electric field is higher than a threshold value, this electric field is also called as critical field (E_{max}). The value of critical field for silicon is about the order of 10^5 [V/cm]. Therefore, the avalanche breakdown voltage is mainly determined by the impurity concentration as shown in Fig. 2.2 [26]. For one-sided abrupt junctions,

$$V_{BD} = \frac{\epsilon_{si} E_{max}^2}{2qN} \tag{2.7}$$

Where N is the doping density of the lightly doped side.

An approximate universal expression can be given as follows [26]:

for abrupt junctions,

$$V_{BD} = 60(\frac{E_g}{1.1\text{eV}})^{3/2}(\frac{N}{10^{16}\text{cm}^{-3}})^{-3/4} \tag{2.8}$$

for linearly graded junctions,

$$V_{BD} = 60(\frac{E_g}{1.1\text{eV}})^{6/5}(\frac{a}{3\times 10^{20}\text{cm}^{-4}})^{-2/5} \tag{2.9}$$

where a is the impurity gradient.

The temperature coefficient of breakdown voltage β is given by:

$$V_{BD} = V_{BD_0}(1 + \beta(T - T_0)) \tag{2.10}$$

where, T_0 is room temperature, and V_{BD_0} is the breakdown voltage at room temperature. When temperature becomes higher, the α value is reduced because the influence of scattering when carriers passing through the depletion region. Therefore, for the purely avalanche breakdown, β is positive and usually larger than $7 \times 10^{-4}\ ^\circ\text{C}^{-1}$ [31].

Tunneling breakdown

For the PN diode that is heavily doped, the electric field in depletion may approach 10^6 [V/cm], which is 10 times higher than the critical field. At this condition, band-to-band tunneling happens and significant current starts to flow[32, 33]. This phenomenon is called as the tunneling breakdown or the Zener breakdown. For diodes that V_{BD} is lower than 3 V, all the

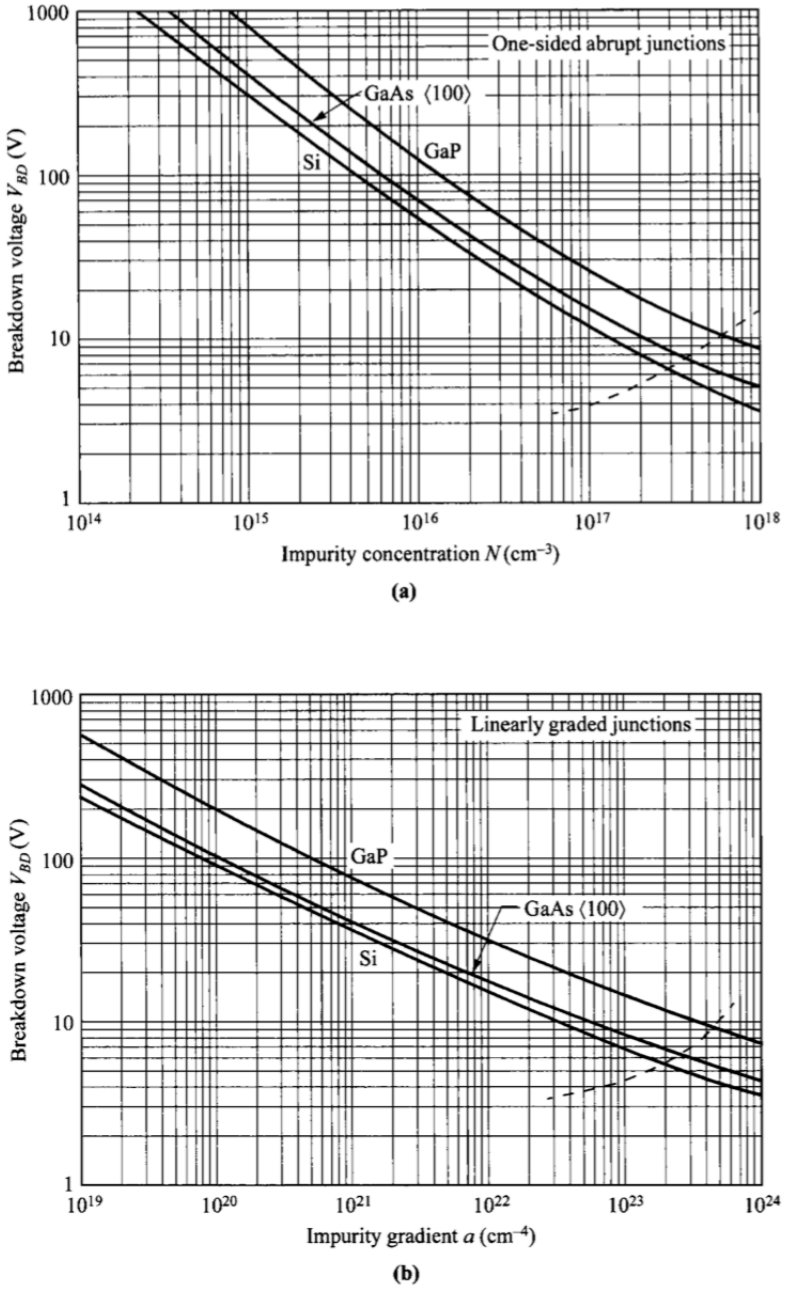


Figure 2.2 Avalanche breakdown voltage in Si, ¡100¿-oriented GaAs, and GaP, for (a) one-sided abrupt junctions (vs. impurity concentration) and (b) linearly graded junctions (vs. impurity gradient).

breakdowns are caused by Zener effect, between 3 V and 14 V both breakdown mechanisms occurs simultaneously, and for diodes that V_{BD} is higher than 15 V, only avalanche breakdown

happens [34, 31].

For the reason that the band-gap energy decreases with temperature increasing, β is negative for the purely tunneling breakdown. β increases with increasing of V_{BD}, and reaches 0 at about 6 V. Thus, β is smaller than diodes $7 \times 10^{-4}\,^{\circ}C^{-1}$ if the diode contains both two kinds of breakdown mechanisms [31].

Since the tunneling breakdown is unrelated to incident photons, and breakdowns triggered by Zener effect are noise for SPADs. Therefore, this kind of breakdown mechanism is not desirable for SPADs and should be prevented.

Edge effects

In order to detect incident photons, a planar avalanche breakdown region is desirable, however, the junction curvature effect at the perimeter can not be ignored [35]. At the perimeter, the depletion region is narrower and the electric field is higher, so that V_{BD} turns to be lower can cause premature breakdown or even tunneling breakdown. Therefore, guard rings are usually necessary for SPADs.

2.1.2 Dark Count Rate

Besides incident photons, the breakdown can also be triggered by the other sources. The generation mechanisms are [25, 36]:

(a) Direct thermal generation and diffusion.

(b) Direct band-to-band thermal generation.

(c) Trap assisted thermal generation.

(d) Trap assisted tunneling generation.

(e) Band-to-band tunneling generation.

as shown in Fig. 2.3. This kind of non-photon triggered breakdown is called as dark count, and the number of dark counts happens in one second is dark count rate (DCR).

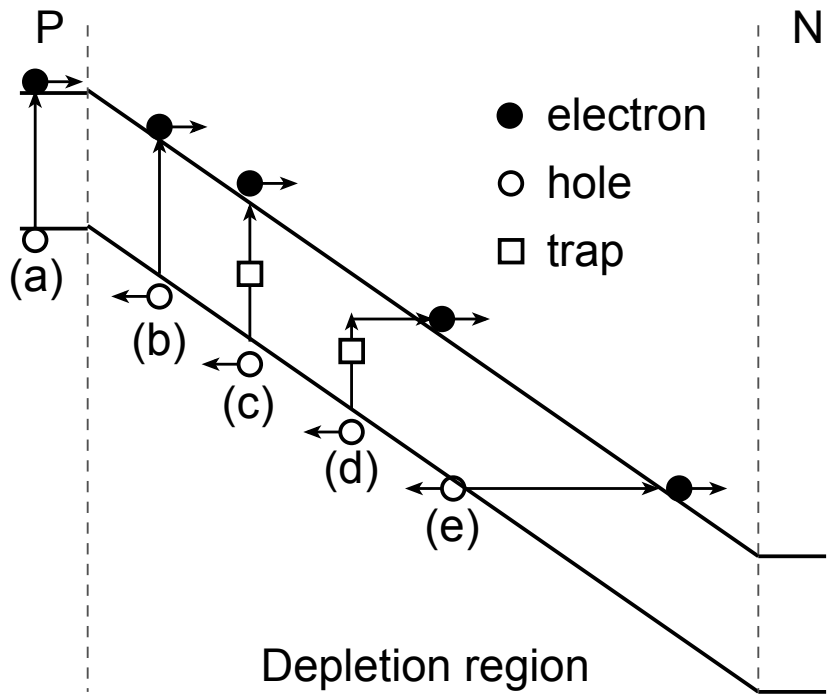


Figure 2.3 Sources of dark counts in a SPAD device.

The probability of dark counts (P_dc) occurrence is determined by the number of dark carriers generated by the sources mentioned previously (N_d), and the probability of triggering the avalanche breakdown by each carrier ($P_a(V_{ex})$) [37]. This probability follows the Poisson statistics:

$$P_{dc} = 1 - e^{-N_d P_a(V_{ex})} \tag{2.11}$$

The value of P_a is related with the electric profile and the electron-hole ionization rate, in other words, is determined by the over-bias voltage (V_{ex}) [38, 39].

$$P_a = 1 - e^{-V_{ex}/V_c} \tag{2.12}$$

where V_c is a normalizing coefficient on the order of E_{gap}/q. Since P_a is also related with the photon detection efficiency of a SPAD, the work about designing low DCR CMOS SPAD mainly focuses on the reduction of dark carriers generation.

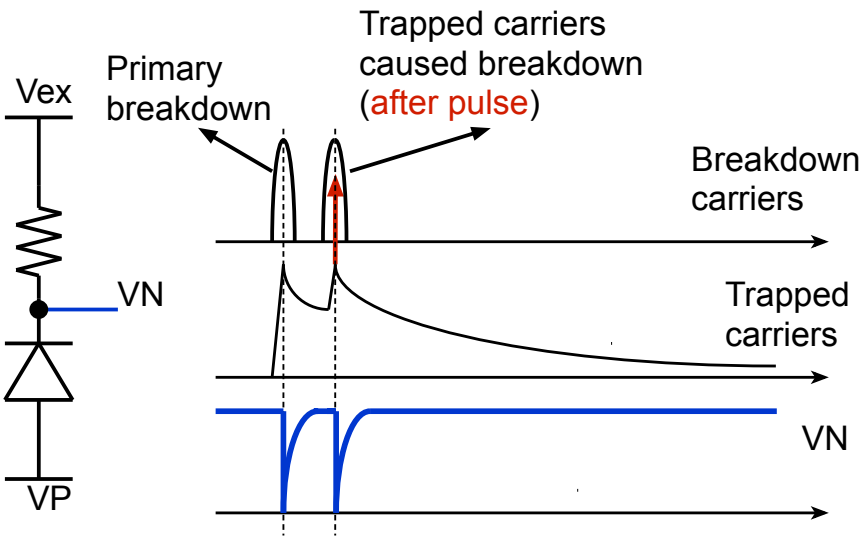


Figure 2.4 Principle of after-pulsing.

After-pulsing

During a breakdown procedure, generated carriers may be trapped in deep levels, and the releasing of these trapped carriers may trigger the breakdown again as shown in Fig. 2.4. This kind of breakdown is also a dark count that is called as after-pulsing[40]. Different from the other kinds of dark counts, the influence of after-pulsing can be reduced by a peripheral circuit. Since the trapped carriers will be released after a period of time, the probability of after-pulsing (PAP) can be reduced by setting a hold-off time as shown in Fig. 2.5 [41, 42].

2.1.3 Photon Detection Efficiency

Photon detection efficiency (PDE) is defined as the breakdown probability when a single photon flies into a SPAD, and this probability is determined by the quantum efficiency $\eta(\lambda)$ and P_a [38]. $\eta(\lambda)$ is the absorption efficiency for incident photons with λ wavelength [22],

$$\eta(\lambda) = (1 - R)e^{-\alpha(\lambda)D}(1 - e^{-\alpha(\lambda)W}) \tag{2.13}$$

where α is the silicon absorption coefficient, W is the depletion region thickness, D is the junction depth, and R is the reflection coefficient for the interface. Therefore, the PDE is,

$$PDE(\lambda) = \eta(\lambda) \times P_a \tag{2.14}$$

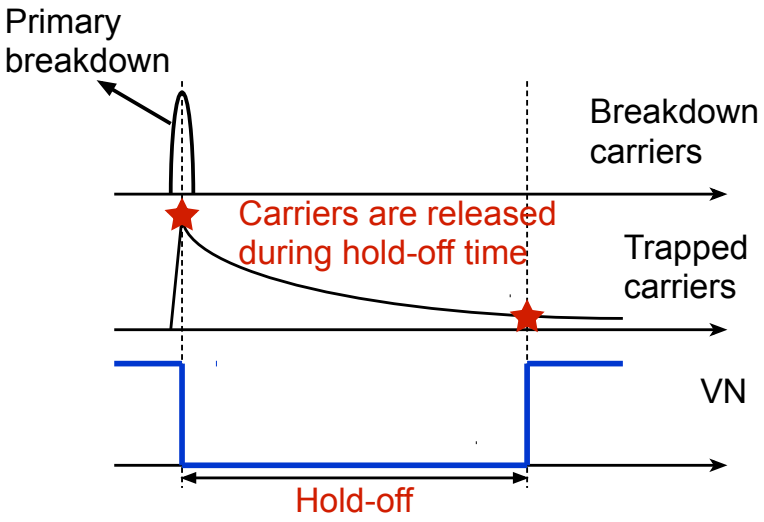


Figure 2.5 Reduction of PAP by setting a hold-off time.

Assuming that there are N_{ph} photons incident into a SPAD, the probability that light signal can be detected (P_{dect}) is:

$$P_{dect}(N_{ph}) = 1 - (1 - PDE)^{N_{ph}} \tag{2.15}$$

P_{dect} as a function of N_{ph} is depicted in Fig. 2.6, where PDE is assumed to be 10%, and 5% respectively.

For the pixel in SPAD imager, the number of incident photons is declined by $N_{ph} \times FF$, where FF is the fill factor of active region of a SPAD. Moreover, SPAD imager have dead time (T_{dead}) due to quenching, recharging, holding-off, and readout procedures, that can not detect incident photons during this period. Therefore, the number of actual incident photons is also reduced by the duty cycle of window time (T_{win}) in one frame, which is also called as temporal aperture ratio (TAR) [43].

$$TAR = \frac{T_{win}}{T_{win} + T_{dead}} \tag{2.16}$$

Assuming that the intensity of incident light is spatially uniform, and the number of incident photons per pixel per second is N_{ph}, For a SPAD sensor with N pixels, the probability that

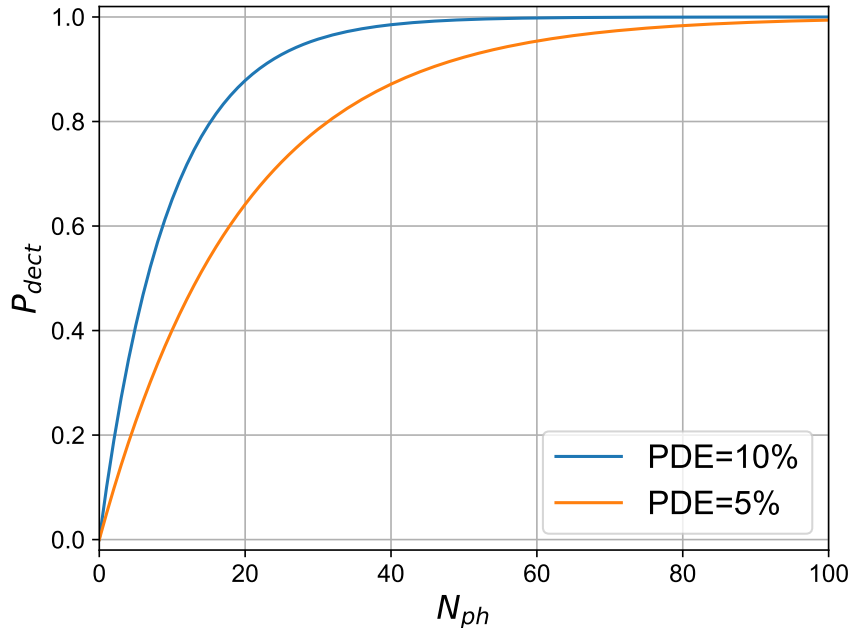


Figure 2.6 P_{dect} as a function of N_{ph}. Blue line: PDE=10%; Orange line: PDE=5%.

N_{dect} pixels are breakdown triggered by photons is,

$$P_{N_{dect}} = \binom{N}{N_{dect}} \times (1 - P_{dect})^{(N-N_{dect})} \times P_{dect}^{N_{dect}} \tag{2.17}$$

The excepted value of N_{dect} is,

$$E[N_{dect}] = N \times P_{dect} \tag{2.18}$$

and the variance is,

$$V[N_{dect}] = N \times P_{dect}(T_{win}) \times (1 - P_{dect}) \tag{2.19}$$

The probability that N_{dect} is larger than N_{th} ($P_{N_{dect}>N_{th}}$) is:

$$P_{N_{dect}>N_{th}}(T_{win}) = 1 - \sum_{k=0}^{Nth} P_{N_{dect}=k}(T_{win}) \tag{2.20}$$

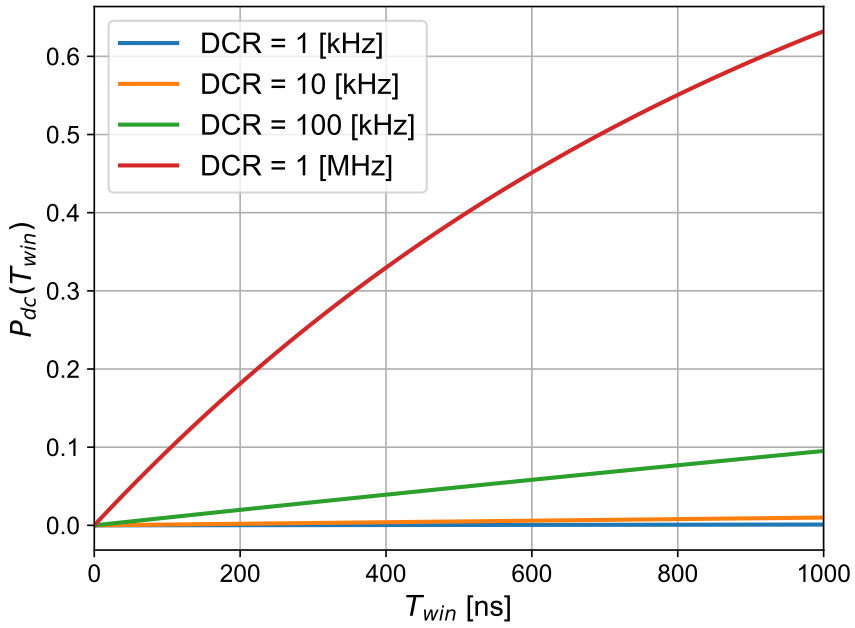


Figure 2.7 $P_{dc}(T_{win})$ as a function of T_{win} at different DCR values.

2.2 Influence of Dark counts

If the dark counts caused by after-pulsing can be ignored, the number of dark counts (k) per time unit (T) follows a Poisson distribution:

$$p(k,T) = \frac{\lambda(T)^k e^{-\lambda(T)}}{k!} \tag{2.21}$$

where p is the probability when the number of dark counts is k in a period of time T, and $\lambda(T)$ is the expected value of dark counts which equals to $T \times \mathrm{DCR}$. For a certain T_{win}, the probability that dark count happens ($P_{dc}(T_{win})$) during T_{win} is:

$$P_{dc}(T_{win}) = 1 - p(0,T_{win}) = 1 - e^{-\mathrm{DCR}\times T_{win}} \tag{2.22}$$

Fig. 2.7 plots the calculated P_{dc} as a function of T_{win} at different DCR values. At the condition that the value of $T_{win} \times DCR$ is very small, P_{dc} is almost linear with T_{win}.

For a SPADs array sensor contains N pixels, the probability that there are N_{dc} pixels having breakdown during T_{win} is:

$$P_{N_{dc}}(T_{win}) = \binom{N}{N_{dc}} \times (1 - P_{dc}(T_{win}))^{(N-N_{dc})} \times P_{dc}(T_{win})^{N_{dc}} \tag{2.23}$$

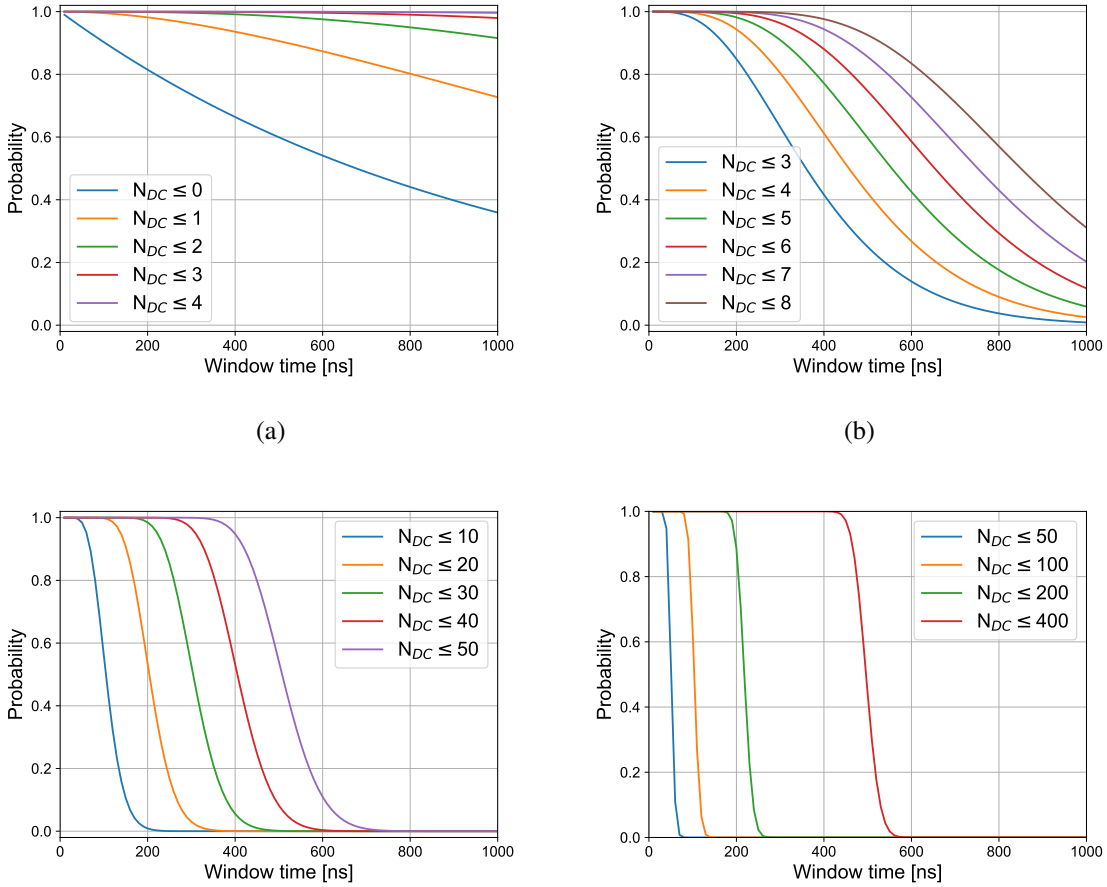


Figure 2.8 $P_{N_{dc} \leq N_{th}}$ as a function of T_{win} at different DCR values: (a) DCR=1 [kHz]; (b) DCR=10 [kHz]; (c) DCR=100 [kHz]; (d) DCR=1 [MHz].

and the excepted value of N_{dc} is:

$$E[N_{dc}(T_{win})] = N \times (1 - e^{-DCR \times T_{win}}) \tag{2.24}$$

variance is:

$$V[N_{dc}(T_{win})] = N \times (1 - e^{-DCR \times T_{win}}) \times (e^{-DCR \times T_{win}}) \tag{2.25}$$

The probability that N_{dc} is not larger than N_{th} ($P_{N_{dc} \leq N_{th}}(T_{win})$) is:

$$P_{N_{dc} \leq N_{th}}(T_{win}) = \sum_{k=0}^{N_{th}} P_{N_{dc}=k}(T_{win}) \tag{2.26}$$

This probability expresses the noise level of a SPAD imager and can be utilized for calculating the influence of DCR for different sensors at different T_{win}. Fig. 2.8(a)-(d) show plots of

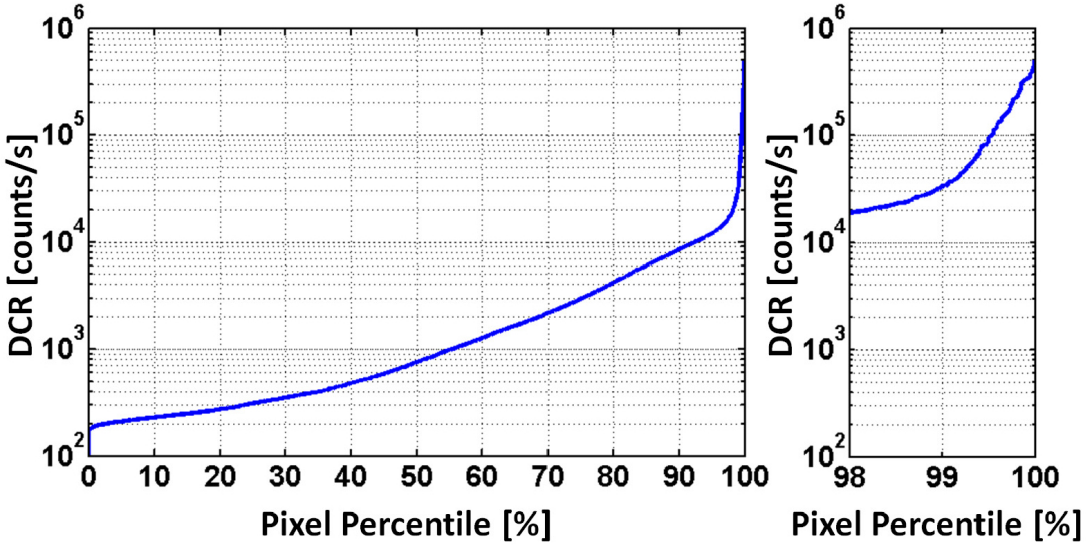


Figure 2.9 An example of DCR variation.

$P_{N_{dc} \leq N_{th}}(T_{win})$ in a 32×32 pixels SPAD imager with different DCR values.

2.2.1 Concerning with process variations

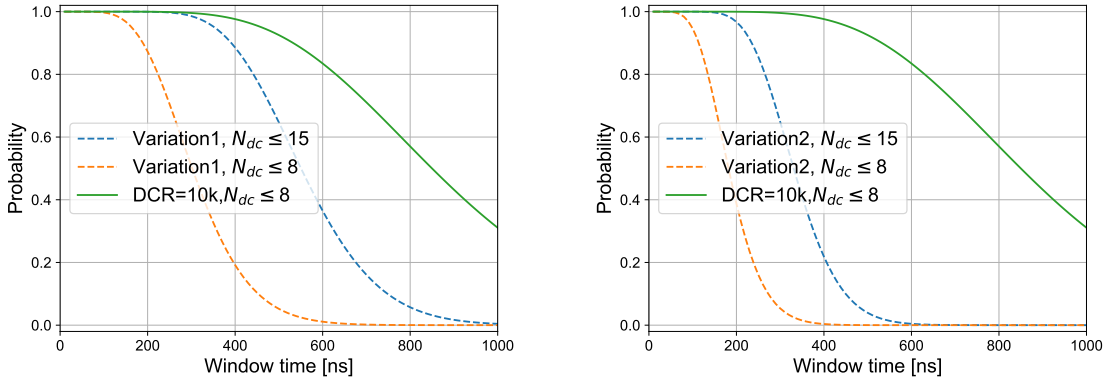
SPAD imagers typically have a DCR distribution that a small fraction of pixels (from 5% to 20% or higher) with very high DCR as shown in Fig. 2.9 [44], and this small proportion high DCR SPADs are influnced by traps [45].

Assuming that the N pixels SPAD array contains N_1 pixels of which DCR values are DCR_1, N_2 pixels with DCR_2, ..., N_n pixels with DCR_n, and

$$N = N_1 + N_2 + ... + N_n \tag{2.27}$$

The probability that $N_{dc,k}$ pixels are breakdown among the N_k pixels with DCR_k ($P_{N_{dc,k}}$) is:

$$P_{N_{dc,k}}(T_{win}) = \binom{N_k}{N_{dc,k}} \times (1 - P_{dc,k}(T_{win}))^{(N_k - N_{dc,k})} \times P_{dc,k}(T_{win})^{N_{dc,k}} \tag{2.28}$$



(a) (b)

Figure 2.10 Comparison on the influences of DCR with different variations: (a) 900 pixels with DCR=10kHz, 100 pixels with DCR=100kHz, and 24 pixels with DCR=1MHz; (b) 800 pixels with DCR=10kHz, 200 pixels with DCR=100kHz, and 24 pixels with DCR=1MHz.

where $k = 1, ..., n$, and $P_{dc,k}(T_{win})$ is

$$P_{dc,k}(T_{win}) = 1 - e^{-DCR_k \times T_{win}} \tag{2.29}$$

Therefore, the probability that N_{dc} pixels are breakdown for this $M \times N$ SPAD array is:

$$P_{N_{dc}}(T_{win}) = \sum_{k_1=0}^{N_{dc}} \sum_{k_2=0}^{N_{dc}-k_1} \cdots \sum_{k_n-1=0}^{N_{dc}-k_1-k_2-\ldots k_{n-2}} (P_{N_{dc,1}=k_1} P_{N_{dc,2}=k_2} \ldots P_{N_{dc,n-1}=k_{n-1}} P_{N_{dc,n}=N_{dc}-\sum_{i=1}^{n-1} k_i}) \tag{2.30}$$

Fig. 2.10 shows a comparison on the influences of DCR with different variations.

2.3 Signal and Noise

2.3.1 Comparing on the breakdown probability

For a SPAD, in order to detect the incident photons, the probability of detecting true incident photons should be larger than the probability of triggering breakdown by dark counts.

$$1 - (1 - PDE)^{N_{ph}} > 1 - e^{-DCR \times T_{win}} \tag{2.31}$$

Therefore,

$$DCR < -\frac{N_{ph} \log(1 - PDE)}{T_{win}} \tag{2.32}$$

Concerning with the influence of dark counts, the breakdown probability for a SPAD with N_{ph} incident photons (P_{bd}) is,

$$P_{bd} = P_{dect} + P_{dc} - P_{dect} \times P_{dc} \tag{2.33}$$

2.3.2 Comparing on the number of breakdown pixels

For SPAD imagers, the main application is single photon imaging and the sensor is used to count the number of incoming photons. Thus, the ratio of number of breakdown pixels caused by incident photons and dark counts is important. $P_{N_{dect}>N_{th}}$ and $P_{N_{dc}\leq N_{th}}$ give a guideline about determine the parameters of SPAD imagers both in designing and utilizing, such as DCR, PDE, T_{win}, etc.

For example, for a NaI(TI) scintillator, totally about 20,000 photons are generated by one scintillation event with $^{137}C_s$ (662 keV) [46]. Assuming that the number of pixels is 1024, the fill factor is about 10%, and PDE is 10%, so that the number of photons incident into a pixel for one event is,

$$N_{ph} = 20,000 \times \frac{1}{6 \times N_{Pixel}} \times FF \approx 0.325 \tag{2.34}$$

Therefore, the excepted number of breakdown pixels caused by incident photons is:

$$E[N_{dect}] = 1024 \times (1 - (1 - 0.1)^{0.325}) \approx 34.47 \tag{2.35}$$

and the excepted number of breakdown pixels caused by dark counts is:

$$E[N_{dc}] = 1024 \times (1 - e^{DCR \times T_{win}}) \tag{2.36}$$

Fig. 2.11 shows a plot about the comparison on $P_{N_{dect}>N_{th}}$ (the red line) and $P_{N_{dc}\leq N_{th}}$ (the blue and black line) with DCR=10kHz and 100kHz when T_{win} is 200 ns, respectively. This figure illustrates that N_{dect} is obviously larger than N_{dc} when DCR is 10 kHz, and N_{dc} is much larger than N_{dect}.

2.4 Summary

This chapter provided an introduction about basic principles and features of SPAD in order to understand the required constraints in designing CMOS SPAD. The breakdown voltage,

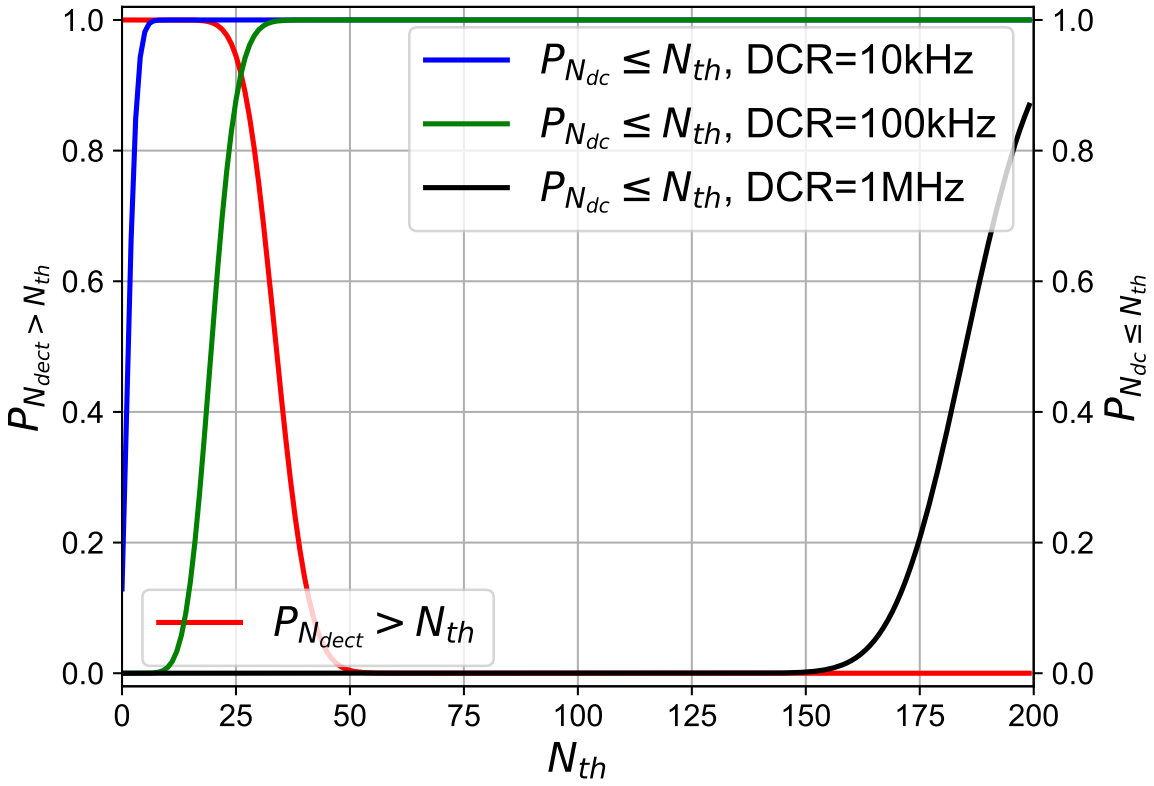


Figure 2.11 Comparison on $P_{N_{dect}>N_{th}}$ and $P_{N_{dc}\leq N_{th}}$ with different DCR values.

dark counts rate (DCR) , and photon detection efficiency (PDE) were introduced. According to the introduction, the breakdown voltage of a SPAD should be greater than 15 V in order to suppress the influence of band to band tunneling, and s suitable guard ring is necessary for preventing premature breakdown due to edge effect. Furthermore, an analysis on the influence of DCR and PDE has been shown, and the desirable DCR for the SPAD imager is about 10 kHz.

Chapter 3

CMOS SPAD Implementation

This chapter focuses on designing and testing about SAPDs that were fabricated by the available standard CMOS process. The details about the design of SPADs that are used for the SPAD imagers in this works are included in this chapter. The structures of three types of CMOS SPADs are reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process are introduced.

According to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V, and a suitable structure is founded according to the measurement results. Then, a test circuit for after-pulsing probability measurement is presented with the experimental results.

3.1 SPAD Design

Fig. 3.1 illustrates the cross-sections of designed SPADs [47, 48, 49] to find the structure of a SPAD with a planar breakdown region and low DCR. The layers used in this work are defined as follows:

- Pdiff and Nidff: drain/source layer of PMOS and NMOS;
- Pwell and Nwell: body of NMOS and PMOS;
- DeepNwell: isolation layer for the body of NMOS
- STI: shallow trench isolation

- PolyGate: Gate layer

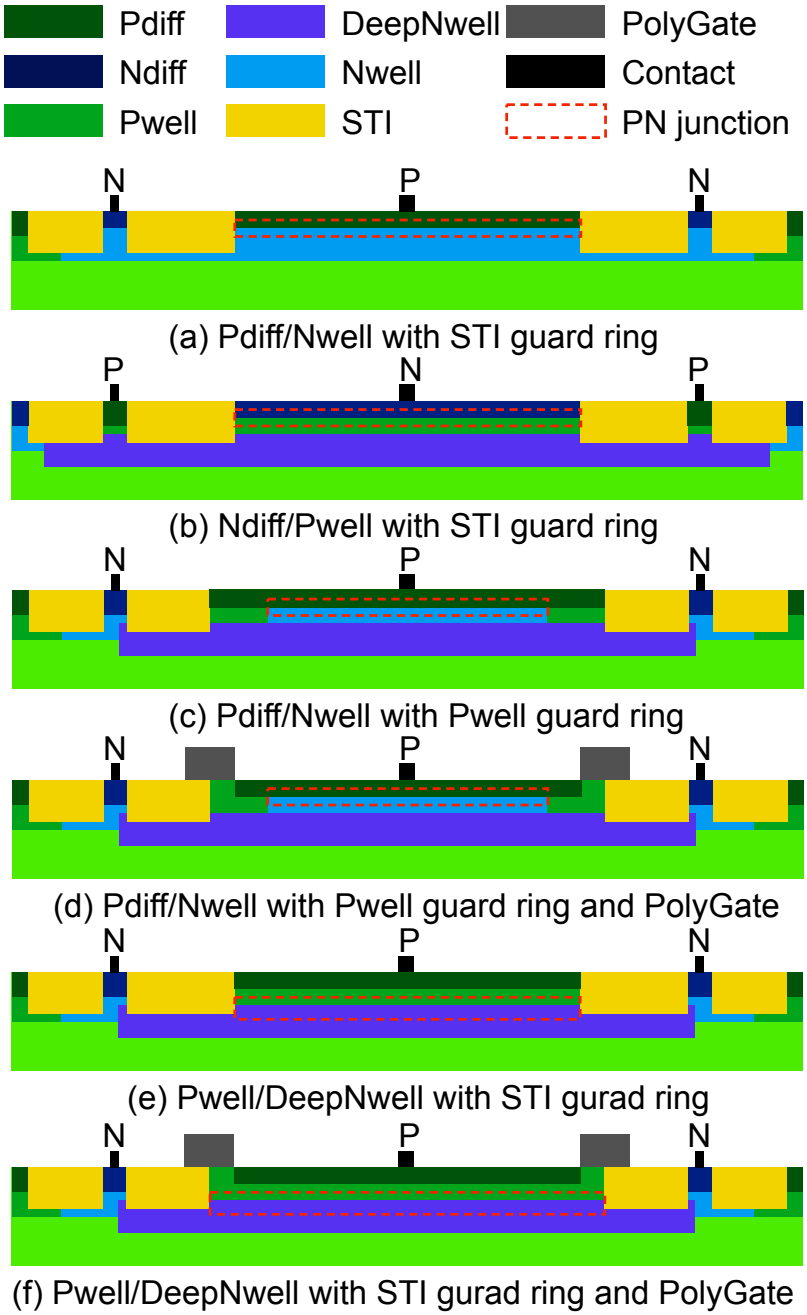


Figure 3.1 The structure of designed SPAD: (a) Pdiff/Nwell with STI guard ring; (b) Ndiff/Pwell with STI guard ring; (c) Pdiff/Nwell with Pwell guard ring; (d) Pdiff/Nwell with Pwell guard ring with PolyGate;(e) Pwell/DeepNwell with Pwell guard ring; (f) Pwell/DeepNwell with Pwell guard ring and PolyGate.

Totally 6 types of SPADs were designed and tested containing Pdiff/Nwell SPAD with STI guard ring (Fig. 3.1(a)), Ndiff/Pwell SPAD with STI guard ring (Fig. 3.1(b)), Pdiff/Nwell SPAD with Pwell guard ring (Fig. 3.1(c)), Pdiff/Nwell SPAD with Pwell guard ring with PolyGate (Fig. 3.1(d)),Pwell/DeepNwell SPAD with STI guard ring (Fig. 3.1(e)), and Pwell/DeepNwell SPAD with STI guard ring and PolyGate (Fig. 3.1(f)).

3.1.1 Pdiff/Nwell with STI guard ring and Ndiff/Pwell with STI guard ring

The shallow trench isolation process has been used to isolate the adjacent transistors in sub-micron CMOS technology [50]. Because of the SiO_2's 30 times higher electric strength, the STI process can be utilized as the guard rings to prevent the premature breakdown for CMOS SPADs [51, 52, 53]. The advantages of STI guard ring is high fill factor and fast response time [52], however, the DCR of these SPADs are very high due to traps located at the Si/SiO_2 interface as shown in table 3.1. The influence of traps can be suppressed by surrounding the STI with several passivation implant [53], however, the passivation process is only available in custom CMOS technology or CMOS image sensor (CIS) technology. For the SPADs designed this work, SPAD(a) has the same structure as [51], and SPAD(b) reverts the cathode and anode with Ndiff and Pwell, respectively.

3.1.2 Pdiff/Nwell with Pwell guard ring

Besides STI, the layer with lower doping concentration can also be utilized as guard rings to prevent premature breakdown [54, 55, 56, 57, 58, 59, 60, 61]. However, STI is still etched everywhere except the Pdiff and Ndiff area by default in almost all the CMOS processes, so that the influence of STI is still existence as shown in Fig. 3.1(c). In [56], a method to prevent the STI process around the active area by drawing a poly-silicon gate layer was proposed as shown in Fig. 3.1(d), and SPADs with the same structures were designed and fabricated in this work.

3.1.3 Pwell/DeepNwell SPAD

The SPADs that use Pdiff/Nwell or Ndiff/Pwell junction as the breakdown region have shown acceptable measurement results in some references, however, there are also some SPADs having very high DCR with the same structures in different processes such as the SPADs in [54]. This high DCR is caused by the high doping concentration of the process, the depletion region is thin with a very high electric field, and this assumption is proved by DCR temperature dependence measurement [53]. This high electric field in the narrow Pdiff/Nwell or Ndiff/Pwell depletion increases the probability band-to-band tunneling [62, 63]. Therefore, the Pdiff/Nwell or Ndiff/Pwell breakdown region should be modified to reduce the field strength, and the layers with lower doping density that can be utilized in CMOS process are the well layers such as Nwell, Pwell, and DeepNwell.

The P-/DeepNwell is used as the breakdown region in [62], P- implant is available in some CIS process to fulfill to role of STI passivation implant, and the STI around P- layer is the guard ring to prevent premature breakdown. In [63], the breakdown region is Pwell and DeepNwell, and an implant stop layer is used for stopping the implanting of either Nwell or Pwell around the breakdown region to make a 'No-well' layer with lower doping density as the guard ring. The same method in [56] was utilized to reduce the influence of STI interface, improved versions of SPADs in [62, 63] were introduced in [60].

Unfortunately, neither the No-well nor the P- layer is available in the process we can use in this work, and the same structure introduced above can not be implemented. On the other hand, the position of DeepNwell is reported to be very shallow, so that STI can be used as the guard ring around breakdown region as shown in Fig. 3.1(e) and (f). The difference between SPAD(e) and SPAD(f) is that there is a distance between Pdiff and STI in (e) by using the same method in [56].

3.2 SPAD Characterization

3.2.1 Breakdown voltage and DCR

Measurement results about the breakdown voltage and DCR of the designed SPADs are shown in table. 3.1 SPAD(a)-SPAD(e). V_{BD} is obtained by extrapolating the linear I-V curve measured above V_{BD} backwards to find its intercept with the voltage axis [39]. DCR is obtained by counting the pulse rate of a passive quenching circuit as shown in Fig. 2.1.

Pdiff/Nwell and Ndiff/Pwell SPAD

For the SPADs using Pdiff/Nwell or Ndiff/Pwell breakdown region, the breakdown voltage is about 8.0 V, which is lower than all the other SPADs reviewed before as shown in table. These SPADs also have very high DCR, and this high value is assumed to be caused by the band-to-band tunneling, and the measurements about the temperature coefficient in the next section proved this assumption. Therefore, these structures are not suitable for SPADs in this process.

Pwell/DeepNwell SPAD

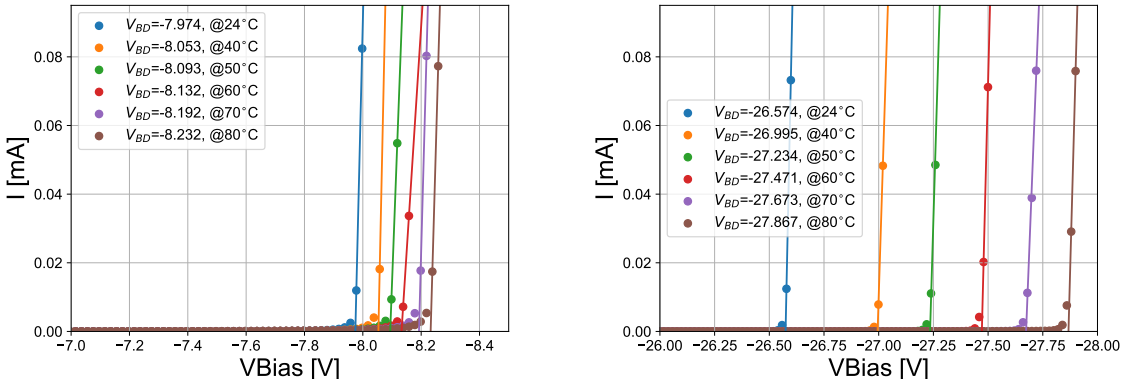
The breakdown voltage of SPADs using Pwell/DeepNwell junction is about 27 V, which is much larger than the Pdiff/Nwell SPADs. This high value also indicate that avalanche breakdown is the dominant kinds of breakdown, the measured I-V characteristics also proved this assumption. Moreover, leaving a distance between Pdiff and STI can reduce the DCR significantly as shown in the table. This low DCR make the SPAD(f) to be available in SPAD imagers, and all the imagers designed in this work were using the same structure with SPAD(f).

3.2.2 Temperature coefficient measurement

I-V characteristics of SPAD(a) and SPAD(f) were measured under different temperature to derive the temperature coefficient and breakdown mechanisms of these SPADs as show in

Table 3.1 SPAD parameters for several SPADs and the designed SPADs in this work

SPAD	Tech. Node [nm]	PN junction	Guard ring	$V_{BD}[V]$	DCR [Hz]@V_{ex}
[51]	180	Pdiff/Nwell	STI	11	N/A
[52]	180	Pdiff/Nwell	STI	11	$\approx 10^6$
[53]	CIS130	Pdiff/Nwell	STI	9.4	300k@1.8 V
[54](1)	90	Ndiff/Pwell	Nwell/Gate	10.4	>100k@0.2 V
[54](2)	65	Ndiff/Pwell	Nwell/Gate	9.5	>100k@0.2 V
[55]	350	Ndiff/Pwell	Nwell	12	10k@1 V
[56]	130	Pdiff/Nwell	Pwell/Gate	9.7	100k@1.7 V
[57]	130	Pdiff/Nwell	Pwell	12.3	231@V1.5 V
[58]	500	Pdiff/Nwell	Nwell/Gap	14.2	3k@0.6 V
[59]	150	Pdiff/Nwell	Nwell	18.2	40@V3 V
[60](3)	CIS130	Pdiff/Nwell	P-	12.4	47@0.8 V
[61](2)	150	Pdiff/Nwell	P-sub	16.1	100@3 V
[62]	CIS130	P-/DeepNwell	STI	12.4	100@1 V
[63]	CIS130	Pwell/DeepNwell	No-well	14.36	50@1 V
[60](1)	CIS130	Pwell/DeepNwell	No-well/Gate	14.36	25@ V
[60](2)	CIS130	P-/DeepNwell	No-well/Gate	17.9	40@ V
[61](1)	150	Pwell/DeepNwell	No-well	23.1	200@3 V
SPAD(a)	180	Pdiff/Nwell	STI	7.9	>1M@0.05 V
SPAD(b)	180	Ndiff/Pwell	STI	8.0	>1M@0.05 V
SPAD(c)	180	Pdiff/Nwell	Pwell	7.9	500k@0.05 V
SPAD(d)	180	Pdiff/Nwell	Pwell/Gate	7.9	1.5M@0.05 V
SPAD(e)	180	Pwell/DeepNwell	STI	27	5.4k@0.1 V 331k@0.3 V >1Mk@1.8 V
SPAD(f)	180	Pwell/DeepNwell	STI/Gate	27	<1k@0.3 V 7.3k@1 V 20.2k@1.8 V



(a) (b)

Figure 3.2 SPADs I-V characteristics: (a) P-diff/Nwell SPAD; (b) P-well/DeepNwell SPAD.

Fig 3.2. Temperature coefficient β is calculated from equation:

$$\beta = \frac{1}{V_{BD_0}} \times \frac{V_{BD} - V_{BD_0}}{T - T_0} \tag{3.1}$$

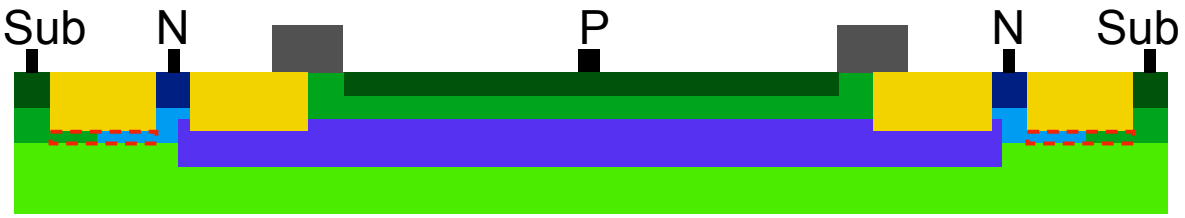
The calculated β of Pdiff/Nwell SPAD is 5.765×10^{-4}, which indicates the existence of band to band tunneling [31]. On the other hand, the β of Pwell/DeepNwell SPAD is 8.455×10^{-4}.

3.2.3 Breakdown region confirmation

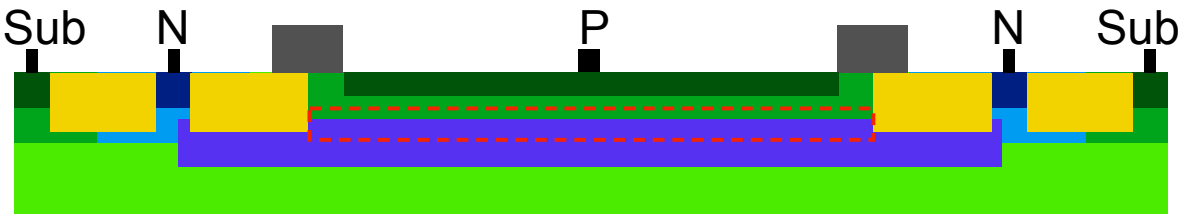
A series of I-V sweep measurements were conducted to confirm the breakdown region of Pwell/DeepNwell SPAD:

1. Connecting the Sub contact to the ground.
2. Applying a constant voltage 'VP' to the P contact.
3. Sweeping the 'VN' of N contact until breakdown.
4. Confirming the breakdown region by the current.
5. Changing the voltage of 'VP', and repeating the measurement.

Table. 3.2 shows the measurement results. When 'VP' is 0 V, breakdown occurs at the condition that 'VN' is 18 V, and the current is flowing through N contact and Sub contact as shown in Fig. 3.3(a),so that the breakdown region is assumed to be Pwell/Nwell. When



(a) Pwell/Nwell breakdown



(b) Pwell/DeepNwell breakdown

Figure 3.3 Confirmation of breakdown region (a) Nwell/Pwell breakdown; (b) Pwell/DeepNwell breakdown.

Table 3.2 Measurement results to confrim breakdown region.

VP	VN at breakdown	VN-VP at breakdown	Breakdown region
0	18	18	PwellNwell
-5	18	23	Pwell/Nwell
-10	17	27	Pwell/DeepNwell
-15	12	27	Pwell/DeepNwell
-20	7	27	Pwell/DeepNwell
-25	2	27	Pwell/DeepNwell

‘VP’ turns to be 5 V, breakdown still happens at the condition that ‘VN’ is 18 V indicating the same breakdown region. However, when ‘VP’ becomes lower than -10 V, the value of ‘VN’ start to change at breakdown, and ‘VN’-‘VP’ keeps to be 27 V, and the breakdown current is flowing through N contact to P contact. Therefore, the breakdown region of SPAD (e) and (f) is confirmed to be the Pwell/DeepNwell region.

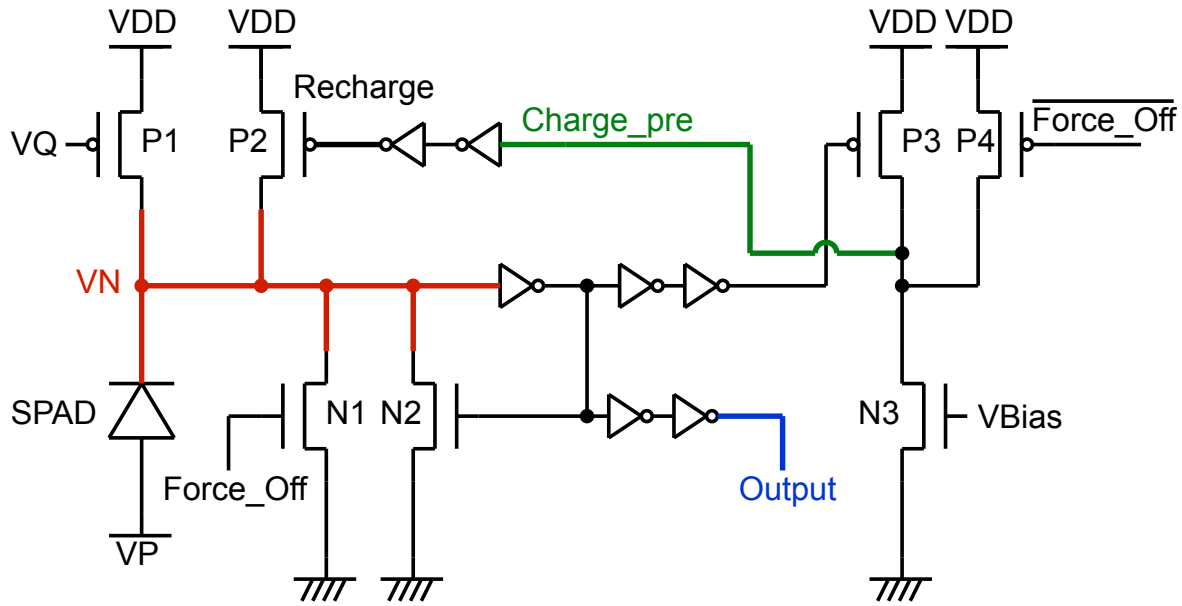


Figure 3.4 Schematic of variable hold-off time active quenching circuit.

3.3 After-pulsing probability measurement

The probability of after-pulsing can be reduced by setting a hold-off time [64], however, longer hold-off time also reduces the duty cycle of T_{win} that is very important in some applications.

3.3.1 Active quenching circuit with variable hold-off time

A variable hold-off time active quenching circuit (VHAQC) was designed to measure the relationship between hold-off time and after-pulsing probability. Fig. 3.4 illustrates the schematics of the VHAQC, and Fig. 3.5 shows the simulation waveforms of this circuit. The SPAD is connected with 4 transistors 'P1', 'P2', 'N1', and 'N2'. 'P1' is worked as the quenching resistor, the voltage of 'VQ' is kept to low, and the voltage of 'VP' is slightly above '-V_{BD}'.

When the SPAD is breakdown, current flows through 'P1', and 'VN' goes down. This low voltage turns on 'N2' to hold the SPAD 'OFF' by biasing the SPAD below the V_{BD}. Then, 'Output' rises up as well as 'P3' is turned off after a delay, so that 'Charge_pre' starts to fall down by the current flowing through 'N3'. The value of this current is controlled by

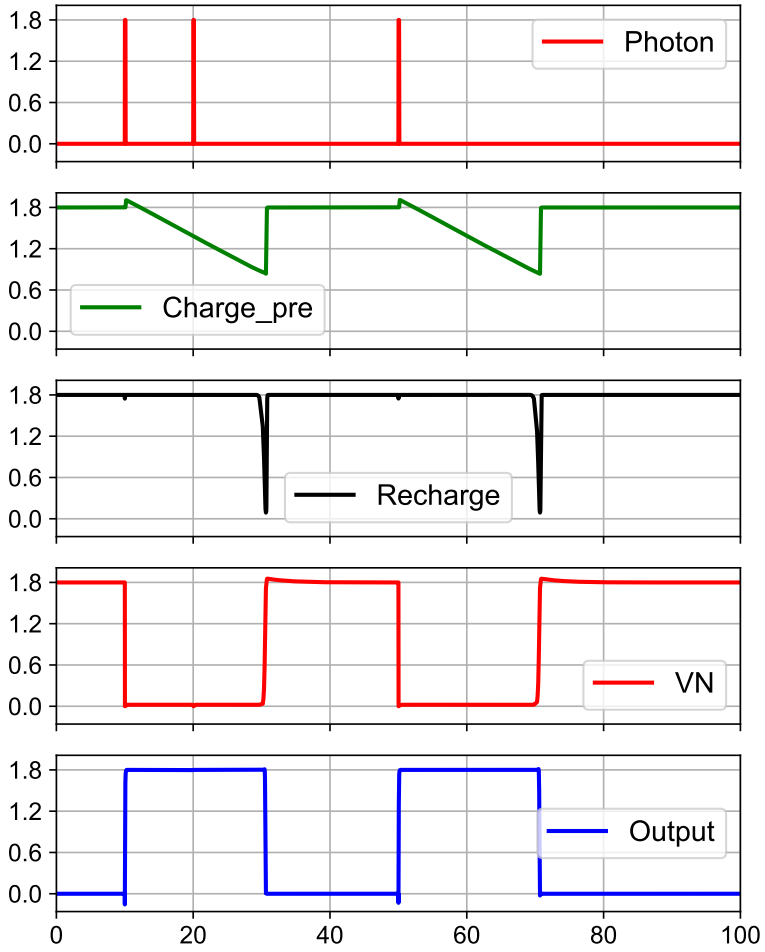


Figure 3.5 Simulation waveforms about VHAQC.

the external bias voltage 'VBias'. When 'Charge_pre' falls below the threshold value of the inverter, 'P2' is turned on to recharge the SPAD to its over-bias voltage. Therefore, the hold-off time is variable while changing the value of 'VBias'. 'N1' and 'P4' are added to force the SPAD 'OFF' in order to achieve a very long hold-off time by the 'Force_Off' signal.

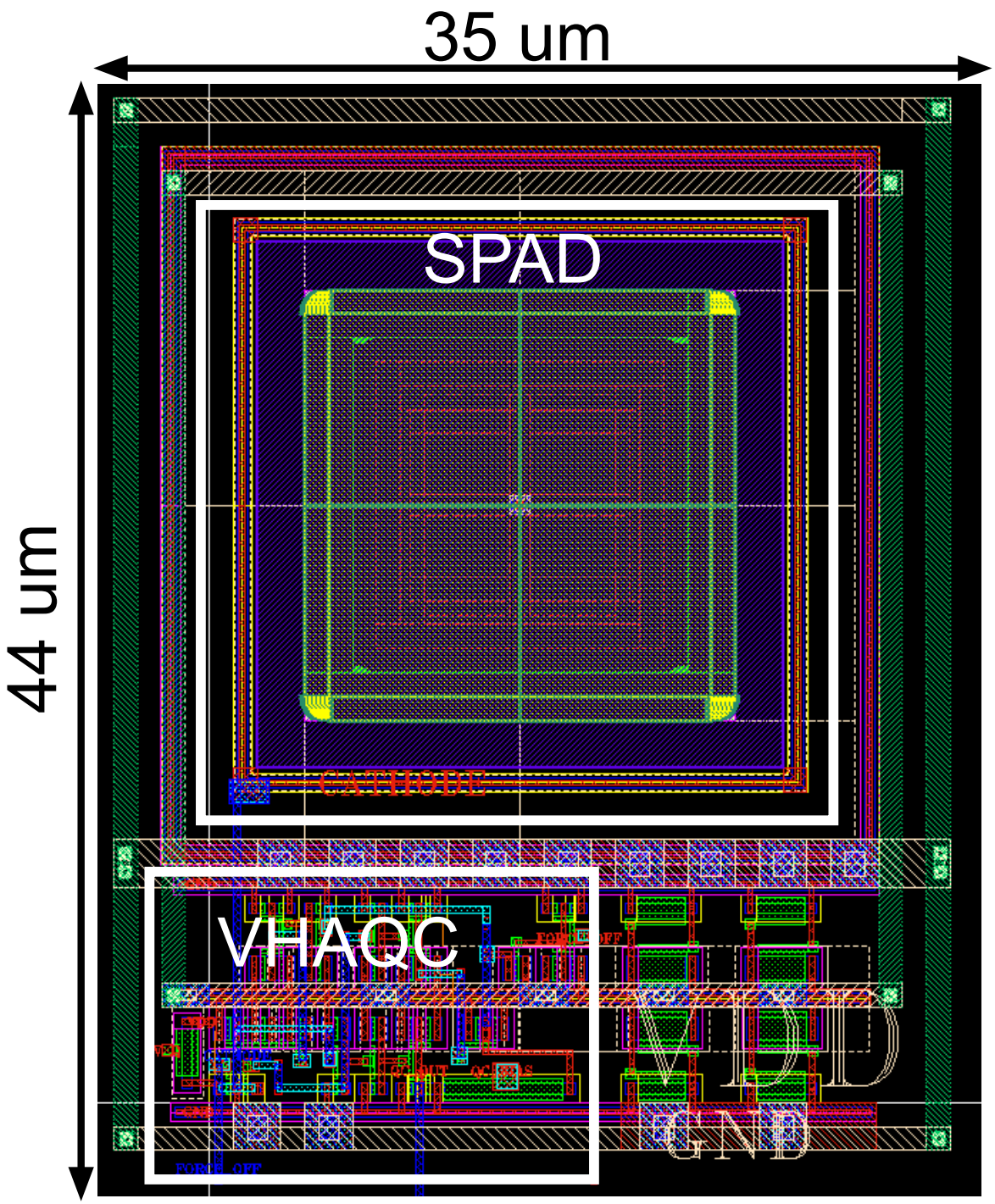


Figure 3.6 Relation between the Hold-off time and after-pulsing probability.

3.3.2 Measurement Results on the VHAQC

A test-of-concept chip about VHAQC was fabricated in the same process, and the layout of VHAQC is shown in Fig. 3.6. Fig. 3.7 illustrates a waveform captured by an oscilloscope

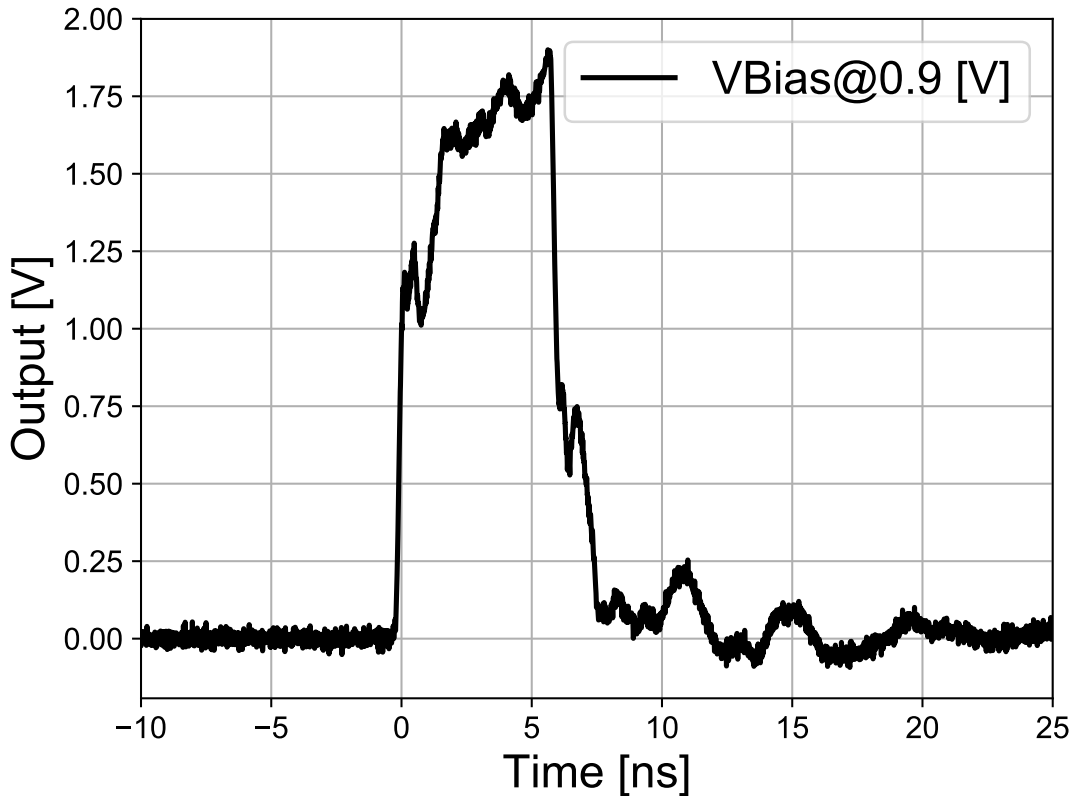


Figure 3.7 Captured output waveform when VBias is 0.9 V.

when VBias is 0.9 V, and the pulse width of this waveform represents the hold-off time. For each bias voltage, 100,000 waveforms were recorded to obtain the hold-off time at different VBias. The measured hold-off time with a function of VBias is plotted in Fig. 3.8.

The DCR and after-pulsing probability can be calculated through measuring the time interval between the falling edge of the first pulse and the rising edge of its next pulse as shown in Fig. 3.9. The time intervals were measured by a logic analyzer with 1 ns resolution. To prevent the breakdown triggered by incident photons, all the measurements were conducted in a black box, so that all the measured breakdowns are triggered by dark counts.

First of all, the time intervals distribution of 'real' dark counts were measured. In order to capture the dark counts free of after-pulsing, 1 ms hold-off time was set by the external input signal 'Force_Off'. The measurement was repeated 250,000 times to get the distribution of time intervals. Since the hold-off time is so long that the after-pulsing can be ignored, all the

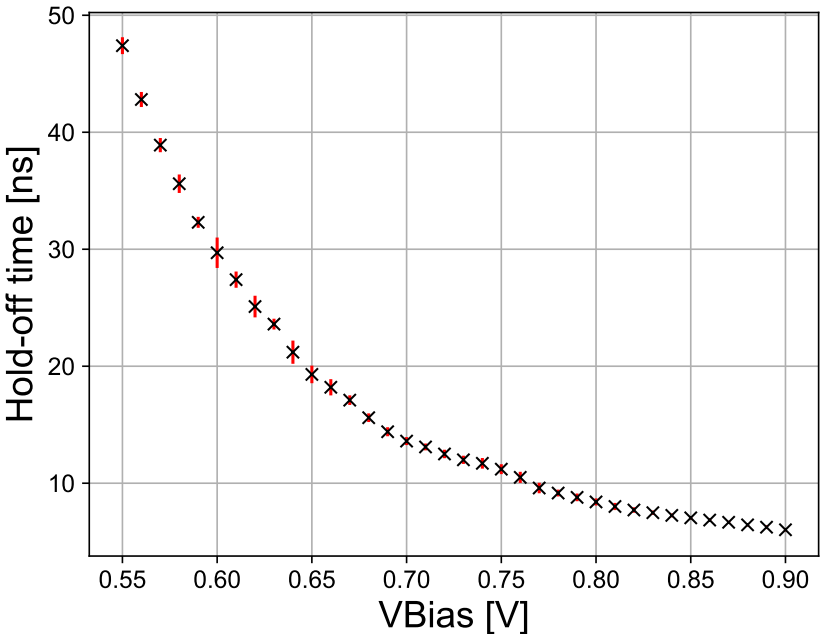


Figure 3.8 Hold-off time with a function of VBias.

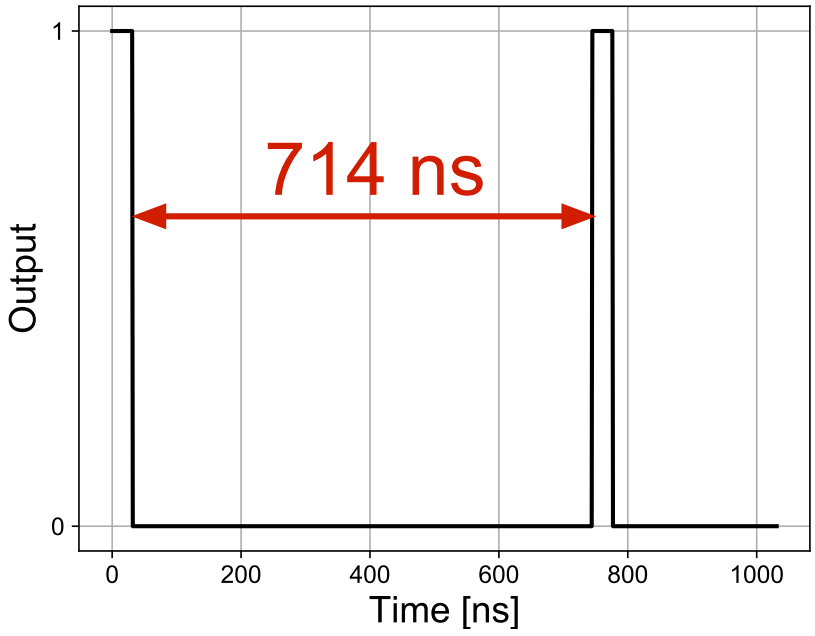


Figure 3.9 Captured waveform by logic analyzer to measure time intervals distribution.

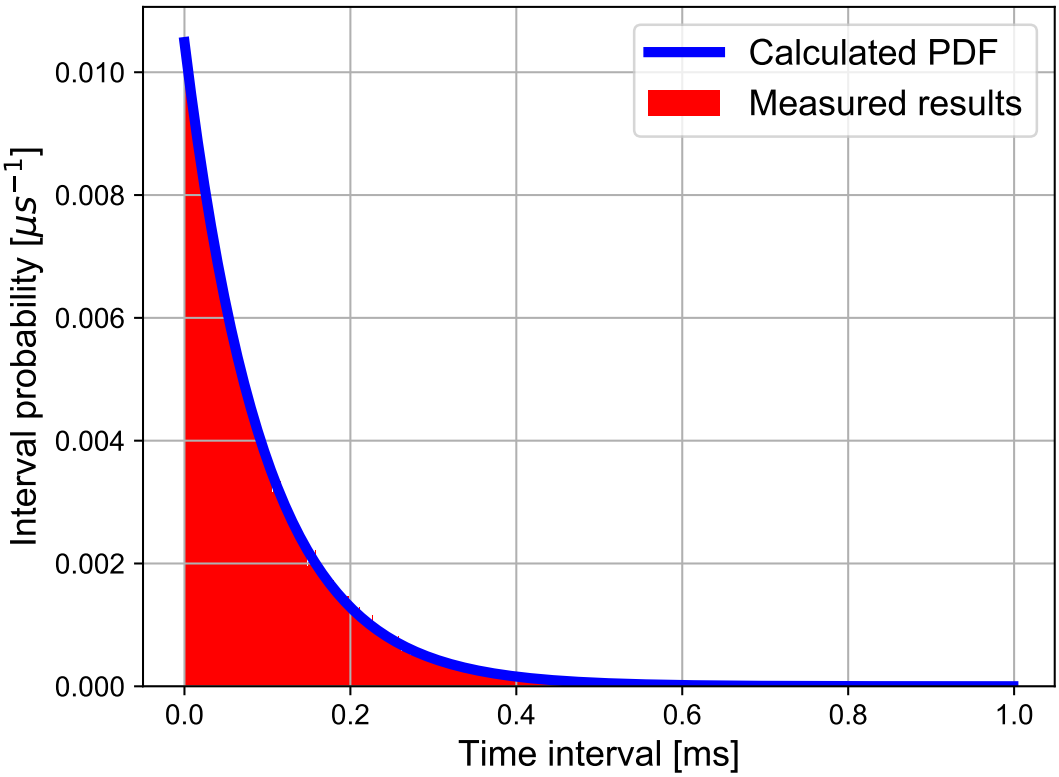


Figure 3.10 Exponential PDF and distribution of measured time intervals.

dark counts are caused by thermal noise or tunnel effects. Therefore, the dark counts occur independently, and the time intervals distribution should follow a exponential distribution.

The mean value of measured intervals ($E[X]$) is 9.532×10^4 ns, the measured variance ($V[X]$) is 8.986×10^9, the measured standard deviation 9.480×10^4 ns, and the measured median ($m[X]$) is 6.636×10^4 ns. These measured values also fit the characteristics of exponential distribution:

$$E[X] = \frac{1}{\lambda} \tag{3.2}$$

$$V[X] = \lambda^2 \tag{3.3}$$

$$m[X] = \frac{\ln(2)}{\lambda} \tag{3.4}$$

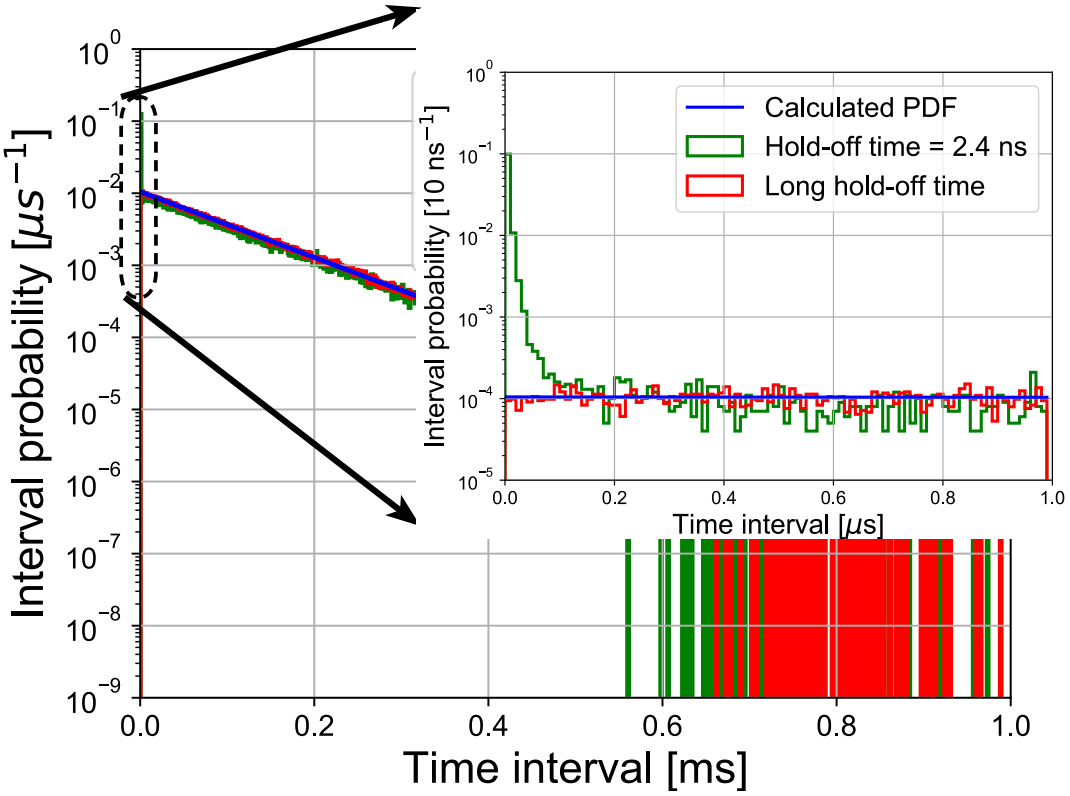


Figure 3.11 Time intervals distribution when hold-off time is 2.4 ns.

Base on the measurement results, the probability density function (PDF) is:

$$p(t) = \lambda e^{-\lambda t}, (\lambda = 1/E[X]) \tag{3.5}$$

The blue line in Fig. 3.10 shows the PDF based on Equation 3.5, and the red histogram represents the probability distribution of time intervals (interval probability) when the width of a single bin is 1 μs.

When hold-off time is very short, the dark counts triggered by after-pulsing can not be ignored. Therefore, the time intervals between two dark counts should also be different with equation 3.5.

Fig. 3.11 shows a comparison on the interval probability with different hold-off time. The green line illustrates the time intervals probability when hold-off time is set at 2.4 ns, and the red line is the distribution of dark counts without after-pulsing. The distributions are almost the same when the time interval is large, on the other hand, the green line's probability is

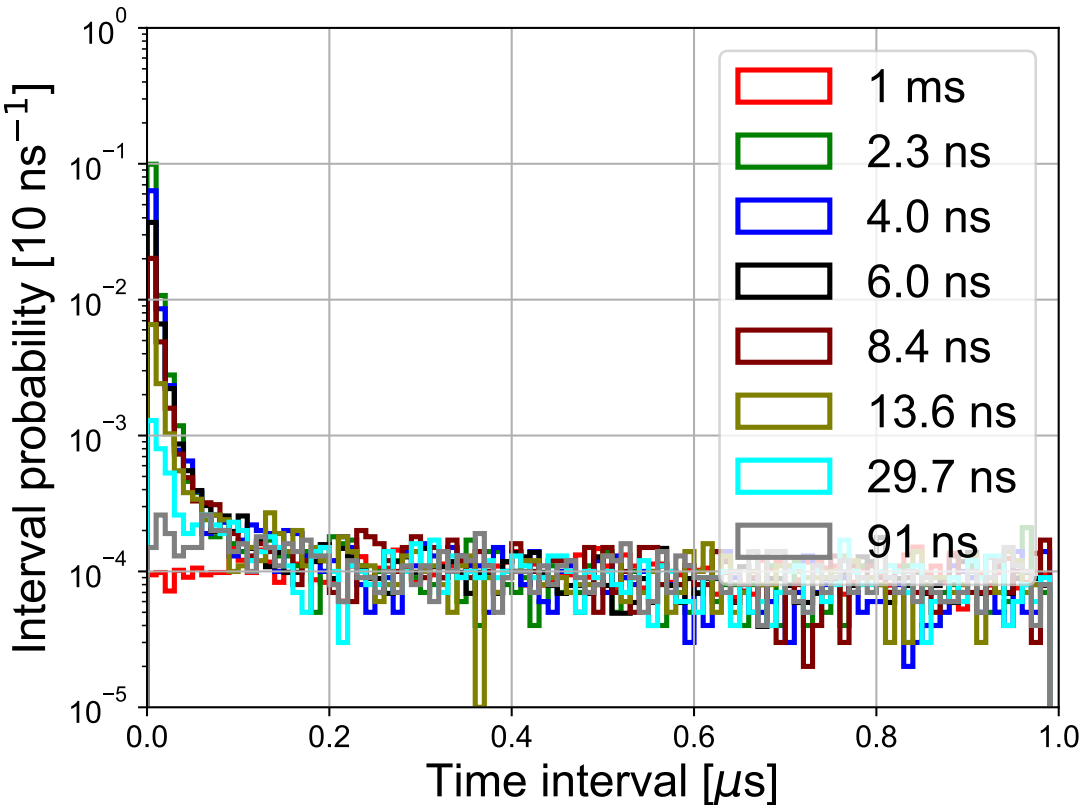


Figure 3.12 Time intervals distribution when hold-off time is 2.4 ns.

significantly larger than the red one when the time interval is small. These additional dark counts are triggered by the trapped carriers that have not been released during the short hold-off time, in other words, the after-pulsing.

Fig. 3.12 shows the normalized distribution of time intervals at different hold-off time, and the width of time bin is set at 10 ns. Therefore, the after-pulsing probability can be calculated by comparing the time interval probability at different hold-off time as shown in equation 3.7.

Supposing that the probability of primary dark count happens during a certain time unit 't' is $P_{DC}(t)$ which can be calculated through the long hold-off time measurement results. $P_{BD}(t)$ is the measured interval probability of dark counts including after-pulsing happens during the same period when the hold-off time is short, and $P_{AP}(t)$ is the after-pulsing probability, so

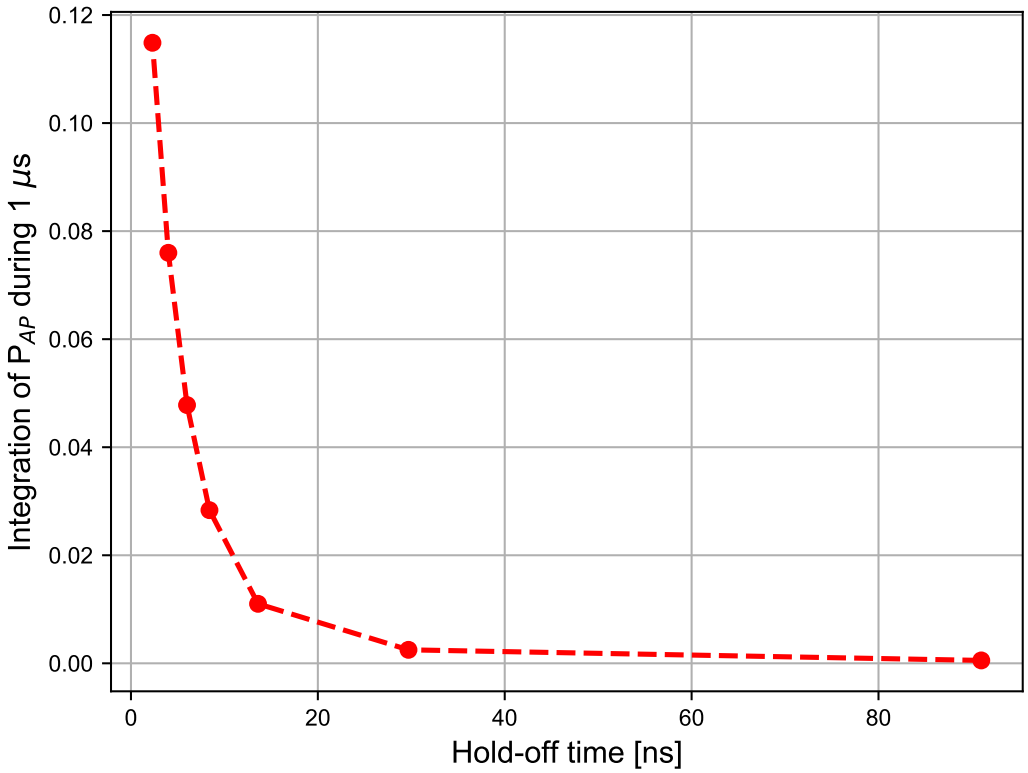


Figure 3.13 After-pulsing probability at different hold-off time.

that

$$P_{BD}(t) = 1 - (1 - P_{DC}(t)) \times (1 - P_{AP}(t)) \tag{3.6}$$

$$P_{AP}(t) = 1 - \frac{1 - P_{BD}(t)}{1 - P_{DC}(t)} \tag{3.7}$$

Since there is almost no difference when the time interval is larger than 1 us as shown in Fig. 3.12, the time period 't' is also set at 1 us, and Fig. 3.13 shows the calculated after-pulsing probability at different hold-off time. The calculation results illustrate that the after-pulsing probability is reduced to about 1% when the hold-off time is 20 ns.

3.4 Summary

This chapter focused on designing and testing about SAPDs that were fabricated by the available standard CMOS process. The detail about the design of SPADs that have been used

for the SPAD imagers in this work were presented in this chapter. The structures of three types of CMOS SPADs have been reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process in order to find a suitable structure of SPADs were introduced.

According to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V. A suitable SPAD of Pwell/DeepNwell with PolyGate around the active region, low DCR with purely avalanche breakdown, and planer breakdown region were confirmed by the experimental results. Then, a test circuit for after-pulsing probability measurement has been presented presented. The experimental results demonstrated the efficiency of hold-off time about reducing the influence of after-pulsing, and the after-pulsing probability can be decreased to lower than 1% with a 20 ns hold-off time.

Chapter 4

SPAD Imagers with Breakdown-Pixel-Extraction Architecture

4.1 Introduction

This chapter targets on the efficient readout architecture for SPAD imagers. A breakdown pixel extraction (BPE) readout architecture is proposed based on the binary feature of SPADs. This architecture only extracts the address of breakdown pixels to achieve a higher readout efficiency. The design of a 15×15 SPAD imager to verify the functionality of the proposed architecture is introduced, and an improved version of imager with 31×31 pixels utilizing background readout method is shown. Then, another BPE based 31×31 SPAD imager with event discriminator is proposed for minimizing the dead time of SPAD.

4.2 Idea of Breakdown Pixel Extraction Architecture

Since the SPADs are too sensitive, the incident light intensity should be relative low in order to obtain available images or fine time resolution. Therefore, breakdown SPAD pixels are very sparse in many applications. For an example, only 1 to 2% pixels of a imager are breakdown for a FLIM measurement [14]. However, in the traditional readout architecture, the entire frame is firstly readout indifferent with the low number of events. Moreover, for the applications that requiring to detect random events such as scintillation detectors, a short readout time under dark conditions is desirable. Therefore, new readout architecture is necessary for SPAD imagers [43].

A breakdown-pixel-extraction (BPE) architecture was proposed in order to improve the

readout efficiency for SPAD imagers [65, 66, 67]. The basic idea of this architecture is to extract the address of breakdown pixels only, and the procedure of BPE architecture is shown in Fig. 4.1. There are three types of pixels in the figure: the blank pixels represent the pixels with stable SPAD, the gray pixels represent the pixels with breakdown SPAD, and the dark gray pixels are the pixels that are under extraction. In order to maximize the readout efficiency, the row parallel scheme is employed in this architecture [68].

The procedure starts with the rise transition of leftmost search signals in each row (Fig. 4.1(a)). These search signals propagate until arriving at a breakdown pixel in a row in one clock cycle as shown in Fig. 4.1(b). If there is no breakdown pixel in a row, the search signal directly propagate to rightmost pixel and trigger a flag signal to indicate the end of readout procedure of this row. The flag signals are connected together by an AND gate tree. Then, at the next clock cycle, a global 'Next' pulse signal (the blue line in Fig. 4.1) is broadcast to resume the propagation of search signals and to start extracting the addresses of the detected

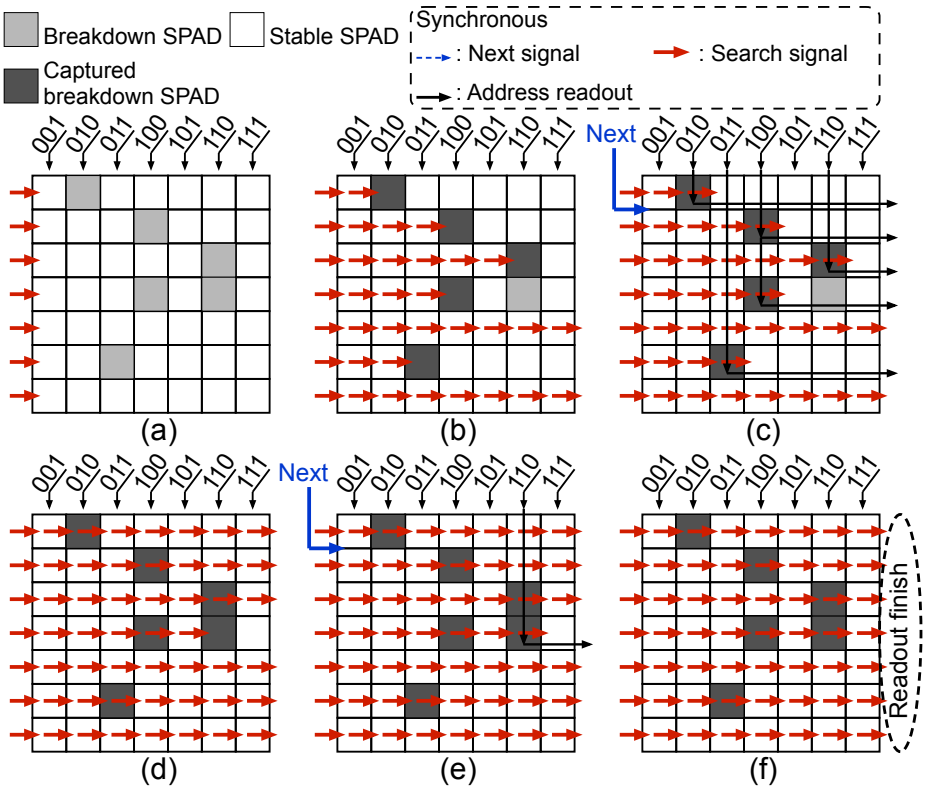


Figure 4.1 Procedure of BPE architecture.

pixels as shown in Fig. 4.1(c). These processes are repeated until all search signals have reached the rightmost pixel and raised flags as shown in Fig. 4.1(d)-(f). Then, a global reset signal is generated to reset the sensor.

Supposing that the number of breakdown pixels in the i-th row is $N_{BD,i}$, readout time ($T_{readout}$) depends on the maximum value of $N_{BD,i}$ ($Max(N_{BD,i})$) in this method. For the dark condition or the application that receives sparse incident photons, only a few SPADs are breakdown, so that $T_{readout}$ should also be shorter than the conventional readout method.

4.3 Analysis on $T_{readout}$

For each detected breakdown pixel, the number of cycles that is needed to extract its address is $1+N_{bit}$, where N_{bit} represents the bit-length of the address, for example, N_{bit} is 5 when there are 31 pixels in a row, and the additional 1 cycle is the global 'Next' pulse signal. Moreover, one more cycle is needed for the first search signal. Therefore, $T_{readout}$ is:

$$T_{readout} = T_{CLK} \times (1 + Max(N_{BD,i}) \times (N_{bit} + 1)) \tag{4.1}$$

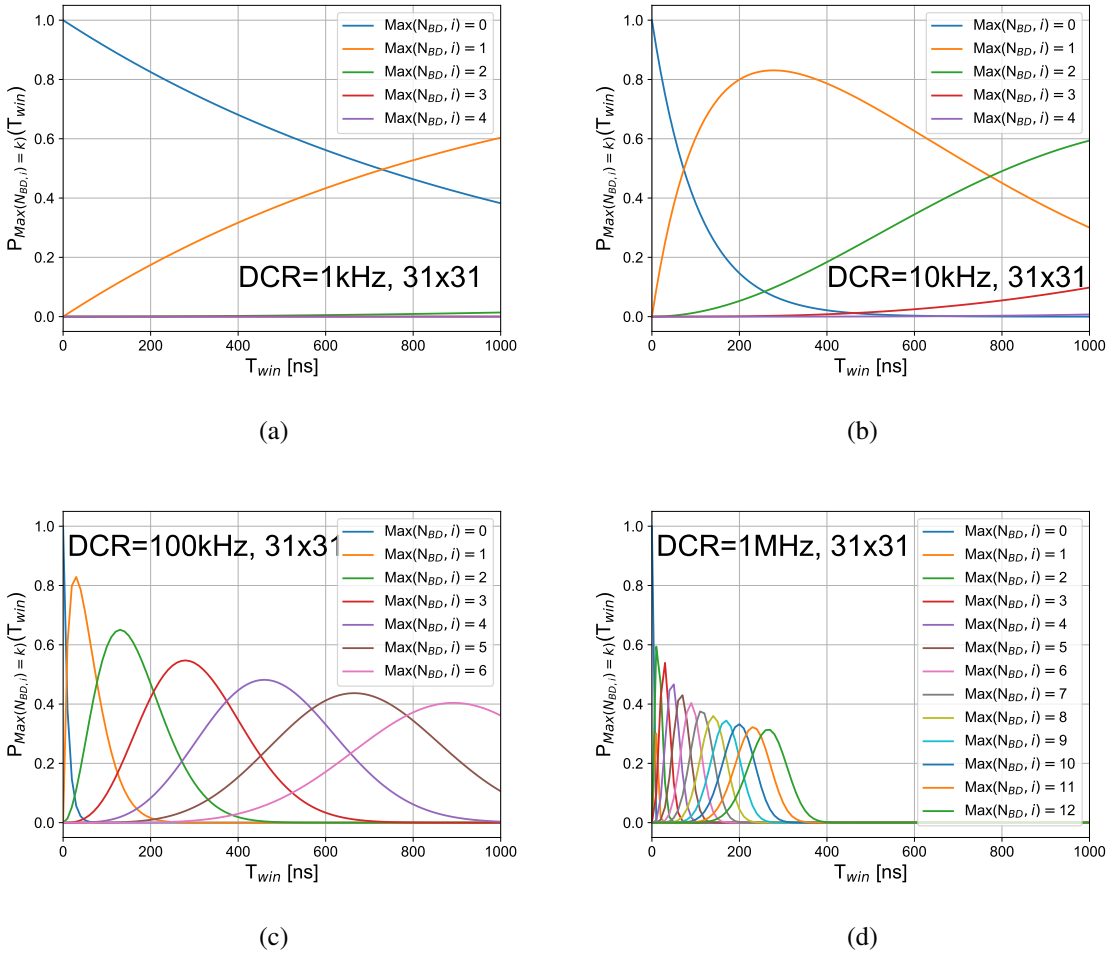
The similar method about the influence of DCR in Chapter 2 is utilized to calculate $T_{readout}$ is this section. Assuming that the SPAD imager contains $M \times N$ pixels, the probability that there are N_{dc} breakdown pixels in a single row with N pixels is:

$$P_{N_{dc}}(T_{win}, DCR, M, N) = \binom{N}{N_{dc}} \times (1 - P_{dc}(T_{win}))^{(N-N_{dc})} \times P_{dc}(T_{win})^{N_{dc}} \tag{4.2}$$

The probability for $Max(N_{BD,i}) = k$ is:

$$P_{Max(N_{BD,i}=k)}(T_{win}, DCR, M, N) = (\sum_{i=0}^{k} P_{N_{dc}=i}(T_{win}))^M - (\sum_{i=0}^{k-1} P_{N_{dc}=i}(T_{win}))^M \tag{4.3}$$

Fig. 4.2 shows the probability of $P_{Max(N_{BD,i}=k)}(T_{win}, DCR, M, N)$ with a function of at T_{win} when DCR=1KHz(a), DCR=10kHz(b), DCR=100kHz(c), and DCR=1MHz(d). These graphs show that when T_{win} is short and DCR is low, the value of $Max(N_{BD,i})$ should also be very small as shown in the Table 4.1. Therefore, $T_{Readout}$ is so short under dark conditions that the duty cycle of T_{win} (TAR) can be improved by this proposed method. A high TAR can help to improve the detection efficiency of randomly happening event such as scintillation event.



(a) (b)

(c) (d)

Figure 4.2 Distribution of $P_{Max(N_{BD,i}=k)}(T_{win}, DCR, M, N)$ in a 31×31 SPAD array at different T_{win} with different DCR: (a) DCR=1kHz; (b) DCR=10kHz; (c)DCR=100kHz; (d)DCR=1MHz

Table 4.1 Calculated results about $P_{Max(N_{BD,i}=k)}$, where N=31, M=31, and DCR=10kHz.

T_{win}	$P_{Max(N_{BD,i}=0)}$	$P_{Max(N_{BD,i}=1)}$	$P_{Max(N_{BD,i}=2)}$	$P_{Max(N_{BD,i}=3)}$	$E[Max(N_{BD,i}]$
100 ns	0.383	0.603	0.014	<0.001	0.632
150 ns	0.237	0.732	0.031	<0.001	0.795
200 ns	0.146	0.800	0.053	0.001	0.909

Besides capturing the random events, the proposed method is also suitable for applications with sparse incident photons such as the FLIM.

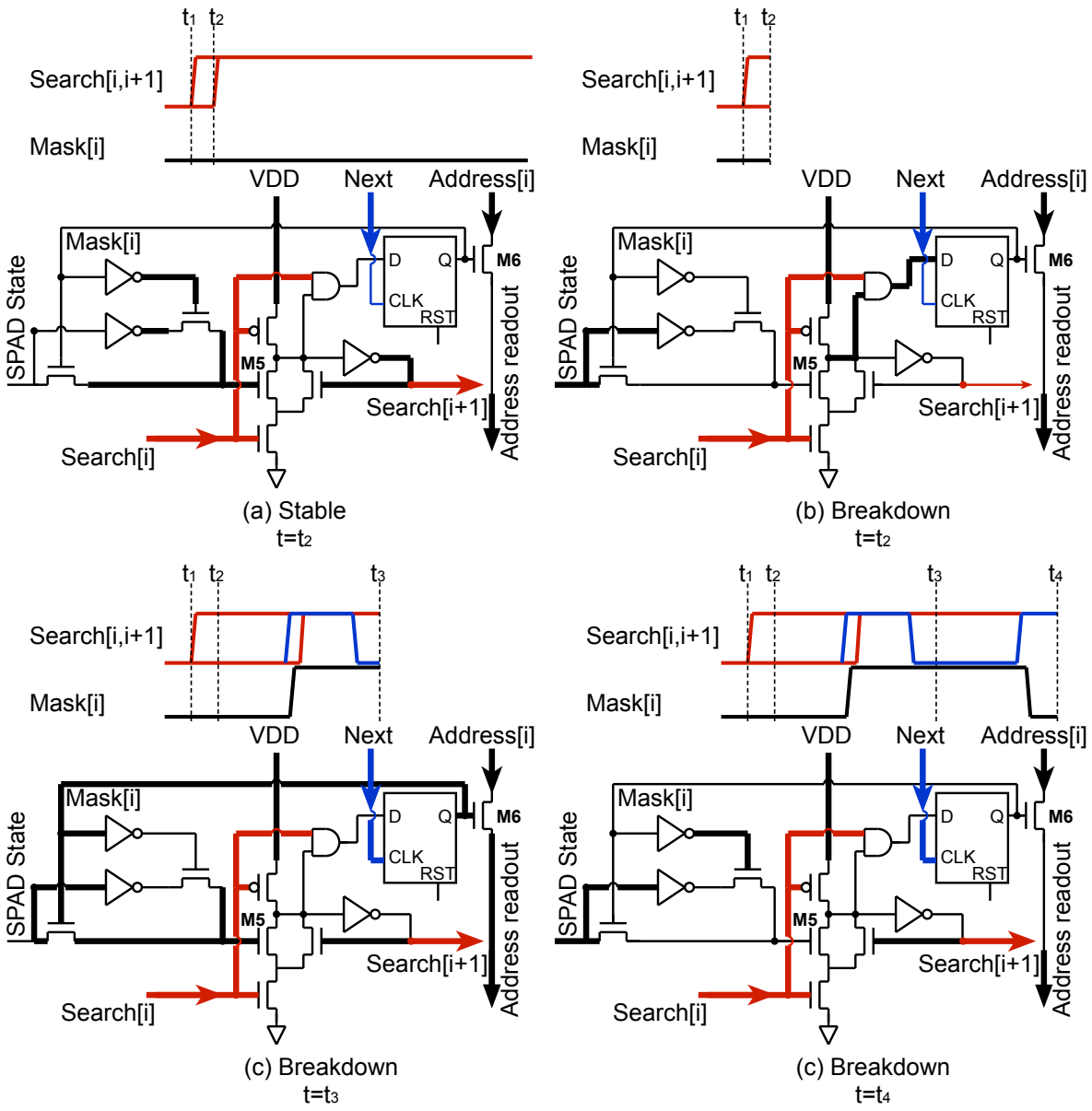


Figure 4.3 Procedure of BPE logic.

4.4 Design of BPE Circuit

Fig. 4.3 illustrates the behavior of the BPE logic. During the BPE procedure, there are two cases that depend on the states of the SPAD in the pixel. If the SPAD is stable, 'SPAD State' is low, so that transistor 'M5' keeps 'ON'. When 'Search[i]' goes high, this high signal propagates to the right neighboring search signal 'Search[i+1]' directly after a delay as shown in Fig. 4.3(a).

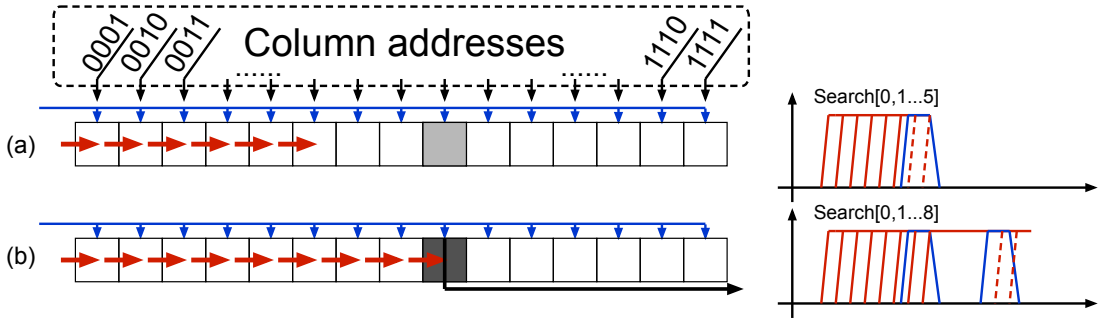


Figure 4.4 Effects of time difference between 'Search[0]' and 'Next'.

In the other case, SPAD is breakdown and 'M5' is turned 'OFF' at first. When 'Search[i]' goes high, the output of the AND gate (input of the DFF) also goes high and 'Search[i+1]' is kept low, so that the propagation of search signals is blocked. Then, when the global 'Next' pulse signal rises up, 'Mask[i]' also goes high to turn on the transistor 'M5' and 'M6'. Since 'M5' is 'ON', the propagation of search signals is resumed. At the same time, 'Address[i]', which is generated by the column address generator located at outside of the pixel array, can be readout through 'M6' (Fig. 4.3(c)). When 'Next' is triggered again, 'Mask[i]' returns low, and 'Address readout' is connected to the address of the next breakdown pixel if such a pixel exists (Fig. 4.3(d)).

If the search operation has not been completed in one clock cycle and the global 'Next' pulse signal goes high, the address of this breakdown pixel can not be readout until 'Next' goes high again shown in Fig 4.4(a) and (b). This kind of situation does not effect the readout results, however, increase $T_{readout}$. Therefore, 'Next' should be triggered after the search operation, and the time difference between 'Search[0]' and the first 'Next' signal is limited by the delay of the propagation of search signals.

The worst delay of search operation is that there is no breakdown pixel in a row. The search signal has to be propagated along all the pixels in this row. Fig 4.5 shows a post-layout simulation result of such case in a row containing 15 pixels. The time difference between the trigger of 'Search[0]' and 'Search[15]' is 3.9 ns. Therefore, the propagation delay for one pixel is 260 ps.

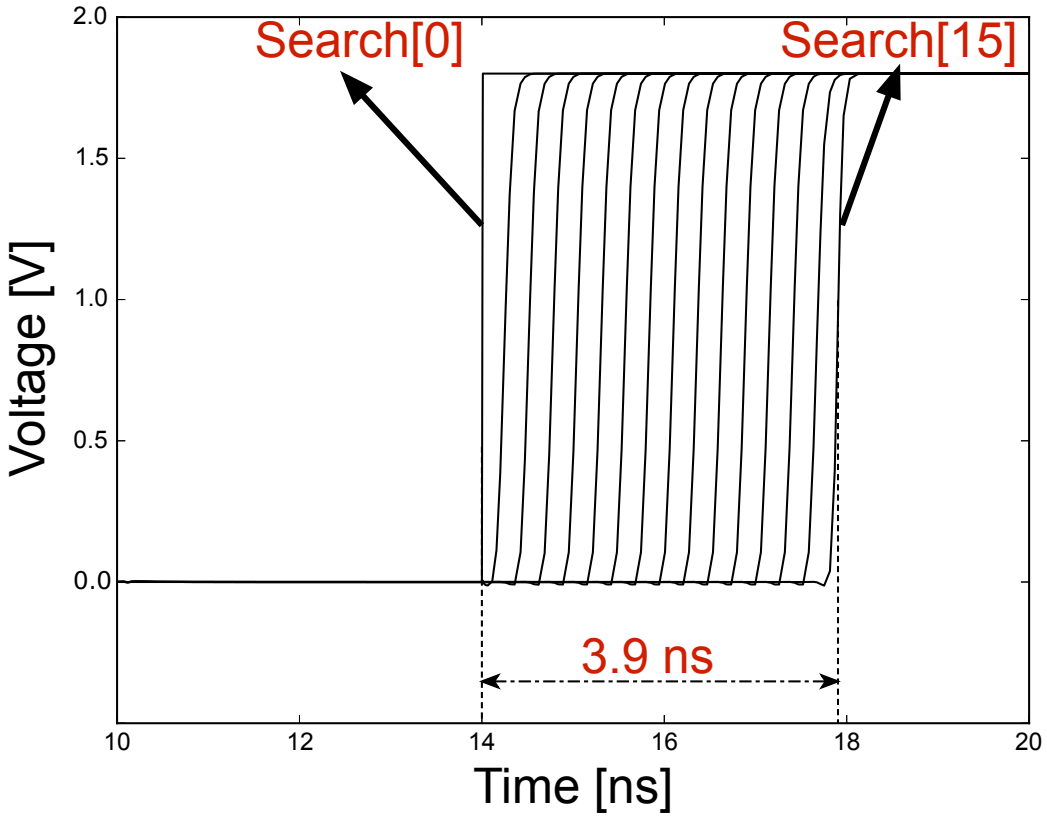


Figure 4.5 Effects of time difference between 'Search[0]' and 'Next'.

4.5 Design of 15×15 SPAD imager featuring BPE architecture

4.5.1 Chip Architecture

In order to verify the functionality of the proposed BPE method, a test-of-concept chip was developed with a 15×15 SPAD array using the same CMOS process. Fig. 4.6 shows the overall architecture of the designed sensor. It contains an array of 15×15 SPAD pixels, a column address generator (CAG), and a global search completion detection block. The CAG is used to generate the addresses of breakdown pixels for readout, and the control signal are input from external. The outputs of this chip are the 15-b row parallel readout addresses representing the addresses of breakdown pixels, and a 1-b readout finish signal.

Fig. 4.6(b) show a block diagram of three neighboring pixels and their interconnections. Each pixel contains a SPAD, a passive quenching circuit (PQC), and a BPE logic. Fig. 4.7(a)

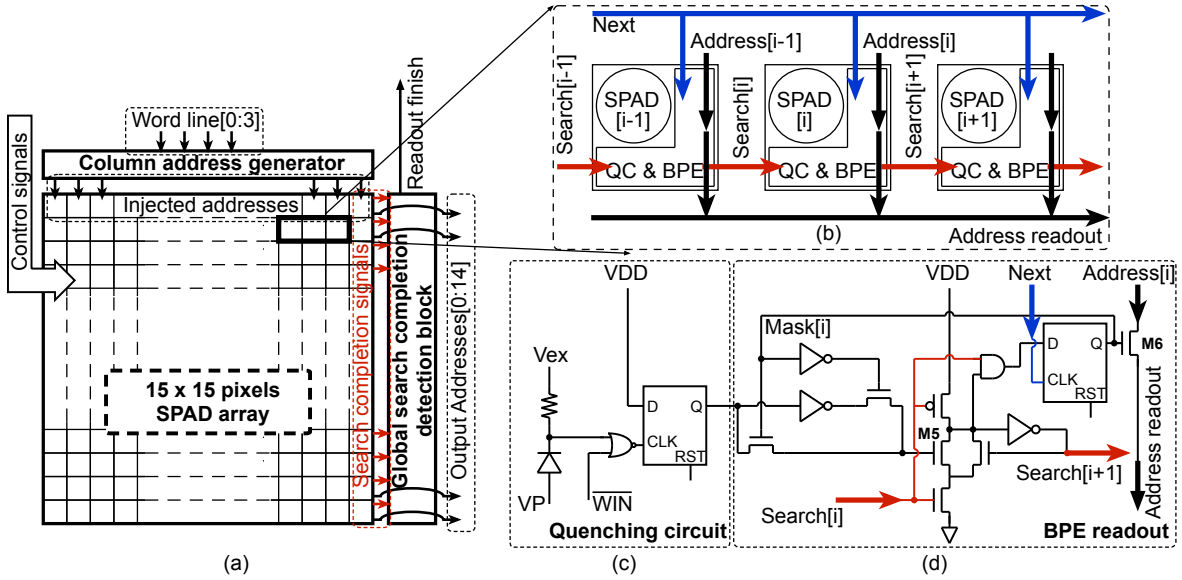


Figure 4.6 (a)Sensor architecture; (b) Pixel diagram; (c) Schematic of a quenching circuit; (d) Schematic of a BPE logic.

shows the layout of the SPAD in this sensor, the active area a circle with a radius of 7.8 μ m and the distance between Pdiff and STI is 0.4 μ m. Fig. 4.6(b) shows the layout of a pixel, the size is 80 μ m×80 μ m, so that the fill factor is about 3%.

4.5.2 Passive Quenching Circuit

Fig. 4.8 illustrates the behavior of PQC in the pixel. The SPAD is in the free-running mode, so that the SPAD is always reversely biased above the breakdown voltage until breakdown happens. T_{win} is controlled by '$\overline{\text{WIN}}$' that is input from the external. Since the output of the NOR gate is always low, the state of SPAD can not be transmitted to the DFF when '$\overline{\text{WIN}}$' is high. On the other hand, during the period that '$\overline{\text{WIN}}$' is low, each breakdown generates a pulse feeding into the DFF. Thus, the output of the DFF (QC_out) will goes high once there is a breakdown happens during T_{win}. At the end of T_{win}, QC_out goes back to low by the 'RST' signal.

The advantage of PQC is its simple circuit that can achieve a high FF, however, this circuit also has some drawbacks. Firstly, T_{win} can not be controlled precisely due to the long and asynchronous recharging time. Moreover, there are no hold-off time for this circuit, therefore,

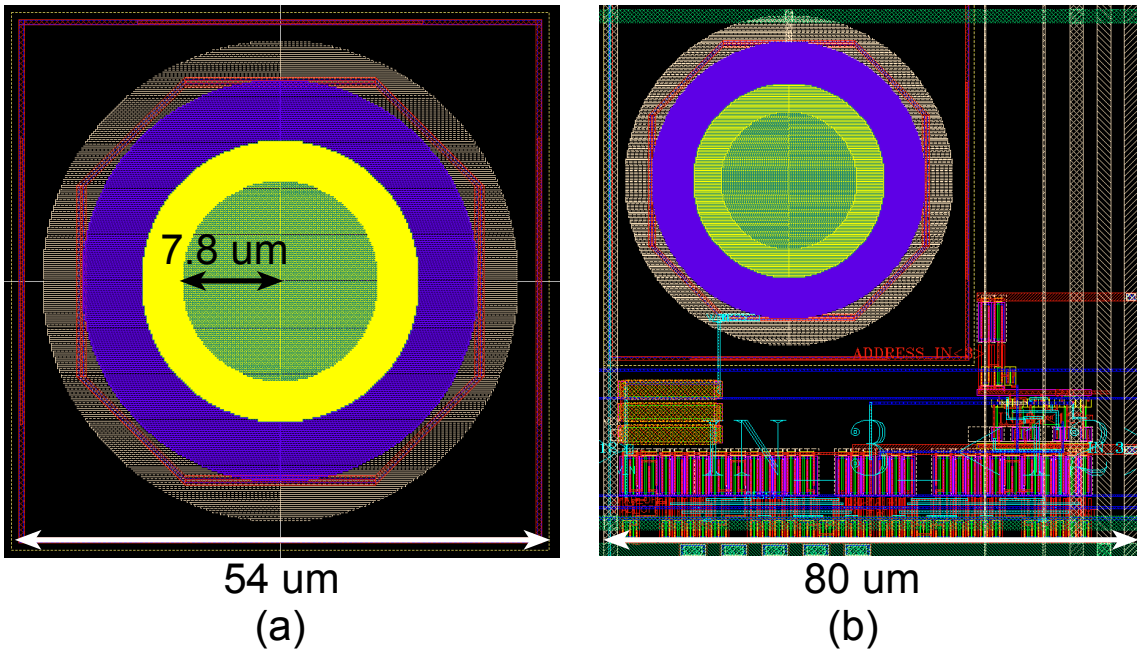


Figure 4.7 (a)Sensor architecture; (b) Pixel diagram; (c) Schematic of a quenching circuit; (d) Schematic of a BPE logic.

the influence of after-pulsing is large.

4.5.3 Timing Diagram

Fig. 4.9 shows a timing diagram of the designed sensor. 'WIN', 'RST', 'Search[0]', 'Next', and 4-b 'WL' are input signals from external. 'WIN' is used to control T_{win}. 'RST' is connected to all the DFFs in PQC and BPE circuits to restart a frame. 'Search[0]' and 'Next' are the control signals for the BPE circuits as mentioned before. 'WL[0:3]' are the 4-b input signals for the CAG. 'SCH_fin' is the output of Global search completion detection block to represent the completion of addresses output procedure. 'Output[0:14]' are the output addresses of 15 rows.

The BPE procedure is activated with the rising of 'Search[0]' at the end's of frame's T_{win}. The first 'Next' goes high after one cycle, and 4 cycles are needed to readout the 4-b address. As a result, the total $T_{readour}$ is (Max($N_{BD,i}$×5+1)) cycles.

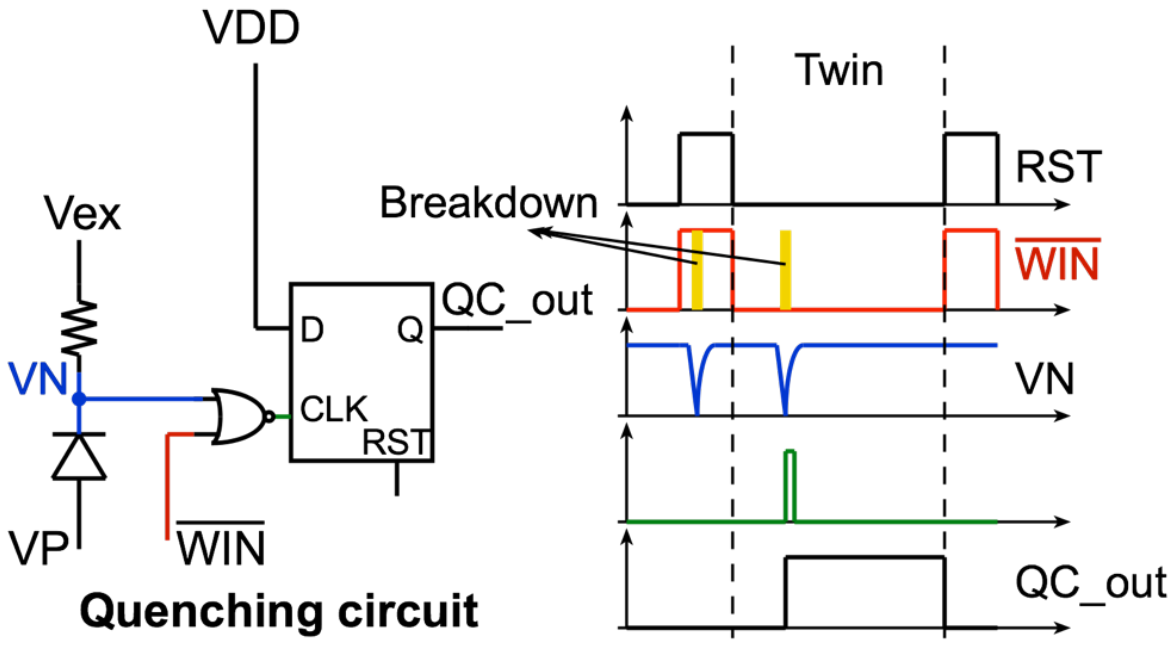


Figure 4.8 Behavior of passive quenching circuit.

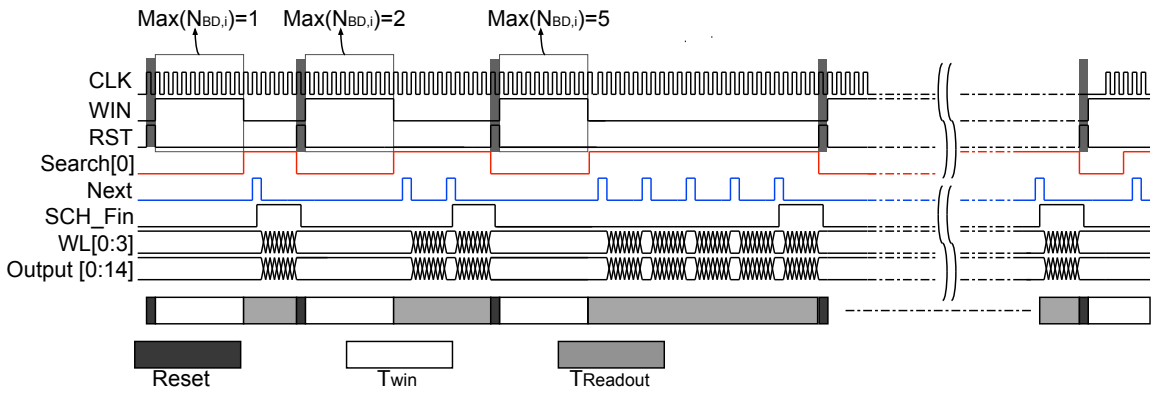


Figure 4.9 Sensor timing diagram.

4.6 Design of 31×31 SPAD Imager based on BPE architecture with Background Readout

In this section, the design of a 31×31 SPAD Imager based on BPE architecture with background readout is introduced [69]. This sensor is also based on the BPE architecture, and an additional 1-b memory in each pixel is utilized to store the value of the previous frame. Thus, the background readout is realized during the T_{win} as shown in Fig. 4.10. Through this read-

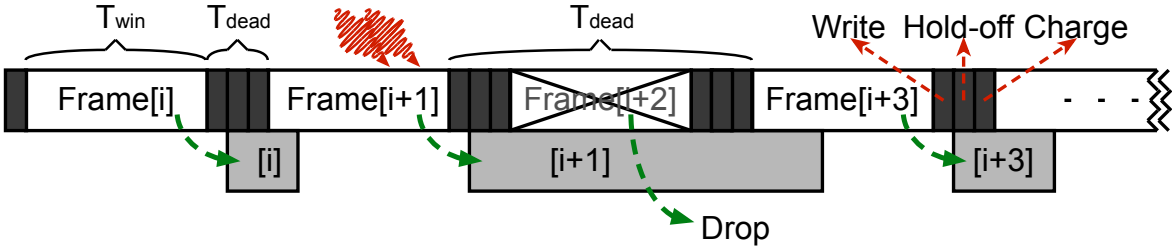


Figure 4.10 Idea of background readout.

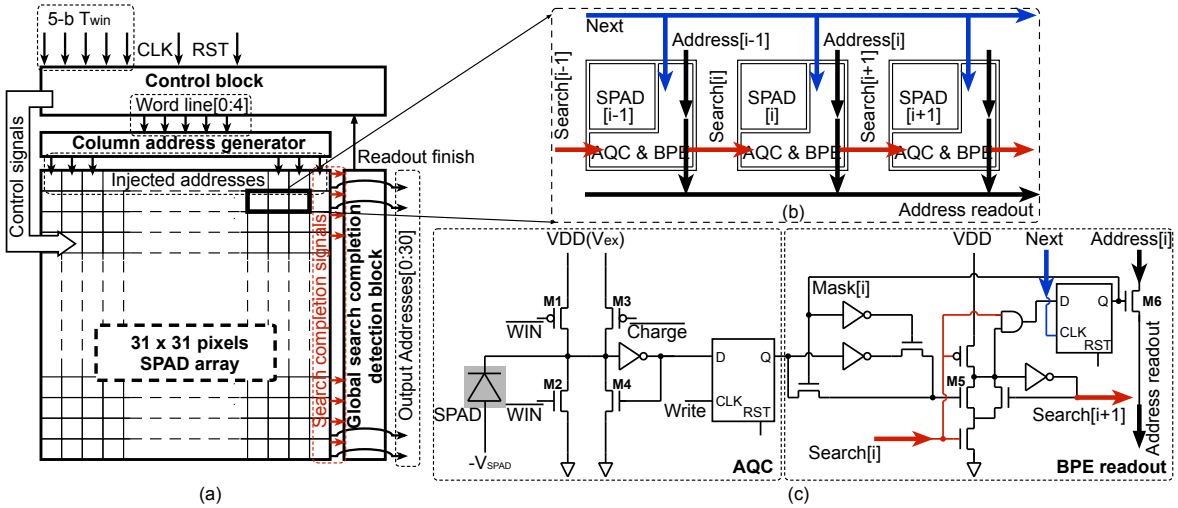


Figure 4.11 (a) Sensor architecture; (b) Pixel Diagram; (c) Detailed schematic of a single pixel.

out scheme, T_{dead} is minimized to 3 cycles if the readout procedure can be completed before the end of next frame's window time. The T_{dead} contains one cycle for 'Write', 'Hold-off' and 'Charge'. On the other hand, if there are a lot of breakdown pixels in a frame, $T_{readout}$ turns to be so long that the readout procedure can not satisfy the minimized T_{dead} requirement, all the data during $T_{readout}$ have to be dropped.

4.6.1 Chip Architecture

Fig 4.11 shows the overall architecture of this sensor. The sensor contains an array of 31×31 SPAD pixels, a CAG, a control block, and a global search completion detection block. Fig. 4.11 shows a block diagram of three pixels which is almost the same with the 15×15

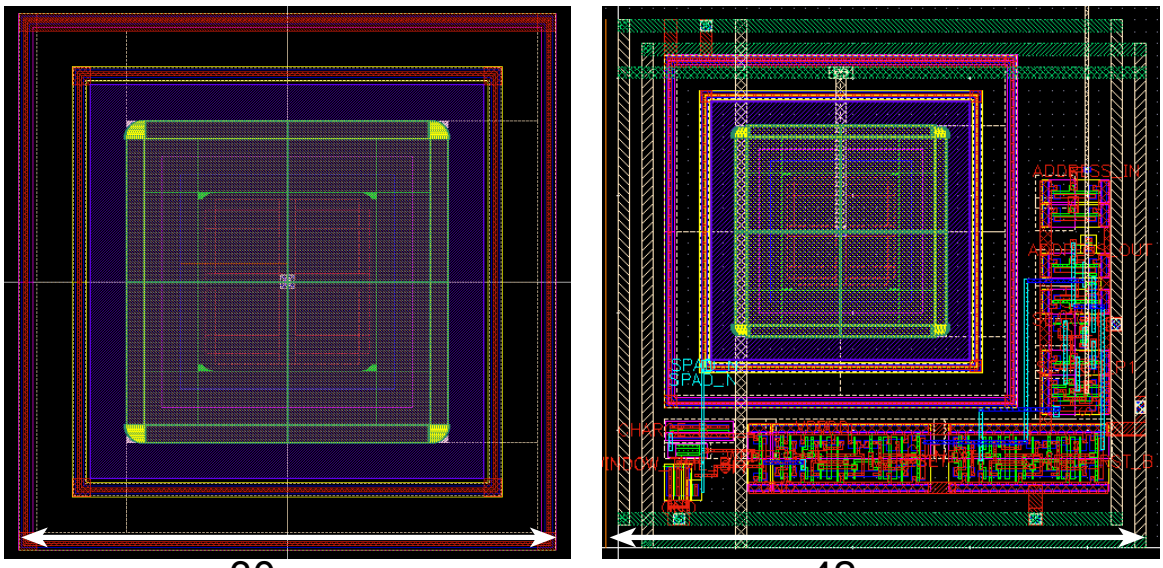


Figure 4.12 (a) Sensor architecture; (b) Pixel Diagram; (c) Detailed schematic of a single pixel.

SPAD imager introduced before. Each pixel contains a SPAD, an active quenching circuit (AQC) and a BPE logic.

Instead of the circular SPADs, rounded corners square SPADs are utilized in this chip to achieve a higher fill factor as shown in Fig. 4.12(a). In order to analysis the relationship between the DCR and the size of a SPAD, three chips are fabricated with different sizes SPADs. The length of the SPADs in this sensor are 9.2 μm, 11.2 μm, and 13.2 μ, respectively. Fig. 4.12(b) shows the layout of a single pixel and the fill factor is 4.8%, 7.1%, and 9.0%.

4.6.2 Active Quenching Circuit

Fig. 4.11 illustrated the schematic of a single pixel containing an active quenching circuit (AQC) and a BPE logic. The BPE logic is the same with the first sensor, however, the AQC is newly designed to achieve the proposed background readout scheme as well as improving the performance comparing with the disadvantages of PQC discussed before.

The behavior of AQC is shown in Fig. 4.13. The anode of a SPAD is slightly biased

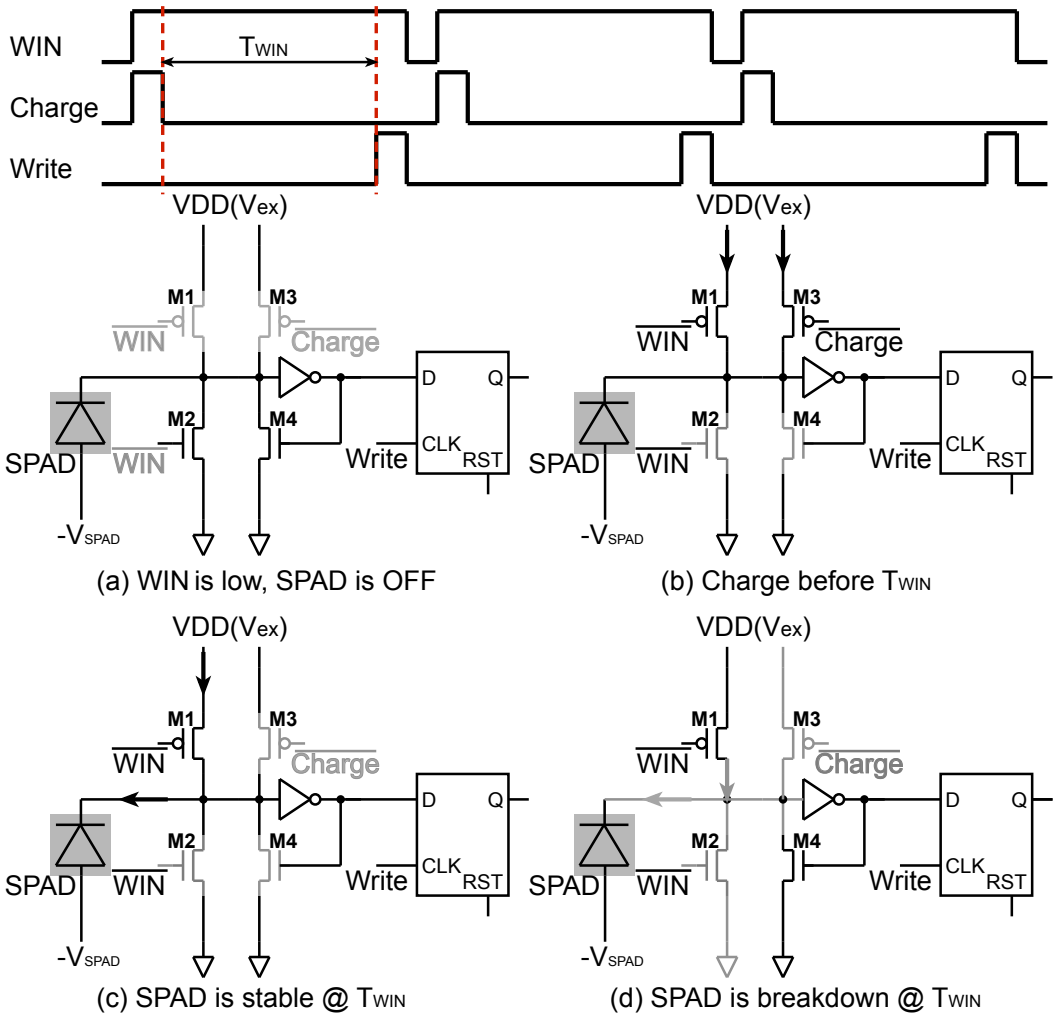


Figure 4.13 Behavior of AQC.

above the breakdown voltage (-V_{SPAD}), and the cathode is connected with 4 transistors and an inverter. When 'WIN' is high, the SPAD is over biased at V_{ex} and is able to detect the incident photons. However, charging the SPAD and writing data into DFF needs another two cycles. Therefore, the actual T_{win} is the pulse width of 'WIN' minus two clock cycles as shown in Fig. 4.13.

During T_{win}, if no breakdown happens, the voltage of cathode keeps high, and the inverter's output is '0' (Fig. 4.13(c)). Once there is a breakdown happening, the voltage of cathode falls down and the inverter's output turns to be '1'. Then, this high voltage turns 'M4' on so that the cathode of SPAD is connected to the ground and keeps low. Therefore, the hold-off

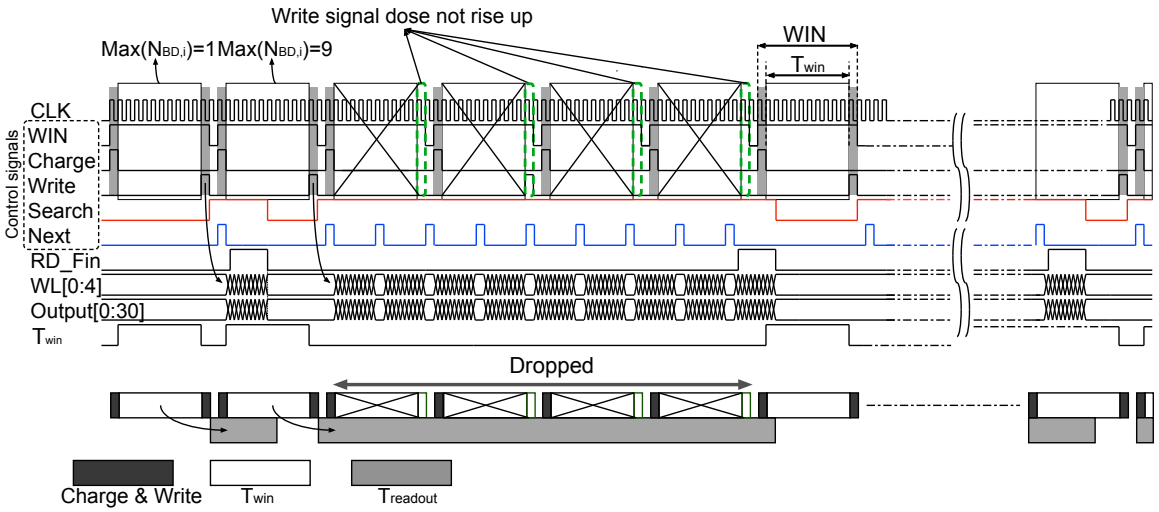


Figure 4.14 Sensor timing diagram.

procedure starts after detecting a breakdown. At the end of T_{win}, the SPAD's state of this frame is written into the DFF. During the next clock cycle, T_{win} goes low to force the SPAD 'OFF', this off period make the SPAD's hold-off time to be one cycle at least.

4.6.3 Timing Diagram

Fig. 4.14 shows a timing diagram of the sensor. 'WIN', 'Charge', 'Write', 'Search', and 'Next' are control signals generated by the control block outside of the array. The pulse width of 'WIN' is controlled by the 5-b external inputs. After writing the frame's data into the registers located in each pixel, the SPADs are turned 'OFF' by the falling of 'WIN' to achieve a certain hold-off time. Then, these SPADs are recharged again for the next frame, and T_{win} starts again. At the same time, the BPE procedure is activated to readout the stored data off the chip in parallel. Since 5 cycles are needed to readout an address for the 31 pixels in a row, the total readout time is:

$$T_{readout} = T_{CLK} \times (Max(N_{BD,i}) \times 6 + 1) \tag{4.4}$$

and the requirement that T_{dead} can be minimized is:

$$T_{readout} < 3T_{CLK} + T_{win} \tag{4.5}$$

$$T_{win} > T_{CLK} \times (Max(N_{BD,i}) \times 6 - 2) \tag{4.6}$$

This condition is defined that the frame is in the safety zone that T_{dead} is minimized and no data is dropped.

If the requirement can not be satisfied, T_{dead} turns to be:

$$T_{dead} = 3T_{CLK} + N_{drop} \times (3T_{CLK} + T_{win}) \tag{4.7}$$

where, N_{drop} represents the number of frames that have to be dropped,

$$(N_{drop} - 1) \times (T_{win} + 3T_{CLK}) \leq T_{readout} < N_{drop} \times (T_{win} + 3T_{CLK}) \tag{4.8}$$

T_{win} is set to 10 cycles (The pulse width of 'WIN' is 12 cycles) in this timing diagram, so that Maximum value for Max($N_{BD,i}$) to satisfy the requirement is one. For the first frame, the value of Max($N_{BD,i}$) is assumed to be one, thus, T_{dead} can be minimized to be 3 clock cycles. For the second frame, Max($N_{BD,i}$) is 8, so that the frame is not in the safety zone. $T_{readout}$ is 49 cycles for this frame, thus, 4 frames have to be dropped, and T_{dead} is 48 cycles.

4.7 Design of 31×31 SPAD Imager with Event Discriminator based on BPE Architecture

The feature of BPE logic is that stable SPAD pixels are automatically skipped, and the search signals are stopped at breakdown pixels in one cycle. Thus, BPE logic is also able to count the Max($N_{BD,i}$) without readout procedure, and the counting time (T_{count}) is,

$$T_{count} = T_{CLK} \times (1 + Max(N_{BD,i})) \tag{4.9}$$

Fig. 4.15 shows a Monte Carlo simulation results to show that the value of Max($N_{BD,i}$) is proportion to the number of total breakdown SPADs (total counts) in an array. Since the difference between dark frame and event frame is the total number of breakdown pixels, event distinction can be conducted through the counted value of Max($N_{BD,i}$). Therefore, the BPE logic can be used as a discriminator to detect the event frames from the dark frames.

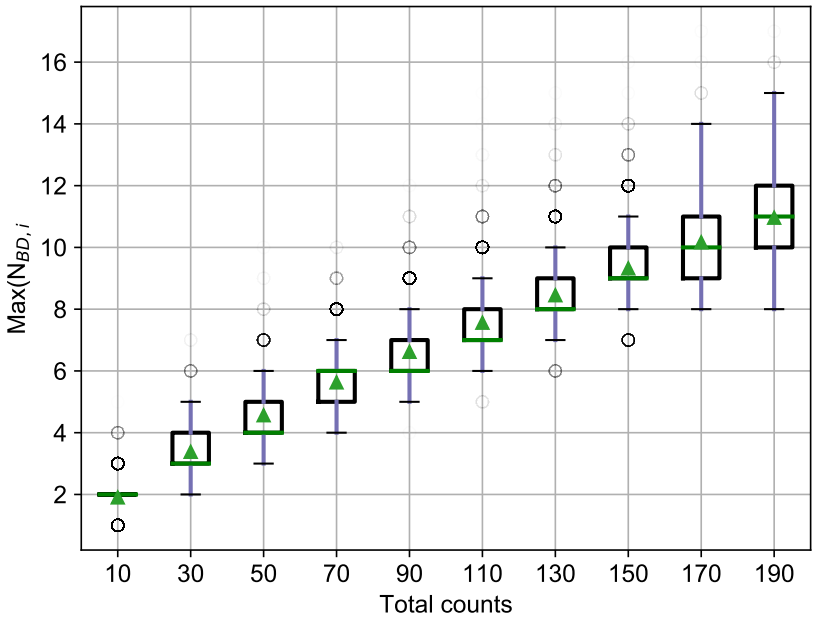


Figure 4.15 A Monte Carlo simulation result about total counts and Max($N_{BD,i}$).

4.7.1 Idea of Event Discriminator Based on BPE Logic

The counting procedure is similar to the BPE readout method introduced before, and an additional counter is utilized to count Max($N_{BD,i}$) as shown in Fig. 4.16. The counter is reset to 0 at the first. The counting procedure starts with the trigger of leftmost search signals in each row Fig. 4.16(a), and these signals propagate until arriving at a breakdown pixel in a row (Fig. 4.16(b)). Then, at the next cycle, a global 'Next' pulse signal is broadcast to resume the propagation, and add 1 to the value of counter as shown in Fig. 4.16(c). These processes are repeated until all search signals have reached the rightmost pixel that ends the counting procedure, and the counter's value equals to Max($N_{BD,i}$).

Fig. 4.17 shows the scheme of proposed idea. The counting procedure is conducted after a frame's T_{win}. If the counter's value is smaller than the threshold value (N_{th}) as shown in the first frame, a global reset signal is triggered to reset the frame without readout. On the other case, if the value becomes larger than NN_{th}, the counting procedure stops and the BPE readout procedure is triggered after one clock cycle. Different from the previous imagers,

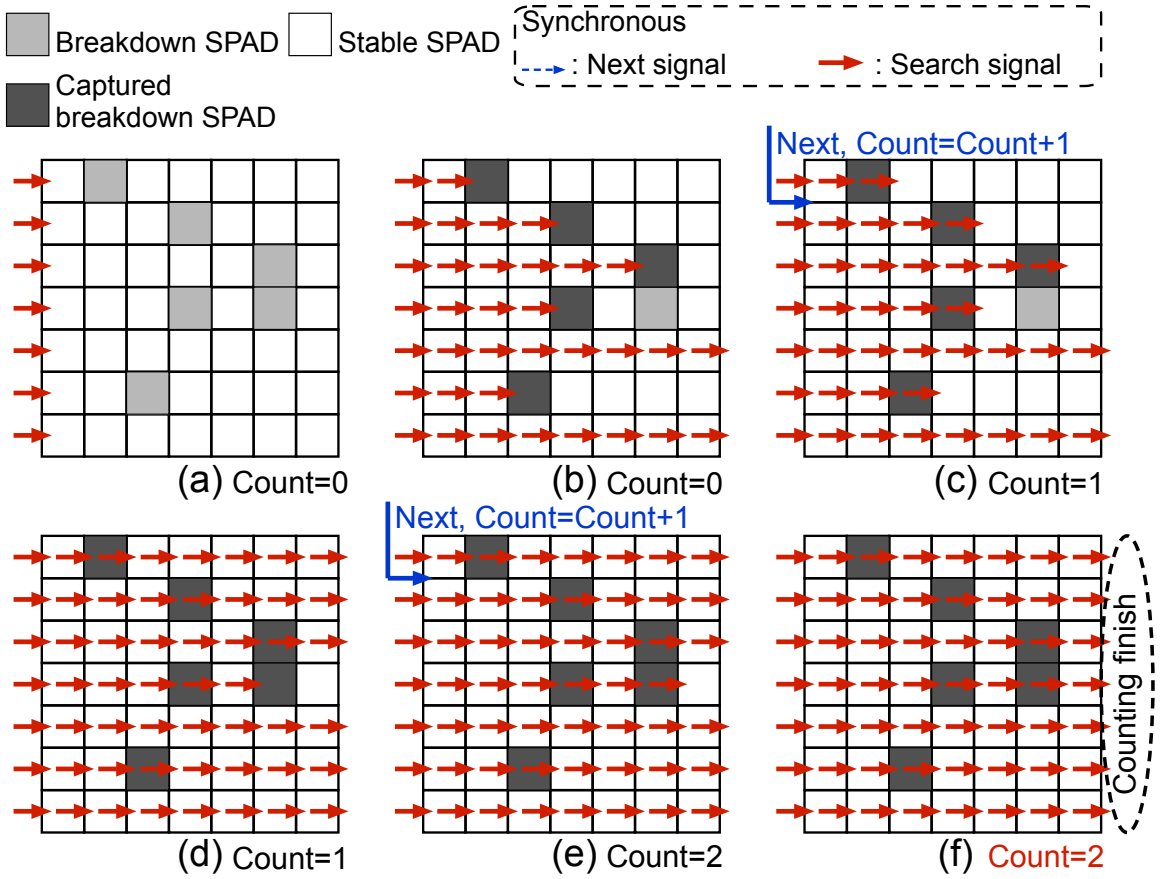


Figure 4.16 Counting procedure of the proposed method.

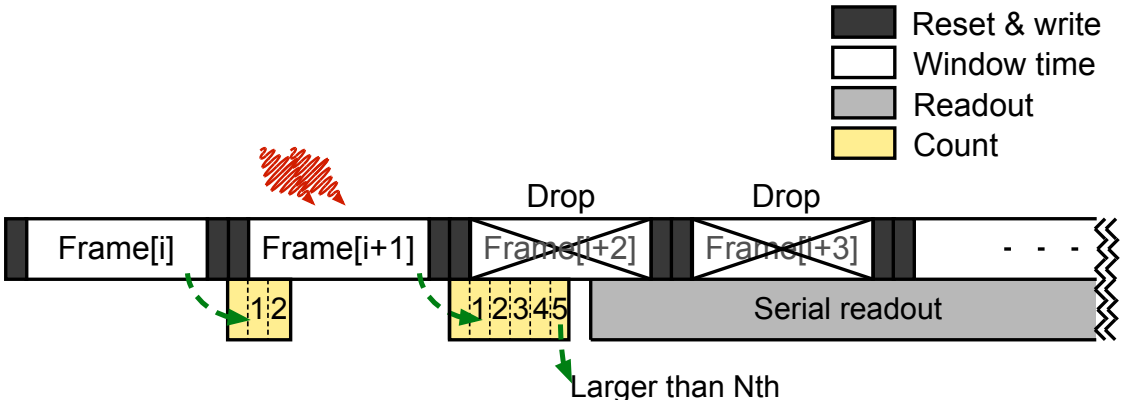


Figure 4.17 Proposed event discriminator scheme.

a serial output method is utilized in this method for two reasons: the serial output reduces the number of output pins from 31 to 1, which make measurement be more convenient; only event frame is readout so that the high-speed readout is unnecessary.

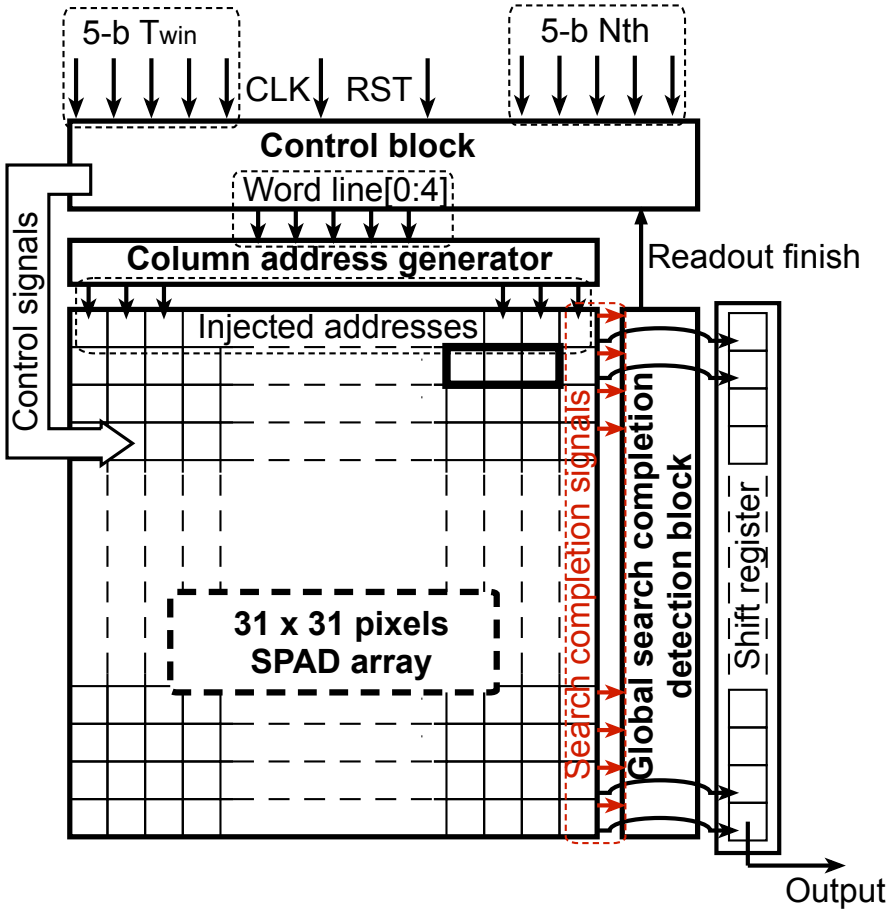


Figure 4.18 Chip architecture.

4.7.2 Chip Architecture

Fig. 4.18 shows the overall architecture of this sensor. The sensor contains an array of 31×31 SPAD pixels, a CAG, a control block, a Global search completion detection block, and shift register. It is almost the same with the last sensor except the control block and the additional shift register. For the control block, additional 5-b inputs are used to represent the N_{th}, and the event distinction function is added.

4.7.3 Timing Diagram

Fig. 4.19 illustrates a timing diagram of this sensor. The pulse width of 'WIN' is controlled by the external inputs, which is 12 cycles in this timing diagram. The same with the last sensor, the actual T_{win} is the pulse width of 'WIN' minus two cycles because of writ-

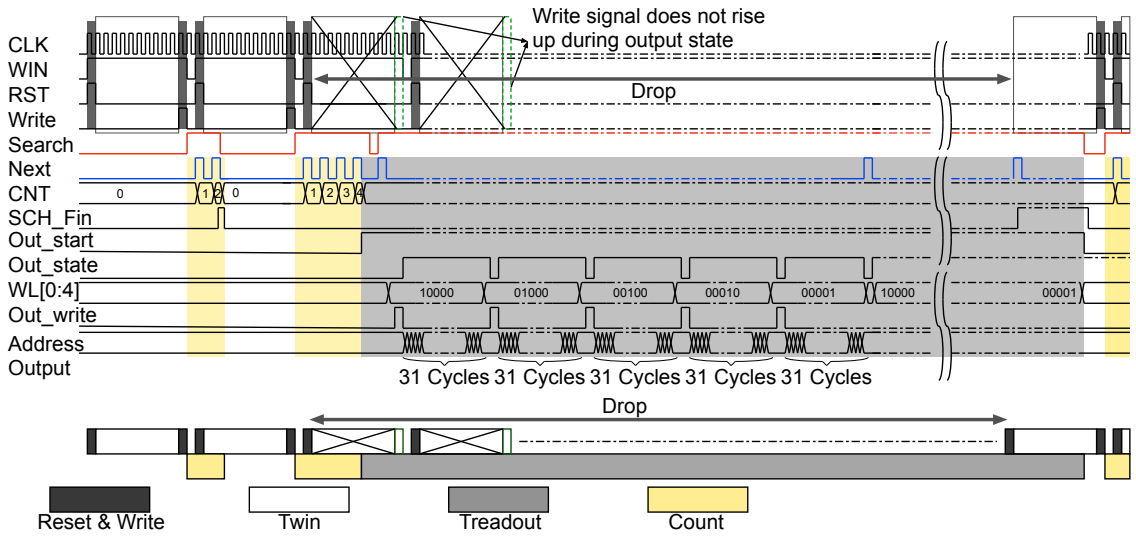


Figure 4.19 Sensor timing diagram.

ing and charging. The value of N_{th} is also controlled by a 5-b external inputs, which is 3 in this diagram. 'RST', 'Write', 'Search', 'Next', 'Out_start', 5-b 'WL[0:4]', 'SCH_Fin', and 'Out_write' are control signals generated by the control block. 'RST', 'Write', 'Search', 'Next', and 'WL[0:4]' have the same functions with the last chip. 'Out_start' goes high when the value of counter becoming larger than N_{th}, and represents the starting of readout procedure. 'SCH_Fin' represents the finish of counting procedure or readout procedure that is feedback to the control block. 'Out_write' is used to write the addresses to the 31-b shift-registers for readout. 'CNT' represents the value of the an internal counter to count $Max(N_{BD,i})$. 'Out_state' is one of the output signal representing the output state. 'Address_Output' is the serially output addresses.

For the first frame in the timing diagram, the $Max(N_{BD,i})$ is 2, which is smaller than N_{th}, so that the readout procedure is not executed for this frame, and 'Write' signal rises up at the end of the second frame's T_{win}.

For the second frame, the counting procedure has not been finished when the value of CNT becomes 4, which indicates that $Max(N_{BD,i})$ is larger than N_{th}. Thus, the 'Search' signal falls down to suspend the counting procedure, and 'Out_start' goes high. At the next clock cycle, 'Search' signal rises up again to start the BPE readout procedure. Then, 'Out_write' rises

up to write addresses to the shift-resisters for readout after one cycle when 'Next' goes high. After one cycle, 'Out_state' also goes high representing the beginning of addresses readout procedure. 'Write' keeps low and drops all the data until the completion of BPE procedure. Since there is no readout procedure for the dark conditions, T_{dead} is always minimized to 3 cycles at all the dark conditions.

4.8 Summary

This chapter targeted on the efficient readout architecture for SPAD imagers. Since the breakdown SPAD pixels are sparse in many application, an architecture that only extracts the address of breakdown pixels can achieve a higher readout efficiency. A breakdown pixel extraction (BPE) readout architecture has been proposed based on the binary feature of SPADs. The design and behavior of BPE architecture has been introduced at first, and the design of a 15×15 SPAD imager to verify the functionality of the proposed architecture has been presented.

Then, a detail design about the imager with 31×31 pixels utilizing background readout method has been shown. This imager added an additional 1-b memory in each pixel to store the value of the previous frame, and to realize the background readout. This method could minimized T_{dead} to 3 cycles under dark conditions or under sparse breakdown pixels.

Furthermore, another BPE based 31×31 SPAD imager with event discriminator has been proposed for minimizing T_{dead} and event detecting. This imager counted the value of $Max(_{BD,i})$ of each frames at first, and the readout procedure only started when $Max(_{BD,i})$ became larger than a threshold value.

Chapter 5

Experimental results of Designed BPE SPAD Imagers

5.1 Introduction

This chapter presents the experimental results including the functionality, DCR distribution, PDE and dead time about the three designed imagers. Then, a comparison on the three designed imagers are presented.

5.2 Experimental Results of the 15×15 SPAD Imager

Fig. 5.1 shows a chip photomicrograph of the 15×15 SPAD imager with BPE architecture fabricated by the same process introduced in Chapter 4. The chip was tested by a logic analyzer, and the measured waveforms when the chip was being operated at 25 MHz are shown in Fig. 5.2. 'Search[0]' (Fig. 5.2(b)), and 'Next' (Fig. 5.2(a)) are input signals that were generated by the logic analyzer. 'Address_out' is one of the 15 rows parallel readout addresses, and the measured waveform is shown in Fig. 5.2(c). This measured waveform indicates that the 2nd and 11th pixels of this row were breakdown at this frame. And $T_{readout}$ for this frame is 11 clock cycles. The search finish signal goes high after all the breakdown pixels had been readout out as shown in Fig. 5.2(b).

5.2.1 DCR Distribution Measurement

To measure the DCR distribution over the chip, the imager was positioned in a black box, and operated with different T_{win}. Fig. 5.3 shows an example of the measured image by sum-

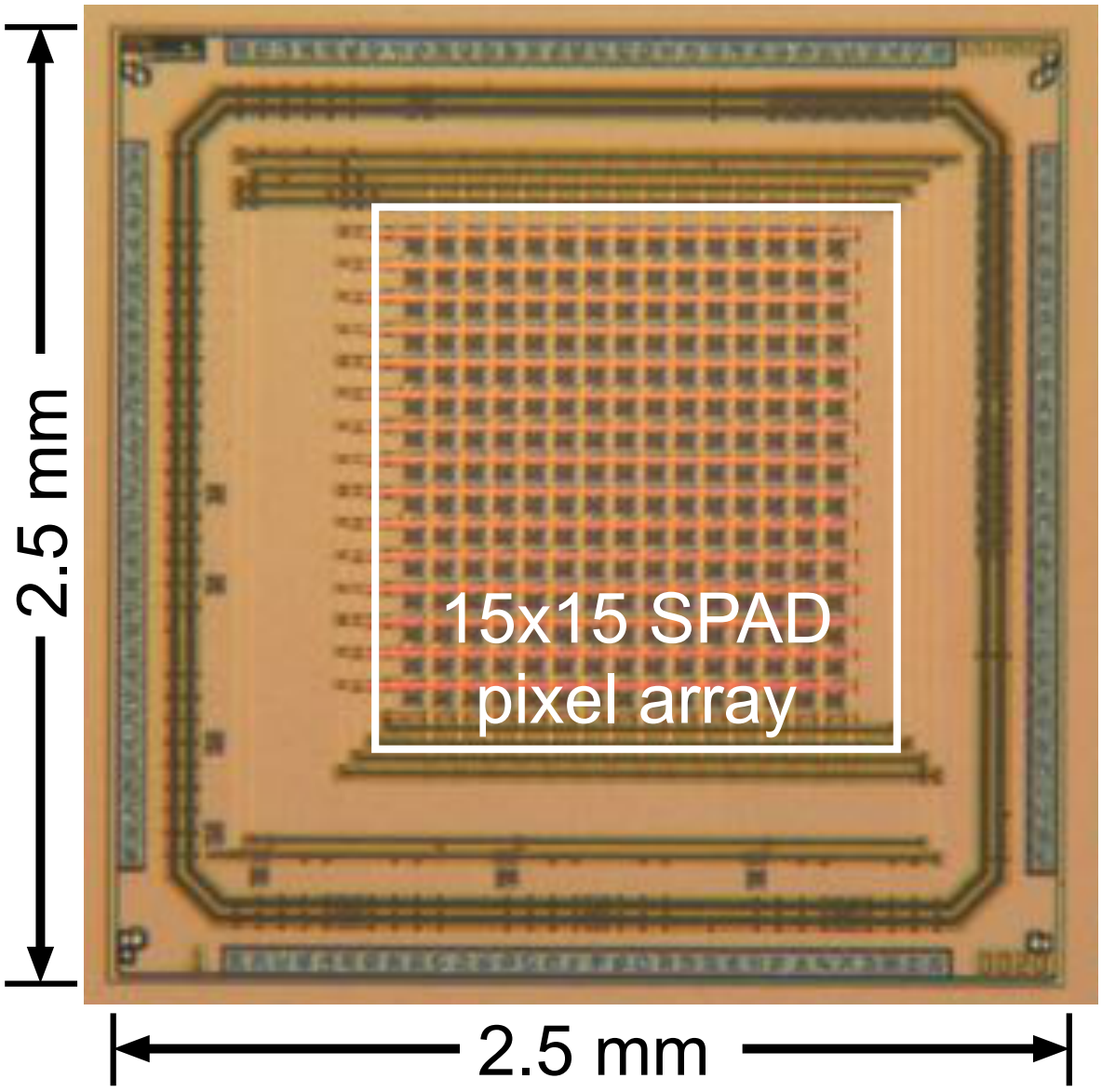


Figure 5.1 Chip photomicrograph of the 15×15 SPAD Imager.

ming up 1000 frames that were measured in the black box with 400 ns T_{win}. Since the SPAD imager can only distinct whether breakdown happens or not during the T_{win}, the number written in each pixels (Counts) represents the probability of breakdown happening (P_{bd}).

$$P_{bd} = \frac{Counts}{1000} \tag{5.1}$$

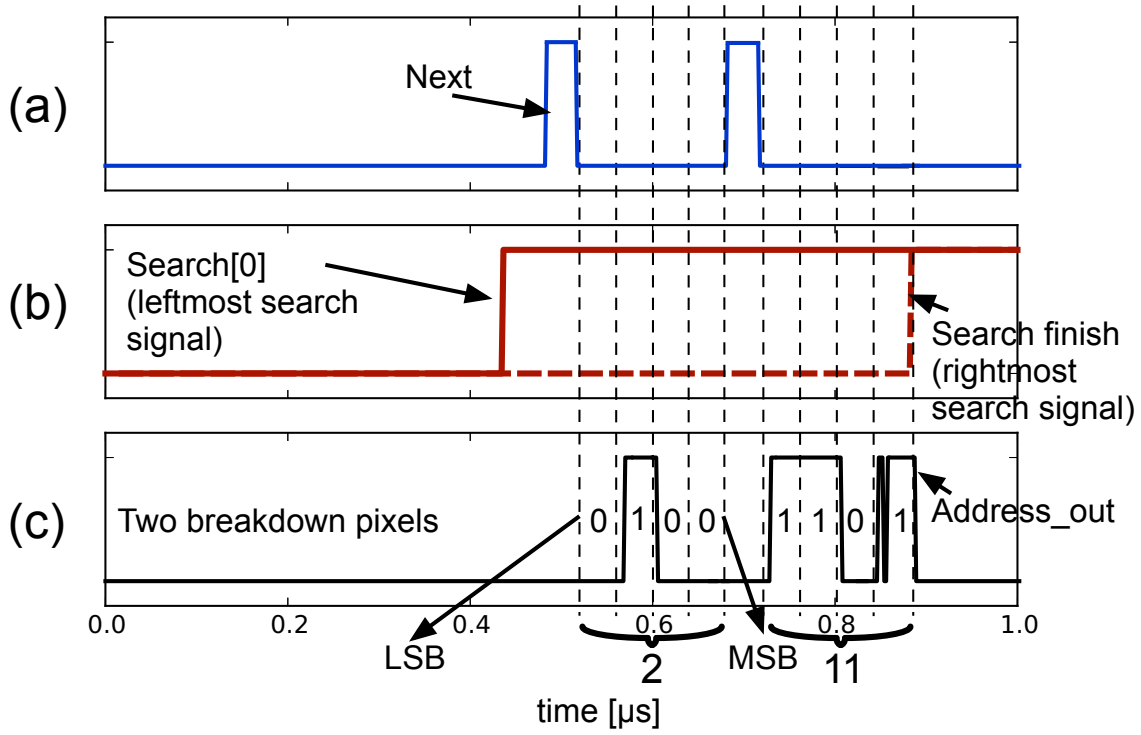


Figure 5.2 Measured waveforms by a logic analyzer.

According to the introduction in Chapter 2, the number of dark counts per time unit (T_{win}) follows a Poisson distribution:

$$p(k, T_{win}) = \frac{\lambda^k e^{-\lambda}}{k!} \tag{5.2}$$

where λ is the expected value of dark counts during T_{win}, so that

$$\lambda = T_{win} \times DCR \tag{5.3}$$

Therefore, P_{bd} is

$$P_{bd} = \sum_{k=0}^{\infty} p(k, T_{win}) \tag{5.4}$$

and, DCR is:

$$1 - P_{bd} = p(0, T_{win}) = e^{-T_{win} \times DCR} \tag{5.5}$$

$$1 - \frac{Counts}{1000} = e^{-T_{win} \times DCR} \tag{5.6}$$

$$DCR = -\frac{\log\left(1 - \frac{Counts}{1000}\right)}{T_{win}} \tag{5.7}$$

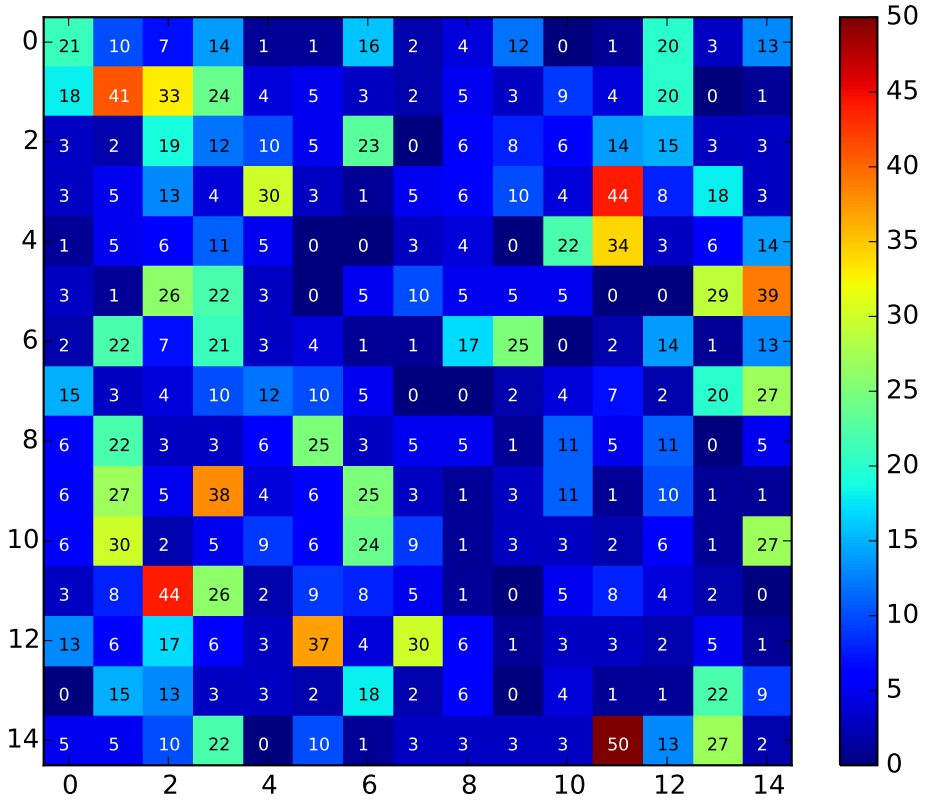


Figure 5.3 Summation of 1000 dark frames when T_{win} was 400 ns.

Fig. 5.4 shows the cumulative DCR plot over the sensor at four different T_{win}. The median value, mean value, and the largest value are 10 kHz, 20 kHz, and 130 kHz, respectively.

5.2.2 Pinhole Imaging

Fig. 5.5 shows the experimental setup to demonstrate the sensor functionality. During the experiments, pinholes with different sizes (the diameters are 5 μm, 25 μm, and 100 μm, respectively) are placed in front of the chip. The photons are generated by a digital modulated laser. The whole system is placed in a black box. The generation of control signals and output data acquisition are conducted by the logic analyzer. The pulse width of laser is 100 ns, and T_{win} is 300 ns. The system operates at 50 MHz, and the power of laser beam is controlled by a PC.

Fig. 5.6(a)-(c) show the simulated diffraction patterns with different size of pinholes. The

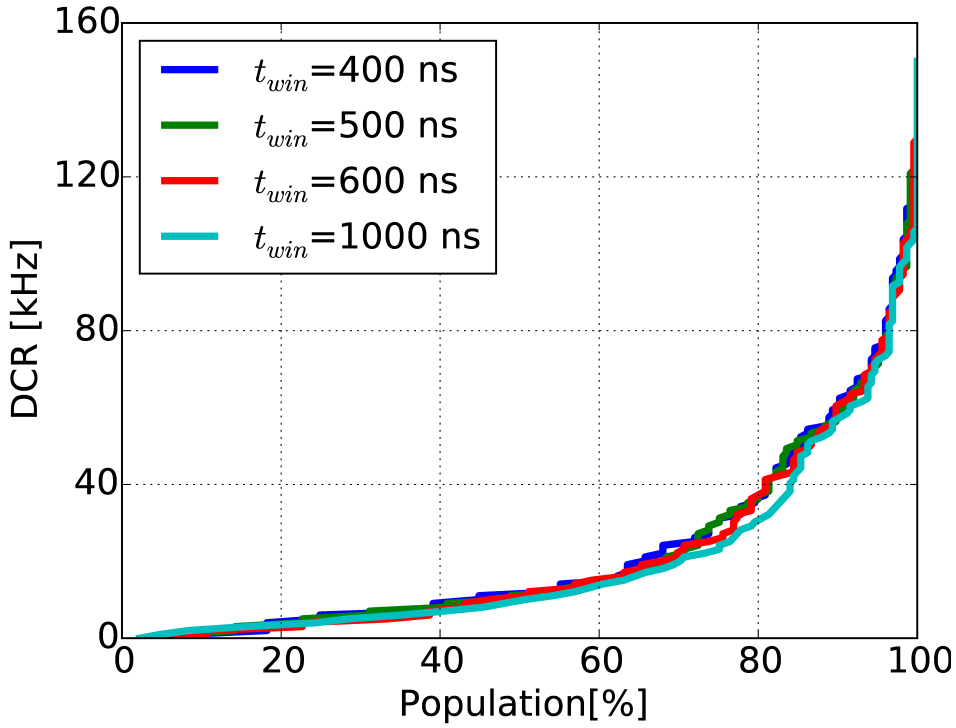


Figure 5.4 Cumulative DCR plot at different T_{win}.

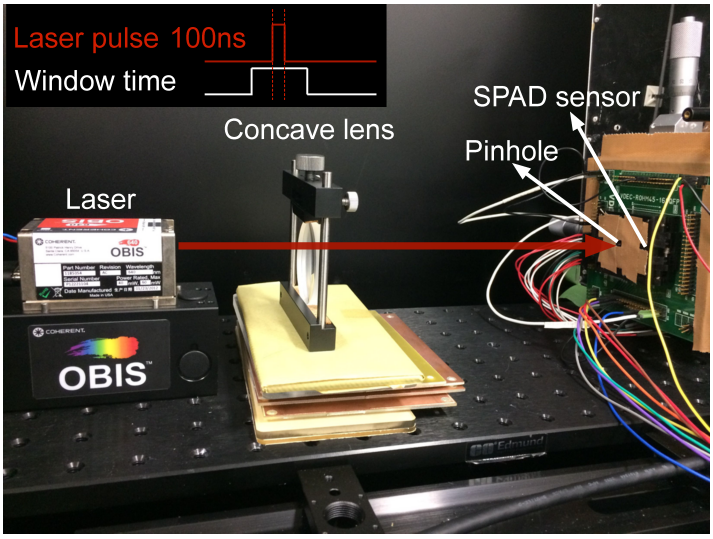
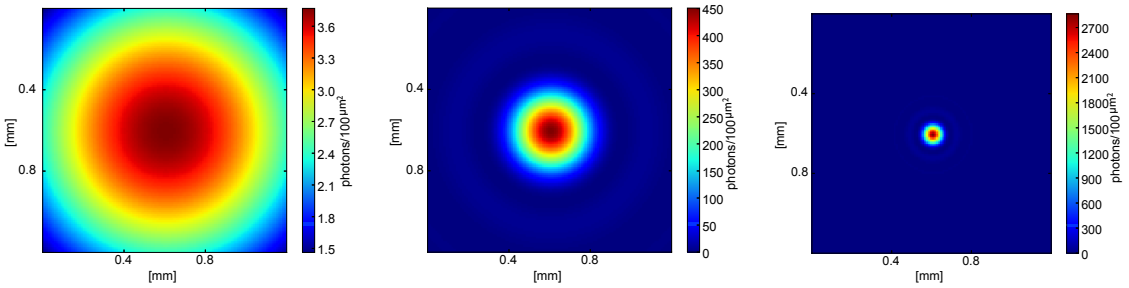


Figure 5.5 Experimental setup of pinhole diffraction pattern measurement.

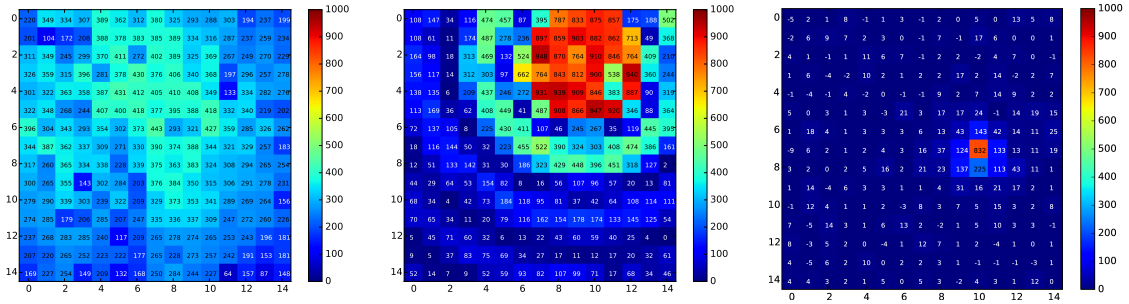
color of these figures represent for the number of incident photons in a 10×10 μm^2 square. Fig. 5.6(d)-(f) show the captured images with different pinholes, by summing 1000 frames together. The pinhole diffraction pattern is clearly observed.



(a) 5 μm pinhole diffraction pattern.

(b) 25 μm pinhole diffraction pattern.

(c) 100 μm pinhole diffraction pattern.



(d) 5 μm pinhole, 40 mw 100 ns laser pulse.

(e) 25 μm pinhole, 8mw 100 ns laser pulse.

(f) 100 μm pinhole, 0.2mw 100ns laser pulse.

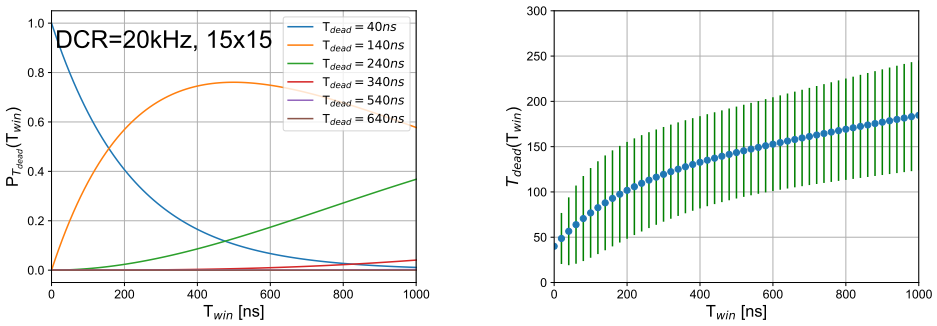
Figure 5.6 Pinhole diffraction patterns simulated with normalization ((a), (b) and (c)) and captured count without normalization ((d), (e) and (f)) at a total integration time of 100 μs (100 ns × 1000 frames).

5.2.3 Calculation about T_{dead} and Temporal Aperture Ratio

For this sensor, before the starting of each frame, one cycle for resetting all the DFFs is needed, so that T_{dead} is,

$$T_{dead} = T_{CLK} + T_{readout} = T_{CLK} \times (2 + 5 \times Max(N_{BD,i})) \tag{5.8}$$

Base on the calculation results about the probability distribution of Max($N_{BD,i}$) in Chapter 4 section 2, the probability of T_{dead} as a function of T_{win} is shown in Fig. 5.7(a) when the chip is operated at 50 MHz. The DCR used in this plot is 20 kHz, which is the measured mean DCR value of the imager. The expected value and standard deviation are calculated derived from the probability distribution, and the calculation results are plotted in Fig. 5.7(b). Fig. 5.8 illustrates the relationship between the temporal aperture ratio (TAR) and T_{win} of this sensor



(a) (b)

Figure 5.7 (a) Probability distribution of T_{dead} at different T_{win}; (b) Excepted value of T_{dead} at different T_{win}.

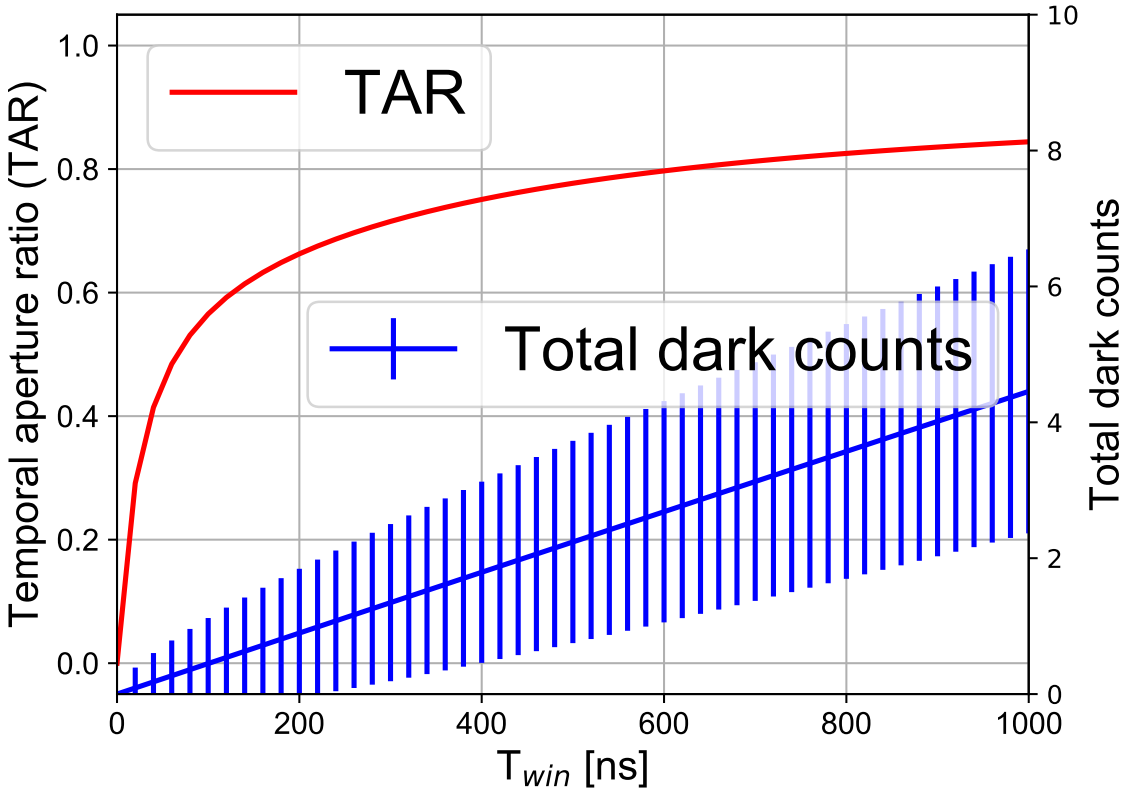


Figure 5.8 Relationship between TAR and T_{win} under dark conditions.

under dark condition comparing with the number of breakdown pixels over the chip, where

$$TAR = \frac{T_{win}}{T_{dead} + T_{win}} \tag{5.9}$$

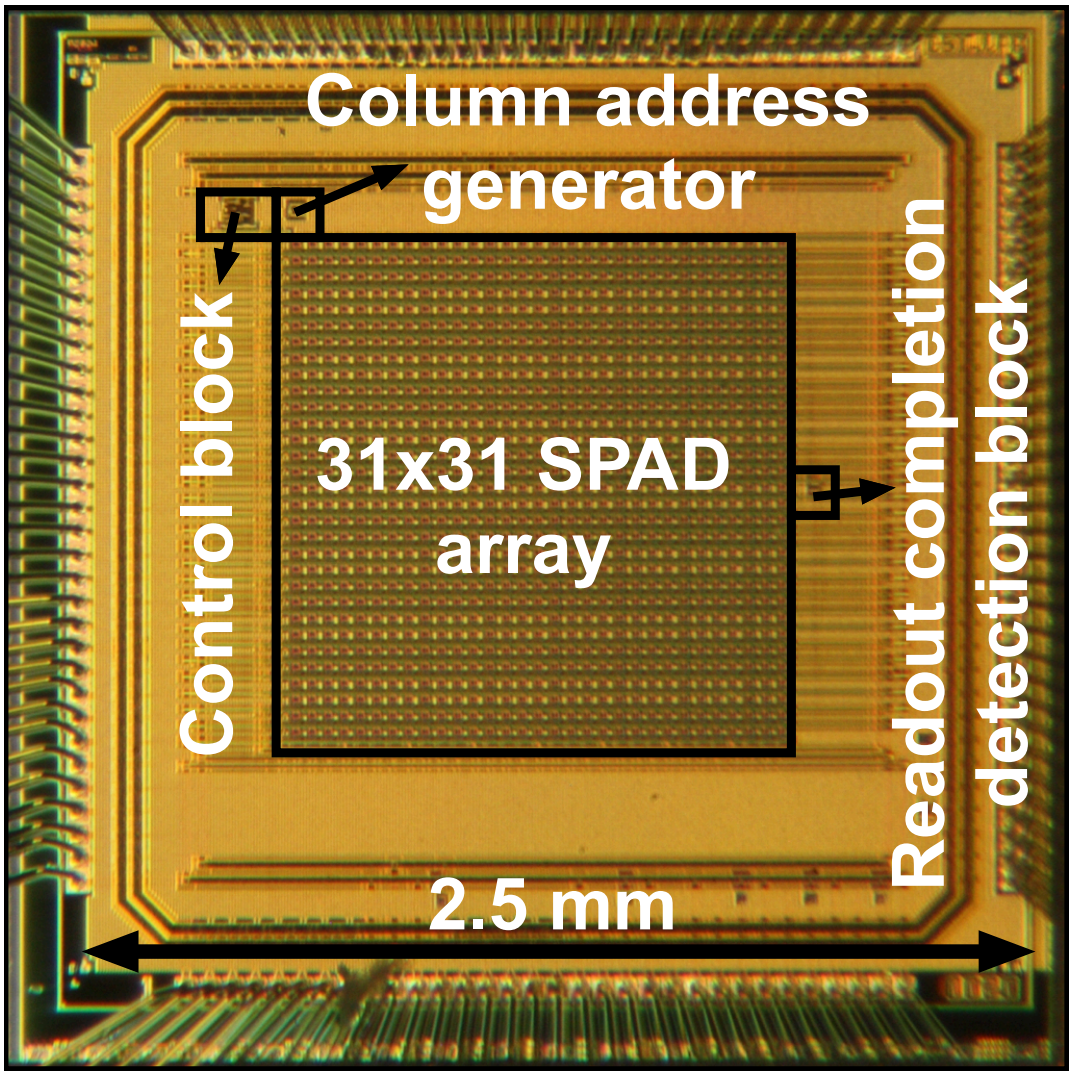


Figure 5.9 Probability distribution of T_{dead} at different T_{win}.

5.3 Experimental Results of the 31×31 SPAD Imager with Background Readout Method

Fig. 5.9 shows a chip photomicrograph of the 31×31 SPAD imager based on BPE architecture with background readout. According to the analysis in Chapter 4, the maximum clock frequency depends on the propagation delay of search signals. The worst case is that there is no breakdown pixel in a row, and the search signal has to be propagated along all the pixels

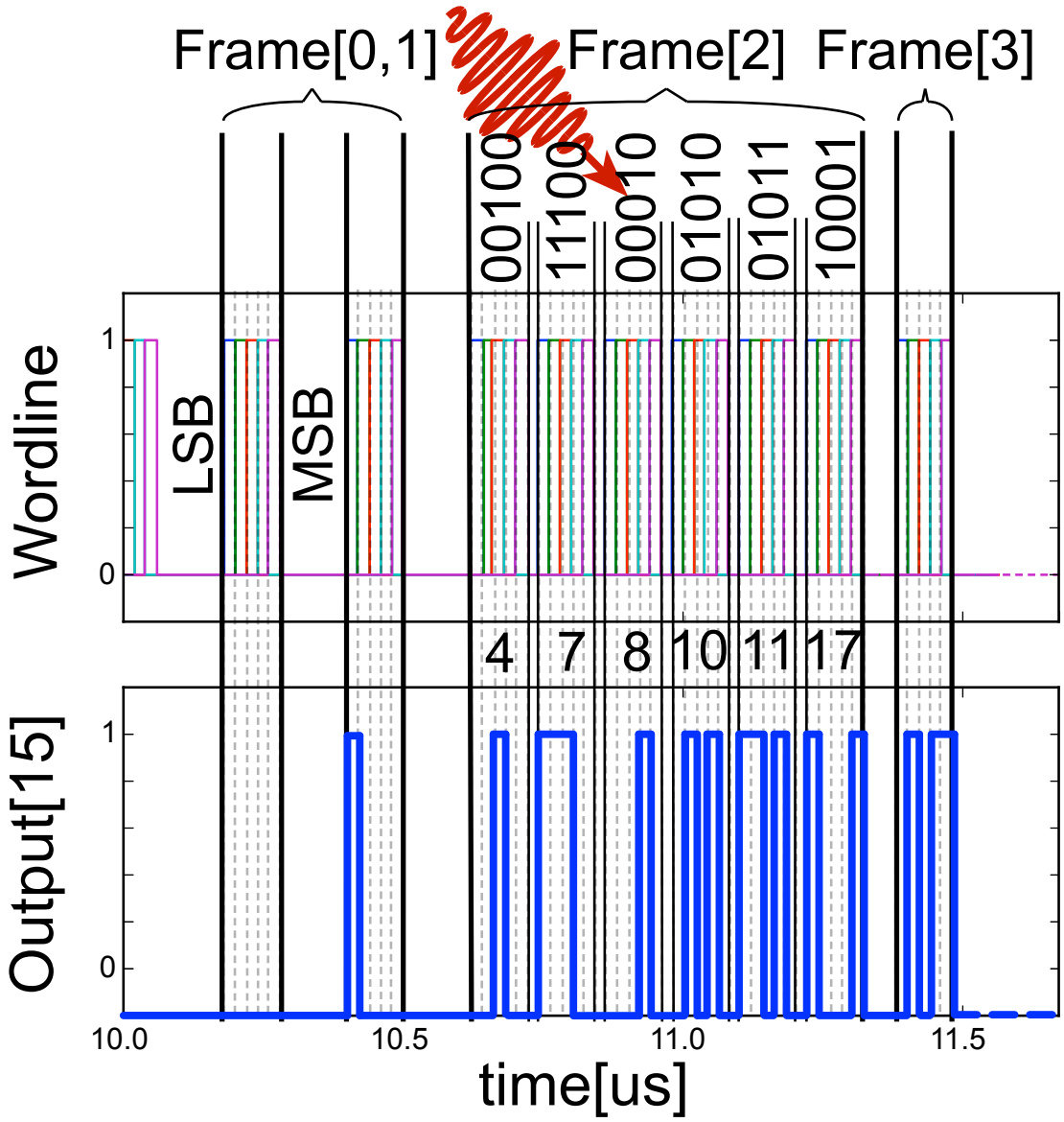


Figure 5.10 Measured output waveforms.

in this row. The post-layout simulation result of such case shows that the time difference between the leftmost search signal and the rightmost search signal is 8.1 ns. Therefore, the maximum clock frequency for this chip is about 120 MHz.

5.3.1 Pulsed Laser Detection

A pulsed laser with 100 ns pulse width was used as the light source to emulate the random event. The measurement setup is the same with the previous chip, and the chip was operated

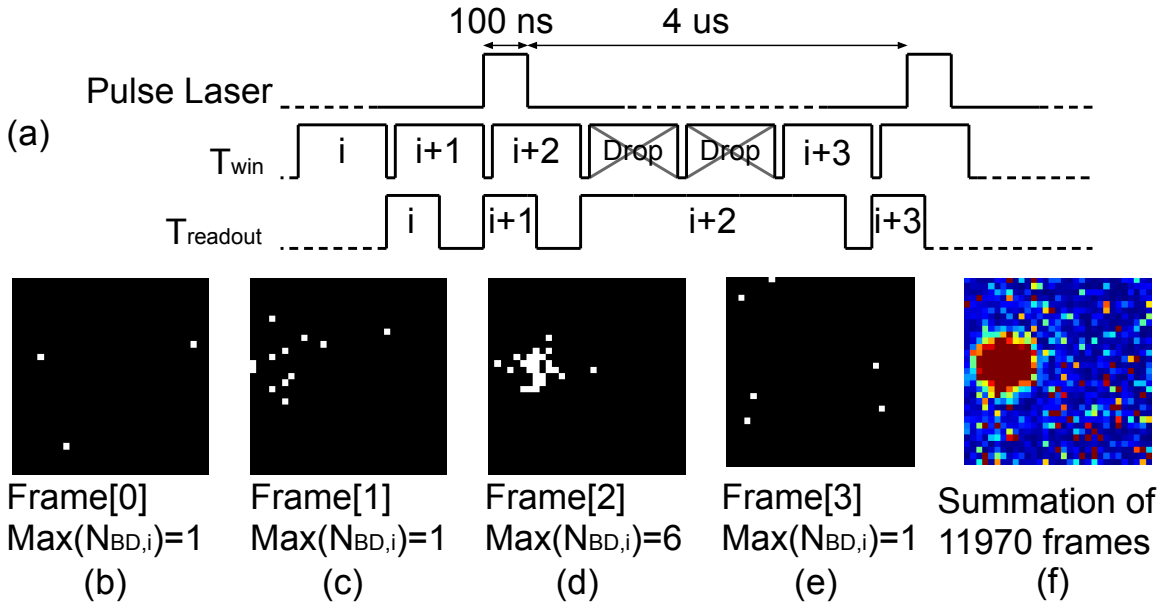


Figure 5.11 Captured images.

at 50 MHz, T_{win} was set at 200 ns. In order to reduce the number of incident photons, a pinhole with a diameter of 25 μm was placed in front of the chip.

Fig. 5.10 shows the measured output waveforms, the blue line is the readout addresses of the 16-th row, and totally 4 frames were recorded. Fig. 5.11(a) illustrates the timing diagram during this measurement period, and Fig. 5.11(b)-(e) show the images of captured frames.

For the first frame 'Frame[0]', the signal had kept low indicating that there was no breakdown pixel in this row. However, there are some breakdown pixels in the other rows and Max($N_{BD,i}$) is 1 as shown in Fig. 5.11(b). Thus, the first frame's Max($N_{BD,i}$) satisfies the requirement of safety zone according to the analysis results in chapter 4, and T_{dead} is minimized to 60 ns (3 clock cycles).

For the 'Frame[1]', the output was '00001' that represents only the first pixel of this row was breakdown, this frame's Max($N_{BD,i}$) is also 1, so that T_{dead} is minimized to 60 ns too, and no data had been dropped.

For the third frame, there were 6 breakdown pixels in this row, that implies the existence of many incident photons during T_{win}, and the assembled breakdown pixel because of pinhole diffraction proved this assumption. On the other hand, since Max($N_{BD,i}$) could not satisfy the

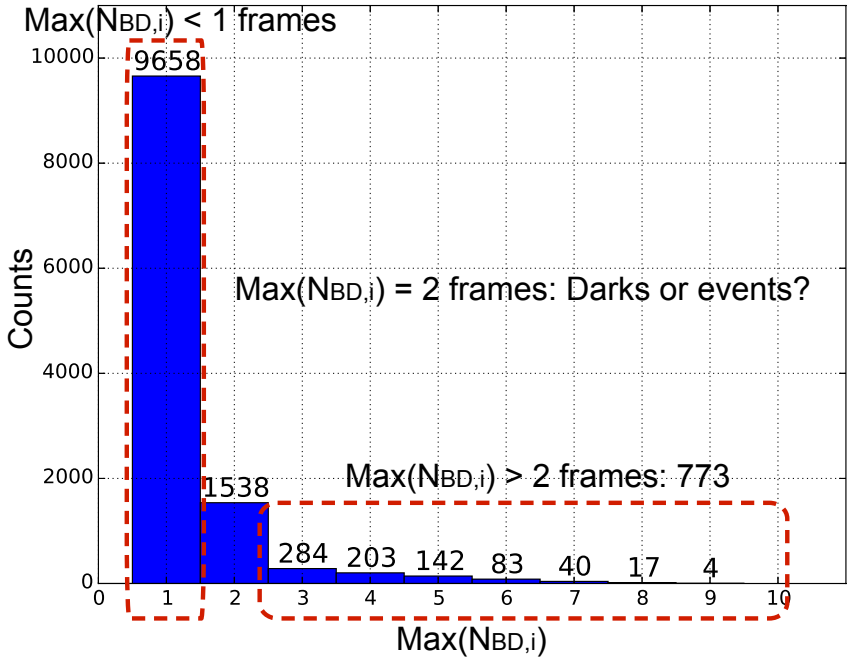


Figure 5.12 Max($N_{BD,i}$) histograms of the captured 11970 frames.

requirement, T_{dead} was 840 ns and 4 frames' data had be dropped. Fig. 5.11(f) shows the summation results of 11970 captured frames in 4 ms with 996 pulsed laser event.

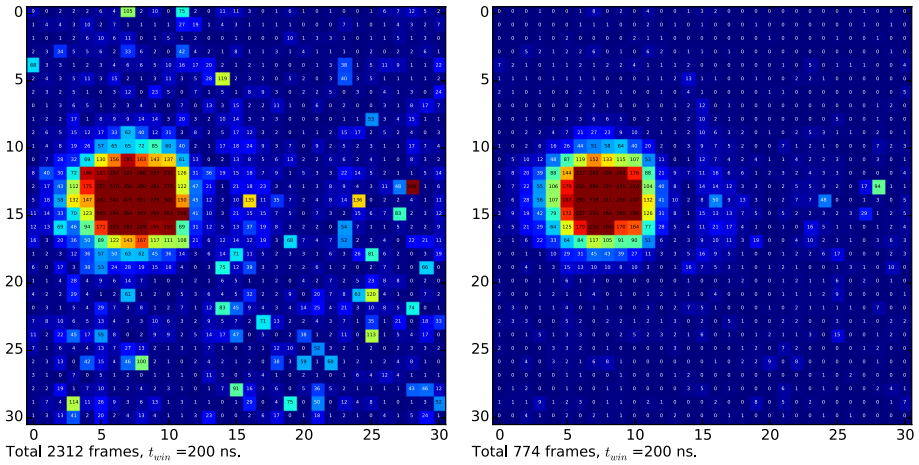


Figure 5.13 (a) Summation of frames that Max($N_{BD,i}$) are larger than 2; (b) Summation of frames that Max($N_{BD,i}$) are larger than 3.

The histograms of Max($N_{BD,i}$) is shown in Fig. 5.12. Among the 11970 captured frames, 773 frames' Max($N_{BD,i}$) are larger than 2, which indicates a high probability of pulsed laser event happened during these frames' T_{win}. For the other frames, there are frames that only contain dark counts, or some frames containing some breakdown pixels caused by incident photons. Fig. 5.13(a) and (b) show the images that only summed the frames that Max($N_{BD,i}$) are larger than 2 or 3, respectively. These clearly diffraction pattern shows the ability of event distinction by counting the value of Max($N_{BD,i}$).

5.3.2 Measurements on DCR Distribution

The DCR distribution of the three types of fabricated sensor with different SPAD sizes were measured and calculated using the same method with the previous chip. For each type of sensor, 3 chips with totally 2883 pixels were measured for each sizes. The detailed measurement results are shown in table 5.1, and the cumulative DCR plots are shown in Fig. 5.14. The same with the introduction in chapter 2, these plots show that most of the pixels have a low DCR, on the other hand, a fraction of SPADs have a very high DCR. It is obviously that a larger SPAD size has a higher DCR.

Table 5.1 Measurement results about DCR.

	Chip1	Chip2	Chip3
Area [μm^2]	144	196	256
Perimeter[μm]	24	28	32
Mean [kHz]	12	19	27
Median [kHz]	2	4	9
Max [kHz]	444	591	966

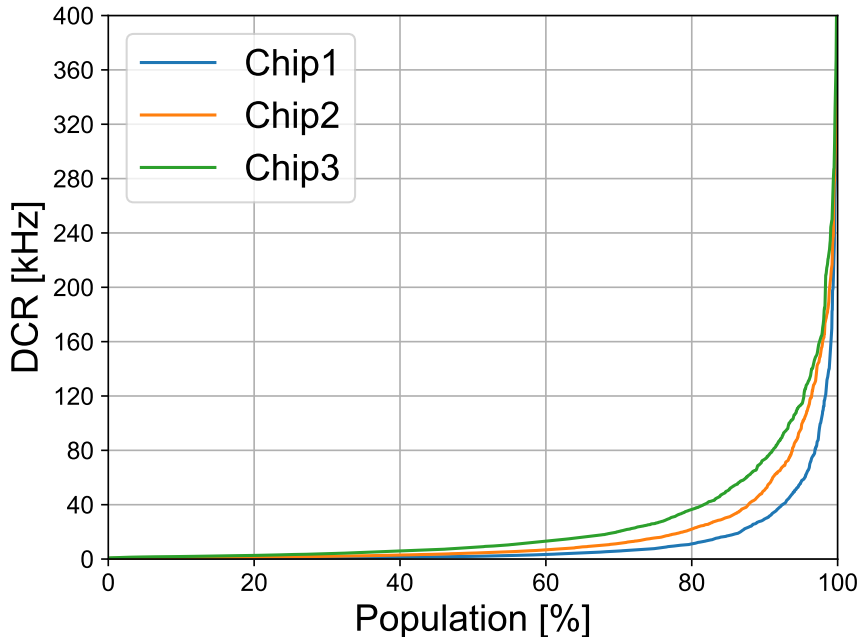


Figure 5.14 Cumulative DCR distributions of the three chips.

5.3.3 Calculation about T_{dead} and TAR

Probability about the safety zone

According to the analysis about T_{dead} in Chapter 4, the largest $Max(N_{BD,i})$ value that can satisfy the requirement of minimized T_{dead} is plotted in Fig. 5.15, and the operation clock is also set at 50 MHz.

The probability that $Max(N_{BD,i})$ is not larger than a threshold value N_{th} is,

$$P_{Max(N_{BD,i}\leq k)}(T_{win}, DCR) = (\sum_{i=0}^{k} P_{N_{dc}=i}(T_{win}))^{M} \tag{5.10}$$

where DCR is 20 kHz, M is 31, and this probability as a function of T_{win} is plotted in Fig. 5.16.

The probability that the frame can be in safety zone can be derived by combining the results in Fig. 5.15 and Fig 5.16 as shown in Fig. 5.17. This plot shows that when T_{win} is larger than 320 ns, the probability that a frame is in the safety zone T_{dead} can be minimized is almost one.

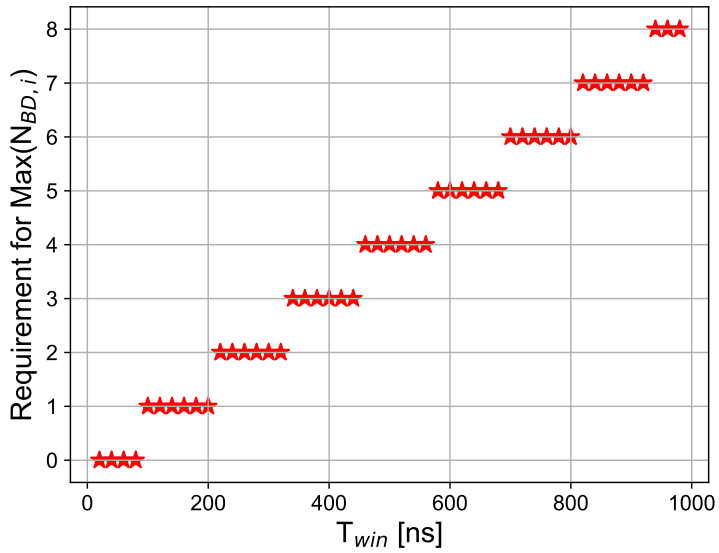


Figure 5.15 Largest Max($N_{BD,i}$) that satisfies the requirement.

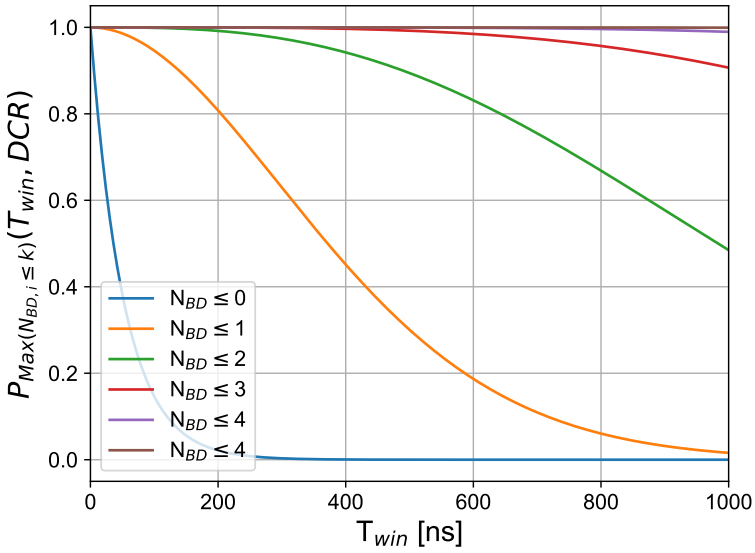


Figure 5.16 $P_{Max(N_{BD,i})} \leq k$ as a function of T_{win}.

Analysis about T_{dead}

Fig. 5.18 shows the relationship between T_{win} and T_{dead} at different Max($N_{BD,i}$). Based this relationship and the probability distribution of Max($N_{BD,i}$) in equation 4.3, the excepted value

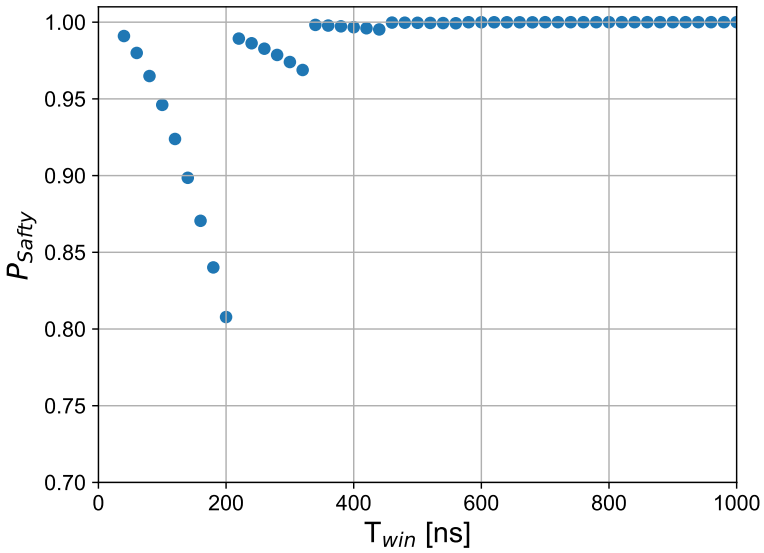


Figure 5.17 Probability for a frame in safety zone at different T_{win}

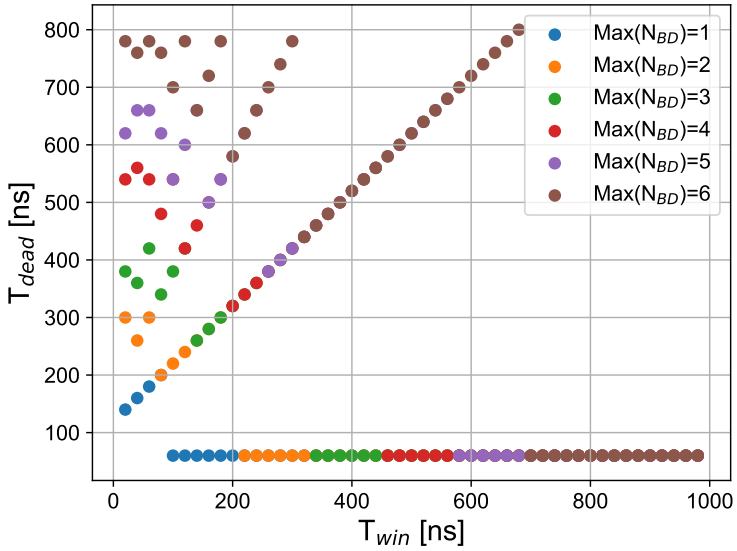


Figure 5.18 T_{dead} at different Max($N_{BD,i}$).

of T_{dead} is plotted in Fig. 5.19, and TAR comparing with the total dark counts are shown in Fig. 5.20. The red line in figure represents the TAR of this method, and the green line is the calculated TAR of the previous chip extended to 31×31 pixels.

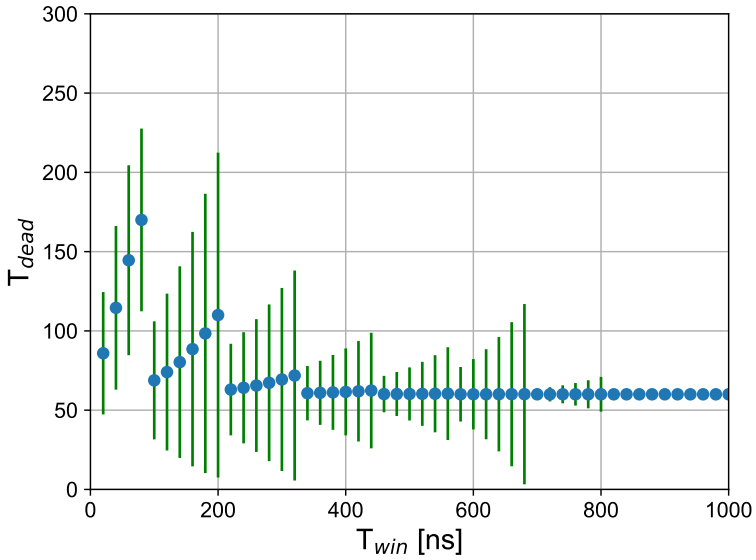


Figure 5.19 Excepted value of T_{dead}.

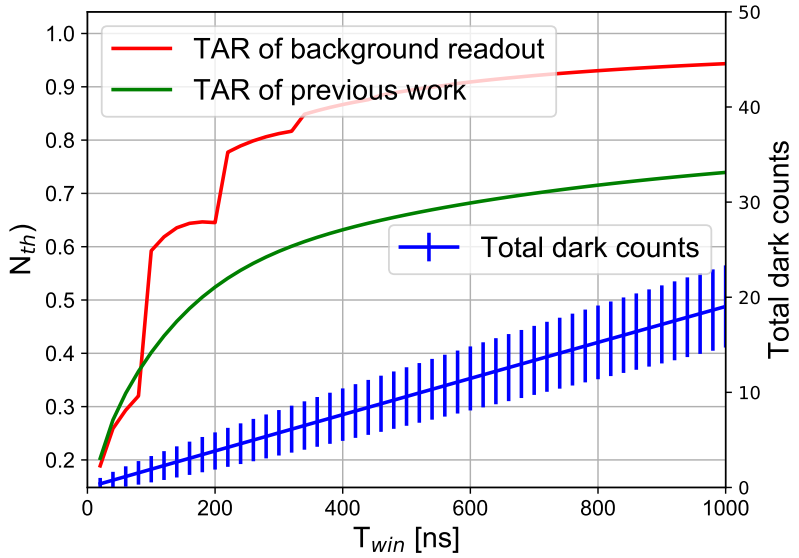


Figure 5.20 Comparison on the excepted TAR with the previous imager.

5.3.4 Measurements about Photon Detection Efficiency

The PDE of the SPAD was measured through pinhole imaging with this imager. Supposing that N_{ph} is the number of photons incident into a SPAD, and the probability that dark counts

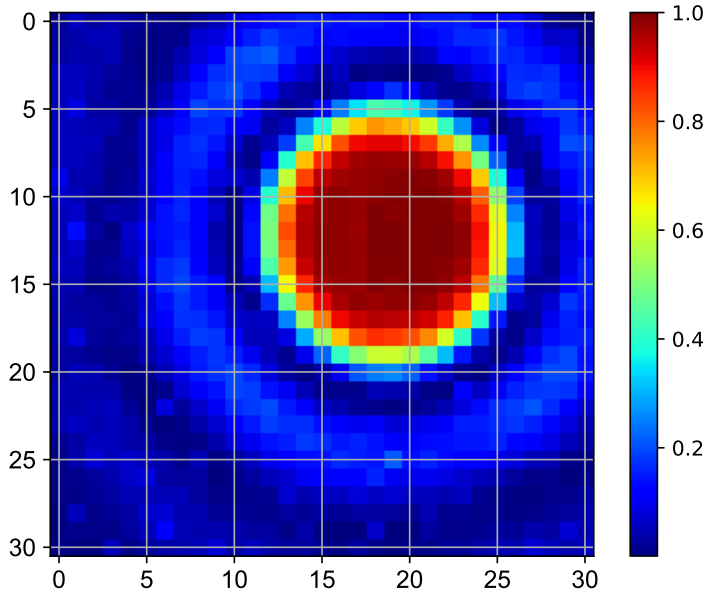


Figure 5.21 Measured P_{BD} mapping.

happens during a measurement is P_{DC}, the probability that the SPAD is breakdown P_{BD} is:

$$P_{BD} = 1 - (1 - PDE)^{N_{ph}} \times (1 - P_{DC}) \tag{5.11}$$

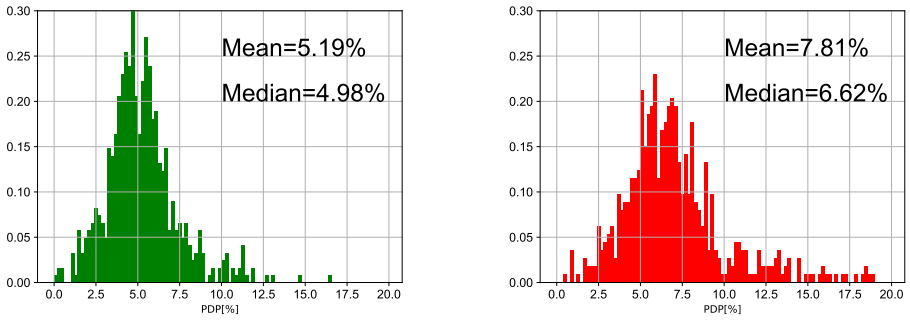
Therefore, PDE is:

$$PDE = 1 - \frac{(1 - P_{BD})^{\frac{1}{N_{ph}}}}{(1 - P_{DC})} \tag{5.12}$$

where, the value of N_{ph} is calculated from the pinhole diffraction pattern and the energy of pulsed laser, P_{DC} is calculated from the measured DCR distribution, and P_{BD} is calculated from the measured counts of pinhole imaging as shown in Fig. 5.21.

$$P_{BD} = \frac{\text{Counts}}{\text{Total number of measured frames}} \tag{5.13}$$

Fig. 5.22(a) and (b) shows the calculated PDE distribution over the chip when the SPAD is over biased at 1.4 V and 1.8 V respectively.



(a) (b)

Figure 5.22 (a) Calculated PDE when V_{SPAD} is -27 V; (b) Calculated PDE when V_{SPAD} is -27.4 V.

5.4 Measurements about 31×31 SPAD Imager with Event Discriminator Based on BPE Architecture

5.4.1 Pulsed Laser Imaging

Fig. 5.23 shows a chip photomicrograph of the 31×31 SPAD imager with event discriminator based on BPE architecture. The experimental setup to test the chip's functionality is the same with the previous chip too. Fig. 5.24 shows the measured output waveforms, when the chip was operated at 50 MHz, pulse width of laser is 20 ns, a 50 μ m pinhole was positioned in front of the chip, T_{win} was set at 200 ns, and N_{th} was set a 4. Based on the analysis about the Max($N_{BD,i}$) in previous section, the probability that Max($N_{BD,i}$) is larger than N_{th} is smaller than 0.01% as shown in Fig. 5.15.

For each test, the measurement period was 200 μs, pulsed laser was activated at 100 μs as shown in the blue line in Fig. 5.24. The red line is 'Search' signal to show the beginning of counting procedure, green line is 'Out_state' that represents the beginning of readout procedure, and black line is 'Address_Output'. Totally 795 frames were captured during the 200 μs, and only one frames was readout because of that frame's Max($N_{BD,i}$) was larger than N_{th}.

Fig. 5.25 shows the same waveforms focusing on the period of readout procedure. Since the value of Max($N_{BD,i}$) was not larger than N_{th}, no data was readout until the pulsed laser was incident. For the frame that 'Laser' was high during its T_{win}, the measured 'OUT_state'

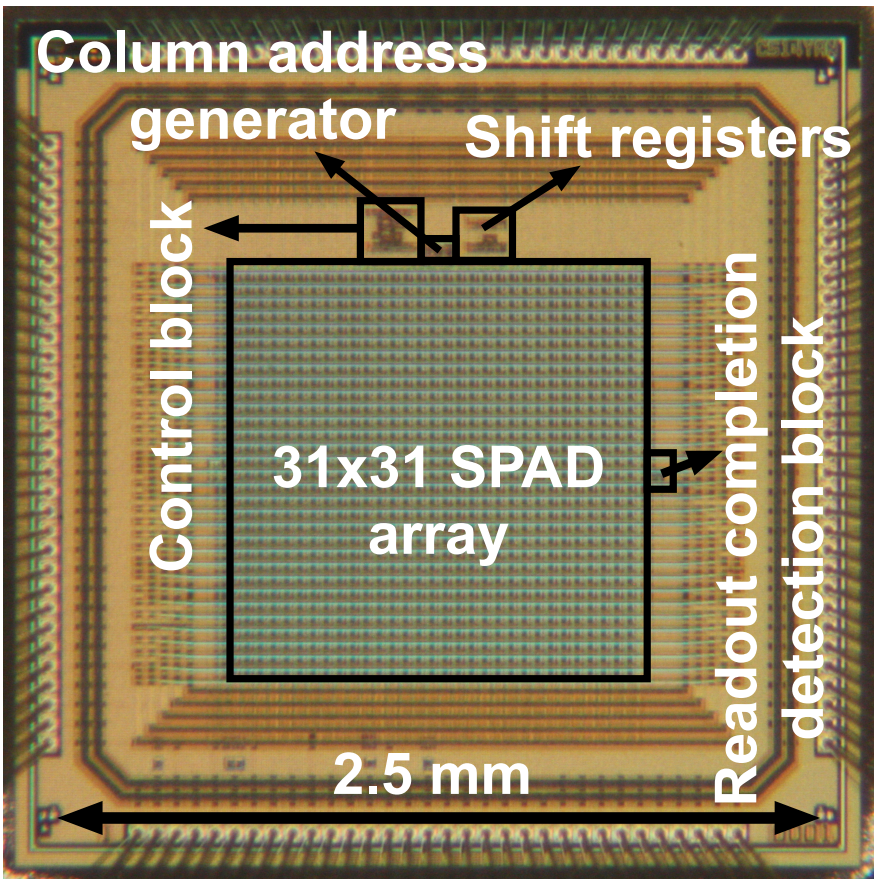


Figure 5.23 Chip photomicrograph of the SPAD imager with Event Discriminator.

went high and this frame's data was readout.

Fig. 5.26 illustrates a summation of the 1000 measured frames, and this diffraction demonstrated the functionality of this imager. Moreover, the noise is also automatically filtered by the reduction of readout frames.

5.4.2 Analysis about the setting of N_{th}

For this imager, T_{dead} can be always minimized to 3 cycles and detect the events efficiently if N_{th} is set appropriately. The appropriate is defined by three requirements:

- Filtering all the dark frames.
- T_{dead} is minimized under dark condition.

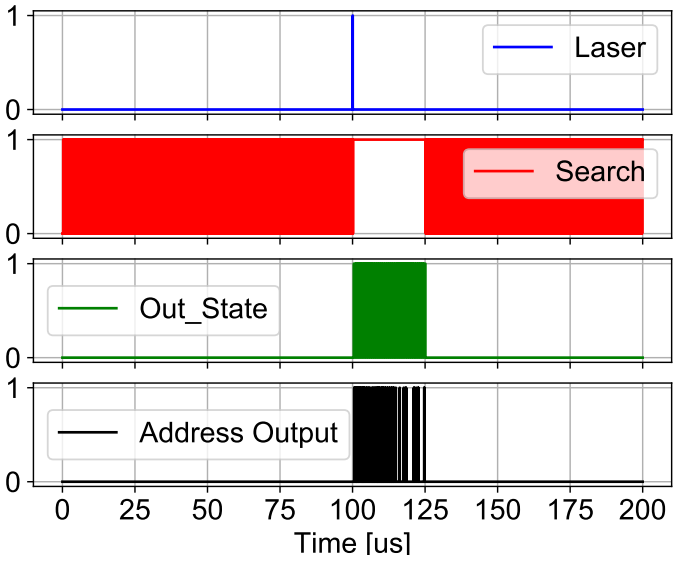


Figure 5.24 Captured waveforms.

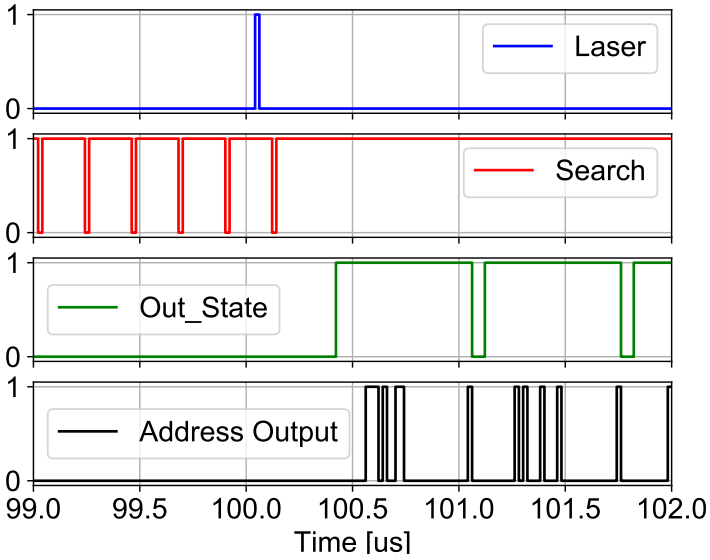


Figure 5.25 Enlarged captured waveforms.

- Detecting events efficiently.

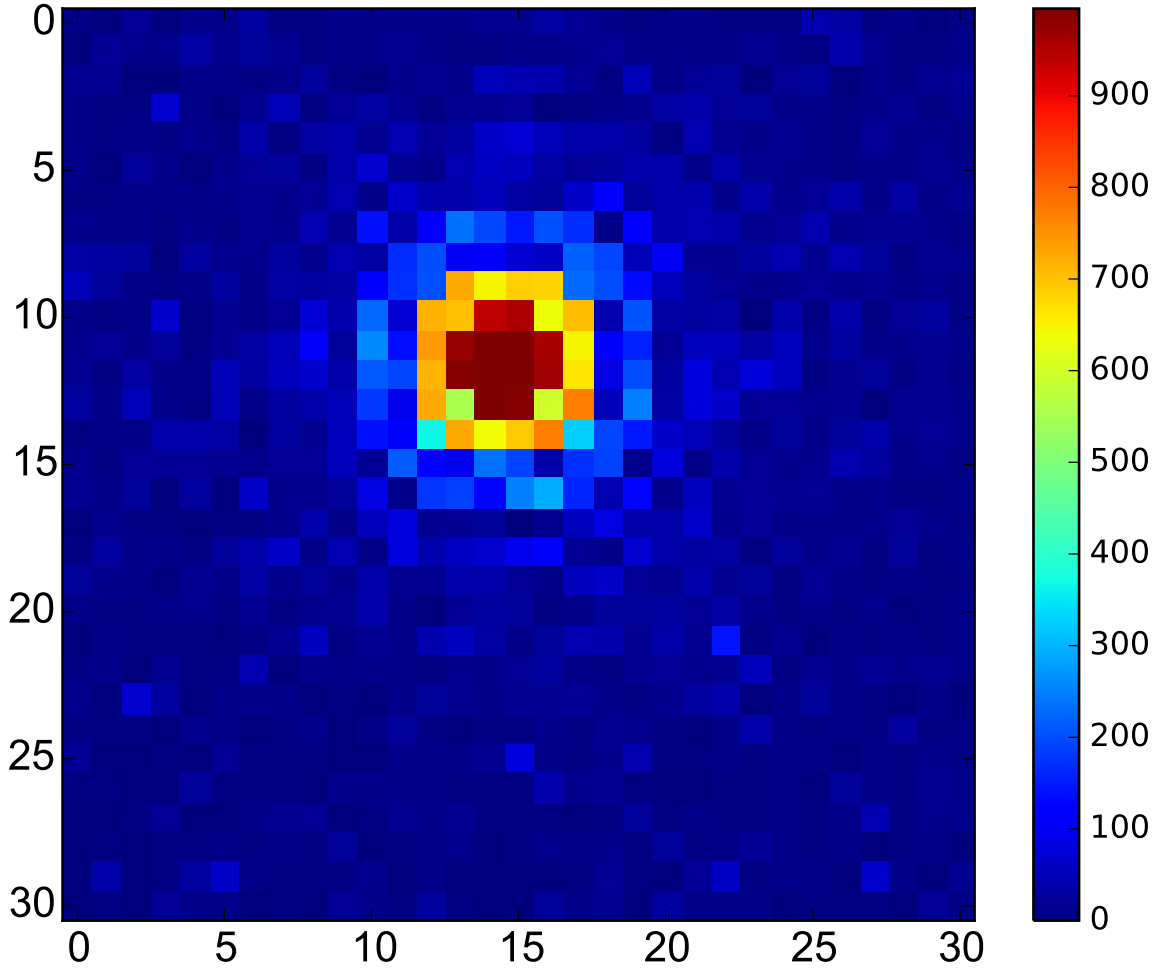


Figure 5.26 Summation of 1000 captured frames.

First requirement: dark frames filtering

The principle of the proposed event discriminator is based on the value of Max($N_{BD,i}$), so that most of the dark frames can be filtered off if N_{th} is high enough. Fig. 5.27 illustrates the minimum value of N_{th} that can filter 99.99% the dark frames. The parameters that relate with the probability distribution of Max($N_{BD,i}$) are the same with the analysis in previous section (CLK=50 MHz, M=31, N=31, and DCR= 20kHz).

Second requirement: minimized T_{dead}

If the counting procedure can be finished before the ending of next frame's T_{win}, T_{dead} can be minimized to 3 cycles. Counting procedure is completed by two cases:

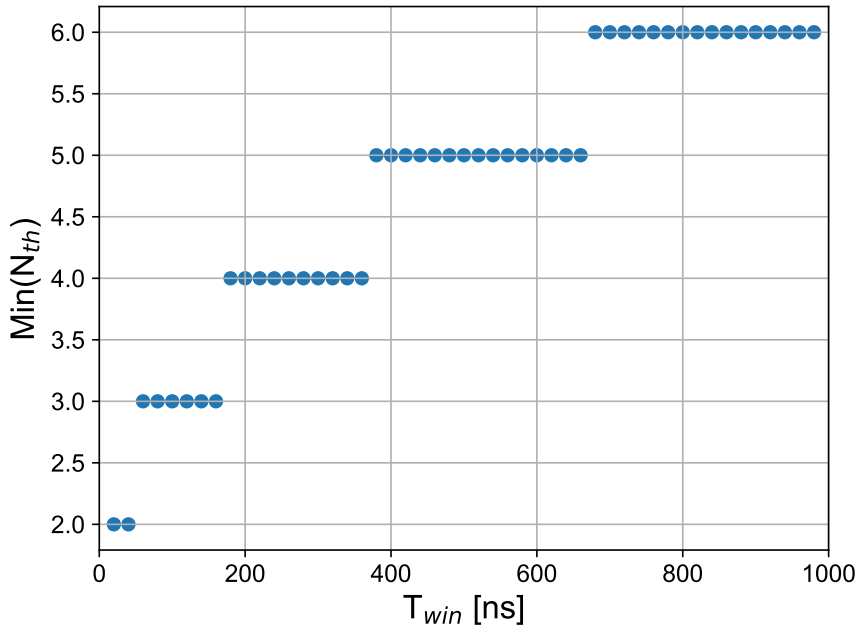


Figure 5.27 Minimum value of N_{th} that can filter 99.99% the dark frames.

- Case 1: Searching procedure is completed and Max($N_{BD,i}$) is not larger than N_{th}.
- Case 2: Max($N_{BD,i}$) becomes larger than N_{th} during the searching procedure.

And the duration of counting procedure (T_{count}) is,

$$\text{Case 1: } T_{count} = T_{CLK} \times (1 + Max(N_{BD,i})) \tag{5.14}$$

$$\text{Case 2: } T_{count} = T_{CLK} \times (1 + N_{th}) \tag{5.15}$$

For the reason that N_{th} must be not smaller than Max($N_{BD,i}$) to satisfy the first requirement, T_{count} discussed in this part is the value of the second case.

$$T_{CLK} \times (1 + N_{th}) \leq 2T_{CLK} + T_{win} \tag{5.16}$$

Fig. 5.28 plots the maximum value of N_{th} that satisfies the second requirement comparing with the minimum value of N_{th} that is calculated in the previous part.

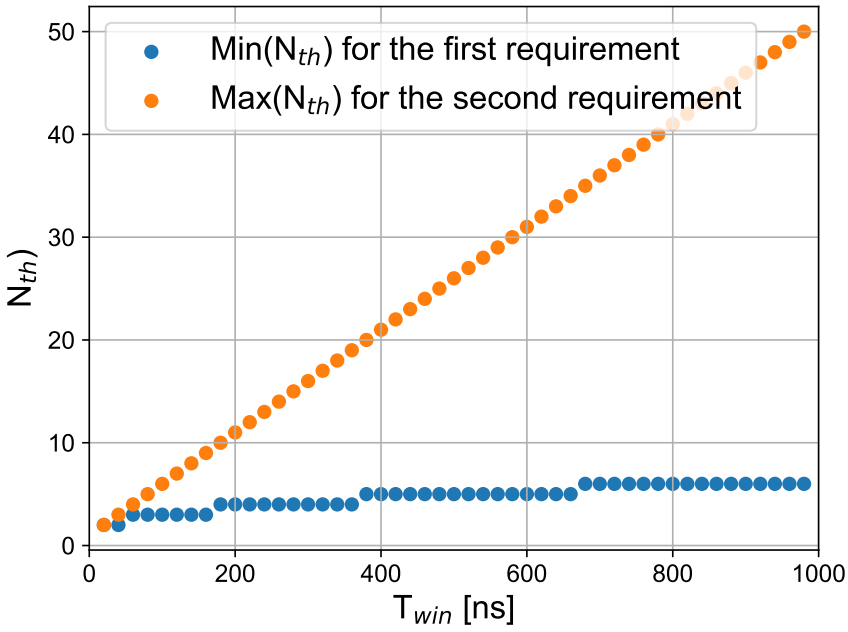


Figure 5.28 Minimum value of N_{th} that can filter 99.99% the dark frames.

Third requirement: event frames distinction

It is difficult to define the efficiency of event distinction since the intensity of incident light varies with applications and measurement conditions. In this part, the total number of incident photons is N_{ph}, and the positions of incident photons are assumed to be randomly distributed over the imager. The fill factor of the imager is 9.0 %, DCR is 20 kHz and PDE is 8 % based on the measurement results of previous section. The breakdown probability for a pixel is:

$$P_{BD} = 1 - (1 - P_{DC}) \times (1 - PDE)^{\frac{N_{ph} \times FF}{961}} \tag{5.17}$$

the probability that number of breakdown pixels is N_{BD} in a row ($P_{N_{BD}}$) is

$$P_{N_{BD}} = \binom{31}{N_{BD}} \times (1 - P_{BD})^{(31-N_{BD})} \times P_{BD}^{N_{BD}} \tag{5.18}$$

so that, the probability for Max($N_{BD,i}$)¿k is:

$$P_{Max(N_{BD,i})>k} = 1 - (\sum_{i=0}^{k} P_{N_{BD}=i})^{31} \tag{5.19}$$

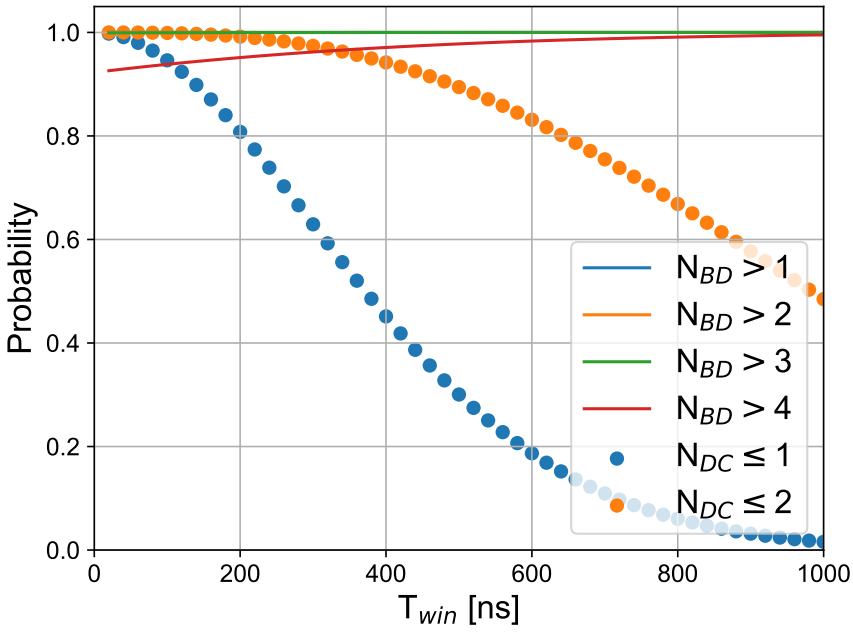


Figure 5.29 A comparison about the Max($N_{BD,i}$) with 10,000 incident photos and under dark condition.

Fig. 5.29 shows a comparison about the value of Max($N_{BD,i}$) with 10,000 incident photos (the solid line) and under dark condition (the dots). According to this figure, both the probability that N_{BD} is larger than 3 and the probability that N_{DC} is not larger than 2 is almost 1 when T_{win} is about 200 ns. Moreover, 3 is also the appropriate value for the N_{th} as shown in Fig. 5.28.

5.5 Summary

This chapter presented the experimental results of the three designed imagers.

For the first designed sensor with 15×15 SPAD array, the functionality of BPE readout method has been experimentally demonstrated. Then, the DCR distribution has been measured, and the median value, mean value, are 10 kHz, 20 kHz, respectively. Based on the measured DCR, an analysis about the temporal aperture ratio (TAR) has been shown.

For the second imager that contains 31×31 SPAD array with background readout method

based on BPE architecture, the ability of random event detection has been shown by pulsed laser imaging at first. Then, measurements about the DCR distributions of the images with different SPAD sizes have been shown. Furthermore, an analysis about the requirements that can minimize T_{dead} has been presented, and TAR as function of T_{win} has been shown comparing with the first imager. A 40% improvement of TAR has been shown based on the calculated results. Finally, Photon detection efficiency of designed SPAD has been measured.

For the third imager that employed an event discriminator based on BPE architecture, the functionality of this sensor has been measured using the same method as the previous one. Then, an analysis about the setting of threshold value has been shown.

Chapter 6

SPAD Imager with Real-Time Current Logic Event Dircriminator

6.1 Introduction

This chapter shows a sensor architecture with real time event discriminator. It employs a current logic to monitor the number of breakdown pixels in real time. A 32×32 SPAD imager with the architecture is shown together with the experimental results.

6.2 Idea of SPAD Imager with Current Logic Event Discriminator

The drawback of the imagers designed in the previous chapter is that there is still a certain T_{dead} of 3 clock cycles due to the global charging, writing, and holding off procedures.

In this chapter, a T_{dead} free architecture with current logic based event discriminator is introduced. The idea of the proposed imager is shown in Fig. 6.1. Instead of the time gated mode, the SPADs are in free-running mode to achieve zero T_{dead}. There is a hold-off time after each breakdown in order to reduce the influence of after-pulsing as well as to realize the current logic based event discriminator. The output of quenching circuit is connected to a current source cell, and a current is generated during the period when SPAD is 'OFF'. All the current cells in each pixel are connected together, so that the value of the current sum are proportion to the number of breakdown pixels as shown in Fig. 6.1. If event happens and the photons that incident into the imagers can trigger many SPADs breakdown, so that the sum will become larger than a threshold value. Then, 'CMP_out' rises up to start the readout procedure.

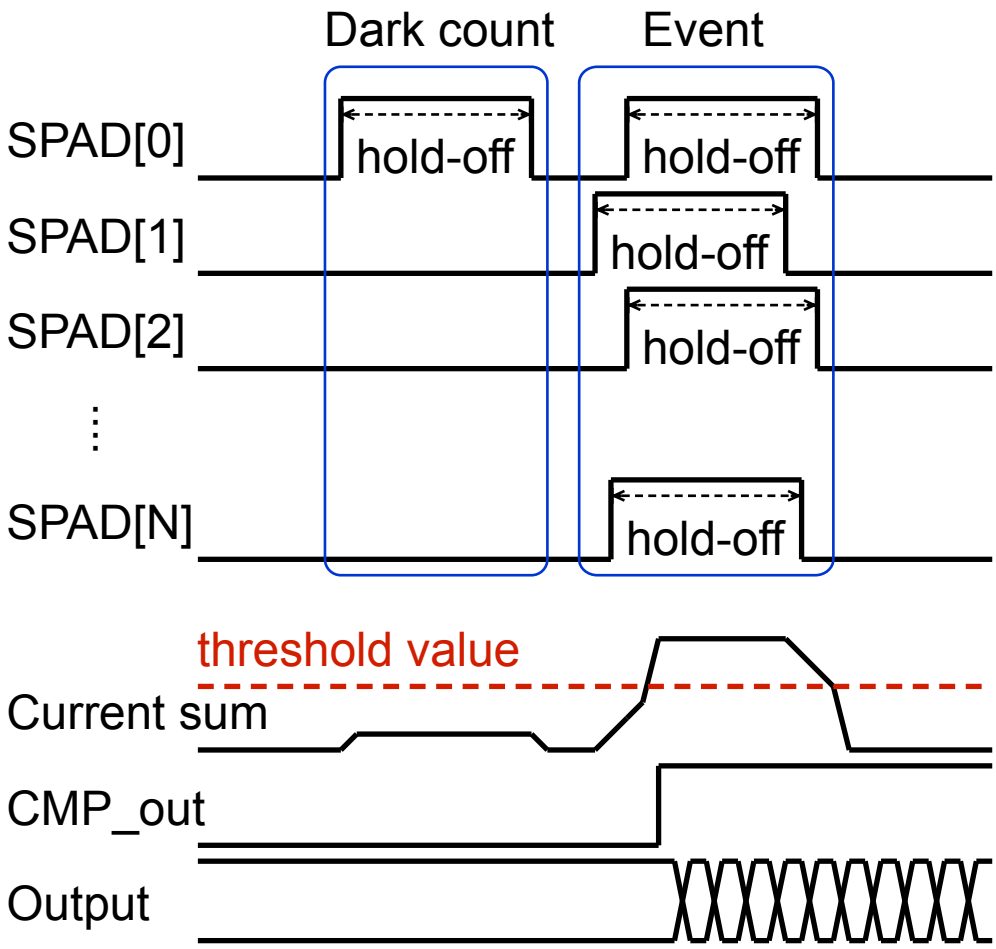


Figure 6.1 Idea of the proposed imager with current logic event discriminator.

A test-of-concept chip was developed with a 32×32 SPAD array imager using the same processes to verify the functionality of this proposed idea.

6.3 Design of SPAD Imager with Real Time Current Logic Based Event Discriminator

Fig. 6.2 illustrates the architecture of the designed imager. It contains a 32×32 SPAD array, a control block generating the control signals, a 6-b DAC to generate the threshold value in chip (V_ref), a comparator comparing 'V_ref' with the current logic output (V_SPAD), and a

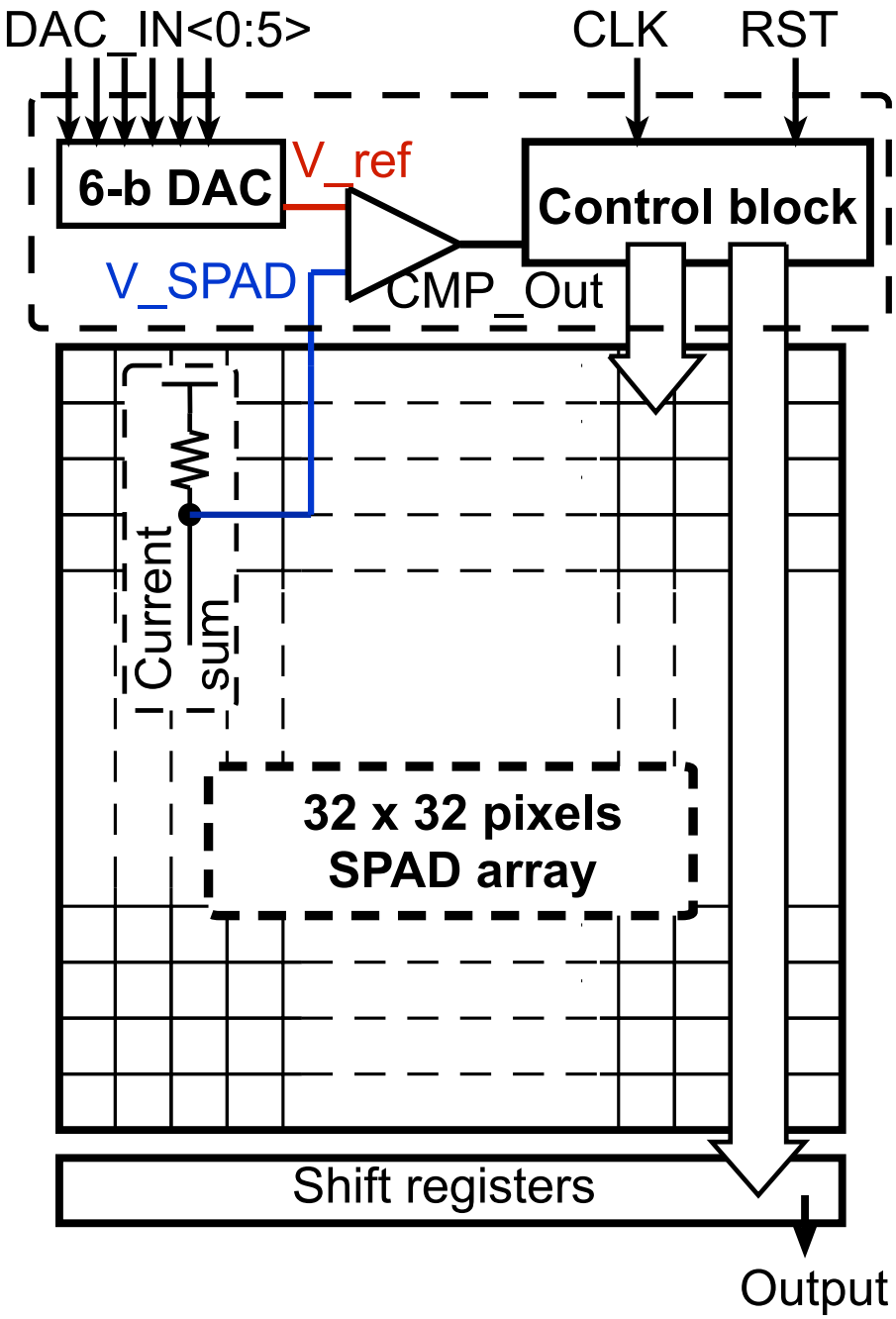


Figure 6.2 Architecture of the proposed sensor.

32-b shift-registers for output.

The readout method utilized in this chip is the conventional raster scan method instead of BPE method for two reasons:

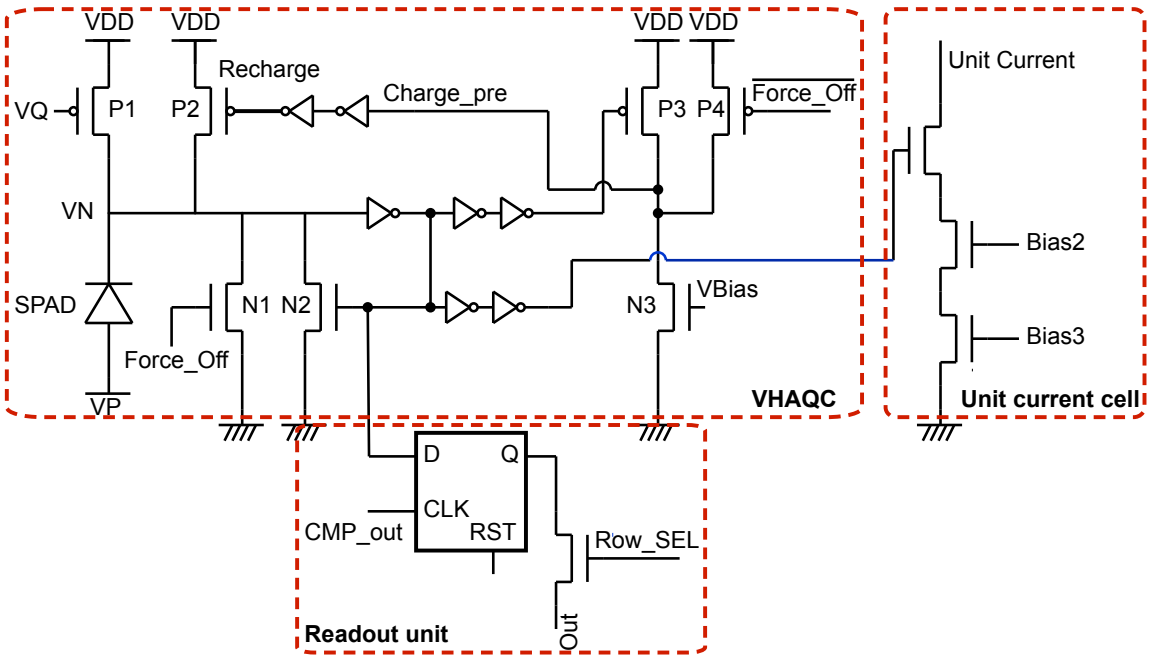


Figure 6.3 Detailed schematic of pixel circuit.

- Simplifying the circuit in pixel to achieve a higher FF.
- High-speed readout is not necessary for this architecture.

6.3.1 Design of Pixel Circuit

Fig. 6.3 shows the detailed schematic design of a pixel circuit. The pixel circuit contains a VHAQC that is the same with the circuit for measuring the after-pulsing probability in Chapter 3, an unit current cell (UCC), and a readout unit. The duration of hold-off time is controlled by the external bias voltage 'VBias'. The value of output current is controlled by the two external bias voltages 'Bias2' and 'Bias3'. The UCC is turned on during the hold-off time, and all UCCs' output are connected together with a resistor as shown in Fig. 6.2 to generate 'V_SPAD'. For the readout unit, the CMP unit's output ('CMP_out') is fed into the 'CLK' of DFF in the unit, so that the SPAD's state is recorded once an event is detected. Then, the data is serially readout through the transistor in readout unit. The layout of a pixel is shown in Fig. 6.4 (a), the area is 42 μm×42 μm with a fill factor about 10.4%.

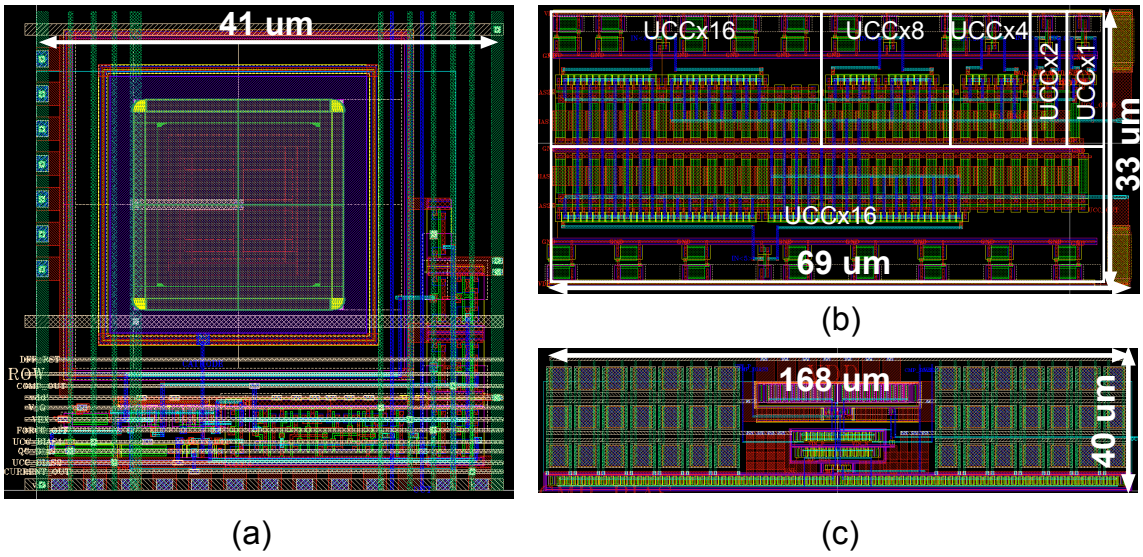


Figure 6.4 (a) Pixel layout; (b) DAC layout; (c) CMP layout.

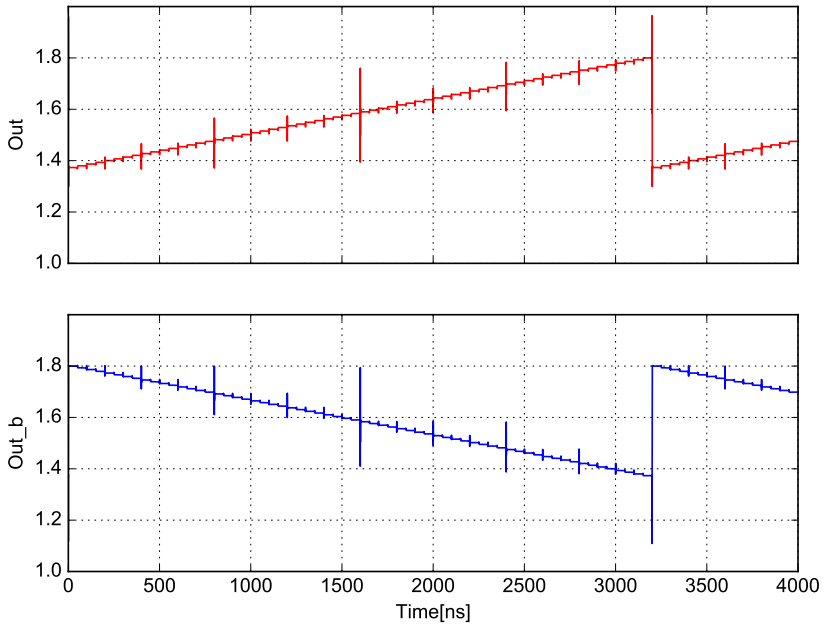


Figure 6.5 DAC simulation.

6.3.2 Peripheral Circuits

Digital-to-analog converter

The 6-b digital-to-analog converter (DAC) in the imager is used to generate the reference voltage for the comparator. The same unit current cell in pixel circuit is utilized in the DAC,

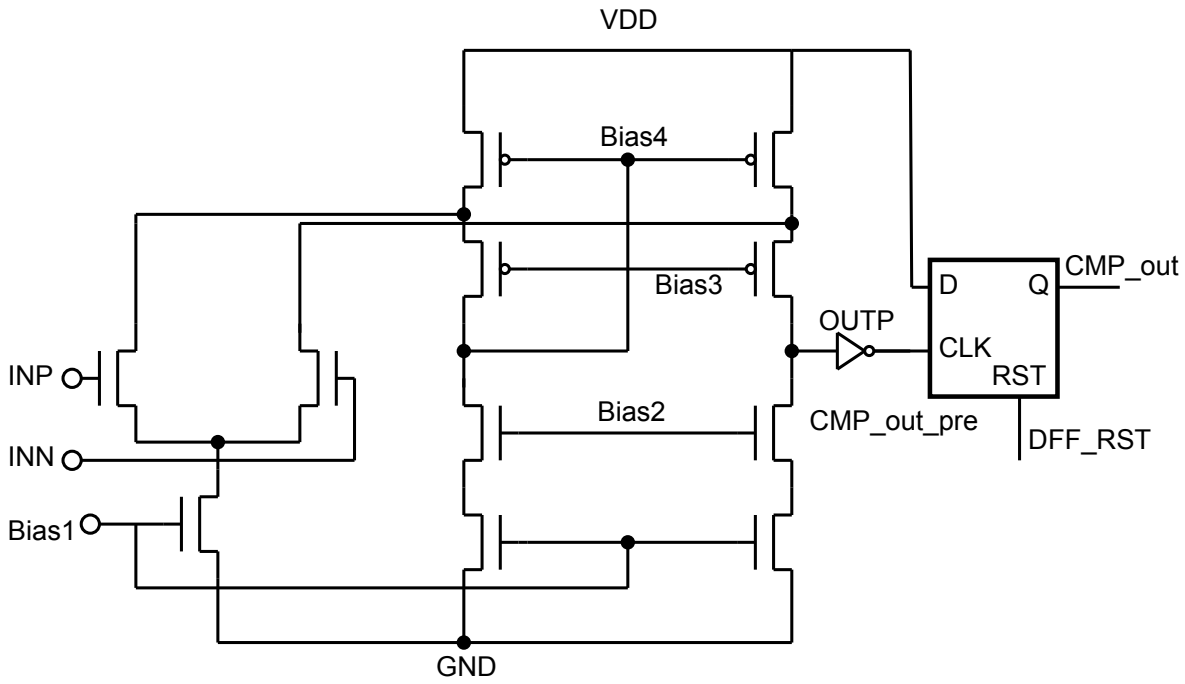


Figure 6.6 Schematic of comparator.

and the layout is shown in Fig. 6.4(b). The simulation result is shown in Fig. 6.5

Comparator

Fig. 6.6 shows the schematic of comparator. A folded cascade comparator is used in the imager for the reason that both V_ref and V_SPAD are near to VDD. The reverted output of comparator ('CMP_out_pre') is connected to the 'CLK' port a DFF in order to prevent the signal falls back during the readout and global recharging procedures. The layout of this circuit is shown in Fig. 6.4(c).

6.3.3 Timing Diagram

Fig. 6.7 shows the timing diagram of the proposed sensor. 'V_SPAD' is the output of current summing circuit as shown in Fig. 6.2. 'V_ref' is the output of DAC, which is controlled by the 6-b external inputs. 'CMP_out_pre' is the internal signal of CMP unit as shown in Fig. 6.6. 'CMP_out' is the output of CMP unit that represents the comparison result of 'V_ref'

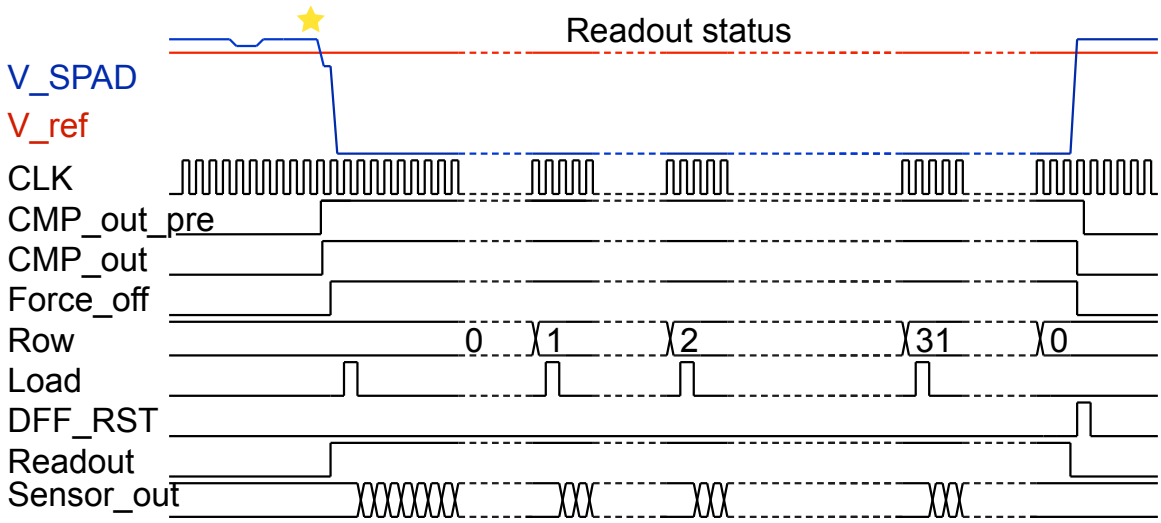


Figure 6.7 Imager timing diagram.

and 'V_SPAD', and rises up when 'V_SPAD' becomes lower than 'V_ref'.

'Force_off', 5-b 'Row', 'Load', 'DFF_RST' and 'Readout' are the control signals generated by the control block. 'Force_off' goes high at the rise edge of a CLK signal when 'CMP_out' is high to hold the SPADs 'OFF', and falls down when readout procedure is completed to restart the global recharging. The 5-b 'Row' signals represent the selected row during readout procedure. 'Load' rises up at the beginning of each row's readout to write the pixels data into shift registers for sensor output. 'DFF_RST' is the global reset signal that is triggered by the finish of readout procedure or the external reset signal. 'Readout' represents the readout state that keeps high during the readout procedure.

All the control signals are kept stable when 'CMP_out' is low, which represents the number of breakdown pixels in a period of hold-off time is small. When event happens and 'CMP_out' falls down, the control block starts to work. At the same time, the states of SPADs are recorded into the registers located in each pixel as shown in Fig. 6.3. At the rising edge of the next clock, 'Force_off' rises up to hold all SPADs 'OFF', and the readout procedure is triggered and 'Readout' goes high. Then, 'Load' goes high to write the first row's data into shift-registers, and the data is shifted out of the chip through 'Sensor_out'. After all the 32 bits data has been shifted out, the value of 'Row' becomes 1, and 'Load' rises up again to

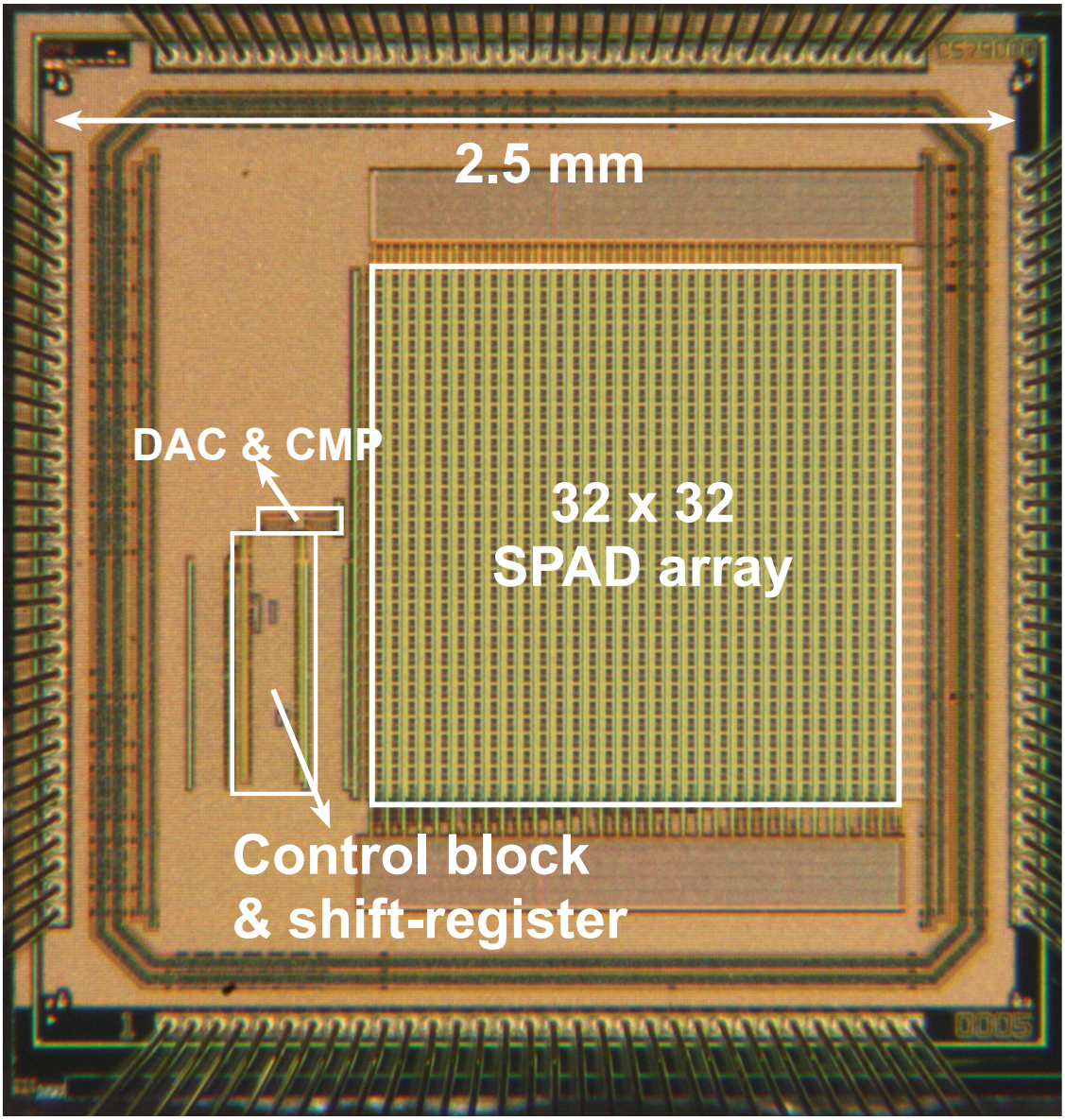


Figure 6.8 Chip photomicrograph of the imager.

write the second row's data. These processes are repeated until all the rows' data have been readout. Then, a global 'DFF_RST' pulse signal is triggered to reset the DFF in pixels and CMP unit, so that both 'Force_off' and 'CMP_out' fall down.

6.4 Experimental Results

Fig. 6.8 shows the chip photomicrograph fabricated in the same process. The mesurement setup was the same the previous chip for pulsed laser imaging, the chip was operated at

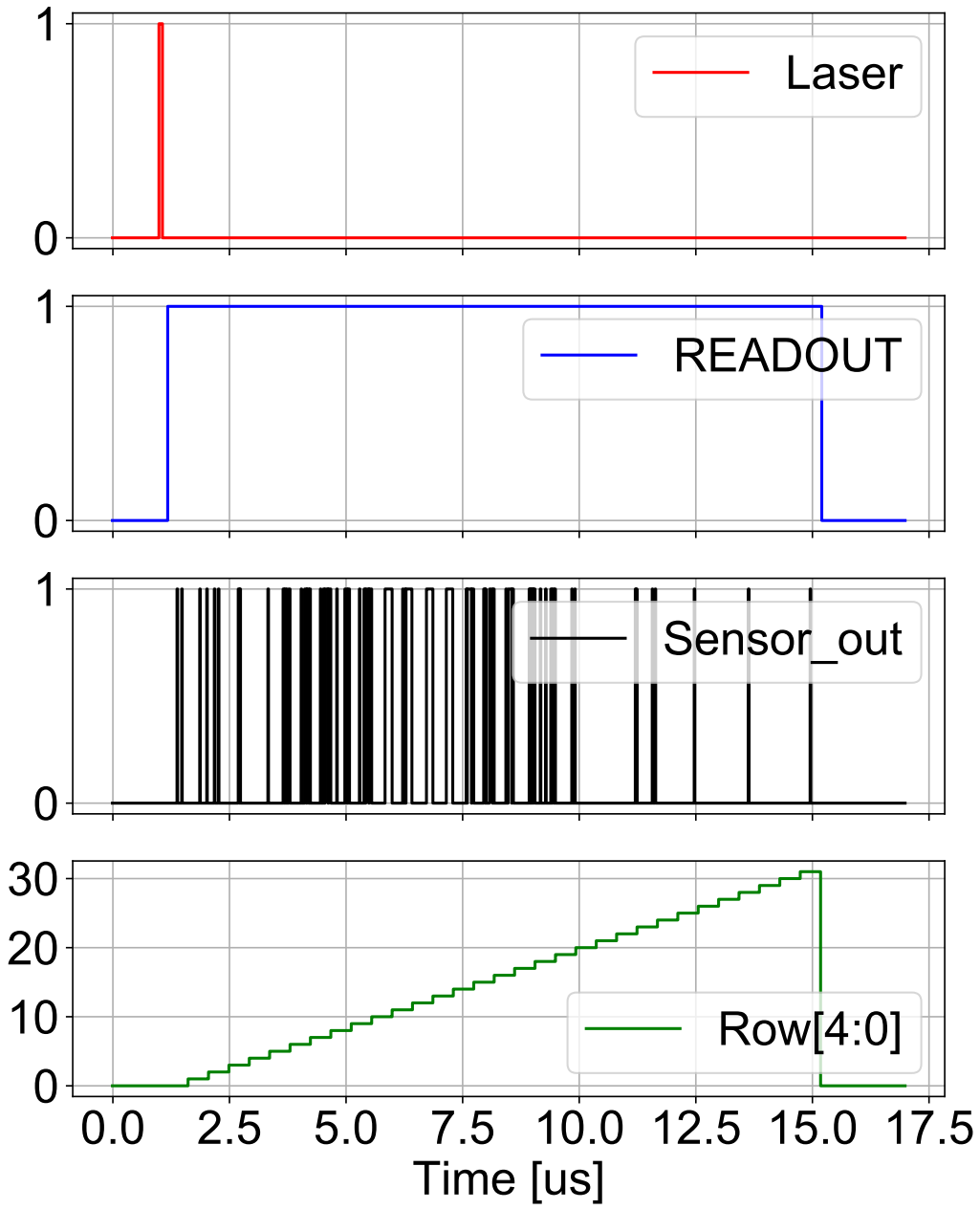


Figure 6.9 Measured waveforems.

80 MHz, the 25 μm pinhole was positioned in front of the chip.

Fig. 6.9 shows the measured waveforms, the red line is the control signal for the pulsed

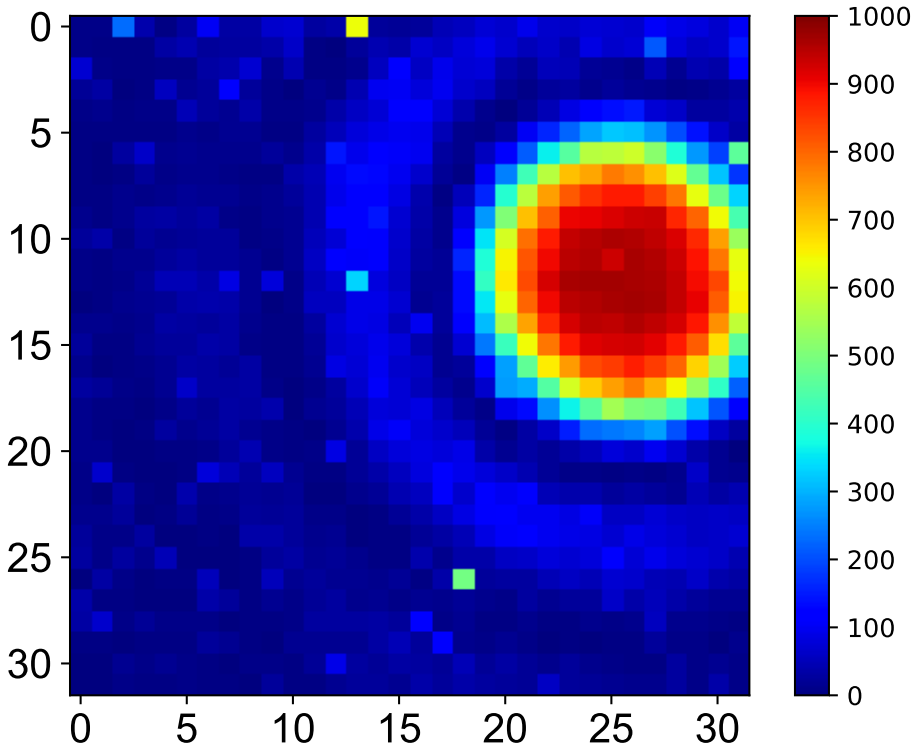


Figure 6.10 Summation of captured frames from 1000 times measurements.

laser, the blue line is 'Readout', the black waveform is 'Sensor_out', and the value of green line (Row[4:0]) represents the row that is under readout procedure.

For each measurment, the pulsed laser was triggered at 1 μs, and the measurement duration is 17 μs. 'Readout' kept low before the triggering of plused laser since there are only a few SPADs under dark conditions, and went high when laser was triggered as shown in Fig. 6.9.

Fig. 6.10 shows a summation of captured frames from 1000 times measurements, and the width of pulsed laser is 62.5 ns. This diffraction pattern demonstrated the functionality of this proposed event discriminator and this prototype imager. However, a further measurements about the performance of the DAC and the comparator are necessary to evaluate the designed imager.

6.5 Summary

We have presented a sensor architecture with real time event discriminator in this chapter. A 32×32 SPAD imager with the architecture has been presented together with the experimental results. This imager employed a current logic to monitor the number of breakdown pixels in real time, and a free-running with variable hold-off time active quenching circuit has been proposed to achieve zero T_{dead}. The ability of random event distinction has been shown through the experimental results.

Chapter 7

Conclusions

This thesis focused on the design of a SPAD in the standard CMOS process, and the design of SPAD imagers. The basic principle and key parameters of a SPAD have been introduced in Chapter 2. Then, structures and experimental results about the designed several types of SPADs have been presented in Chapter 3. From Chapter 4 to Chapter 5, a new sensor architecture with high readout efficient and 3 SPAD imagers utilizing the proposed architecture have been shown. In Chapter 6, a SPAD imager with real-time event discriminator has been introduced.

Chapter 2

This chapter provided an introduction about basic principles and features of SPAD in order to understand the required constraints in designing CMOS SPAD. The breakdown voltage, dark counts rate (DCR) , and photon detection efficiency (PDE) were introduced. According to the introduction, the breakdown voltage of a SPAD should be greater than 15 V in order to suppress the influence of band to band tunneling, and s suitable guard ring is necessary for preventing premature breakdown due to edge effect. Furthermore, an analysis on the influence of DCR and PDE has been shown, and the desirable DCR for the SPAD imager is about 10 kHz.

Chapter 3

This chapter focused on designing and testing about SAPDs that were fabricated by the available standard CMOS process. The detail about the design of SPADs that have been used

for the SPAD imagers in this work were presented in this chapter. The structures of three types of CMOS SPADs have been reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process in order to find a suitable structure of SPADs were introduced.

According to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V. A suitable SPAD of Pwell/DeepNwell with PolyGate around the active region, low DCR with purely avalanche breakdown, and planer breakdown region were confirmed by the experimental results. Then, a test circuit for after-pulsing probability measurement has been presented presented. The experimental results demonstrated the efficiency of hold-off time about reducing the influence of after-pulsing, and the after-pulsing probability can be decreased to lower than 1% with a 20 ns hold-off time.

Chapter 4

This chapter targeted on the efficient readout architecture for SPAD imagers. Since the breakdown SPAD pixels are sparse in many application, an architecture that only extracts the address of breakdown pixels can achieve a higher readout efficiency. A breakdown pixel extraction (BPE) readout architecture has been proposed based on the binary feature of SPADs. The design and behavior of BPE architecture has been introduced at first, and the design of a 15×15 SPAD imager to verify the functionality of the proposed architecture has been presented.

Then, a detail design about the imager with 31×31 pixels utilizing background readout method has been shown. This imager added an additional 1-b memory in each pixel to store the value of the previous frame, and to realize the background readout. This method could minimized T_{dead} to 3 cycles under dark conditions or under sparse breakdown pixels.

Furthermore, another BPE based 31×31 SPAD imager with event discriminator has been proposed for minimizing T_{dead} and event detecting. This imager counted the value of $Max(_{BD,i})$ of each frames at first, and the readout procedure only started when $Max(_{BD,i})$ became larger than a threshold value.

Chapter 5

This chapter presented the experimental results of the three designed imagers.

For the first designed sensor with 15×15 SPAD array, the functionality of BPE readout method has been experimentally demonstrated. Then, the DCR distribution has been measured, and the median value, mean value, are 10 kHz, 20 kHz, respectively. Based on the measured DCR, an analysis about the temporal aperture ratio (TAR) has been shown.

For the second imager that contains 31×31 SPAD array with background readout method based on BPE architecture, the ability of random event detection has been shown by pulsed laser imaging at first. Then, measurements about the DCR distributions of the images with different SPAD sizes have been shown. Furthermore, an analysis about the requirements that can minimize T_{dead} has been presented, and TAR as function of T_{win} has been shown comparing with the first imager. A 40% improvement of TAR has been shown based on the calculated results. Finally, Photon detection efficiency of designed SPAD has been measured.

For the third imager that employed an event discriminator based on BPE architecture, the functionality of this sensor has been measured using the same method as the previous one. Then, an analysis about the setting of threshold value has been shown.

Chapter 6

We have presented a sensor architecture with real time event discriminator in this chapter. A 32×32 SPAD imager with the architecture has been presented together with the experimental results. This imager employed a current logic to monitor the number of breakdown pixels in real time, and a free-running with variable hold-off time active quenching circuit has been proposed to achieve zero T_{dead}. The ability of random event distinction has been shown through the experimental results.

Bibliography

[1] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 x 128 Single-Photon Image Sensor with Column Level 10-bit Time-to-digital Converter Array," *IEEE Journal of Solid State Circuits*, vol. 43, no. 12, pp. 2977–2989, 2008.

[2] C. L. Niclass, A. Rochas, P.-A. Besse, and E. Charbon, "Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1847–1854, 2005.

[3] M. Gersbach, Y. Maruyama, R. Trimananda, M. W. Fishburn, D. Stoppa, J. A. Richardson, R. Walker, R. Henderson, and E. Charbon, "A time-resolved, low-noise single-photon image sensor fabricated in deep-submicron CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1394–1407, 2012.

[4] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, "A 100-m range 10-Frame/s 340 $\times$, 96-pixel time-of-flight depth sensor in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 559–572, 2013.

[5] F. Remondino and D. Stoppa, "TOF range-imaging cameras," *TOF Range-Imaging Cameras*, vol. 9783642275, pp. 1–240, 2013.

[6] C. Niclass, M. Soga, H. Matsubara, M. Ogawa, and M. Kagami, "A 0.18-m cmos soc for a 100-m-range 10-frame/s 200 $\times$ 96-pixel time-of-flight depth sensor," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 1, pp. 315–330, 2014.

[7] M. E. Casey, C. Reynolds, D. M. Binkley, and J. M. Rochelle, "Analysis of timing performance for an APD-LSO scintillation detector," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 504, no. 1-3, pp. 143–148, 2003.

[8] C. J. Stapels, M. R. Squillante, W. G. Lawrence, F. L. Augustine, and J. F. Christian, "CMOS-based avalanche photodiodes for direct particle detection," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 579, no. 1, pp. 94–98, 2007.

[9] L. H. Braga, L. Gasparini, L. Grant, R. K. Henderson, N. Massari, M. Perenzoni, D. Stoppa, and R. Walker, "A fully digital 8 $\times$ 16 sipm array for pet applications with per-pixel tdcs and real-time energy output," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 1, pp. 301–314, 2014.

[10] N. DAscenzo, W. Brockherde, S. Dreiner, A. Schwinger, A. Schmidt, and Q. Xie, "Design and Characterization of a Silicon Photomultiplier in 0.35 μm CMOS," *IEEE Journal of the Electron Devices Society*, vol. 6734, no. c, pp. 1–1, 2017.

[11] C. Chang, D. Sud, and M. Mycek, "Fluorescence lifetime imaging microscopy," in *Digital Microscopy, 3rd Edition*, ser. Methods in Cell Biology. Academic Press, 2007, vol. 81, no. Supplement C, pp. 495 – 524.

[12] H. C. Gerritsen, M. A. Asselbergs, A. V. Agronskaia, and W. G. Van Sark, "Fluorescence lifetime imaging in scanning microscopes: Acquisition speed, photon economy and lifetime resolution," *Journal of Microscopy*, vol. 206, no. 3, pp. 218–224, 2002.

[13] L. Parmesan, N. A. Dutton, N. J. Calder, L. A. Grant, and R. K. Henderson, "A 256x256 SPAD array with in-pixel Time to Amplitude Conversion for Fluorescence Lifetime Imaging Microscopy," *International Image Sensor Workshop*, pp. 8–11, 2015.

[14] R. M. Field, S. Realov, and K. L. Shepard, "A 100 fps, time-correlated single-photon-counting-based fluorescence-lifetime imager in 130 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 867–880, 2014.

[15] Y. Maruyama, J. Blacksberg, and E. Charbon, "A 1024 $\times$ 8, 700-ps time-gated spad line sensor for planetary surface exploration with laser raman spectroscopy and libs," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 1, pp. 179–189, 2014.

[16] J. Kostamovaara, J. Tenhunen, M. Kögler, I. Nissinen, J. Nissinen, and P. Keränen, "Fluorescence suppression in Raman spectroscopy using a time-gated CMOS SPAD," *Optics Express*, vol. 21, no. 25, p. 31632, 2013. [Online]. Available: https://www.osapublishing.org/oe/abstract.cfm?uri=oe-21-25-31632

[17] I. Nissinen, J. Nissinen, P. Ker??nen, A. K. L??nsman, J. Holma, and J. Kostamovaara, "A 2 ?? (4) ?? 128 multitime-gated SPAD line detector for pulsed Raman spectroscopy," *IEEE Sensors Journal*, vol. 15, no. 3, pp. 1358–1365, 2015.

[18] G. Gariepy, N. Krstajić, R. Henderson, C. Li, R. R. Thomson, G. S. Buller, B. Heshmat, R. Raskar, J. Leach, and D. Faccio, "Single-photon sensitive light-in-fight imaging," *Nature Communications*, vol. 6, p. 6021, 2015. [Online]. Available: http://www.nature.com/doifinder/10.1038/ncomms7021

[19] N. A. W. Dutton, I. Gyongy, L. Parmesan, N. Calder, B. R. Rae, S. Pellegrini, L. A. Grant, and R. K. Henderson, "A SPAD - based QVGA Image Sensor for Single Photon Counting and Quanta Imaging," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 1–6, 2016.

[20] M. Buttafava, J. Zeman, A. Tosi, K. Eliceiri, and A. Velten, "Non-line-of-sight imaging using a time-gated single photon avalanche diode," *Optics Express*, vol. 23, no. 16, p. 20997, 2015. [Online]. Available: https://www.osapublishing.org/abstract.cfm?URI=oe-23-16-20997

[21] S. V. Polyakov, "Photomultiplier Tubes," *Experimental Methods in the Physical Sciences*, vol. 45, pp. 69–82, 2013.

[22] F. Zappa, S. Tisa, A. Tosi, and S. Cova, "Principles and features of single-photon avalanche diode arrays," *Sensors and Actuators, A: Physical*, vol. 140, no. 1, pp. 103–112, 2007.

[23] R. G. W. Brown, K. D. Ridley, and J. G. Rarity, "Characterization of silicon avalanche photodiodes for photon correlation measurements 1: Passive quenching," *Applied Optics*, vol. 25, no. 22, p. 4122, 1986.

[24] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, p. 1956, 1996.

[25] R. H. Haitz, "Mechanisms contributing to the noise pulse rate of avalanche diodes," *Journal of Applied Physics*, vol. 36, no. 10, pp. 3123–3131, 1965.

[26] S. Sze, "Semiconductor Devices : Physics and Technology," 2001.

[27] P. A. Ekstrom, "Triggered-avalanche detection of optical photons," *Journal of Applied Physics*, vol. 52, no. 11, pp. 6974–6979, 1981.

[28] A. Rochas, M. Gani, B. Furrer, P. A. Besse, R. S. Popovic, G. Ribordy, and N. Gisin, "Single photon detector fabricated in a complementary metal-oxide-semiconductor high-voltage technology," *Review of Scientific Instruments*, vol. 74, no. 7, pp. 3263–3270, 2003.

[29] H. D. E. Man, "MEASUREMENT OF THE IONIZATION RATES IN DIFFUSED SILICON p-n JUNCTIONS," *Solid-State Electronics*, vol. 13, no. 1, pp. 583–608, 1970.

[30] S. L. Miller, "Ionization rates for holes and electrons in silicon," *Physical Review*, vol. 105, no. 4, pp. 1246–1249, 1957.

[31] M. Singh Tyagi, "Zener and avalanche breakdown in silicon alloyed p-n junctions—II," *Solid-State Electronics*, vol. 11, pp. 117–128, 1968.

[32] H. Albrecht and L. Lerach, "Distinction between avalanche and tunneling breakdown in one-sided abrupt junctions," *Applied Physics*, vol. 16, no. 2, pp. 191–194, 1978.

[33] G. A. Hurkx, H. C. De Graaff, W. J. Kloosterman, and M. P. Knuvers, "A New Analytical Diode Model Including Tunneling and Avalanche Breakdown," *IEEE Transactions on Electron Devices*, vol. 39, no. 9, pp. 2090–2098, 1992.

[34] M. Singh Tyagi, "Zener and avalanche breakdown in silicon alloyed p-n junctions—I," *Solid-State Electronics*, vol. 11, pp. 99–115, 1968.

[35] K. B. C. Basavanagoud, "Effect of Lateral Curvature on the Breakdown Voltage of Planar Diodes," *IEEE Electron Device Letters*, vol. EDL-6, no. 6, pp. 276–278, 1985.

[36] Y. Xu, P. Xiang, and X. Xie, "Comprehensive understanding of dark count mechanisms of single-photon avalanche diodes fabricated in deep sub-micron CMOS technologies," *Solid-State Electronics*, vol. 129, pp. 168–174, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2016.11.009

[37] Y. Kang, H. X. Lu, Y. H. Lo, D. S. Bethune, and W. P. Risk, "Dark count probability and quantum efficiency of avalanche photodiodes for single-photon detection," *Applied Physics Letters*, vol. 83, no. 14, pp. 2955–2957, 2003.

[38] H. Dautet, P. Deschamps, B. Dion, A. D. MacGregor, D. MacSween, R. J. McIntyre, C. Trottier, and P. P. Webb, "Photon-counting techniques with silicon avalanche photodiodes," *Applied Optics*, vol. 32, no. 21, pp. 240–250, 1993. [Online]. Available: http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1007517

[39] V. Savuskan, I. Brouk, M. Javitt, and Y. Nemirovsky, "An estimation of single photon avalanche diode (SPAD) photon detection efficiency (PDE) nonuniformity," *IEEE Sensors Journal*, vol. 13, no. 5, pp. 1637–1640, 2013.

[40] B.-W. Tzou, J.-Y. Wu, Y.-S. Lee, and S.-D. Lin, "Method to evaluate afterpulsing probability in single-photon avalanche diodes," *Optics Letters*, vol. 40, no. 16, p. 3774, 2015. [Online]. Available: https://www.osapublishing.org/abstract.cfm?URI=ol-40-16-3774

[41] D. Bronzi, S. Tisa, F. Villa, S. Bellisai, A. Tosi, and F. Zappa, "Fast sensing and quenching of CMOS SPADs for minimal afterpulsing effects," *IEEE Photonics Technology Letters*, vol. 25, no. 8, pp. 776–779, 2013.

[42] D. P. Palubiak, Z. Li, and M. J. Deen, "Afterpulsing Characteristics of Free-Running and Time-Gated Single-Photon Avalanche Diodes in 130-nm CMOS," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3727–3733, 2015.

[43] N. Teranishi, "Required conditions for photon-counting image sensors," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2199–2205, 2012.

[44] C. Niclass, K. Ito, M. Soga, H. Matsubara, I. Aoyagi, S. Kato, and M. Kagami, "Design and characterization of a 256x64-pixel single-photon imager in CMOS for a MEMS-based laser scanning time-of-flight sensor," *Optics Express*, vol. 20, no. 11, p. 11863, 2012. [Online]. Available: https://www.osapublishing.org/oe/abstract.cfm?uri=oe-20-11-11863

[45] E. A. Webster and R. K. Henderson, "A TCAD and spectroscopy study of dark count mechanisms in single-photon avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4014–4019, 2013.

[46] H. P. K. K, "7: Scintillation Counting," *Hamamatsu PMT Handbook*, 2007.

[47] 楊驍, 朱弘博, 名倉徹, and 浅田邦博, "C-12-39 標準 cmos 技術による単一光子アバランシェフォトダイオード (有線通信, c-12. 集積回路, 一般セッション)," **電子情報通信学会総合大会講演論文集**, vol. 2015, no. 2, p. 100, 2015.

[48] X. Yang, H. Zhu, T. Nakura, T. Iizuka, and K. Asada, "An asynchronous projection and summation circuit for in-pixel processing in single photon avalanche diode sensors," in *Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2015 IEEE 18th International Symposium on*. IEEE, 2015, pp. 131–136.

[49] ——, "An asynchronous summation circuit for noise filtering in single photon avalanche diode sensors," *Journal of Circuits, Systems and Computers*, vol. 25, no. 03, p. 1640017, 2016.

[50] M. Nandakumar, a. Chatterjee, S. Sridhar, K. Joyner, M. Rodder, and I.-C. Chen, "Shallow trench isolation for advanced ULSI CMOS technologies," *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, pp. 133–136, 1998.

[51] H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology," *IEEE Electron Device Letters*, vol. 27, no. 11, pp. 887–889, 2006.

[52] M. J. Hsu, H. Finkelstein, and S. C. Esener, "A CMOS STI-bound single-photon avalanche diode with 27-ps timing resolution and a reduced diffusion tail," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 641–643, 2009.

[53] M. Gersbach, C. Niclass, E. Charbon, J. Richardson, R. Henderson, and L. Grant, "A single photon detector implemented in a 130nm CMOS imaging process," *ESSDERC 2008 - Proceedings of the 38th European Solid-State Device Research Conference*, no. 029217, pp. 270–273, 2008.

[54] M. A. Karami, H. J. Yoon, and E. Charbon, "Single-photon Avalanche Diodes in sub-100nm Standard CMOS Technologies," *Intl. Image Sensor Workshop (IISW)*, 2011. [Online]. Available: http://infoscience.epfl.ch/record/178147

[55] K. Jradi, D. Pellion, and D. Ginhac, "Design, characterization and analysis of a 0.35 um CMOS SPAD," *Sensors (Switzerland)*, vol. 14, no. 12, pp. 22 773–22 784, 2014.

[56] C. Niclass, M. Gersbach, R. Henderson, L. Grant, and E. Charbon, "A single photon avalanche diode implemented in 130-nm CMOS technology," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 13, no. 4, pp. 863–869, 2007.

[57] R. M. Field, J. Lary, J. Cohn, L. Paninski, and K. L. Shepard, "A low-noise, single-photon avalanche diode in standard 0.13 μm complementary metal-oxide-semiconductor process," *Applied Physics Letters*, vol. 97, no. 21, 2010.

[58] B. Zhang, Z. Li, and M. E. Zaghloul, "A Single-Photon Avalanche Diode in CMOS 0.5 um n-well process," *2012 IEEE Sensors*, pp. 1–4, 2012. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6411333

[59] H. Xu, L. Pancheri, G.-F. D. Betta, and D. Stoppa, "Design and characterization of a p+/n-well SPAD array in 150nm CMOS process," *Optics Express*, vol. 25, no. 11, p. 12765, 2017. [Online]. Available: https://www.osapublishing.org/abstract.cfm?URI=oe-25-11-12765

[60] J. A. Richardson, E. A. Webster, L. A. Grant, and R. K. Henderson, "Scaleable single-photon avalanche diode structures in nanometer CMOS technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 7, pp. 2028–2035, 2011.

[61] L. Pancheri, N. Massari, F. Borghetti, and D. Stoppa, "A 32x32 SPAD Pixel Array with Nanosecond Gating and Analog Readout," *the International Image Sensor Workshop*, no. November 2015, pp. 4–7, 2011.

[62] R. K. Henderson, L. A. Grant, and J. A. Richardson, "Reduction of Band-to-band Tunneling in Deep-submicron CMOS Single Photon Avalanche Photodiodes," *International Image Sensor Workshop*, pp. 2–6, 2009.

[63] J. A. Richardson, L. A. Grant, and R. K. Henderson, "Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology," *IEEE Photonics Technology Letters*, vol. 21, no. 14, pp. 1020–1022, 2009.

[64] G. Kawata, J. Yoshida, K. Sasaki, and R. Hasegawa, "Probability Distribution of Afterpulsing in Passive-quenched Single-photon Avalanche Diodes," *IEEE Transactions on Nuclear Science*, vol. 64, no. 8, pp. 2386–2394, 2017.

[65] X. Yang, H. Zhu, T. Nakura, T. Iizuka, and K. Asada, "F-1-4 A CMOS SPAD Sensor Featuring Asynchronous Event-Extraction Readout Architecture for Faint Light Detection," in *Solid State Device and Materials*, 2015, pp. 812–813.

[66] ——, "A 15 × 15 single photon avalanche diode sensor featuring breakdown pixels extraction architecture for efficient data readout," *Japanese Journal of Applied Physics*, vol. 55, no. 4, 2016.

[67] ——, "A 15 x 15 SPAD Array Sensor with Breakdown-Pixel-Extraction," in *ASP-DAC*, vol. 3, 2017, pp. 23–24.

[68] Y. Oike, M. Ikeda, and K. Asada, "A 375 ?? 365 high-speed 3-D range-finding image sensor using row-parallel search architecture and multisampling technique," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 444–453, 2005.

[69] X. Yang, K. Xu, T. Iizuka, T. Nakura, H. Zhu, and K. Asada, "A SPAD Array Sensor based on Breakdown Pixel Extraction Architecture with Background Readout for Scintillation Detector," in *IEEE Sensors*, vol. 3, no. c, 2017, pp. 525–527.

List of Publications

Journal Papers

1. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ An asynchronous summation circuit for noise filtering in single photon avalanche diode systems, ” Journal of Circuits, Systems, and Computers (JCSC), vol. 25, No. 3, pp. 1640017-1-1640017-16, 2016.

2. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ A 15 x 15 single photon avalanche diode sensor featuring breakdown pixels extraction architecture for efficient data readout, ” Japanese Journal of Applied Physics (JJAP), vol. 55, No. 4s, 04EF04, 2016

International Conference Papers

1. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ An asynchronous projection and summation circuit for in-pixel processing in single photon avalanche diode systems, ”in proceedings of 2015 International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), pp. 131-136, Belgrade, Serbia, April, 2015.

2. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ A CMOS SPAD sensor featuring asynchronous event-extraction readout architecture for faint light detection, ” in proceedings of 2015 International Conference on Solid State Devices and Materials (SSDM), pp. 812-813, Sapporo, Japan, September, 2015.

3. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ A 15 x 15 SPAD array sensor with breakdown-pixel-extraction architecture for efficient data read-

out, ” in proceedings of 2017 Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 23-24, Chiba, Japan, Jan. 2017.

4. Xiao Yang, Kai Xu, Tetsuya Iizuka, Toru Nakura, Hongbo Zhu, Kunihiro Asada, “ SPAD Array Sensor based on Breakdown Pixel Extraction Architecture with Background Readout for Scintillation Detector, ” in proceedings of IEEE Sensors 2017, pp. 525-527, Glasgow, UK, Oct. 2017.

Domestic Conference Papers

1. Xiao Yang, Hongbo Zhu, Toru Nakura, Kunihiro Asada, “ Single photon avalanche diode based on standard CMOS technology, ” in proceedings of the 2015 IEICE General Conference, C-12-39, kusatsu, Japan, March, 2015.

2. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada, “ A 31x31 SPAD array sensor with variable readout time for scintillation light detection, ” in proceedings of the 2016 IEICE Society Conference, C-12-11, Sep. 2016.

3. Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada,“ A 15x15 single photon avalanche diode sensor featuring breakdown pixels extraction architecture for efficient data readout, LSI and systems workshop, Tokyo, Japan, April, 2016.