論文の内容要旨

Thesis Summary

Study on SPAD Imagers with Quick Readout Circuits

(高速読み出し SPAD イメージャに関する研究)

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This thesis focuses on the design of a SPAD in the standard CMOS process, and the design of SPAD imagers. The basic principle and key parameters of a SPAD are introduced in Chapter 2. Then, structures and experimental results about the designed several types of SPADs are presented in Chapter 3. From Chapter 4 to Chapter 5, a new sensor architecture with high readout efficient and 3 SPAD imagers utilizing the proposed architecture are shown. In Chapter 6, a SPAD imager with real-time event discriminator is introduced.

Chapter 2 provides an introduction about basic principles and features of SPAD in order to understand the required constraints in designing CMOS SPAD. The breakdown voltage, dark counts rate (DCR) , and photon detection efficiency (PDE) are introduced. According to the introduction, the breakdown voltage of a SPAD should be greater than 15 V in order to suppress the influence of band to band tunneling, and s suitable guard ring is necessary for preventing premature breakdown due to edge effect. Furthermore, an analysis on the influence of DCR and PDE is introduce, and the desirable DCR for the SPAD imager is about 10 kHz.

Chapter 3 focuses on designing and testing about SAPDs fabricated by the available standard CMOS process. The detail about the design of SPADs used for the SPAD imagers in this work are presented in this chapter. The structures of three types of CMOS SPADs are reviewed and discussed at first. Then, several test chips fabricated in the Rohm standard 180 nm CMOS process in order to find a suitable structure of SPADs are introduced. Ac- cording to the analysis in the previous chapter, the target specification of the desirable SPAD is that a low DCR about 10 kHz when SPADs are over-bias at 1.8 V. A suitable SPAD of Pwell/DeepNwell with PolyGate around the active region, low DCR with purely avalanche breakdown, and planer breakdown region were confirmed by the experimental results. Then, a test circuit for after-pulsing probability measurement is presented. The experimental results demonstrate the efficiency of hold-off time about reducing the influence of after-pulsing, and the after-pulsing probability can be decreased to lower than 1% with a 20 ns hold-off time.

This chapter targets on the efficient readout architecture for SPAD imagers. Since the breakdown SPAD pixels are sparse in many application, an architecture that only extracts the address of breakdown pixels can achieve a higher readout efficiency. A breakdown pixel extraction (BPE) readout architecture is proposed based on the binary feature of SPADs. The design and behavior of BPE architecture has been introduced at first, and the design of a 15×15 SPAD imager to verify the functionality of the proposed architecture is presented. Then, a detail design about the imager with 31×31 pixels utilizing background read- out method is shown. This imager adds an additional 1-b memory in each pixel to store the value of the previous frame, and to realize the background readout. This method can minimize T*dead* to 3 cycles under dark conditions or under sparse breakdown pixels. Furthermore, another BPE based 31×31 SPAD imager with event discriminator is proposed for minimizing T*dead* and event detecting. This imager counts the value

of Max(*BD*,*i*) of each frames at first, and the readout procedure only starts when Max(*BD*,*i*) became larger than a threshold value.

Chapter 5 presents the experimental results including the functionality, DCR distribution, PDE and dead time about the three designed imagers in Chapter 4. For the first designed sensor with 15×15 SPAD array, the functionality of BPE readout method is experimentally demonstrated firstly. Then, the DCR distribution is measured, and the median value, mean value, are 10 kHz, 20 kHz, respectively. Based on the measured DCR, an analysis about the temporal aperture ratio (TAR) is show. For the second imager that contains 31×31 SPAD array with background readout method based on BPE architecture, the ability of random event detection has been shown by pulsed laser imaging at first. Then, measurements about the DCR distributions of the images with different SPAD sizes are presented. Furthermore, an analysis about the requirements that can minimize T*dead* is presented, and TAR as function of T*win* has been shown comparing with the first imager. A 40% improvement of TAR is shown based on the calculated results. Finally, Photon detection efficiency of designed SPAD is measured. For the third imager that employs an event discriminator based on BPE architecture, the functionality of this sensor is measured using the same method as the previous one. Then, an analysis about the setting of threshold value is shown.

Chapter 6 shows the design a 32×32 SPAD imager with the real time current logic event discriminator together with the experimental results. This imager employs a current logic to monitor the number of breakdown pixels in real time, and a free-running with variable hold- off time active quenching circuit is proposed to achieve zero T*dead*. The ability of random event distinction is shown through the experimental results.