A Study of
Carrier Mobility and Variability
in Silicon Nanowire MOSFETs

（シリコンナノワイヤ MOSFET におけるキャリア移動度と特性ばらつきに関する研究）

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Abstract

In the past several decades, the size of a metal-oxide-semiconductor field-effect-transistor (MOSFET), the basic element in very-large-scale integrated circuits (VLSI), has been scaled down for higher integration and higher performance. As of 2012, the gate length of MOSFETs has reached a sub-30 nm regime. However, as the scaling proceeds, several problems stand out and prevent more miniaturization of MOSFETs. Among all the issues which arise to handicap the continuous device scaling, two issues are with great importance, one is the short channel effect (SCE), and the other is the variability. Among all the promising post-planar structures proposed for solving the scaling issues, the silicon nanowire MOSFETs, have attracted much attention in recent year, for their high immunity to short-channel effect.

The purpose of this work is to evaluate the potential of silicon nanowire MOSFETs for promising "More Moore" device in terms of both device performance enhancement and stability improvement. In this work, silicon nanowire FETs with tri-gate structure is extensively studied for carrier mobility and variability. This work is based mainly on the experiments including device design, sample fabrication and characteristic measurement.

In this paper, on the base of split C-V method, experimental and theoretical investigations of carrier mobility characteristics in single silicon nanowires are described systematically for the first time. The hole mobility in [110]-direction silicon nanowires is higher than (100) universal curve even in a single nanowire FET, which originates from the effect of (110) side surface with high hole mobility. Low temperature measurements were performed with [110]- direction NWs on (100) SOI to investigate the scattering mechanisms in tri-gate silicon nanowire. Surface roughness limited mobility and phonon limited mobility are extracted and analyzed. It is found that the orientation and roughness quality of nanowire surface plays the key role that determinates

the mobility modulation in nanowires.

And, it is experimentally found that within-device variability of not only V_{TH} but also those of DIBL and COV are suppressed in intrinsic channel nanowire FETs owing to the non intentionally doped channel and the absence of gate work-function variability. The intrinsic channel silicon nanowire MOSFET is promising for a future scaled device structure in terms of not only the short channel effect suppression but also the variability suppression.

In conclusion, the results obtained in this thesis show important information on the carrier mobility and variability characteristics in silicon nanowire MOSFETs, which are promising for a future scaled device structure in terms of not only the short channel effect suppression but also the performance enhancement and variability suppression.

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Chapter 1

Introduction

1.1 Background

Integrated Circuit (IC) technology, which has been regarded as one of the most important inventions in engineering history, achieved tremendous progress in the past decades. And the progress in IC technology has become the driving power of the Information Technology (IT) revolution, which has greatly changed our lives and the whole world. The secret to create this miracle in IC technology is actually simple: scaling down the dimension of each transistor, the basic element of integrated circuits, and increasing the total number of transistors in one IC chip. The device scaling has been successfully predicted by Moore's law, which was predicted in 1965 [1], the number of transistors on one IC chip has doubled every eighteen months and the feature area of each transistor has shrunk to half of its original value at the same time, as shown in Fig. 1.1.

After continuous scaling down for higher integration and higher performance for decades, the conventional silicon metal oxide semiconductor field-effect transistor (MOSFET), the basic element in very-large-scale integrated circuits (VLSI), approaches its scaling limit. Despite achieving this great progress until now, it is clear that there is a physical limit at the end of scaling and we can not shrink the device size forever. As of 2012, the gate length of MOSFETs has reached a sub-30 nm regime. When the size scales down into deep sub-micron regime, conventional device scaling concept loses its effect and new physics turn to dominate device

performance. In ITRS, three different but related concepts are proposed: “More Moore”, “More than Moore”, and “Beyond CMOS” [2]. Until now, we still have no concrete image that what will happened in “Beyond CMOS”, but it is clear that we need to achieve further performance gain in Si-based devices before we enter into “Beyond CMOS” era. However, as the scaling proceeds, several problems such as short-channel effects, rapid increase in power dissipation, parasitic effects, and characteristics fluctuations stand out and prevent more miniaturization of MOSFETs[3]. One strategy for overcoming the limitations of current VLSI technology is to introduce novel devices with new structure and operation principle different from conventional devices and whose performance is enhanced in a smaller dimension, that is to say, which has the higher scaling potential.

With the help of “nanotechnology”, which has attracted worldwide extensive attention for recent years, a lot of promising new-principle devices are proposed to aid the further performance enhancement. Although the definition of “nanotechnology” can be different from person to person, one feasible definition could be “The technology deals with developing materials, devices, or other structures possessing at least one dimension sized from 1 to 100 nanometres.” So far, various kinds of ultra-small materials such as silicon, compound semiconductors, nano-carbon, organic materials, biomedical materials, etc. have been utilized in nanotechnology. T silicon-based technology is the most promising candidate, for its natural affinity to conventional VLSI technology. The advanced silicon fabrication techniques required for the silicon nano-device, are highly compatible with the techniques which have been used for miniaturization of MOSFETs in the existing CMOS VLSI technology.

Among all the issues which arise to handicap the continuous device scaling, two issues are with most great importance, one is the short channel effect (SCE), and the other is the variability. To curb the short channel effect, devices with multiple gates have been developed to improve the

gate-channel controllability for better electrical characteristics with the progress in nano-scale fabrication technology. For example, ultra-thin-body (UTB) MOSFETs with a double gate (DG) structure [4,5], fin-type FETs (FinFETs) with a tri-gate structure [6,7] and nanowire MOSFETs with a gate-all-around (GAA) structure [8,9] are proposed for promising candidates for future VLSI technologies with high performance, as shown in Fig. 1.2. Ultrathin SOI MOSFET can effectively reduce the short channel effect and eliminate most of the leakage paths. The multiple-gate MOSFET can curb the short channel effect and decreasing the leakage current. The increased number of gates enhances electrostatic control of the gate electrode over the charge carriers flowing from source to drain in the channel, and therefore reduces the parasitic short-channel effects. Ultimately, the GAA structure with virtually "infinite" number of gates provides the best gate electric field control with all the gates in close vicinity of the channel.

With the merits from both ultrathin channel and multi-gate structure, the nanowire is considered a potential candidate to take CMOS electronics to the "end-of-the-silicon technology roadmap" by shrinking the gate length along with the nanowire diameter. This special “one-dimension” transport structure owns two-dimensional quantum confinements and plays an important role in “More Moore”. In actual applications, we care about the devices performance, such as drive current and operation speed; however, the underlying physical mechanism is the carrier mobility in the transport channel. Carrier mobility has been widely studied in planar bulk MOSFETs and ultrathin-body (UTB) MOSFETs and also FinFETs with a tri-gate (TG) structure [10-23]. For the silicon nanowire MOSFETs, theory works show different opinions for the carrier mobility behavior, some suggests large degradation, while some predicts an improvement. But experimental study on carrier mobility behavior in silicon nanowire MOSFETs is of limit number. In order to understand more about nanowires transport characteristics and figure out effective methods to get further performance enhancement, it is necessary to achieve experimental data of

intrinsic carrier mobility in nanowires with high accuracy. Although there are some experimental works on mobility in silicon nanowires, most of these studies are carried on with either indirect extraction method or special structure (for example, multiple nanowire array) to circumvent the difficulty originated from the ultra-small size of the silicon nanowire, for example, the ultra-small capacitance between the gate and the channel of single nanowire; the serious parasitic effect. The intrinsic capacitance of single nanowire is too difficult to be measured directly. Over-/under-estimation of parasitic resistance or capacitance results in large deviation in the carrier mobility. The intrinsic carrier mobility of single nanowire is still in the dark.

Along with the rapid device scaling, the variability turns to be one of the critical concerns [24]. Threshold voltage (V_{TH}) variability considerably degrades the stability of integrated circuits. The minimum operation voltage (V_{min}) in logic circuits is limited by device variability, and static random access memory (SRAM) fails at a low supply voltage owing to transistor unbalance in a cell. It is now mandatory to take this variability into consideration in circuit design to maintain a high yield. It is known that random dopant fluctuation (RDF) is the dominant origin of random V_{TH} variability in conventional bulk MOSFETs [25]. Recently, it is reported that the variability of both DIBL (drain induced barrier lowering) and COV (current-on-set voltage) is also caused by RDF [26-28] and leads to instability of SRAM cells [29] and drain-current variability [26]. It is shown that intrinsic channel fully depleted (FD) silicon-on-insulator (SOI) MOSFETs have not only a smaller V_{TH} variability but also smaller DIBL and COV variabilities owing to the absence of RDF[30]. However, the DIBL and COV variabilities still remain, possibly owing to the variability of workfunction in the metal gate electrode, and further reduction of variability is strongly required for better circuit performance variability and SRAM stability. The variability in silicon nanowire MOSFETs should be studied to investigate the variability mechanism for the possibility of further variability suppression.

1.2 Objectives

The objective of this work is to evaluate the potential of silicon nanowire MOSFETs for promising "More Moore" device in terms of both device performance enhancement and stability improvement. More specifically, objectives of this work are divided into the following four parts.

To fabricate silicon nanowire MOSFETs with high process stability and reproducibility.

To experimentally extract carrier mobility in single nanowire MOSFETs.

To investigate the carrier mobility behavior in silicon nanowire.

To develop new evaluation method of intrinsic variability in silicon nanowire MOSFETs.

To evaluate the variability in silicon nanowire MOSFETs.

1.3 Chapter Organizations

This paper is organized into 6 chapters. In Chapter 2, basic theory and physics of the MOSFETs that are used in this thesis were overviewed. The split C-V measurement method and mobility extraction method were reviewed. In Chapter 3, [100]- and [110]- direction NWs MOSFETs on (100)- oriented SOI with tri-gate structure are fabricated and characterized. The electron and hole mobility in "single" nanowire FETs is extracted from split C-V measurement. In Chapter 4, low temperature measurements were performed with [110]- direction NWs MOSFETs on (100) SOI to investigate the scattering mechanisms in tri-gate silicon nanowire. In Chapter 5, various kinds of variability, V_{TH} , DIBL and COV in intrinsic channel silicon nanowire MOSFETs was evaluated to investigate the underlying physical mechanisms of variability. Finally, in Chapter 6, the results obtained in this thesis are summarized and the future work is discussed.

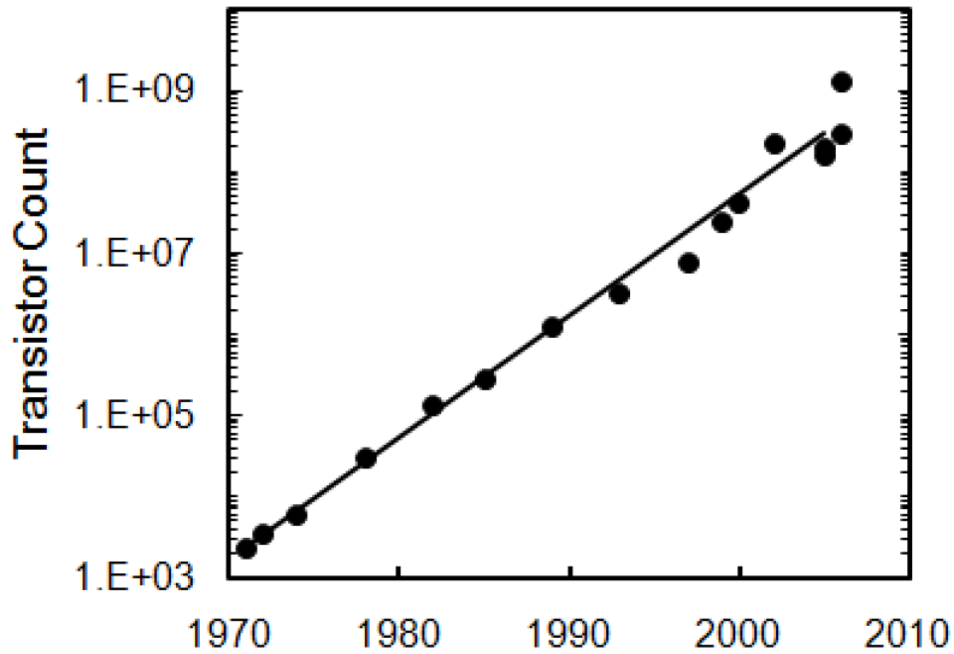

Fig. 1.1. The Moore's law. The number of transistors on one IC chip has doubled every eighteen months [31].

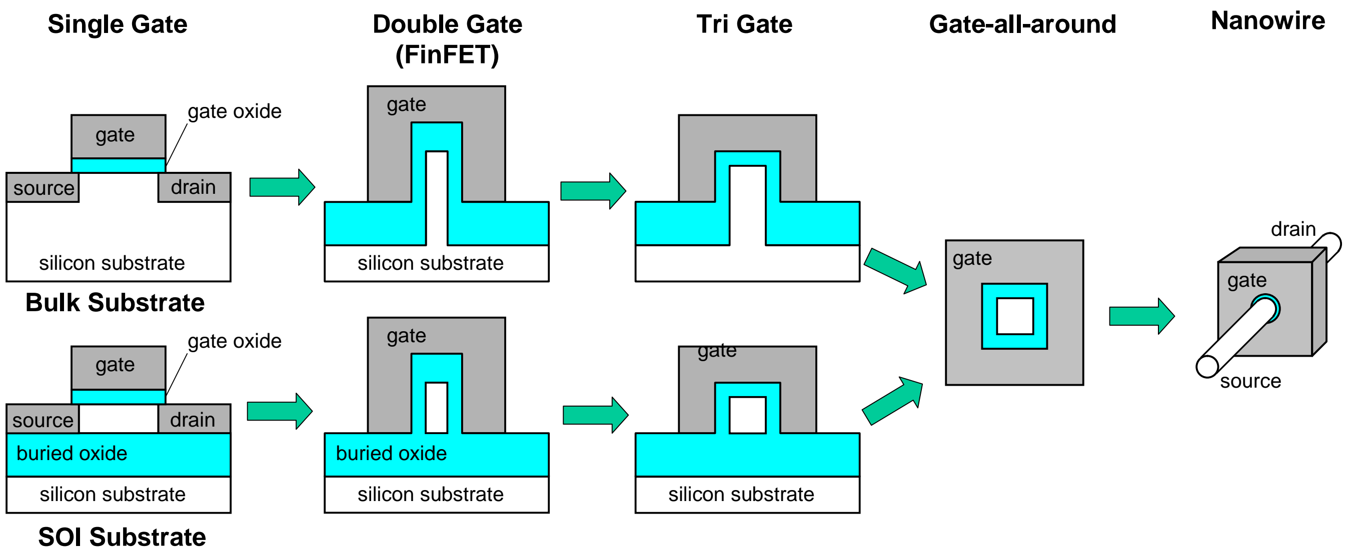

Fig. 1.2. Evolution of device structure from single-gate FET to nanowire MOSFET. The merits of ultra-thin body and multiple-gate are combined in the nanowire FET.

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Chapter 2

Fundamentals of Carrier Mobility in Silicon Nanowire MOSFETs

2.1 Introduction

As the conventional silicon metal oxide semiconductor field-effect transistor (MOSFET) approaches its scaling limits, many novel device structures are being extensively explored. To suppress the serious short channel effect (SCE) in extensively scaled traditional planar MOSFETs, devices with multiple gates have been developed, including MOSFETs with double-gate (DG) structure [1,2], FinFETs[3,4], and also nanowire FETs [5-9]. These structures have been extensively studied in either fabrication techniques or electrical properties [10-20], they show great potential in improving the performance of scaled device. Among them, the silicon nanowire transistor has attracted broad attention from both the semiconductor industry and academia. However, there are still a lot of things unknown in electrical transport mechanisms in extensively scaled MOSFET devices. Especially, the carrier mobility in silicon nanowire has not been thoroughly studied.

In actual applications, we care about the devices performance, such as drive current and operation speed; however, the underlying physical mechanism is the carrier mobility in the transport channel. Carrier mobility has been widely studied in planar bulk MOSFETs and ultrathin-body (UTB) MOSFETs and also FinFETs with a tri-gate (TG) structure. For the silicon

nanowire MOSFETs, theory works show different opinions for the carrier mobility behavior, some suggests large degradation, while some predicts an improvement. In order to understand more about nanowires transport characteristics and figure out effective methods to get further performance enhancement, it is necessary to achieve experimental data of intrinsic carrier mobility in nanowires with high accuracy. But experimental study on carrier mobility behavior in silicon nanowire MOSFETs is of limit number. Due to the ultra-small capacitance between the gate and the channel of single nanowire and serious parasitic effects, the intrinsic capacitance of single nanowire is too difficult to be measured directly. Over-/under- estimation of parasitic resistance or capacitance results in large deviation in the carrier mobility.

In this chapter, starting from the basics of the physics on carrier mobility, the split C-V measurement and mobility extraction method are introduced. In order to obtain the intrinsic carrier mobility, various methods used to remove the parasitic effects are discussed.

2.2 Physics on Carrier Mobility

The drive current Id in a FET is described as follows.

$$\frac{I_D}{W} = qN_{inv}v_d \tag{1}$$

Where W, q, N_{inv}, and v_d are the gate width, the unit charge, the surface inversion charge density and the carrier velocity, respectively. This simple equation means that the current is the multiplication of the "number of carriers" by "velocity of carriers". This equation is always true.

In a long channel FET, v_d is proportion to the multiplication of the low-field mobility μ by the lateral electric field E and it approaches to the saturation velocity (v_{sat}) as E increases.

$$v_d = \mu E < v_{sat} \tag{2}$$

Once the velocity saturation occurs, the mobility no longer affects the drive current. However, the higher mobility leads to higher velocity at a certain electric field, which means it takes less time to charge the capacitance of the next nodes in a CMOS circuit. Thus, the mobility is a direct indicator of a CMOS performance.

It is well known carriers in the inversion layer of bulk FETs are mainly scattered by three factors [21]:

Coulomb scattering

Substrate impurities, interface state densities, charges trapped in gate oxide

Phonon scattering

Lattice vibrations by finite temperature

Surface roughness scattering

Spatial nanoscale heterogeneity of Si/SiO_2 interface

Coulomb scattering, phonon scattering, and surface roughness scattering are dominant at the low-, middle-, and high- surface electric field, repectively. The total mobility curve is schematically shown in Fig. 2.1. Empirically, total mobility is evaluated by the Matthiessen's ruls as

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{coulomb}} + \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{sr}} . \qquad (3)$$

where $\mu_{coulomb}$ is the coulomb scattering limited mobility, μ_{phonon} is the phonon scattering-limited mobility, and μ_{sr} is the surface roughness scattering-limited mobility.

Though there are other scattering mechanisms in inversion layer carriers, such as the remote coulomb scattering, the remote phonon scattering, or the δt_{SOI} scattering mechanism. In UTB MOSFETs, mobility starts to degrade due to the increase of acoustic phonon scattering as t_{SOI} is reduced below 20 nm. This is due to the increased acoustic phonon scattering induced by limited

inversion layer thickness that is physically confined by thin SOI layer. And another special scattering mechanism is the δt_{SOI} scattering [13]. As t_{SOI} becomes around less than 5 nm, mobility is dominated by t_{SOI} fluctuation-induced scattering. δt_{SOI} fluctuation locally induces large potential barriers, which scatter the inversion layer carriers as shown in Fig. 2.2. It is experimentally confirmed that mobility limited by local t_{SOI} fluctuation is proportional to t_{SOI}^6 in ultrathin body (UTB) FETs. In the case of top-down fabricated Si nanowires with relatively rougher surface compared to planar SOI, this scattering may be a determining factor of the overall mobility behavior, due to the additional channel dimension confinement.

2.3 Mobility Extraction Method

Mobility measurement is usually performed by the split C-V method [22], measuring drain current and gate capacitance with respect to gate voltage respectively. The basic equation is expressed as:

$$\mu = \frac{L_{eff}}{W_{eff} V_d} \cdot \frac{I_d(V_g)}{Q_i(V_g)} = \frac{L_{eff}^2}{V_d} \cdot \frac{I_d(V_g)}{\int_{-\infty}^{V_g} C_{gc}(V_g) dV_g} \qquad (4)$$

Where L_{eff} / W_{eff} is the effective channel length / width, V_d is the applied drain bias, and $I_d(V_g)$ and $C_{gc}(V_g)$ are the measured drain current and gate-channel capacitance at a certain gate voltage V_g, respectively.

The split C-V of devices can be measured at frequencies ranging from 1 kHz to 1MHz, using a semiconductor parameter analyzer. The examples of measured capacitance voltage curves in nanowire nFETs are shown in Fig. 2.3, the oscillation frequency are varied to show the frequency dependence. At lower frequencies, which are closer to the quasi-static device operation, dielectric interface traps would respond and lead to overestimation of the inversion charge. Though

measurements at higher frequencies overcome the interface traps problem and also benefit from less measurement noise, the measured capacitance can be misinterpreted due to the external resistance dependence of measured impedance. Therefore, the measurements in this thesis were performed at 100 kHz where the aforementioned problems were minimized.

In our device structure ($L_g > L_{nw}$), the gate overlaps with source and drain partially, as depicted in Fig. 2.4, so there are three kinds of capacitance included in the measured capacitance: constant parasitic capacitance C_{con} from the Al pattern, parasitic MOSFET capacitance C_{MOS} from the overlap region between the gate and the source/drain, and intrinsic nanowire capacitance $C_g = C_{nw} \times L_{nw.}$, as shown in Fig. 2.5. To remove the effects of parasitic capacitance and resistance (R_p) in nanowire MOSFETs, various kinds of processing method are performed to extract the intrinsic C-V and I-V data from measurement result [11].

Double L_{eff} method

Among all these methods, the double L_{eff} method is always used for scaled device which is hard to determine the portion of parasitic effect in the measurement results directly [8]. In the double L_{eff} method, devices containing nanowires of different lengths are compared to remove parasitic effects. Supposing identical parasitic capacitance ($C_{con} + C_{MOS}$) and resistance (R_p) in the two compared devices with different L_{NW} values, $V_d/I_{d,1(2)}=Rp+R_{NW} \times L_{NW,1(2)}$, $C_{gc,1(2)}=C_{NW} \times L_{NW,1(2)}+C_{MOS}+C_{con}$. Here, $L_{NW,1(2)}$, $I_{d,1(2)}$ and $C_{gc,1(2)}$ are the designed L_{NW} and the measured I_d and C_{gc} in the two devices, respectively. Then, the intrinsic characteristics of nanowires with L_{NW} of $L_{NW,1}- L_{NW,2}$ can be derived. The parameters in eq. (4) can be replaced with the following definitions:

$$L_{eff} = L_{NW,1} - L_{NW,2}\ ,$$
$$I_d(V_g) = (I_{d,1}^{-1} - I_{d,2}^{-1})^{-1}\ ,$$
$$C_{gc}(V_g) = C_{gc,1}(V_g) - C_{gc,2}(V_g)\ . \tag{5}$$

The average surface carrier density is defined as

$$N_{inv} = \frac{\int_{-\infty}^{V_g} [C_{gc,1}(V_g) - C_{gc,2}(V_g)] dV_g}{(L_{NW,1} - L_{NW,2}) W_{eff}} \tag{6}$$

In bulk MOSFETs, UTB MOSFETs, FinFETs with double gates, and even [100]/(100) nanowires with a rectangular cross section, N_{inv} in eq. (6) denotes the average carrier density of a certain orientation surface. However, in [110]/(100) nanowires with a rectangular cross section, there exist not only (100)- but also (110)-orientation surfaces. Therefore, N_{inv} in eq. (6) denotes the average carrier density by considering the three surfaces in tri-gate structure [110]/(100) nanowires as a whole. It should be noted that the W_{eff} in the eq. (6) is the circumference for the tri-gate nanowire, while for tri-gate nanowires, it is $W_{eff} = W_{NW} + 2 \times H_{NW}$.

Open circuit method

Another method to remove the parasitic capacitance is to fabricate an open circuit reference with all the same structure with the real nanowire, but without the nanowires conducting channel. The measured capacitance result of open circuit reference is exactly the parasitic capacitance ($C_{open} = C_{con} + C_{MOS}$). Thus the intrinsic capacitance of nanowires can be derived with the following definition,

$$C_{gc}(V_g) = C_{gc,measured}(V_g) - C_{open}(V_g)\ . \tag{7}$$

In this study, we would like to push forward the measurement accuracy to investigate the intrinsic carrier mobility in single silicon nanowire, which is truly a direct evidence for reasoning

the mobility mechanism lying underneath.

2.4 Summary

In this Chapter, basic theory and physics of the MOSFETs that are used in this thesis were briefly reviewed. Common scattering mechanisms that affect the mobility of MOSFETs were reviewed. The split C-V measurement method and mobility extraction method were reviewed, and various methods to remove the parasitic effects were also extensively discussed.

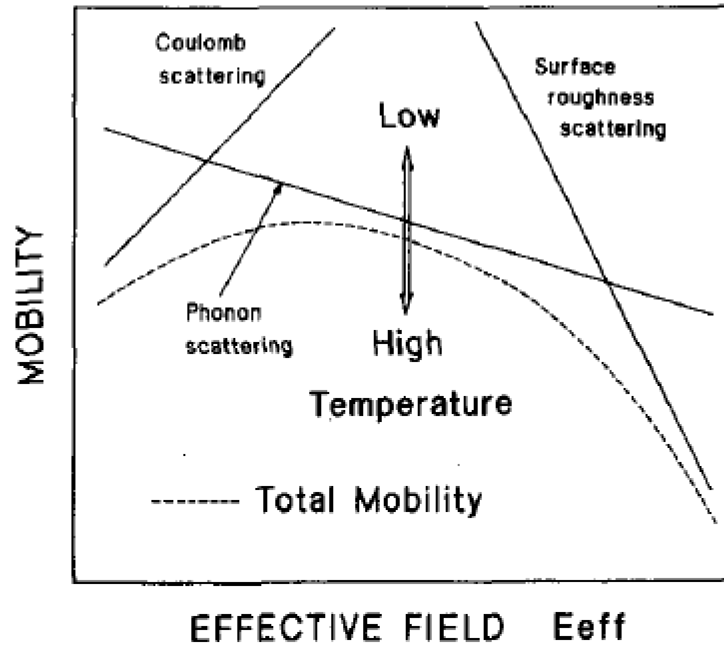

Fig. 2.1. A schematic showing mobility behavior in bulk MOSFET [7]. Each scattering mechanism is combined by the Matthiessens's Rule. Note that only phonon scattering is temperature dependent.

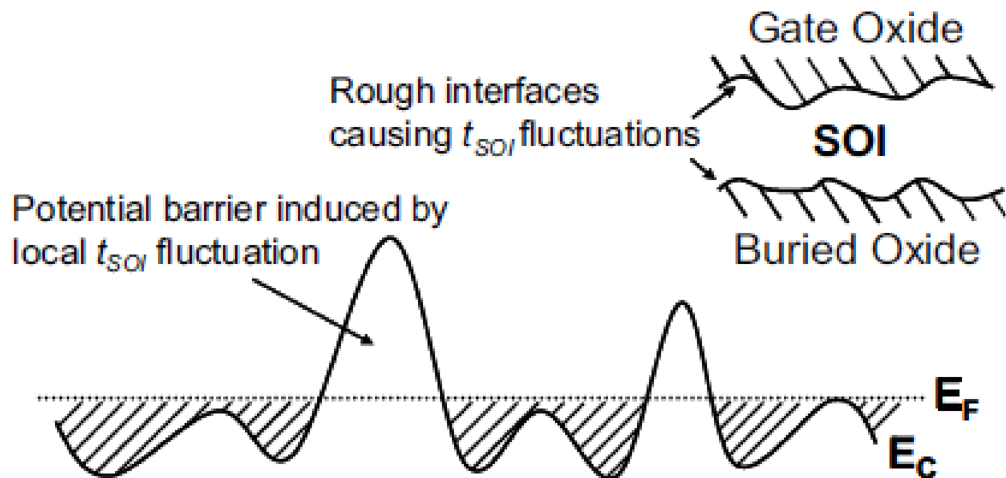

Fig. 2.2. Schematic showing an interface fluctuation. A large potential barrier is locally formed by t_{SOI} fluctuation in an atomic level, which scatters the conducting carriers.

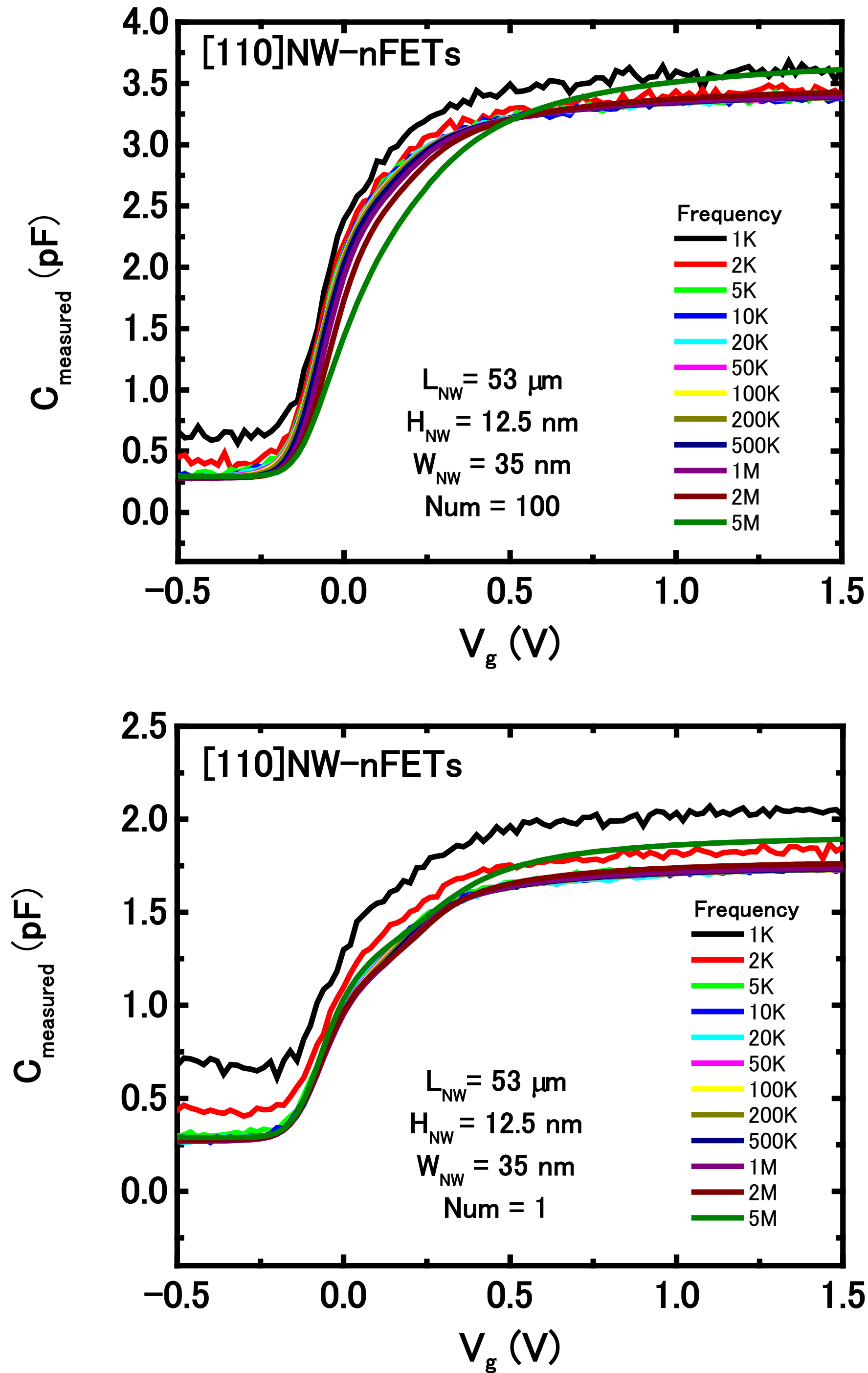

Fig. 2.3 Measurement C-V curves with different oscillation frequency. The existence of parasitic capacitance and deviation at low/high frequency can be seen.

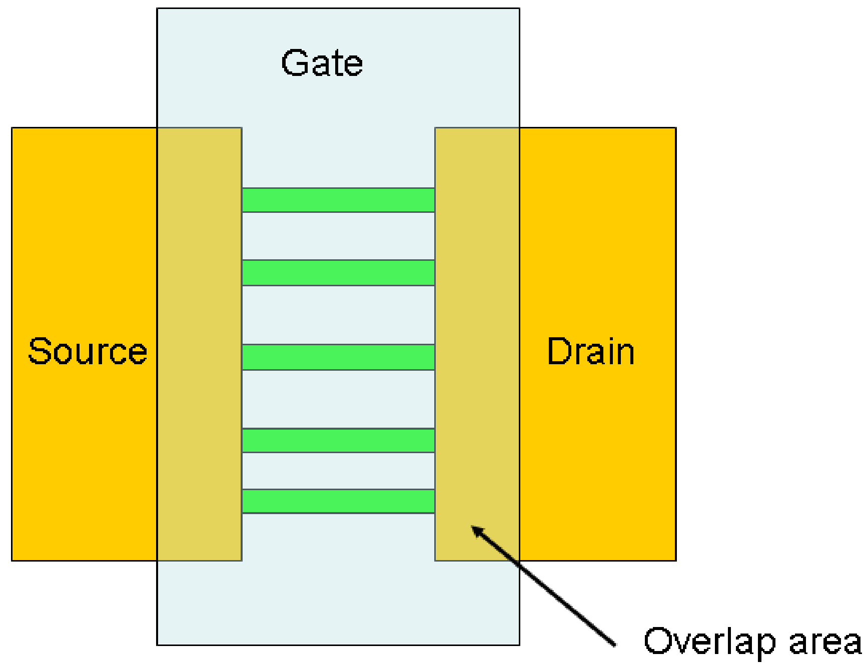

Fig. 2.4 Schematic of the overlapping area between gate and source/drain pad.

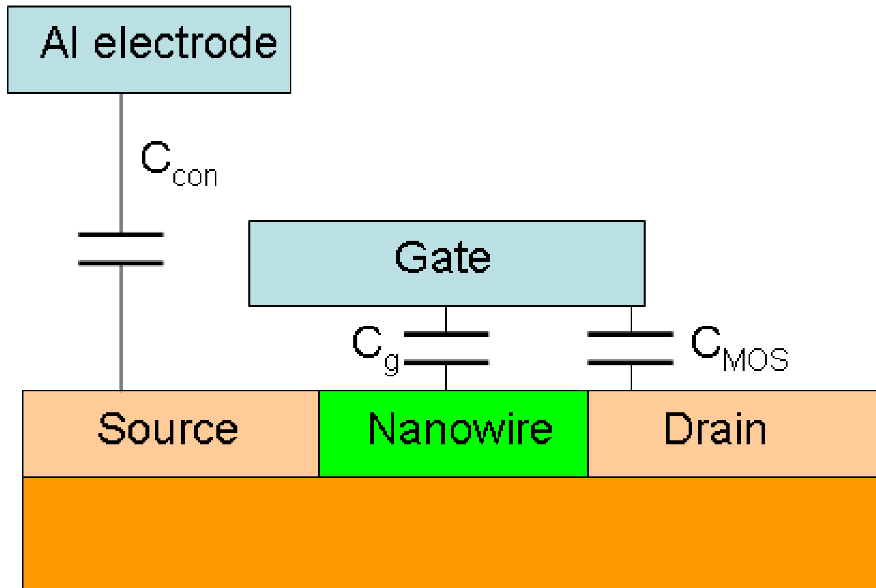

Fig. 2.5 Three kinds of capacitance included in the measured capacitance: constant parasitic capacitance C_{con} from the Al pattern, parasitic MOSFET capacitance C_{MOS} from the overlap region between the gate and the source/drain, and intrinsic nanowire capacitance C_g.

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Chapter 3

Carrier Mobility in Single Silicon Nanowire MOSFETs

3.1 Introduction

Among all the promising post-planar structures, have attracted much attention with their high immunity to short-channel effect in recent year. The nanowire structure could be scaling down while keeping good gate control on the channel. Among all these promising post-planar structures, the silicon nanowire MOSFET has its unique advantage – the silicon nanowire MOSFET is based on silicon, a material that the semiconductor industry has been working on for over thirty years; it would be really attractive to stay on silicon and also achieve good device metrics that nanoelectronics provides. As a result, the silicon nanowire transistor has obtained broad attention from both the semiconductor industry and academia [1-12]. But the experimental study on carrier mobility behavior in silicon nanowire MOSFETs is of limit number [13,14].

Most of the mobility in the experimental studies of silicon nanowire MOSFETs are obtained with either indirect extraction method (for example, estimated values of channel capacitance rather than directly measured channel capacitance) or special structure (for example, multiple nanowire array) to circumvent the difficulty originated from the ultra-small size of the silicon nanowire. This means that the reported mobility in literatures Ref. 3-6 has been actually an average value instead of an accurate value of individual silicon nanowire. The intrinsic carrier mobility of single nanowire is still in the dark. For further investigation of mobility mechanism,

the intrinsic carrier mobility of “single” silicon nanowire is strongly required.

Aiming at accurate mobility in single nanowire, the main difficulties originate from the ultra-small capacitance between the gate and the channel, as well as serious parasitic effects. In other words, the intrinsic capacitance of single nanowire is very difficult to be measured directly [12]. Accordingly, special channel structures are necessary for feasible capacitance measurement. Furthermore, parasitic effects removing need to be done before the intrinsic mobility data could be extracted. In nanowire MOSFETs, over-/under- estimation of parasitic resistance or capacitance results in large deviation in the carrier mobility. In our work, accurate carrier mobility is estimated by using split C-V method together with various methods to remove the parasitic effects.

In Chapter 2, basic theory and physics of the MOSFETs that are used in this thesis were overviewed. Common scattering mechanisms that affect the mobility of MOSFETs were reviewed. And the split C-V measurement and mobility extraction method are described in detail. In order to obtain the intrinsic carrier mobility, various methods used to remove the parasitic effects are also discussed.

In this chapter, the device design of ultra long single silicon nanowire MOSFETs with tri-gate structure are proposed and fabricated. Due to the “ultra-small” size of the silicon nanowire channel, the electrical signals are also extremely small. Based on the advanced split C-V method, accurate carrier mobility in nanowire MOSFETs with tri-tate structures was obtained with improved parasitic effects removing method. The electron and hole mobility in “single” nanowire FETs is directly extracted from split C-V measurement for the first time. It is found that the hole mobility is higher than (100) universal curve even in a single nanowire pFET.

3.2 Device Design and Measurement Setup

The gate-channel capacitance of silicon nanowire MOSFETs is extremely small, which is quite difficult to extract the mobility with split C-V method. Therefore, multiple parallel nanowire channel are often utilized in previous experimental studies on carrier mobility, to enlarge the extremely small capacitance signal from several femto-Farad level to the order of pico-Farad which can be easily measured with our capacitance analyzer with much higher accuracy. But as stated earlier, this carrier mobility of multiple nanowires, is actually an average value instead of an accurate value of individual silicon nanowire, which will conceal many details of the mobility behaviors.

Another way to enhance the ultra-small gate-channel capacitance of silicon nanowire MOSFETs is to use ultra-long silicon nanowires as the channel. But in the normal GAA nanowire process, there is a process step where the nanowire is freely suspended between the source and drain Si mesa. It makes the nanowire easily to be down bended or even broken. The down bending may induce extra inaccuracy (additional channel stress or other effects) in the final mobility result. Different to the GAA structure multiple nanowire MOSFETs in previous work by Dr. Chen, tri-gate ultra long silicon nanowire structure is proposed to avoid the low reproducibility and low uniformity of GAA structure silicon nanowire device. In tri-gate nanowire structure, the BOX underneath the nanowire channel is kept intact, which provides a solid support to the nanowire channel, avoids the bending of the silicon nanowire. The key point to avoid the undercut of BOX, is using a dry etching process instead of BHF wet etching to remove the EB resist. The fabrication process of tri-gate silicon nanowire MOSFET device is detailed described in the Appendix.

Intrinsic channel tri-gate single silicon nanowire FETs are fabricated on (100) SOI wafers

with both [110]- and [100]- channel direction. Fig. 3.1 shows a schematic demonstration of the side surface orientation of [110]- and [100]- channel direction NWs on (100) SOI. The nanowire channel is patterned at the recessed region between source and drain regions. Gate oxidation is performed at 1000 °C for 5 minutes, which formed 10.7 nm SiO_2 on (100) surface and 15.2 nm SiO_2 on (110) surface. The dry oxidation SiO_2 is covered with Poly Si as gate stacks. The final height of silicon nanowire after gate oxidation is H_{NW} = 12.5 nm for [110]-direction nanowire, and H_{NW} = 14.4 nm for [100]-direction nanowire. The nanowire width W_{NW} is from 35nm down to 11nm. The nanowire length which is defined by the width of the pre-made trench between drain and source is from 5 to 50 μm, and the gate covers the whole nanowire array and part of the drain and source edges. The overlap between gate and source/drain pads is 5 μm on each side. Multiple nanowire channel FETs, UTB FETs, and open circuit structure without channel are also fabricated on the same wafer for comparison.

The nanowire length is defined by the width of the pre-made trench between drain and source. Due to the fluctuation of laser lithography and wet etching used to define the drain/source mesa trench, the width of the trench is not always the designed width. And also the SEM observation of nanowire length (ie. the trench width) is with certain errors, because of the limit of the resolution. This error in nanowire length will add up in the double length method, for the need of two separate nanowire devices with different gate length. And also this error is more significant in the device with shorter nanowire length, for it is nearly constant error originated from the fabrication process quality and observation limit. Thus, measuring longer nanowires with open circuit method is more favorable for our target of accurate mobility in single silicon nanowire MOSFETs.

3.3 Electrical Characteristics

Figs. 3.2 and 3.3 compare linear and logarithmic I_{ds}-V_{gs} characteristics of [110]/(100) nFETs with single nanowire FETs and multiple nanowire FETs with hundred channels. I_{ds} of single nanowire FETs is approximately 1/100 of that of multiple nanowire FETs. The subthreshold slope (S.S.) values are around 62 mV/dec, which confirm good gate oxide interface around nanowires. The subthreshold slope is derived with the equation below,

$$S.S. = \left[\frac{d \log_{10} I_d}{dV_g} \right]^{-1} \quad . \tag{1}$$

Fig. 3.4 shows C_{gc}-V_{gs} characteristics of nFETs with single nanowire channel.

On-currents I_{on} (I_{ds} at V_{gs}=2.5V) of nanowire nFETs show a clear linear relation with the number of nanowires in the channel in Fig. 3.5 Fig. 3.6 shows on-state total resistance ($R_{on}=V_{ds}/I_{on}$) versus nanowire length in nFETs with different numbers of nanowires in the channel. The parasitic resistance can be extracted with L-array method. It is found that the influence of parasitic resistance is much weaker in longer channel with fewer nanowires, for the parasitic resistance is mainly from the source/drain area, and is usually a constant value. In the single nanowire nFET with a length of 53 μm, the parasitic resistance is approximately 1% in the total resistance, which is negligible. Therefore, the single nanowire FET with L_{NW} = 53 μm is used for the mobility extraction.

On the other hand, the on-state capacitances C_{on} (C_{gc} at V_{gs}=2.5V) shown in Fig. 3.7 suggests the existence of serious parasitic capacitance which is mainly from the overlap part between poly Si gate and source/drain regions. Fig. 3.8 and Fig. 3.9 are the nanowire length and nanowire number dependence of on-state capacitance, respectively. The parasitic capacitance can be respectively extracted from Figs 3.7 - 3.9, and the extracted values are nearly the same, which

means the parasitic capacitance is irrelevant to neither nanowire width/length nor nanowire number. Moreover, these parasitic capacitance values are also the same as the capacitance of an open circuit reference. So, we can remove the parasitic part by subtracting the open circuit capacitance from the nanowire nFET. Fig 3.10 shows the small difference in measured capacitance between a single nanowire nFET and a corresponding open circuit device. Fig. 3.11 is the intrinsic channel capacitance obtained after removing the parasitic capacitance by subtracting the open circuit capacitance from measured capacitance. Five different devices with all the same structure and parameters are shown to point out the significant random noise, which is originated from the limit of measurement equipment. Fig. 3.12 shows the calculated inversion charge amount, which is the purpose of capacitance measurement and also vital to mobility extraction. We can see, the five different devices have similar inversion charge with very little difference. Though the noise level in C-V curves is relatively high comparing to the small gate channel capacitance, thanks to the random nature of this noise, after integrating the Cgc-Vgs to the Qinv-Vgs, its influence in the inversion charge amount is quite small. Therefore the obtained intrinsic channel capacitance is adequate for accurate mobility extraction.

3.4 Carrier Mobility in Single Silicon Nanowire MOSFETs

After considering the influence of both parasitic resistance and parasitic capacitance, the intrinsic carrier mobility of single nanowire FETs is extracted with a high accuracy for both [110]- and [100]- direction silicon nanowire MOSFETs on (100) SOI. Fig. 3.13 compares extracted electron mobility of [110]-direction nanowire nFETs with different number of nanowires. The electron mobility in 54 μm -wide UTB is in good agreement with the (100) universal curve. The lower mobility in multiple nanowire nFETs is due to larger ratio of parasitic

resistance to the total resistance.

Fig. 3.14 and Fig. 3.15 show electron and hole mobility in FETs with single nanowire in [110]-direction. The mobility decreases with decreasing nanowire width for both electron and hole. It is found that hole mobility is higher than (100) universal curve even in a single nanowire FET, which originates from the effect of (110) side surface with high hole mobility.

Fig. 3.16 and Fig. 3.17 show electron and hole mobility in FETs with single nanowire in [100]-direction. The degradation of both electron and hole mobility is also seen in [100]-direction nanowires. For the tri-gate nanowire pMOS, the top surface and two side surface are all with (100) orientation, which has lower hole mobility than (110) surface, thus the high hole mobility is not seen in the [100]-direction nanowire.

And it is worthy noted that, for both electron and hole mobility, the mobility in 35 nm wide nanowire is very close to that in 25 nm wide nanowire, while significant decrease can be seen in nanowires with 15 nm and 11 nm width. Fig. 3.18 shows the width dependence of carrier mobility at $N_{inv} = 8 \times 10^{12}$ cm^{-2}. This width dependence indicates the possibility of significant roughness related scattering in these nanowire MOSFETs. In order to further analyze the mobility behaviors in the tri-gate silicon nanowires, low temperature measurement should be performed to separate different origins of scattering mechanisms.

3.5 Summary

In this Chapter, [100]- and [110]- direction NWs MOSFETs on (100)- oriented SOI with tri-gate structure are fabricated and characterized. The electron and hole mobility in "single" nanowire FETs is directly extracted from split C-V measurement for the first time. Mobility degradation is observed in either [110]- or [100]- direction nanowires. The electron and hole

mobility decreases as narrowing nanowire width due to process-induced roughness in narrower nanowires. It is found that hole mobility in [110]-direction silicon nanowires is higher than (100) universal curve even in a single nanowire FET, which originates from the effect of (110) side surface with high hole mobility. It indicates that surface orientation plays a key role in nanowire mobility.

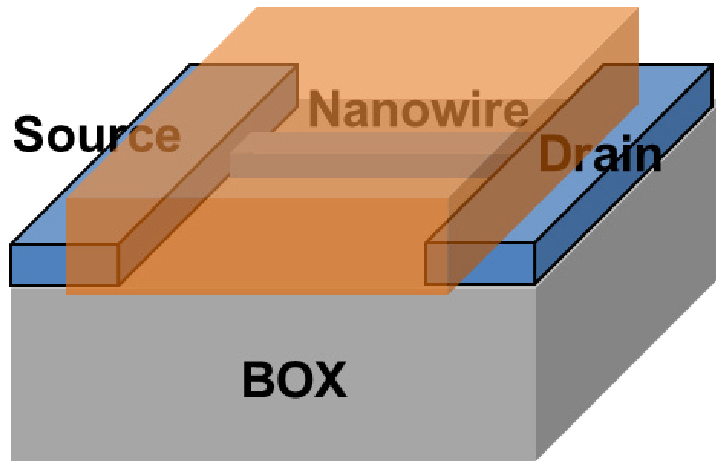

Fig. 3.1 3-D schematic of fabricated nanowire MOSFETs. The whole nanowire channel and part of the source/drain pad are covered by the poly-Si gate.

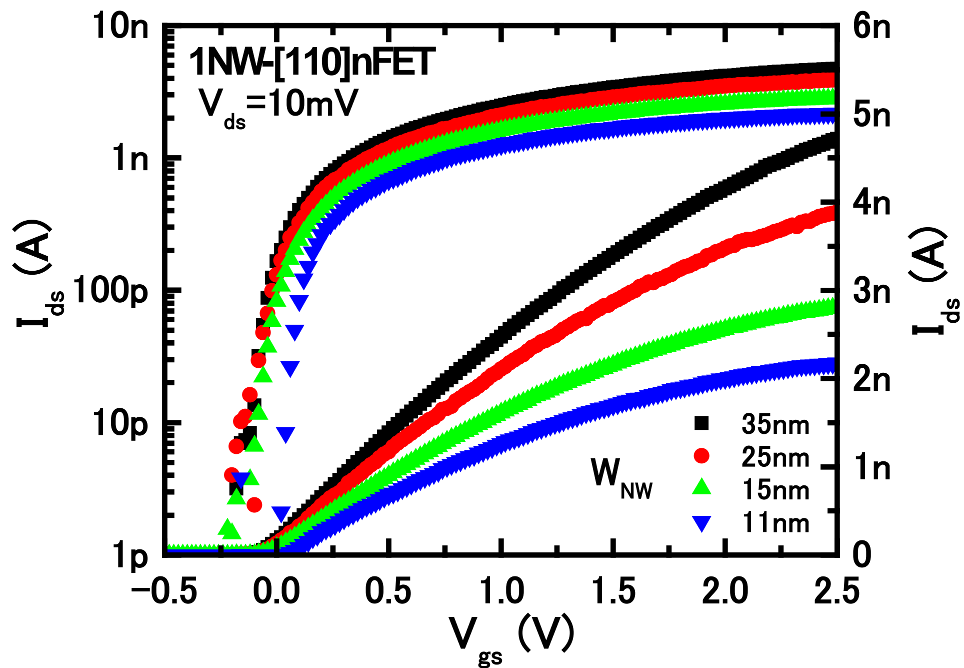

Fig.3.2 Measured I_{ds}-V_{gs} of [110]-direction single nanowire nFETs with L_{NW} = 53 μm.

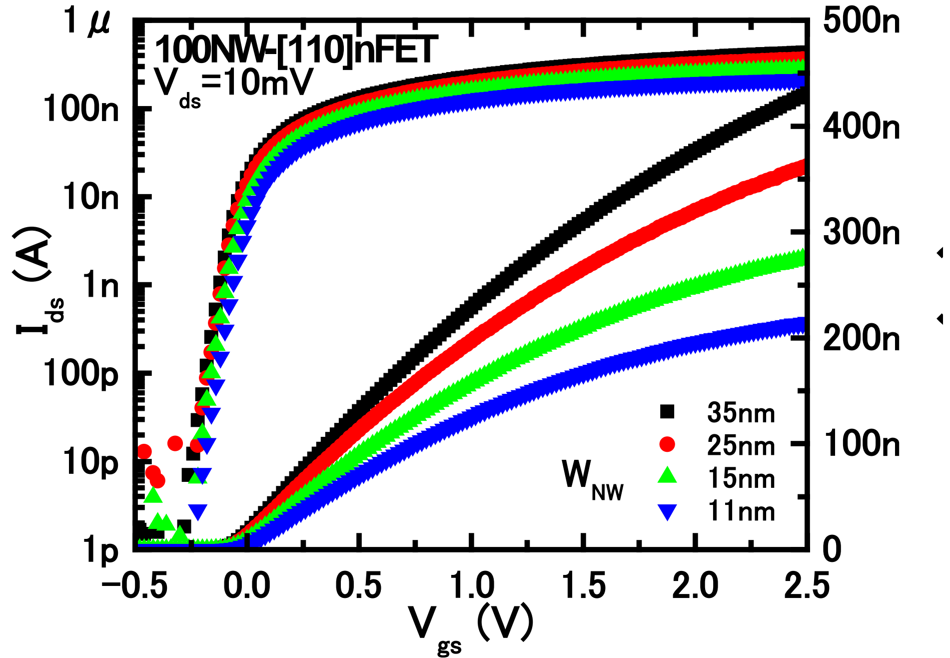

Fig.3.3 Measured I_{ds}-V_{gs} of [110]-direction nanowire nFETs with 100 NWs in the channel, L_{NW} = 53 μm.

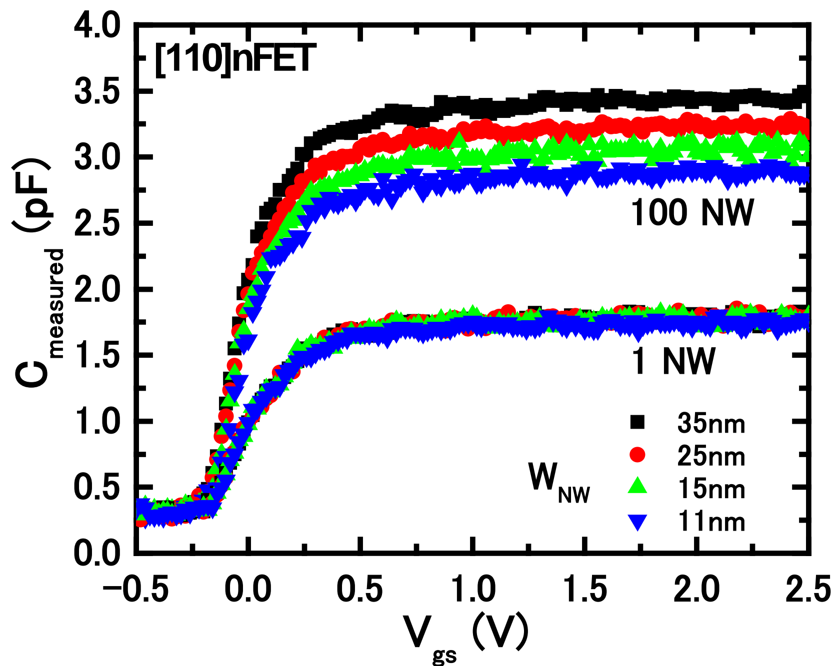

Fig.3.4 Measured C_{gc}-V_{gs} of NW-nFETs. Here, L_{NW} = 53 μm.

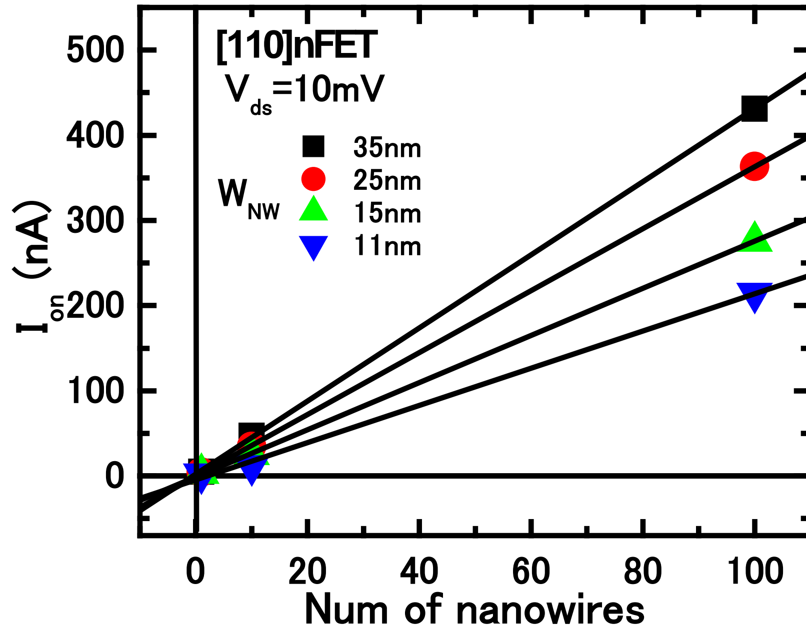

Fig.3.5 Nanowire number dependence of I_{on}. Here, L_{NW} = 53 μm.

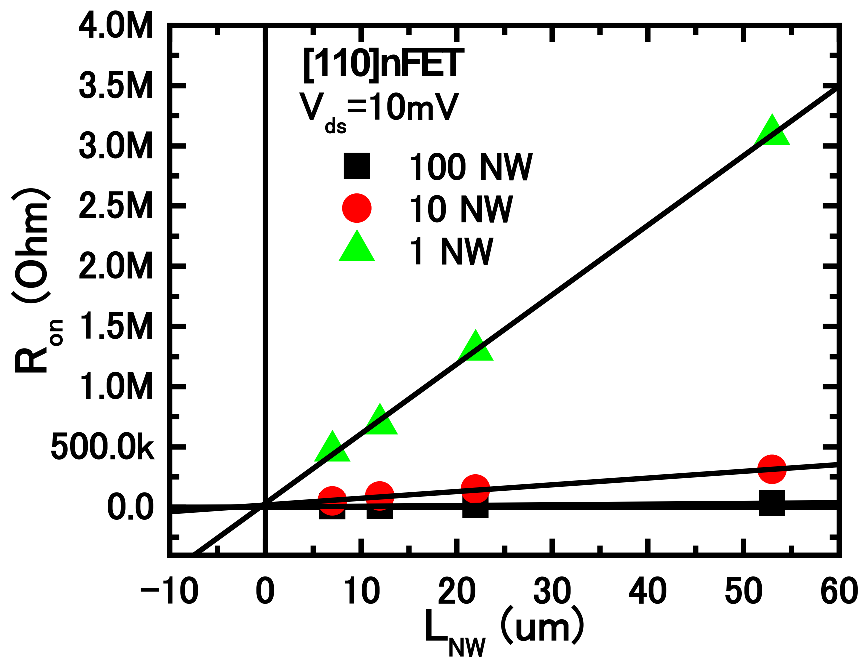

Fig.3.6 Nanowire length dependence of R_{on}. Here, W_{NW} = 35 nm.

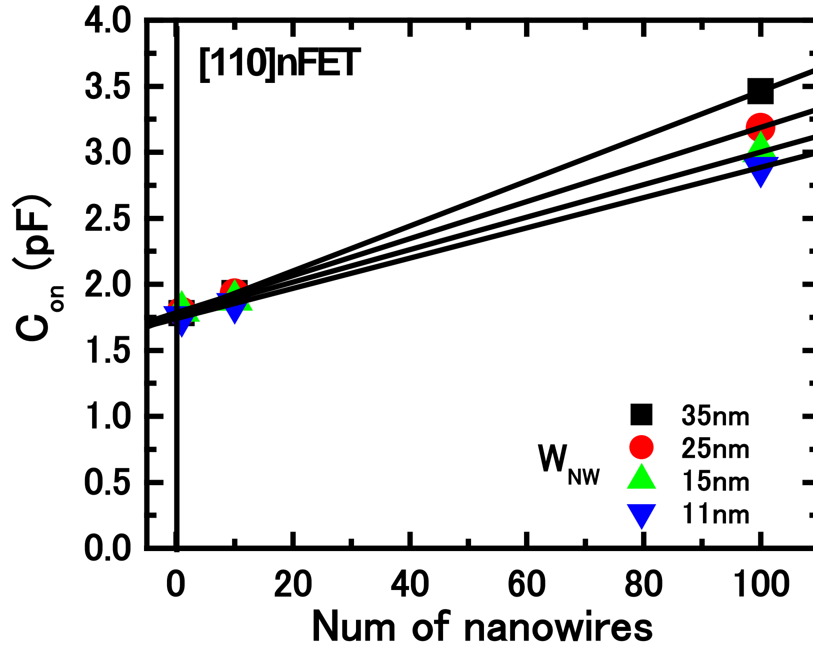

Fig.3.7 Nanowire number dependence of C_{on}. Here, L_{NW} = 53 μm.

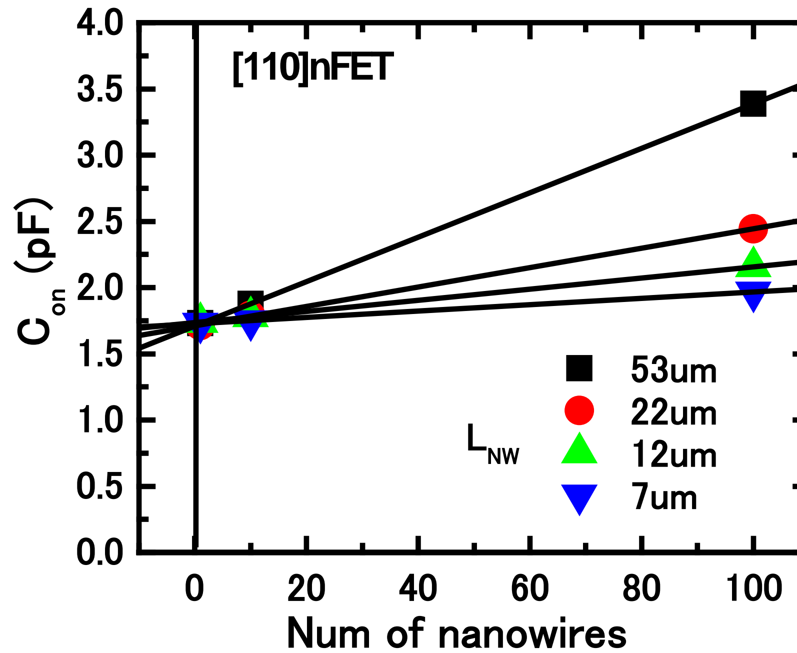

Fig.3.8 Nanowire number dependence of C_{on}. Here, W_{NW} = 35 nm.

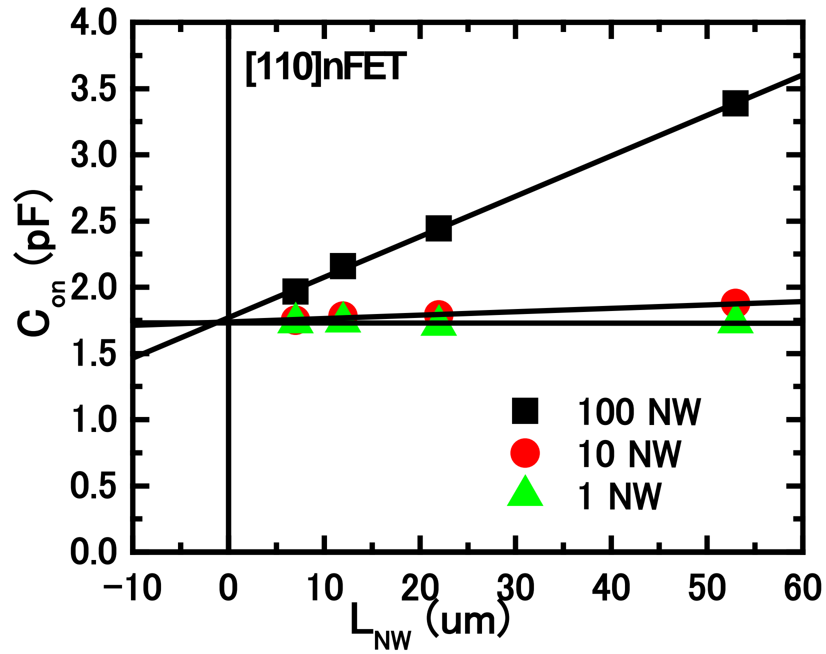

Fig.3.9 Nanowire length dependence of C_{on}. Here, W_{NW} = 35 nm.

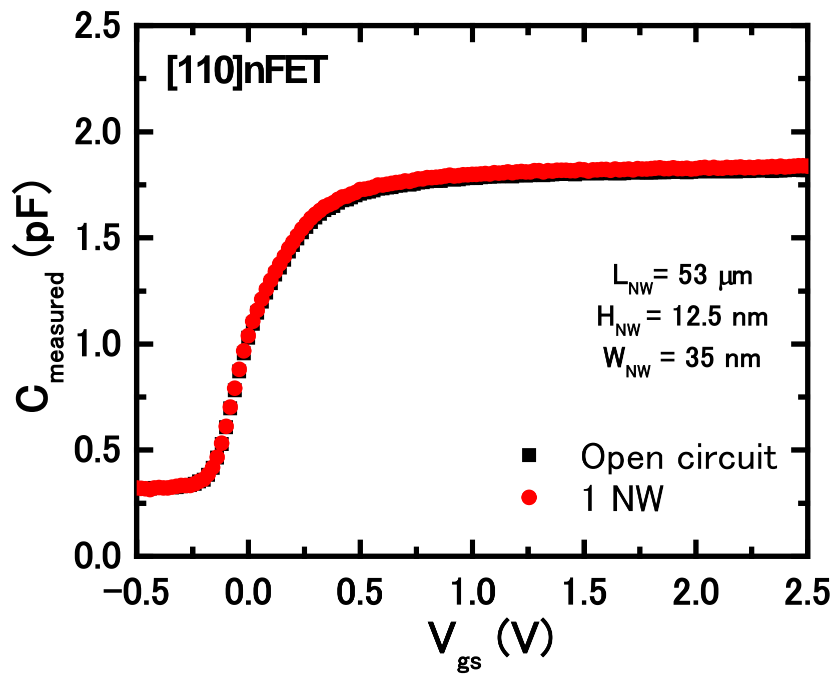

Fig.3.10 Measured capacitance in open circuit and single nanowire device.

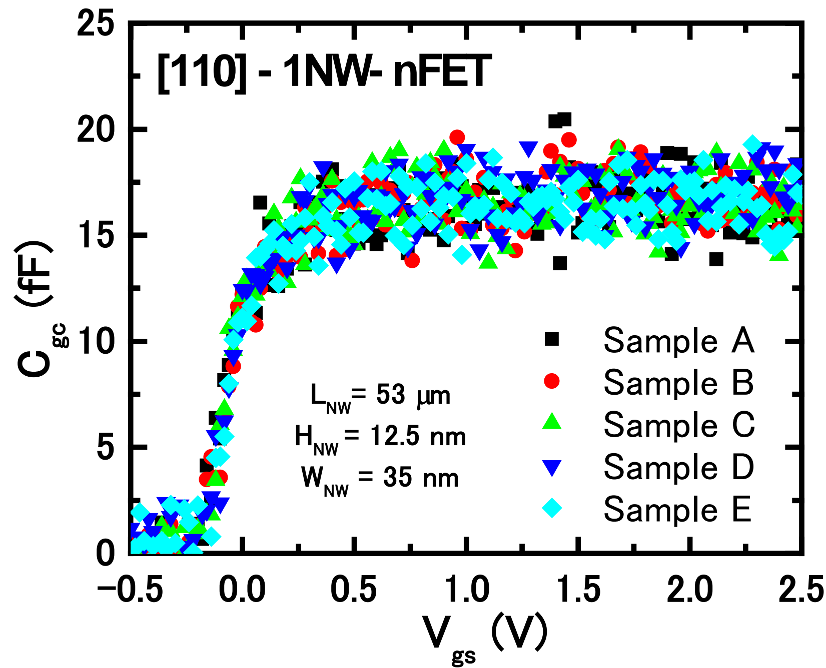

Fig.3.11 Intrinsic channel capacitance obtained after removing parasitic capacitance.

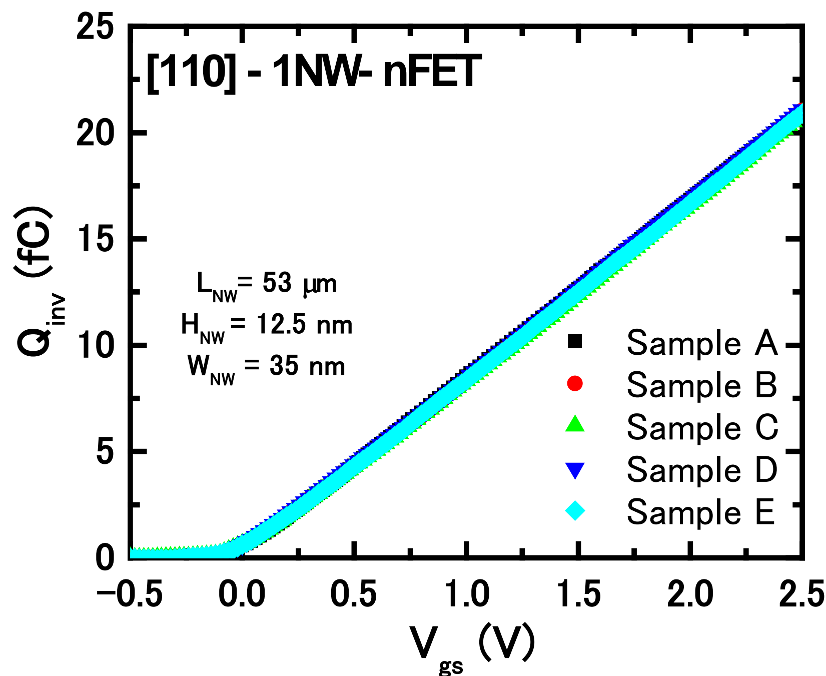

Fig.3.12 Calculated inversion charge for five different 1NW- nFETs.

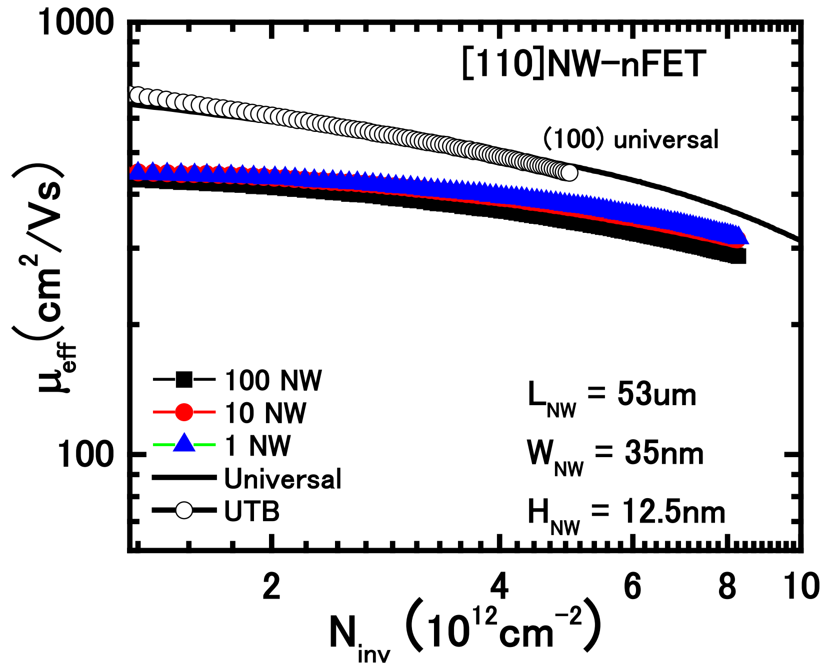

Fig.3.13 Electron mobility in [110] NW-nFETs with different number of nanowires in the channel.

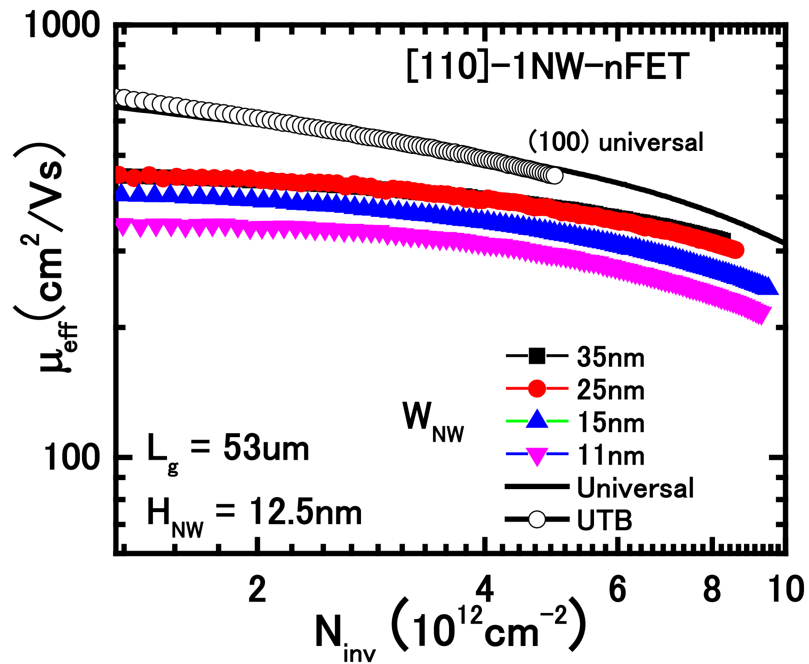

Fig.3.14 Electron mobility in [110] NW-nFETs with single nanowire in the channel.

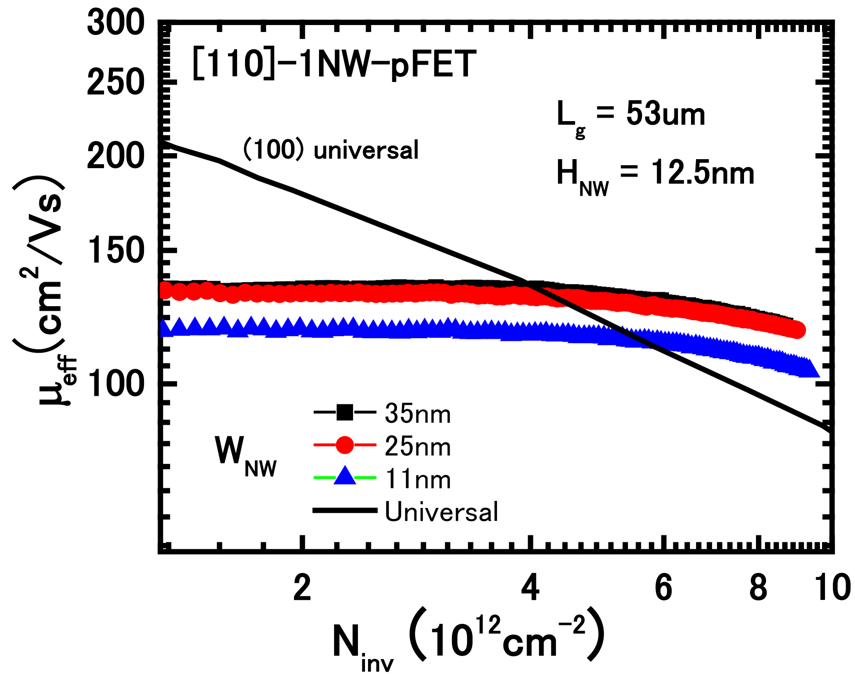

Fig.3.15 Hole mobility in [110] NW-pFETs with single nanowire in the channel.

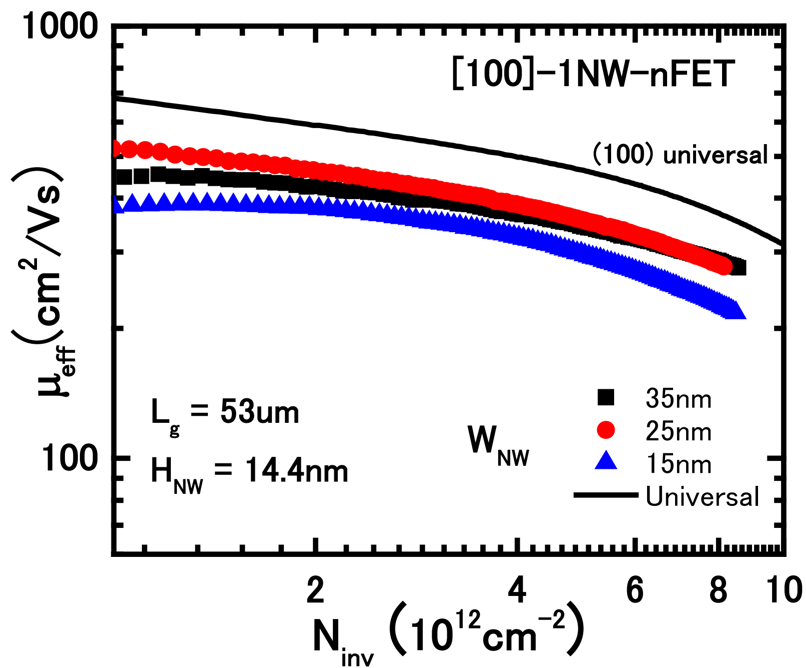

Fig.3.16 Electron mobility in [100] NW-nFETs with single nanowire in the channel.

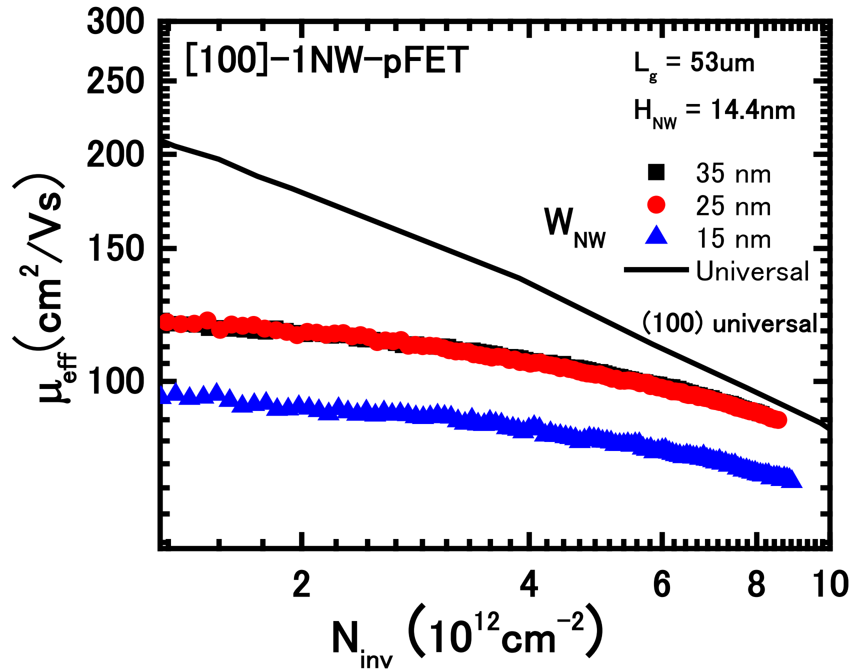

Fig.3.17 Hole mobility in [100] NW-pFETs with single nanowire in the channel.

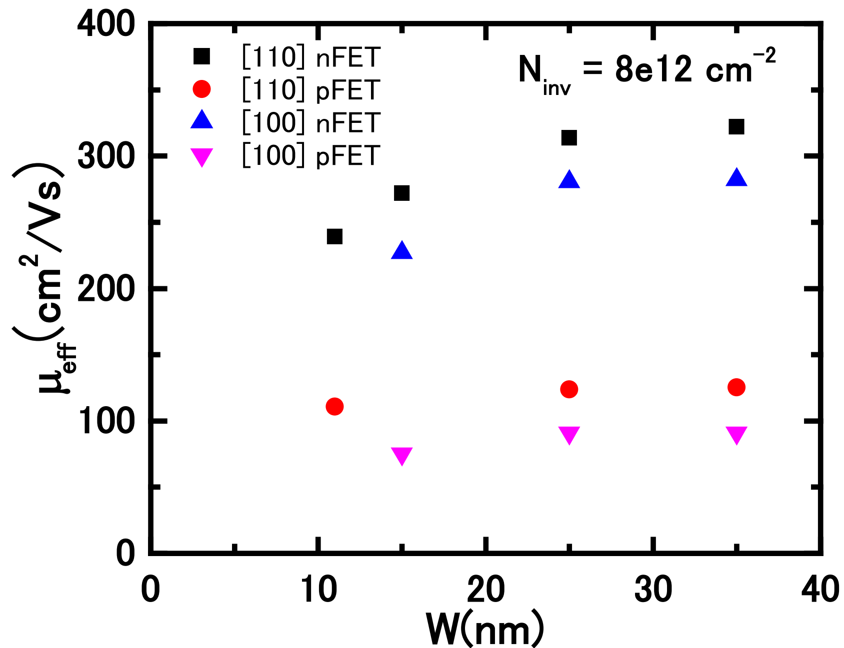

Fig.3.18 Width dependence of mobility at $N_{inv} = 8 \times 10^{12}$ cm^{-2} in single nanowire MOSFETs. Here, L_{NW} = 53 µm, H_{NW} is 12.5 nm in [110] nFET and [110] pFET, and 14.4 nm in [100] nFET and [100] pFET.

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Chapter 4

Analysis of Carrier Mobility in Silicon Nanowire MOSFETs

4.1 Introduction

Since mobility is one of the most important physical quantities determining the MOSFET performance, the physical mechanisms of the mobility lowering have been discussed by many authors [1-11]. For nanowire MOSFETs, some theoretical [12-14] and experimental [15-19] works had investigated the electronic transport properties, but not much experiments on the physical mechanism for carrier mobility behavior was done [17,18].

As discussed in the Chapter 2, carrier mobility behavior in MOSFET is dominated by three different scattering mechanisms. Thus the carrier mobility is affected by three parts, Coulomb scattering mobility ($\mu_{coulomb}$), phonon scattering mobility (μ_{phonon}) and surface roughness scattering mobility (μ_{sr}). $\mu_{coulomb}$ dominates the low electric field mobility and μ_{sr} affects mostly the high electric field mobility. And both Coulomb scattering and surface roughness scattering mechanisms have no temperature dependence, while μ_{phonon} has strong temperature dependence and dominate the mobility behaviors at higher temperature. In low temperature, μ_{phonon} will be suppressed, thus an enhancement in carrier mobility can be observed.

To understand the physical mechanisms that dominate mobility properties in nanowires, low temperature measurements are the most fundamental experiment method. At low temperature, the phonon scattering will be suppressed, thus the scattering mechanisms can be decomposed to be investigated thoroughly.

In this chapter, low temperature measurements are performed to investigate the mechanisms that dominate the mobility degradation in narrower nanowires.

4.2 Carrier Mobility at Low Temperature

Low temperature measurements are performed from room temperature (RT) down to 6 K. Fig. 4.1 – 4.3 shows the results of [110]-direction single Si nanowire MOSFETs on (100) SOI. The carrier inversion density (N_{inv}) dependence changes as lowering the temperature.

Fig. 4.4 and Fig. 4.5 show the temperature dependence of carrier mobility in [110]-NWs with H_{NW} of 12.5 nm and various nanowire widths. Effective carrier mobility saturates at temperature below 20 K, thus effective carrier mobility at 6 K can be considered as μ_{sr}, since μ_{phonon} is weak enough and can be ignored at such low temperature. The μ_{sr} degrades significantly as W_{NW} decreases, implies there is much stronger surface roughness related scattering in the narrower NWs.

Fig. 4.6 and Fig. 4.7 show the width dependence of carrier mobility in [110]- NWs at different temperature in double logarithmic plot. Considering the stronger quantum confinement in nanowire comparing to that in UTB SOI, there is a possibility of observing the diameter fluctuation induced δt_{SOI} scattering in wider nanowire. The slope in Fig. 4.6 and Fig. 4.7 is much smaller than the slope of 6 for the δt_{SOI} scattering case. δt_{SOI} scattering is not the reason of mobility degradation in our nanowire.

4.3 Phonon Scattering Limited Mobility

By using the Matthinessen's rule of $\frac{1}{\mu_{phonon}} = \frac{1}{\mu_{eff}} - \frac{1}{\mu_{eff}(6K)}$, μ_{phonon} in [110]-direction NW

nFETs on (100) SOI is extracted at different temperature in Fig. 4.8 – 4.11. For phonon scattering, there are two important components: phonon momentum ($p_{phonon} = \hbar\omega / c \sim K_B T / c \propto T$) and Fermi momentum ($p_{Fermi} = \hbar\pi^{0.5} N_{inv}^{0.5} \propto N_{inv}^{0.5}$) [22,23]. Due to the competition of these two factors, μ_{phonon} behavior follows the conventional model and decreases along with respect to N_{inv} at lower N_{inv} region; while in the higher N_{inv} region, where the Fermi momentum is larger than phonon momentum, the large angle scattering is restricted, and μ_{phonon} increases with respect to N_{inv}, as shown in Fig. 4.12. Due to the temperature dependence of phonon momentum, the N_{inv} value of the “transition point” within μ_{phonon} decreases as the temperature lowering, which can be seen in Fig. 4.10 and Fig. 4. 11.

The temperature dependence of phonon limited mobility in nanowires is shown in Fig. 4.13 and Fig. 4.14. The phonon scattering in the nanowire has little width dependence and the slope of the double logarithmic scale curve is in good agreement to the reported experimental value of -1.75 in planar bulk MOSFET. It confirms that μ_{phonon} degradation is small in nanowires with width and height larger than 10 nm, and indicates the mobility degradation in narrower nanowires is originated from the degradation of μ_{sr} in narrower nanowires.

4.4 Discussion on Mobility degradation mechanisms

Due to the top-down approach used in fabrication, the cross section of nanowires in this work is usually rectangular. Nanowire has four surfaces, one is supported by the BOX to form the tri-gate structure, and the other three surfaces are wrapped by the gate stack. These three surfaces contribute to the carrier conduction, and these surfaces are usually with different orientation as shown in Fig. 4.15. And due to the limit of fabrication process the roughness on the three surfaces

may be different. Usually, there is larger roughness in the two side surfaces, which is defined by lithography and etching.

Thus the effective mobility extracted experimentally by using $W_{eff} = W_{NW} + 2 \times H_{NW}$ as the channel width is actually a mixture of these three surfaces. With first order approximation, this effective mobility can be understood as the weighted average of mobility contribution from the three surfaces [20]. The weighted average of mobility is given by

$$\mu_{NW} = \mu_{top} \frac{W_{NW}}{W_{NW} + 2H_{NW}} + \mu_{side} \frac{2H_{NW}}{W_{NW} + 2H_{NW}},$$

Here, we define a factor called "side surface ratio" as,

$$\alpha = \frac{2H_{NW}}{W_{NW} + 2H_{NW}}.$$

Then, the nanowire mobility can be expressed as,

$$\mu_{NW} = (1-\alpha)\mu_{top} + \alpha\mu_{side} = \mu_{top} + \alpha(\mu_{side} - \mu_{top}).$$

μ_{top} is top surface mobility and μ_{side} is side surface mobility. In [110]-NWs on (100) SOI, the top surface is (100) and side surfaces are (110).

With this model, the width dependence of carrier mobility at low temperature is plot against the side surface ratio. Fig. 4.16 and Fig. 4.17 show α dependence of μ_{NW} at various temperatures. Since μ_{NW} at 6K corresponds to μ, top surface μ_{sr} (α=0) and side surface μ_{sr} (α=1) are successfully derived from these figures. Apparently, μ_{sr} of (110) side surfaces are severely degraded in both electrons and holes, possibly due to process-induced roughness..

In Fig. 4.18 and Fig. 4.19, measured μ_{NW} as well as extracted μ_{sr} and μ_{phonon} are plotted against α at 300K. Here, the blue line is the "ideal" μ_{NW} at 300K, which is obtained using universal (100) and (110) mobility [9]. In NW nFETs, measured μ_{NW} is on the ideal μ_{NW} line.

Although μ_{sr} of (110) side surfaces is degraded, electron mobility in the (110) side surface is originally low and the effect of degraded μ_{sr} is very small. It is confirmed that the decrease in μNW in narrower NW nFETs is simply caused by low electron mobility in side (110) surface.

In NW pFETs, on the other hand, measured μ_{NW} is much smaller than the ideal μ_{NW}, and extracted μ_{sr} and μ_{phonon} are comparable. Ideally, μ_{NW} should increase in narrower NW pFETs thanks to high hole mobility in side (110) surface. However, it is found that μ_{NW} in narrower NW pFETs is severely degraded because high mobility in side surfaces is seriously degraded by surface roughness. In order to take full advantage of high (110) hole mobility in NW pFETs, the improvements of side surface quality are mandatory.

4.5 Summary

In this chapter, low temperature measurements were performed with [110]- direction NWs on (100) SOI to investigate the scattering mechanisms in tri-gate silicon nanowire. Surface roughness limited mobility and phonon limited mobility are extracted and analyzed. The phonon momentum and Fermi momentum competition phenomenon in phonon limited mobility is observed in nanowire mobility behaviors below 100 K. The phonon scattering has little nanowire width dependence, indicating that the mobility degradation in our tri-gate nanowire MOSFETs is caused by the surface roughness scattering. The Mobility degradation mechanisms in NW FETs are analyzed with an α-factor model. It is found that, the serious process-induced roughness on the side surface is the main source of mobility degradation in NW pFETs.

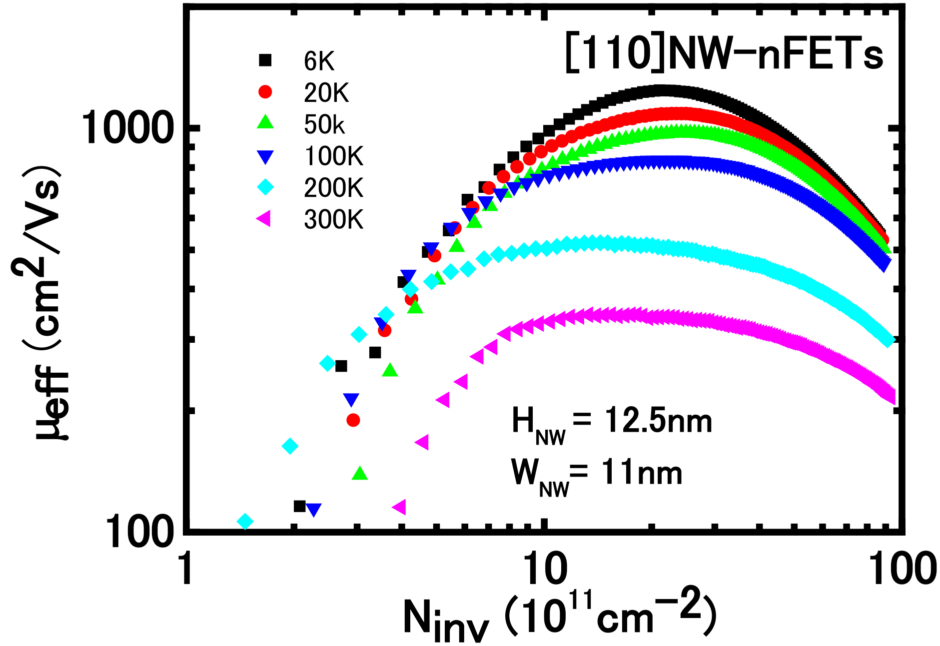

Fig. 4.1 N_{inv} dependence of electron mobility in NW with W_{NW} of 11 nm from 6 K to RT. Here, L_{NW} = 53 μm.

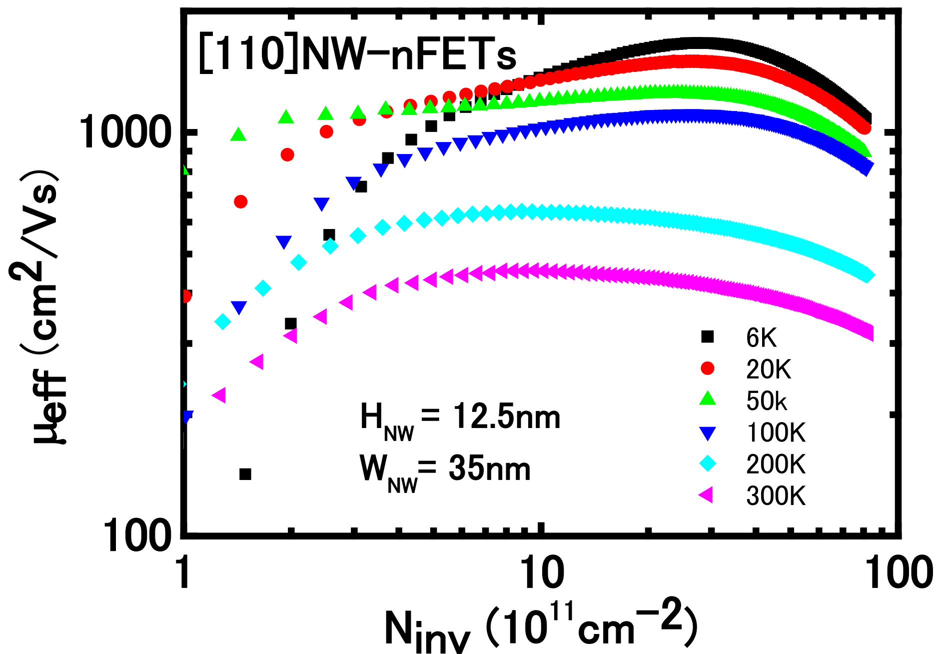

Fig. 4.2 N_{inv} dependence of electron mobility in NW with W_{NW} of 35 nm from 6 K to RT. Here, L_{NW} = 53 μm.

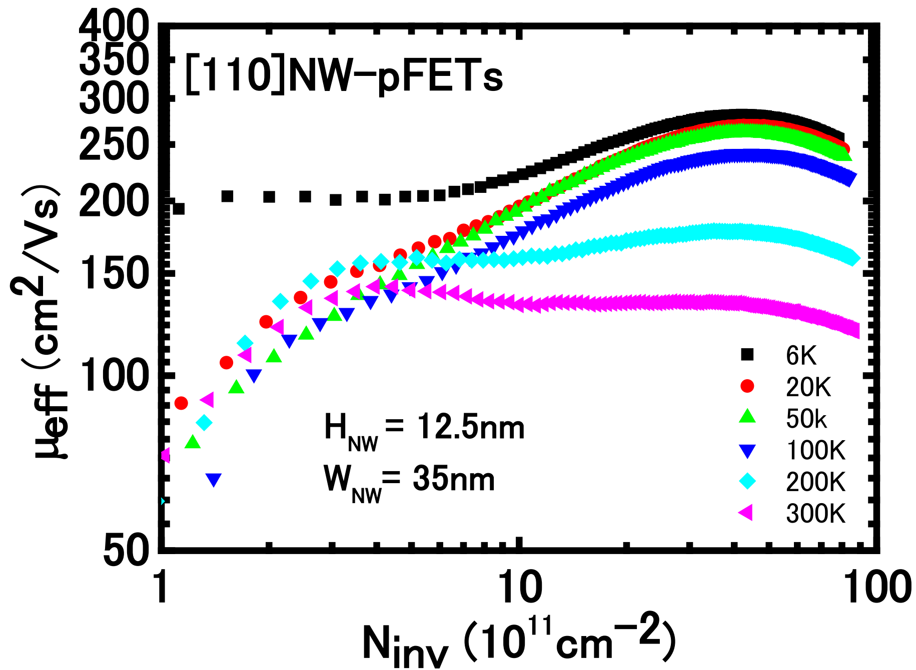

Fig. 4.3 N_{inv} dependence of hole mobility in NW with W_{NW} of 35 nm from 6 K to RT. Here, L_{NW} = 53 μm.

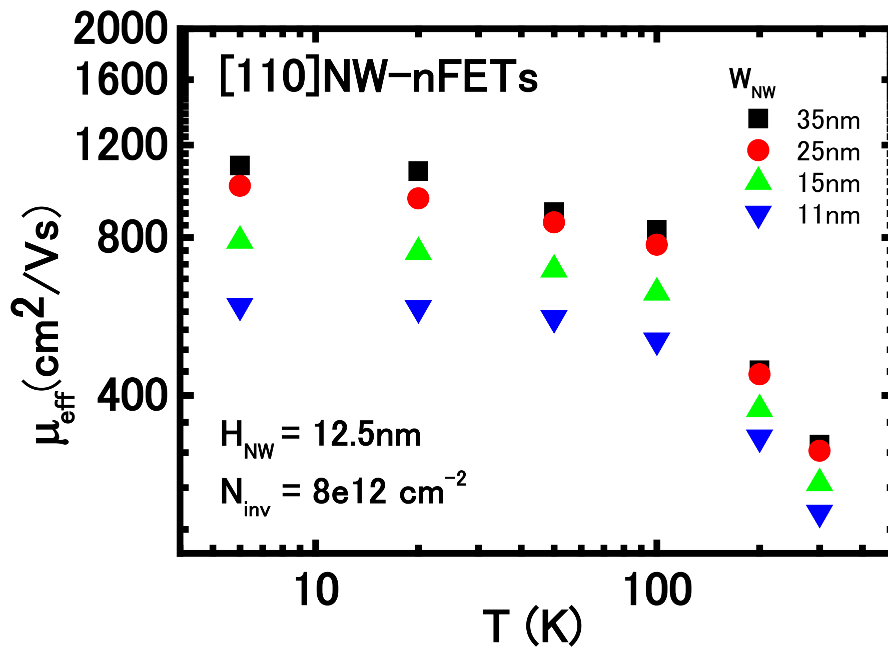

Fig. 4.4 Temperature dependence of electron mobility at $N_{inv} = 8 \times 10^{12}$ cm^{-2}. Here, L_{NW} = 53 μm.

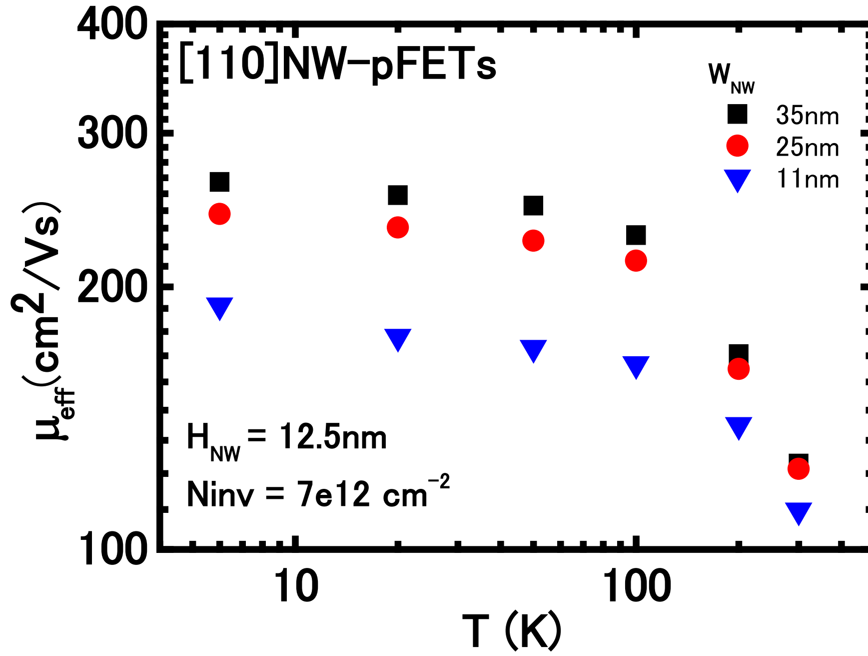

Fig. 4.5 Temperature dependence of hole mobility at $N_{inv} = 7 \times 10^{12}$ cm^{-2}. Here, L_{NW} = 53 μm.

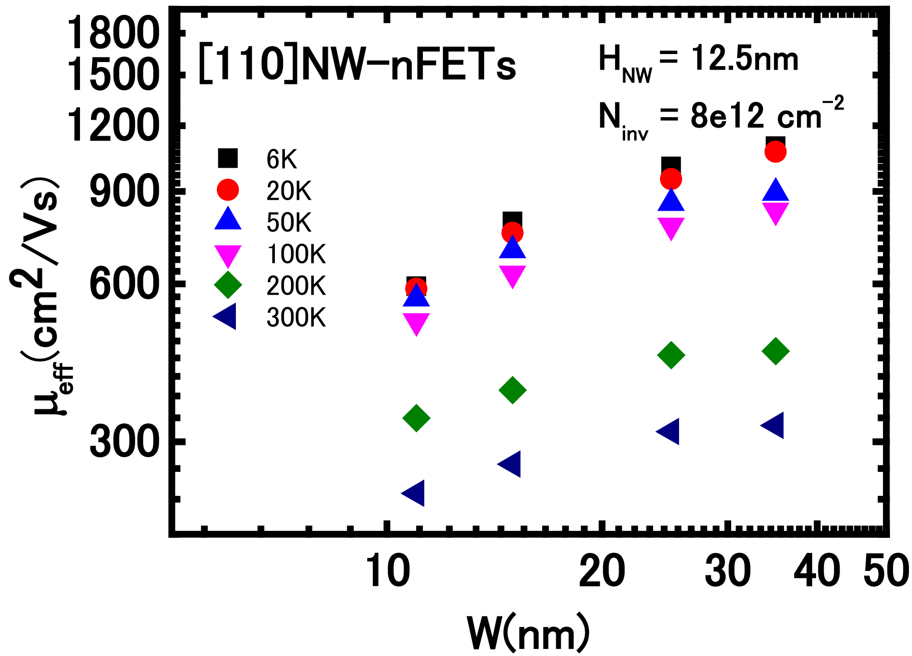

Fig. 4.6 Nanowire width dependence of electron mobility at $N_{inv} = 8 \times 10^{12}$ cm^{-2}. Here, L_{NW} = 53

μm.

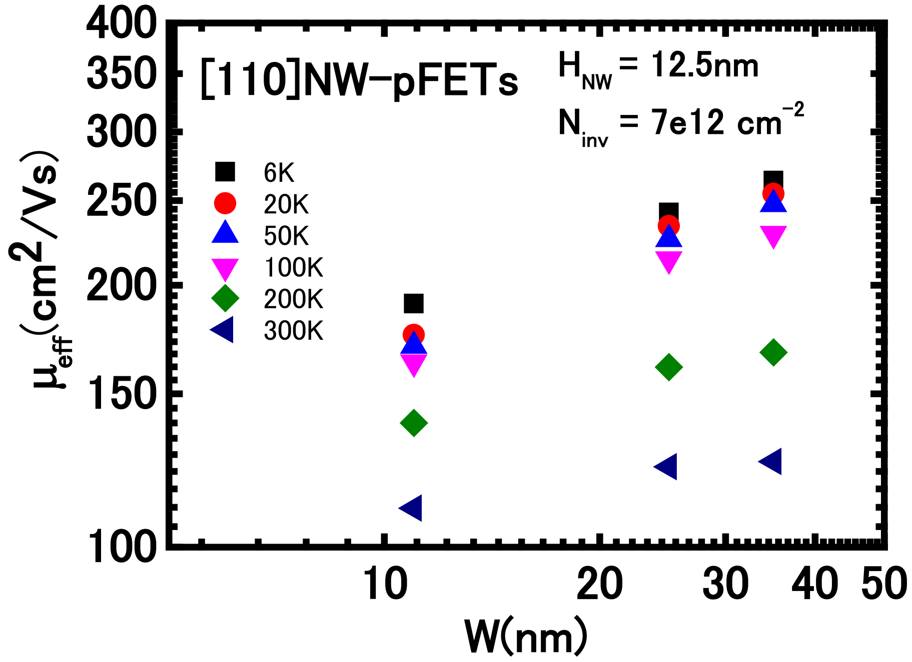

Fig. 4.7 Nanowire width dependence of hole mobility at $N_{inv} = 7 \times 10^{12}$ cm^{-2}. Here, L_{NW} = 53 μm.

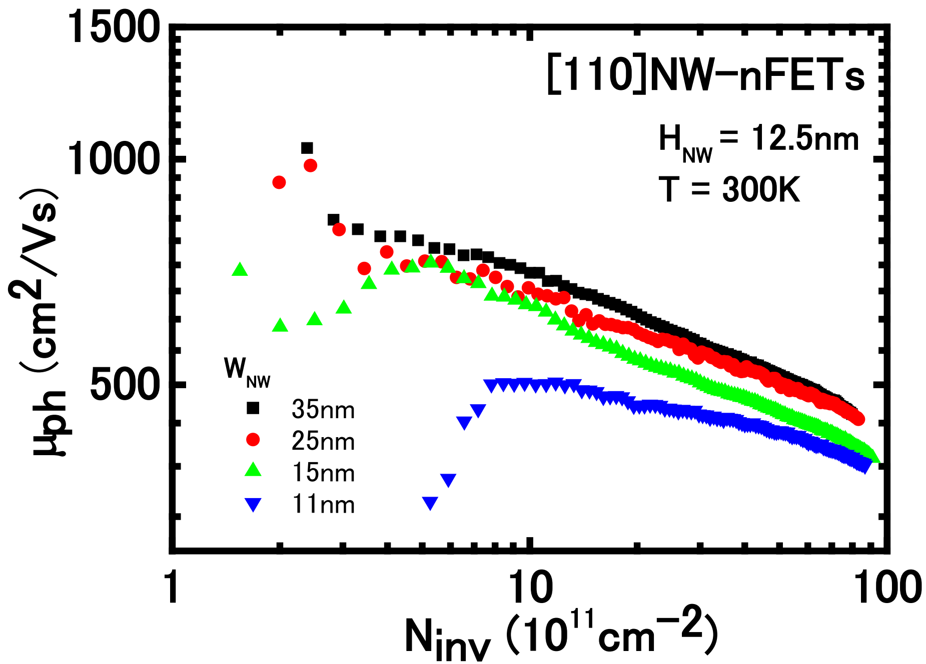

Fig. 4.8 Extracted phonon limited mobility at RT. Here, L_{NW} = 53 μm.

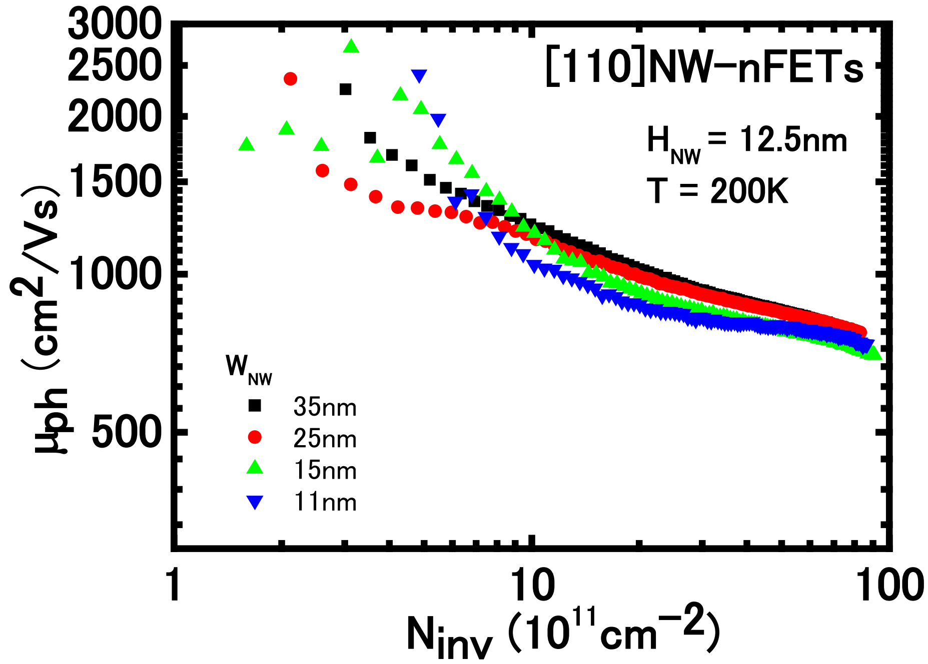

Fig. 4.9 Extracted phonon limited mobility at 200 K. Here, L_{NW} = 53 μm.

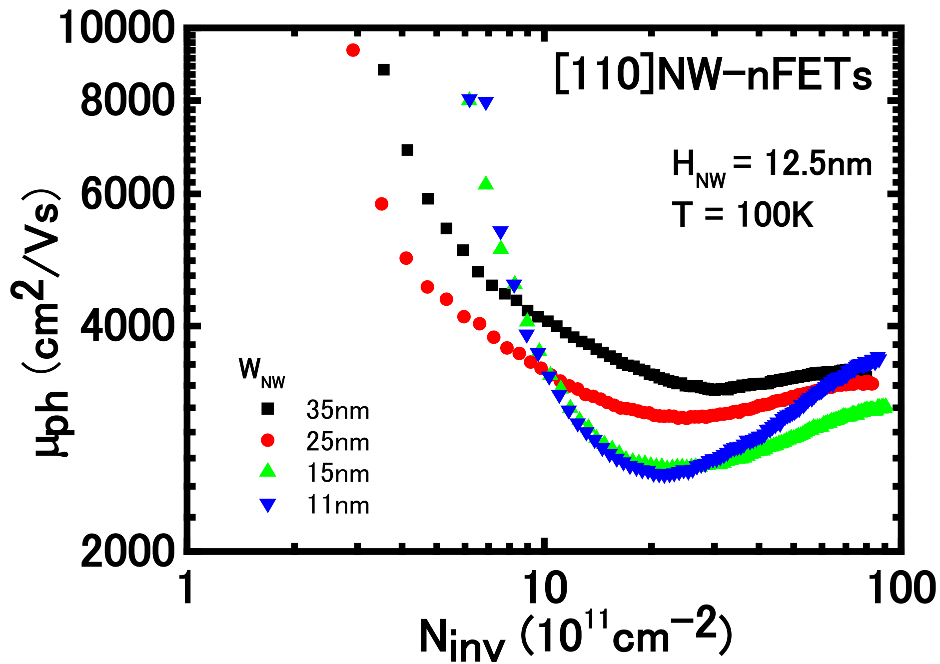

Fig. 4.10 Extracted phonon limited mobility at 100 K. Here, L_{NW} = 53 μm.

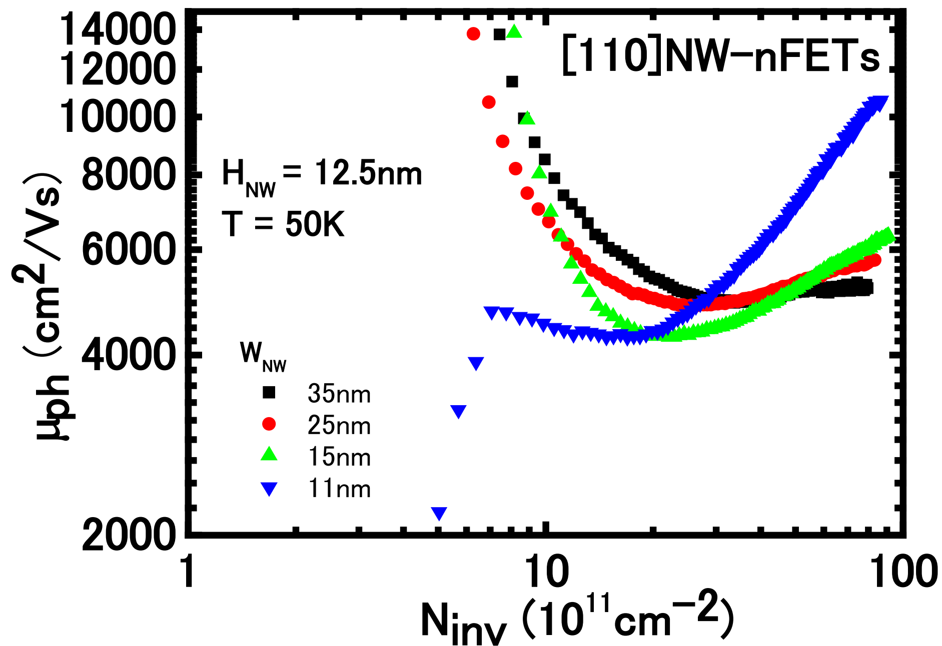

Fig. 4.11 Extracted phonon limited mobility at 50 K. Here, L_{NW} = 53 μm.

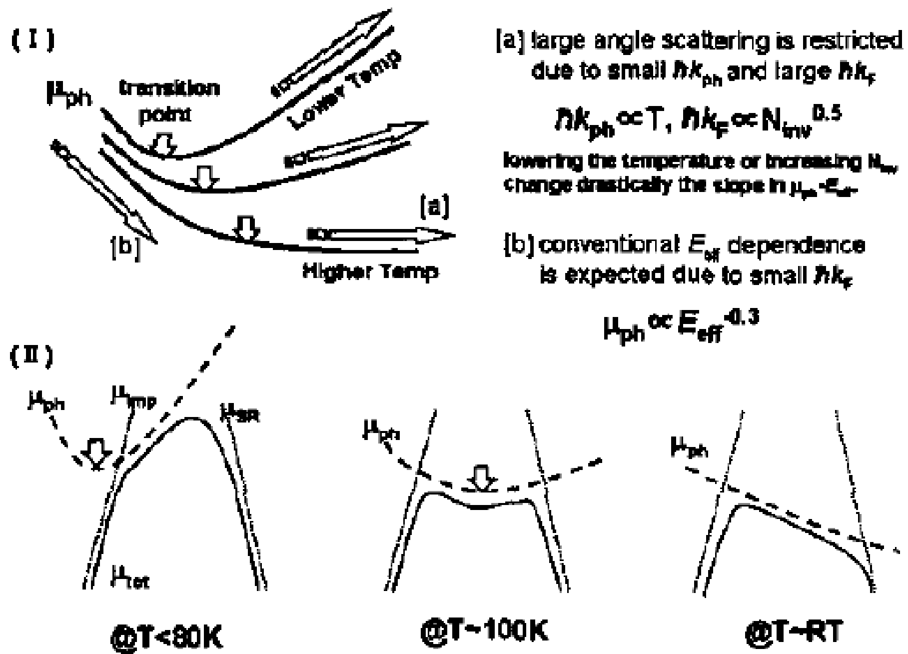

Fig. 4.12 (I) Schematic illustration of N_{inv} dependence of phonon limited mobility at medium low temperature. (II) Temperature dependence of phonon limited mobility [22].

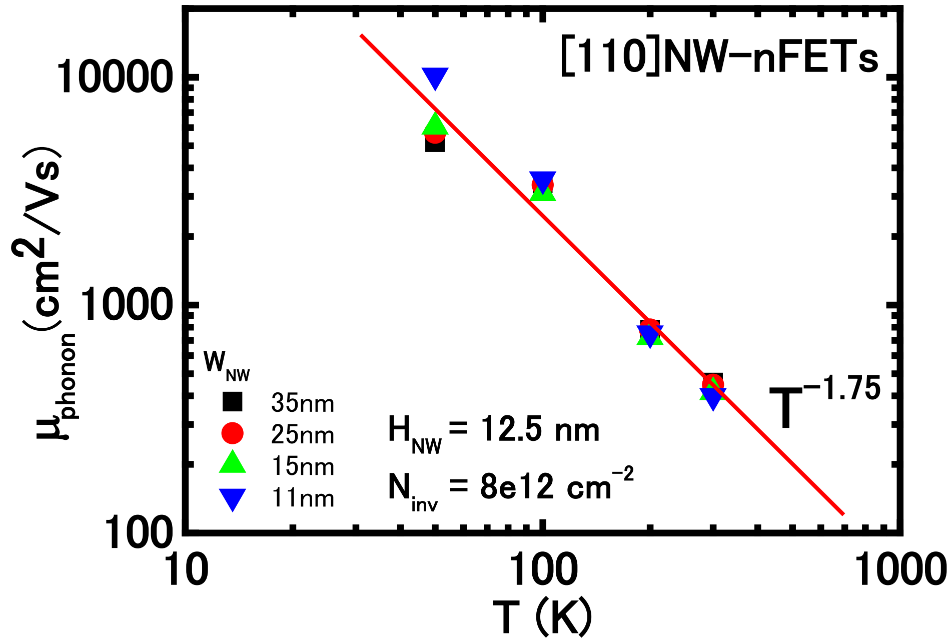

Fig. 4.13 Temperature dependence of phonon limited mobility in NW nFETs. Here, L_{NW} = 53 μm.

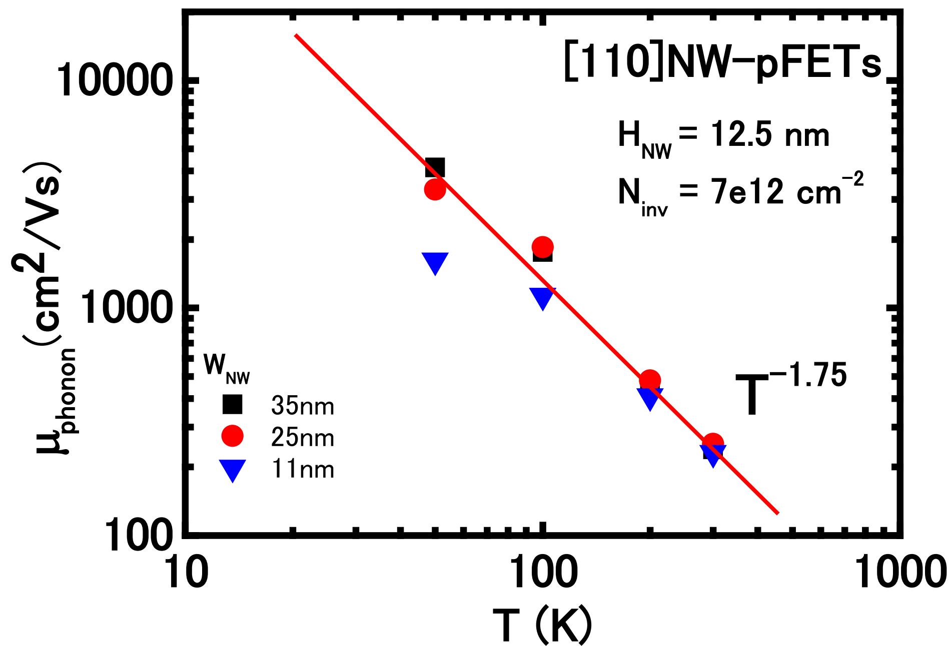

Fig. 4.14 Temperature dependence of phonon limited mobility in NW pFETs. Here, L_{NW} = 53 μm.

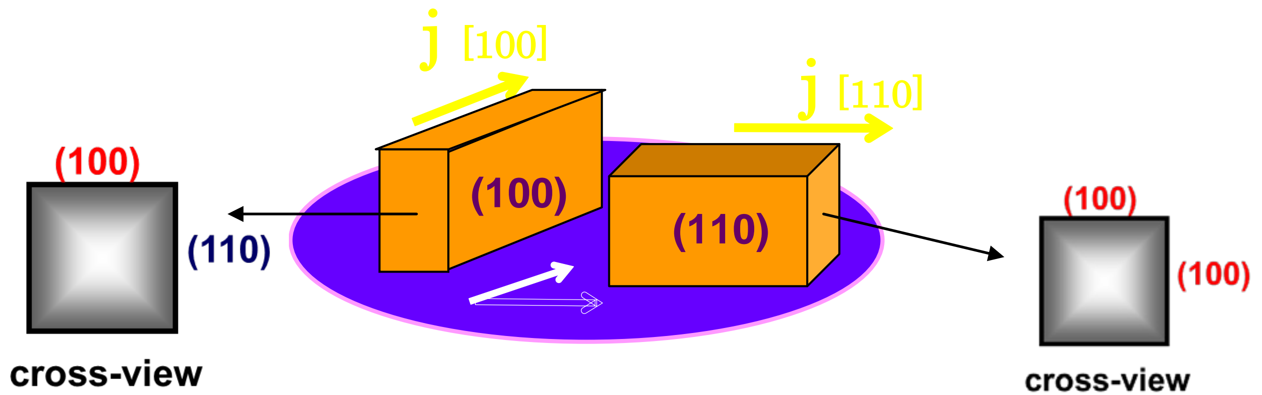

Fig. 4.15 Schematics of [100]- and [110]- directed nanowires and their relative side surface orientation.

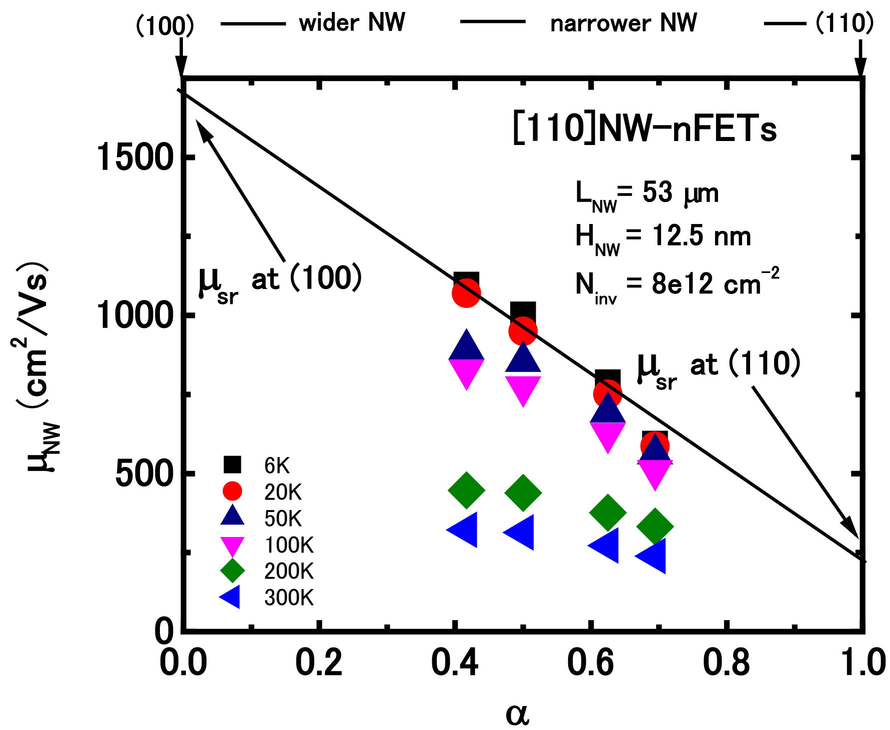

Fig. 4.16 Side surface ratio dependence of electron mobility at $N_{inv} = 8 \times 10^{12}$ cm^{-2}.

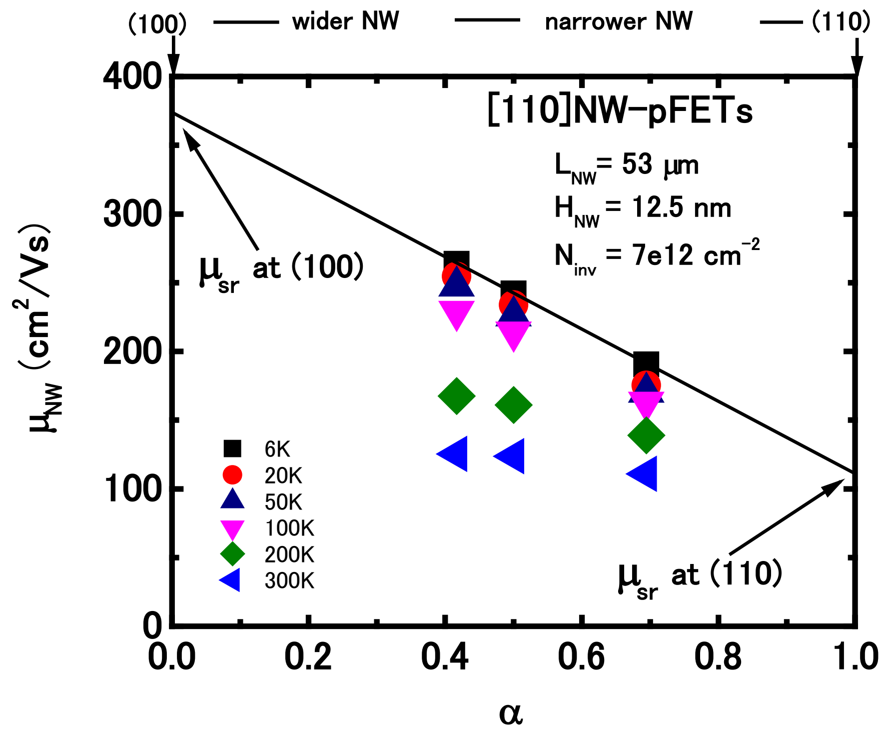

Fig. 4.17 Side surface ratio dependence of hole mobility at $N_{inv} = 7 \times 10^{12}$ cm^{-2}.

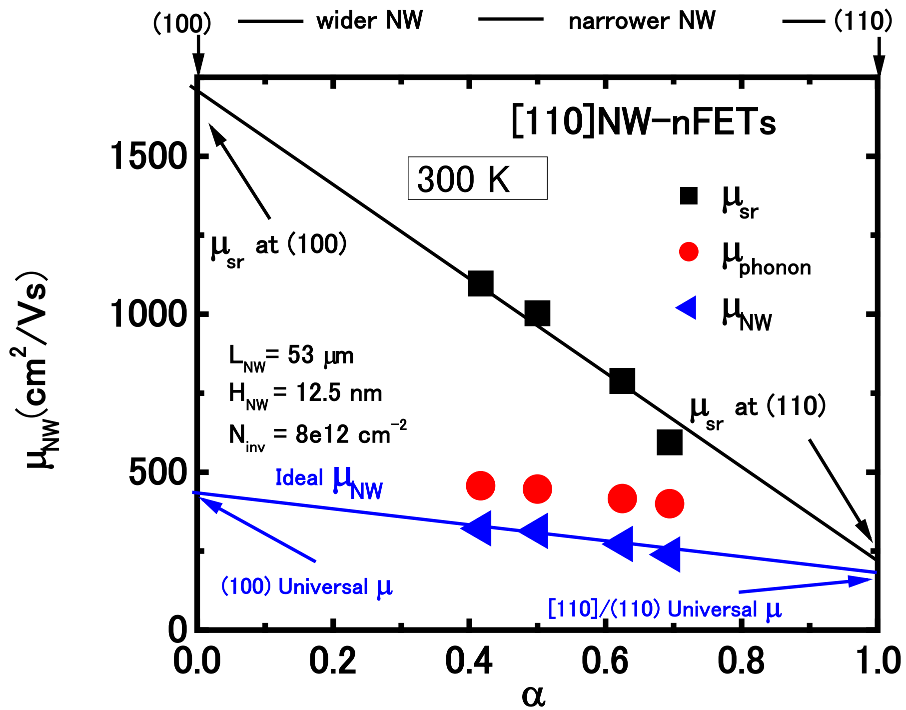

Fig. 4.18 Side surface ratio dependence of electron mobility at RT in [110] NW-nFETs.

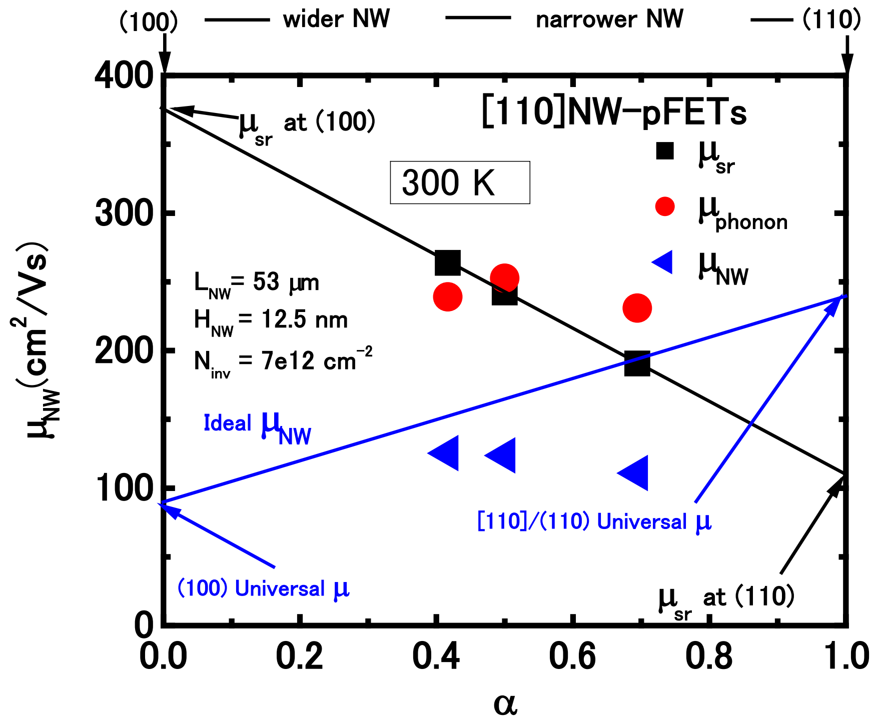

Fig. 4.19 Side surface ratio dependence of hole mobility at RT in [110] NW-nFETs.

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Chapter 5

Variability in Silicon Nanowire MOSFETs

5.1 Introduction

The electrical characteristic variability of metal-oxide-semiconductor field-effect transistors (MOSFETs) is one of the important issues in developing scaled very-large-scale integration (VLSI) devices. Along with the rapid device scaling, the variability turns to be one of the critical concerns [1-11]. Threshold voltage (V_{TH}) variability considerably degrades the stability of integrated circuits. The minimum operation voltage (V_{min}) in logic circuits is limited by device variability, and static random access memory (SRAM) fails at a low supply voltage owing to transistor unbalance in a cell. It is now mandatory to take this variability into consideration in circuit design to maintain a high yield.

Generally, the variability is classified into two components [12,13]. One is the random component, which has no positional correlation and obeys the normal distribution. For example, the V_{TH} variation between a pair of MOSFETs is a random component. The other is the systematic component, which varies in the X- and Y-directions and does not exhibit a normal distribution. For example, intrawafer variability caused by process variability in a wafer and intrachip variability caused by layout variability in a chip are systematic components.

Prior to the significant miniaturization of MOSFETs, the systematic component was much larger than the random component. It is well known that the random component increases with MOSFET miniaturization, since the random component of V_{TH} variation is proportional to

$1/\sqrt{LW}$ [1], where L and W are the gate length and gate width, respectively. As a result, the random component is comparable to or even larger than the systematic component in the latest LSIs.

It is possible to reduce systematic variability using the improved process uniformity (e.g., advanced process control, and design for manufacturing) [14,15]. However, it is difficult to reduce the random component because it stems from the random dopant fluctuations (RDFs) in the channel, which is the dominant origin of random V_{TH} variability in conventional bulk MOSFETs [16-20]. It is reported that the variabilities of both drain induced barrier lowering (*DIBL*) [21] and current-on-set voltage (*COV*) [22-26] are also caused by RDF. It has been recently found that the *DIBL* variability leads to the instability of SRAM cells [27]. It also turns out that the drain-current variability is enhanced by the *COV* variability [21,22]. Therefore, the suppression of not only V_{TH} variability but *DIBL* and *COV* variability is essential for further device scaling and higher integration.

Recently, it is shown that intrinsic channel fully depleted (FD) silicon-on-insulator (SOI) MOSFETs have not only a smaller V_{TH} variability but also smaller *DIBL* and *COV* variabilities owing to the absence of RDF [28]. However, the *DIBL* and *COV* variabilities still remain, possibly owing to the variability of workfunction in the metal gate electrode, and further reduction of variability is strongly required for better circuit performance variability and SRAM stability.

In this chapter, the variabilities of threshold voltage (V_{TH}), drain-induced barrier lowering (*DIBL*), and current onset voltage (*COV*) in intrinsic channel silicon nanowire MOSFETs were evaluated and compared with those of conventional bulk and fully depleted (FD) silicon-on-insulator (SOI) MOSFETs. The random component of variability is extracted by a

"within-device" variability method to exclude the systematic component. It is found that the within-device variabilities of *DIBL* and *COV* as well as V_{TH} are extremely small in intrinsic channel nanowire MOSFETs owing to the non-intentionally doped channel and small gate workfunction variability. The intrinsic channel nanowire MOSFET is promising for a future scaled device structure in terms of not only the short channel effect suppression but also the variability suppression.

5.2 Experiment Method

Intrinsic channel tri-gate silicon nanowire nFETs with [110] channel direction were fabricated on (100) SOI wafers with a 24-nm-thick SOI film [29]. A polycrystalline Si gate and 4 nm SiO_2 are used as gate stacks. No impurities are intentionally doped into the channel region. Raised S/D with 25-nm-thick epi-Si is employed to reduce S/D resistance.

The nanowire width W_{NW} is fixed to 30 nm, and the nanowire gate length L_g is varied (300 nm, 1 μm, and 5 μm). The nanowire FETs are measured in both the linear region (V_{ds} =50mV) and saturation region (V_{ds} =1.2V). Figure 5.1 shows the I_{ds}-V_{gs} characteristics of 18 nanowire nFETs with W_{NW} = 30 nm and L_g = 300 nm in a wafer in the linear and saturation regions. Some variations of characteristics are observed.

In this study, V_{TH} is evaluated on the basis of two definitions: V_{THEX} and V_{THC}. V_{THC} is V_{TH} defined by subthreshold constant current ($I_0=10^{-8}$ x W/L) and V_{THEX} is extrapolated V_{TH} (the V_{gs} intercept of the tangent line with the largest slope in I_{ds} - V_{gs}). V_{THEX} is a vital parameter that determines drain current at on-state, while V_{THC} is also an indispensable parameter that determines off-state current. The variabilities of both V_{THEX} and V_{THC} largely affect the circuit variability and performance; therefore, the variabilities of these parameters should be intensively

examined.

Since the number of measured FETs with the same size is only 18 and the measured variability may include a systematic component, within-device variability (difference between forward and reverse devices by exchanging S/D) is mainly evaluated in order to examine the intrinsic variability of devices [30, 31].

5.3 V_{TH} Variability in Tri-gate Silicon Nanowire MOSFETs

The statistical characteristics of V_{TH} variation are evaluated using the normal probability plot. Figure 5.2 shows the normal probability plots of V_{THC} and V_{THEX} in both the linear and saturation regions in 18 measured nanowire nFETs with W_{NW} = 30 nm and L_g = 300 nm. The V_{THEX} variations show good linearity in the probability plot, indicating a normal distribution with extrapolated threshold voltage. The slope of this plot gives $1/\sigma V_{THEX}$, and the variability of V_{THEX}, particularly in the linear region, is small even in a wafer, where σV_{THEX} is the standard deviation of V_{THEX}. On the other hand, the V_{THC} variation plots show poor linearity, indicating that there are significant wafer-level systematic components in the V_{THC} variation data.

The variability in MOSFETs increases when device area decreases [1]. The measured σV_{THEX} data in linear region are plotted in the Pelgrom plot in Fig. 5.3, and compared with the data of conventional bulk and FD SOI references [28]. The conventional bulk and FD SOI MOSFETs are fabricated by the 65 nm technology. L_g is 60 nm, and gate width W_g is varied from 500 nm to 2 μm. The thickness of the SiON gate dielectric is 2.0 nm for both the bulk and SOI devices. The channel doping is approximately 2×10^{18} cm^{-3} for the bulk while the channel is not intentionally doped for FD SOI MOSFETs.

The slope of the Pelgrom plot, A_{VT}, is a conventional index of Vth variation and is given by

$$\sigma V_{TH} = A_{VT} \frac{1}{\sqrt{LW}}. \tag{1}$$

Noted that, in the case of a tri-gate structure nanowire, we use the effective channel width $W_{eff} = 2H_{NW} + W_{NW}$ for the W in the equation above, where H_{NW} is the nanowire height. In Fig. 5.3, compared with bulk nFETs (A_{VT}=4.25) and SOI nFETs (A_{VT}=1.36), a clear variability suppression can be seen in nanowire nFETs. The slope A_{VT}=0.71 is close to the "universal line" of A_{VT}=0.6 reported in ref. 32, indicating that the systematic component is small enough in V_{THEX} in the linear region and the present variability data are validated.

However, the variability data in V_{THC} in Fig. 5.2 and Fig. 5.4 apparently include the systematic components. In order to extract the random component of V_{THC} variation, the difference in V_{THC} values ($\Delta V_{THC} = V_{THC\text{-}forward} - V_{THC\text{-}reverse}$) of two different source/drain configurations, that is, forward and reverse configurations, was measured [30,31], instead of measuring those of paired transistors. This differential value gives an index of local within-device variability because the potentials of the source or drain regions within a device are significantly different owing to the random displacement of impurity dopants and random configuration of gate workfunction among others. Note that this within-device variability method is applicable to only the saturation region.

Fig. 5.5 shows the normal probability plots of ΔV_{THC} of intrinsic channel nanowire MOSFETs in the saturation region, compared with those of bulk and FD SOI MOSFETs with almost the same gate areas. ΔV_{THC} of nanowire MOSFETs shows better linearity and smaller variability than V_{THC} in Fig. 5.3. This result indicates that the random within device component of V_{THC} variation is successfully extracted using the V_{THC} forward and reverse difference. Moreover, from the slope of the normal probability plot, the standard deviation of ΔV_{THC}, $\sigma\Delta V_{THC}$, is much

smaller in nanowire MOSFETs than in bulk and FD SOI MOSFETs. Fig. 5.6 shows a comparison of Pelgrom plots of $\sigma\Delta V_{THC}$ in nanowire, bulk, and FD SOI MOSFETs. It is found that $\sigma\Delta V_{THC}$ is plotted on straight lines in the Pelgrom plots and an extremely small A_{VT} of 0.17 is achieved in nanowire MOSFETs.

5.4 DIBL Variabilities in Tri-gate Silicon Nanowire MOSFETs

DIBL is defined as

$$DIBL = \frac{V_{TH_saturation} - V_{TH_linear}}{V_{ds_saturation} - V_{ds_linear}}. \qquad (2)$$

It have been reported that *DIBL* is not constant and has variations [21]. The origin of the *DIBL* variability is the potential distribution along the channel length direction due to RDF [21]. When the channel impurity concentration near drain is higher than that near source, higher *DIBL* is observed. In the present nanowire FETs whose channel is not intentionally doped, it is expected that *DIBL* variability is greatly suppressed.

In order to exclude the effect of systematic components, "within device" *DIBL* ($\Delta DIBL$) is measured by exchanging source and drain, and its variability ($\sigma\Delta DIBL$) is investigated. Fig. 5.7 and Fig. 5.8 compare the Pelgrom plot of $\sigma DIBL$ and $\sigma\Delta DIBL$ in nanowire, bulk, and FD SOI MOSFETs. The within-device *DIBL* variability is extremely small in nanowire FETs. Fig. 5.9 shows normal probability plots of $\Delta DIBL$ of three types of devices, which confirms the suppression of $\Delta DIBL$ variability in nanowire nFETs once again.

5.5 COV Variabilities in Tri-gate Silicon Nanowire MOSFETs

COV is defined as [22-26],

$$COV = \left| V_{THEX} - V_{THC} \right|. \tag{3}$$

Since V_{THEX} is determined in the strong inversion region while V_{THC} is determined in the subthreshold region, *COV* reflects the difference in V_{TH} between the strong inversion region and subthreshold region. It has been found that a large *COV* is observed when there is a deep potential valley in the channel in the subthreshold region [25]. Fig. 5.10 and Fig. 5.11 show the *COV* variability (σCOV) and within-device *COV* variability ($\sigma \Delta COV$) respectivley. Fig. 5.12 shows the normal probability plot of ΔCOV. Again, within-device *COV* variability is extremely small in nanowire MOSFETs compared with those in bulk and SOI MOSFETs.

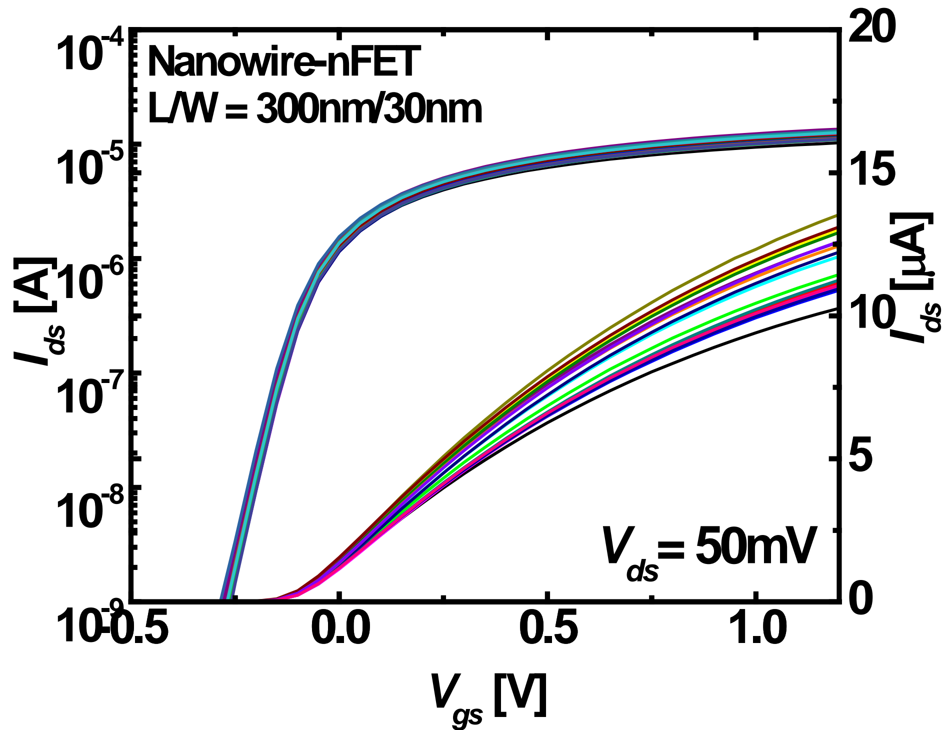
5.6 Discussion

As mentioned above, intrinsic channel FD SOI MOSFETs still have considerably large V_{TH}, *DIBL*, and *COV* variabilities in spite of a reduced RDF due to the intrinsic channel [28]. The remaining variability is caused by the workfunction variability in the metal gate [28]. In the present nanowire FETs, the workfunction variability is negligible owing to the use of the poly-Si gate and grain alignment along the nanowire channel [32]. The further suppression of variability in the measured data in the present study indicate that the negligibly small *DIBL* and *COV* variabilities as well as V_{TH} variability can be achieved as long as both RDF and the gate workfunction variability are completely suppressed.

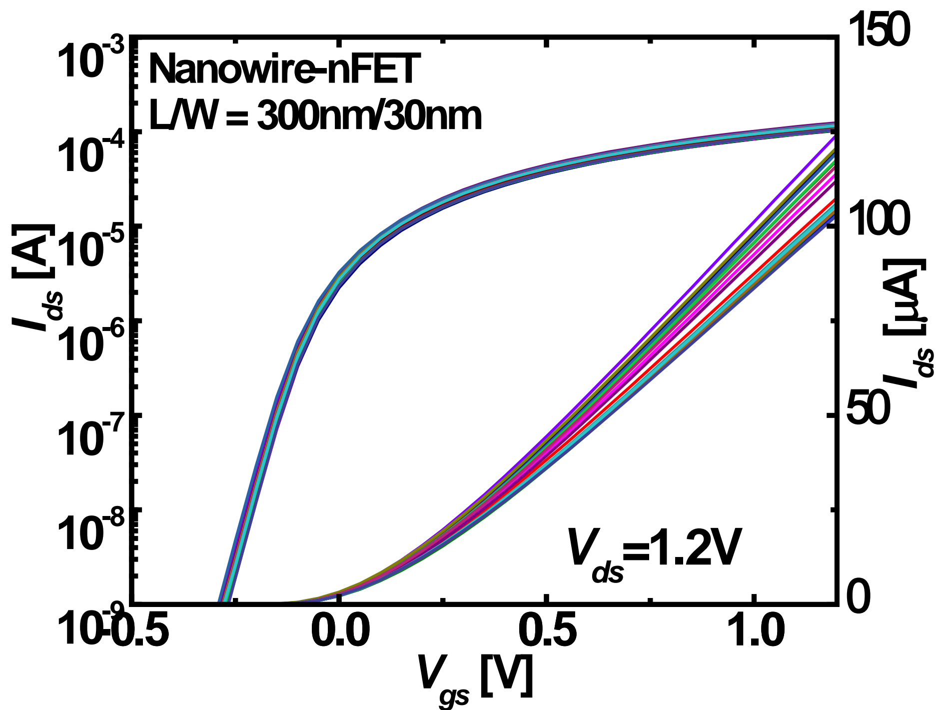
5.7 Summary

In this chapter, intrinsic channel tri-gate silicon nanowire nFETs with [110] channel direction on (100) SOI wafers were measured for variability evaluation. It is experimentally found that within-device variability of not only V_{TH} but also that of *DIBL* and *COV* is suppressed in intrinsic

channel nanowire FETs owing to the non intentionally doped channel and the absence of gate workfunction variability. The intrinsic channel silicon nanowire MOSFET is promising for a future scaled device structure in terms of not only the short channel effect suppression but also the variability suppression.



(a)



(b)

Fig. 5.1. Measured I_{ds}-V_{gs} curves of 18 nanowire nFETs with W_{NW} = 30 nm and L_g = 300 nm. (a) Linear region. (b) Saturation region.

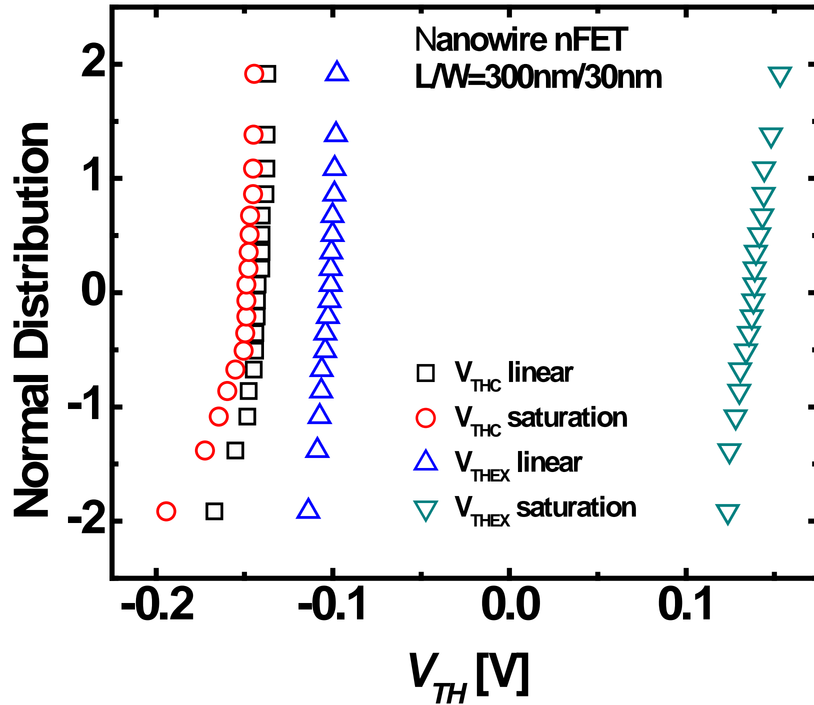


Fig. 5.2 Normal probability plots of measured V_{THC} and V_{THEX} in both linear and saturation regions in measured 18 nanowire nFETs with W_{NW} = 30 nm and L_g = 300 nm.

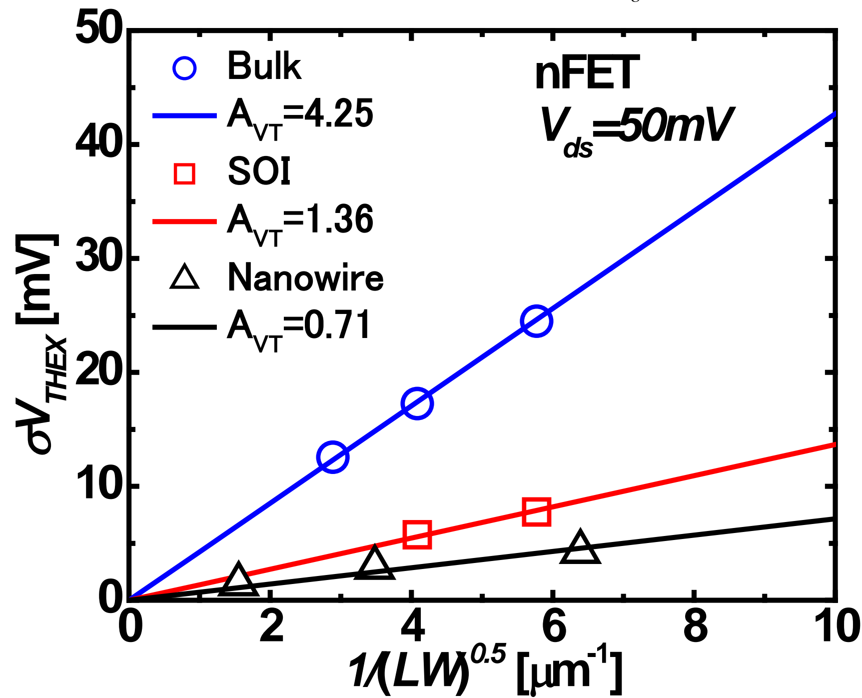


Fig. 5.3. Pelgrom plots of measured σV_{THEX} in linear region in nanowire nFETs compared with bulk and FD SOI MOSFETs.

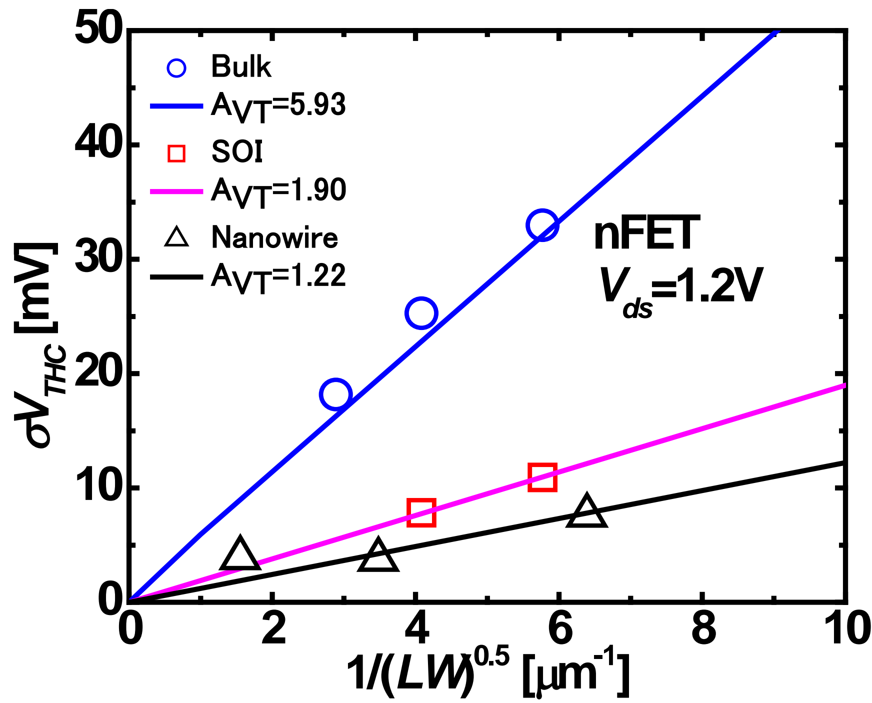


Fig. 5.4. Pelgrom plots of measured σV_{THC} in saturation region in nanowire nFETs compared with bulk and FD SOI MOSFETs.

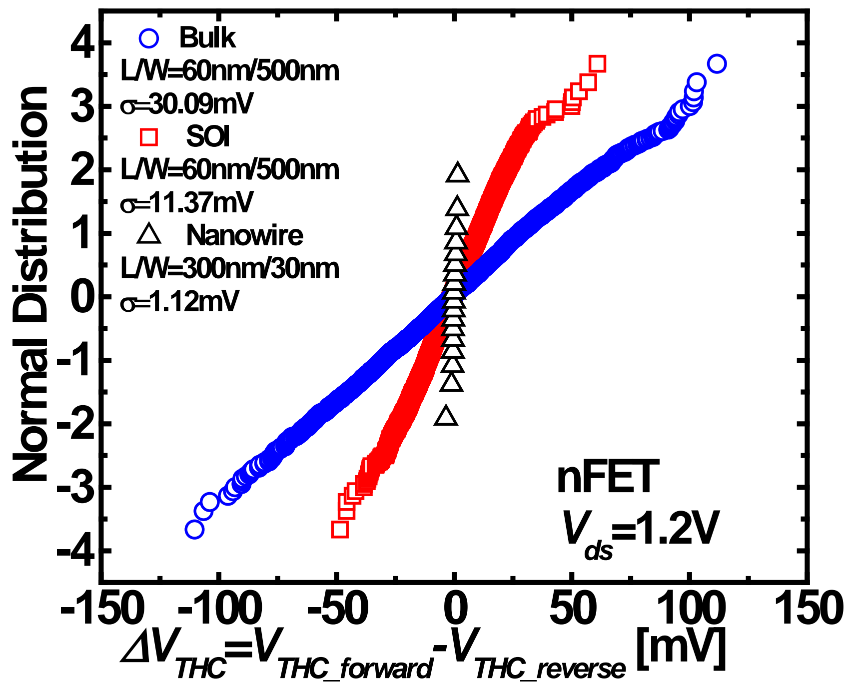


Fig. 5.5. Normal probability plots of ΔV_{THC} in nanowire, bulk, and FD SOI MOSFETs.

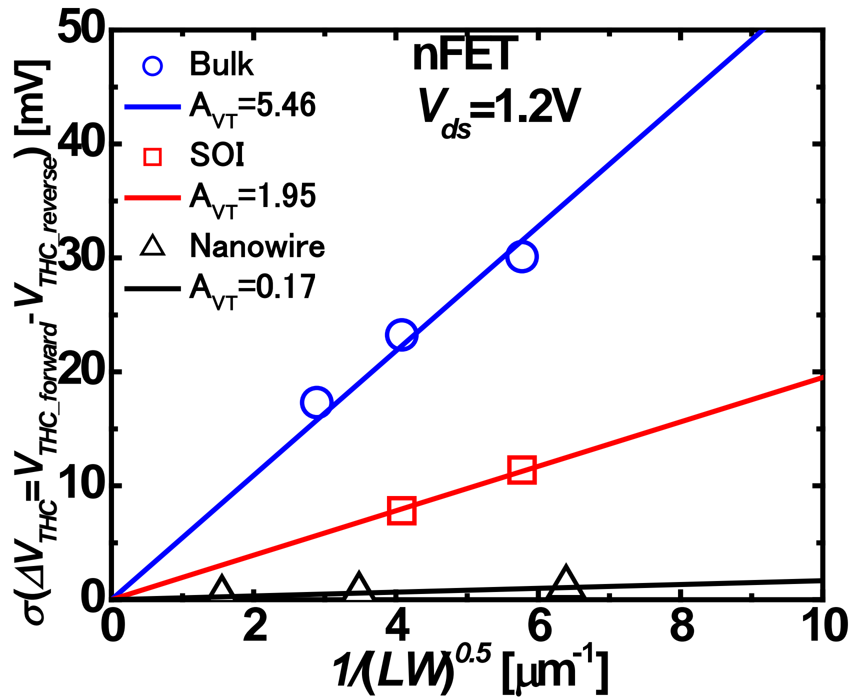


Fig. 5.6. Pelgrom plots of within-device V_{THC} variation in nanowire nFETs compared with bulk and FD SOI MOSFETs.

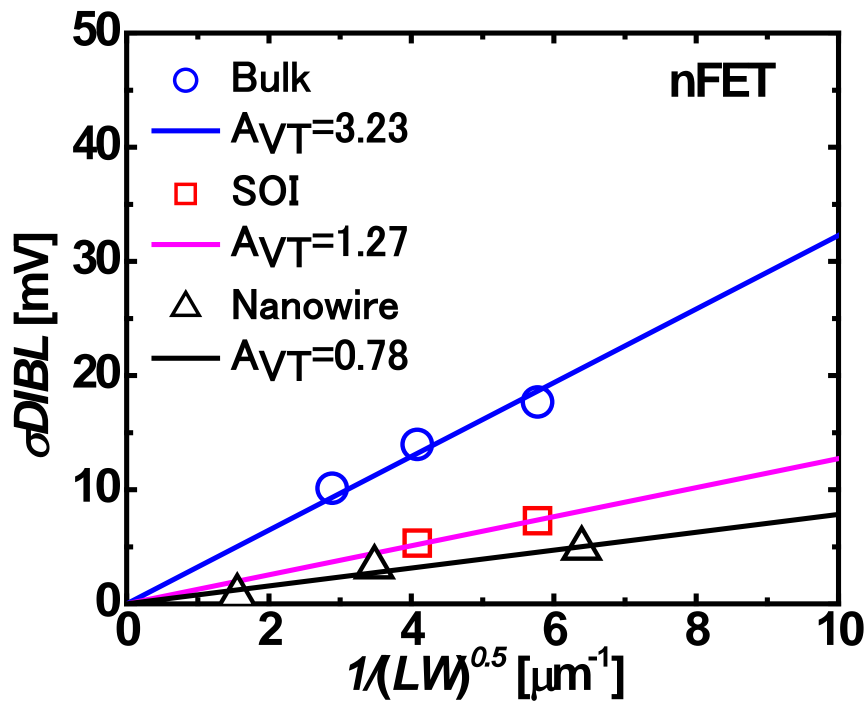


Fig. 5.7. Pelgrom plots of *DIBL* variation in nanowire nFETs compared with bulk and FD SOI MOSFETs.

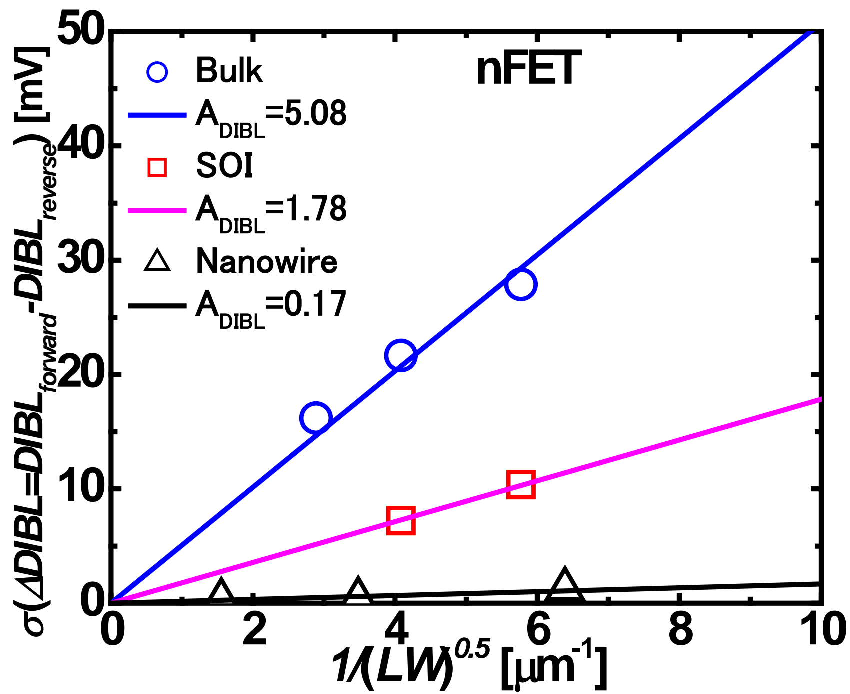


Fig. 5.8. Pelgrom plots of within-device *DIBL* variation in nanowire nFETs compared with bulk and FD SOI MOSFETs.

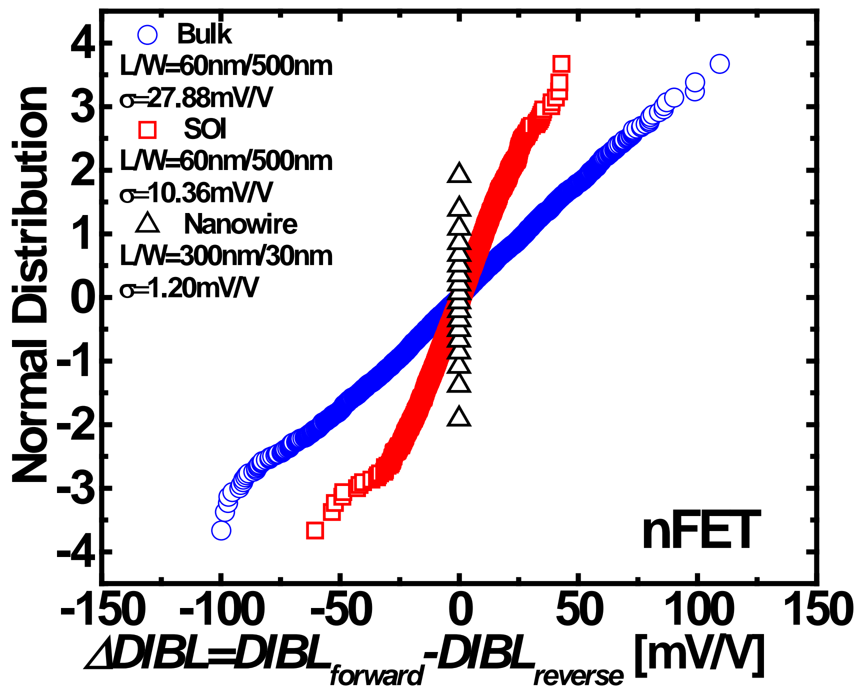


Fig. 5.9. Normal probability plots of Δ*DIBL* in nanowire, bulk, and FD SOI MOSFETs.

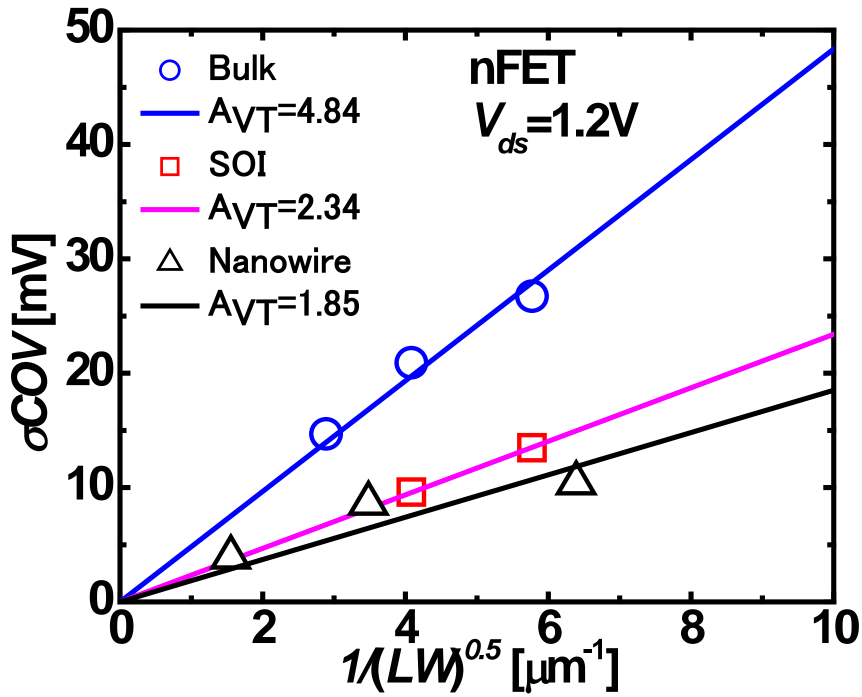


Fig. 5.10. Pelgrom plots of *COV* variation in nanowire nFETs compared with bulk and FD SOI MOSFETs.

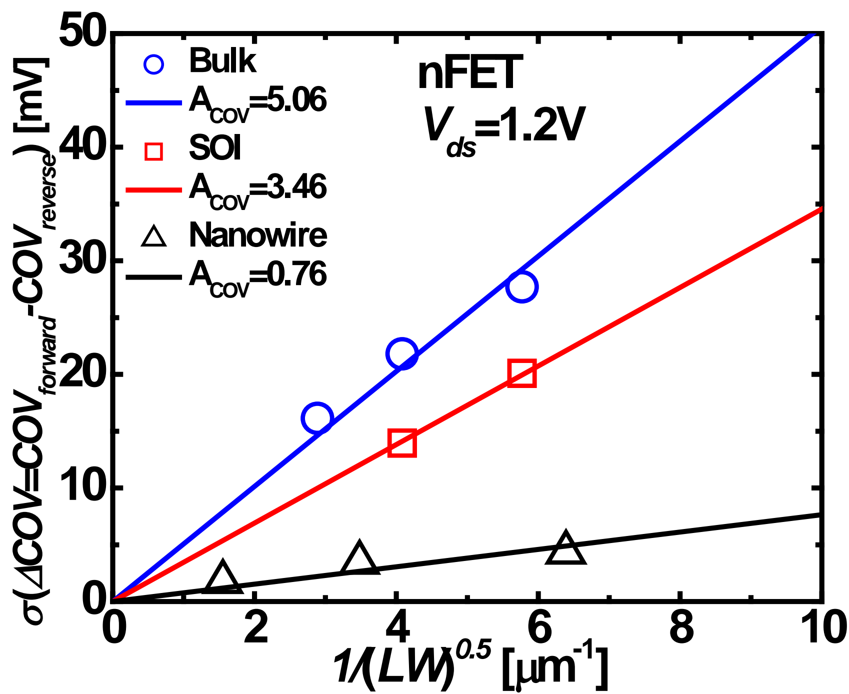


Fig. 5.11. Pelgrom plots of within-device *COV* variation in nanowire nFETs compared with bulk and FD SOI MOSFETs.

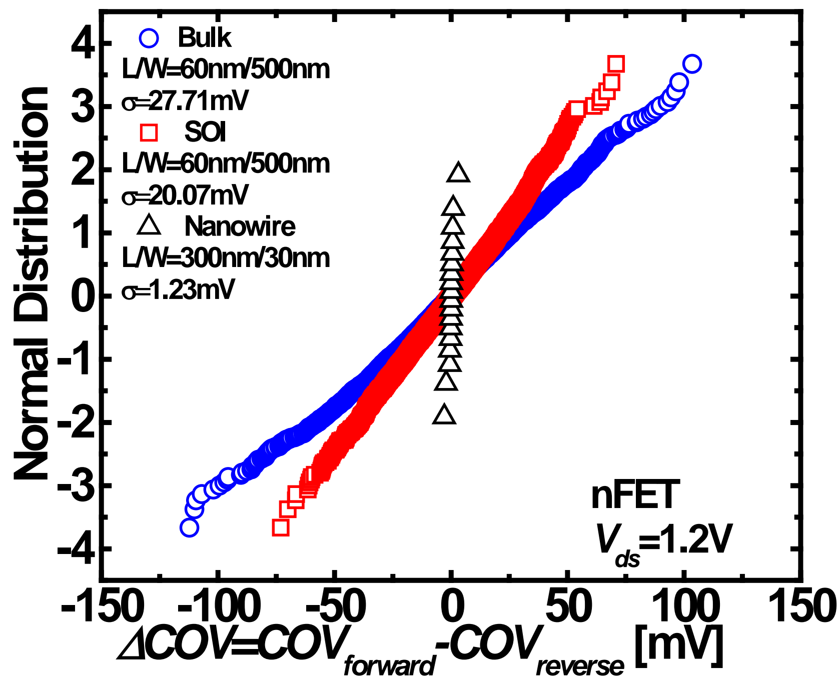


Fig. 5.12. Normal probability plots of Δ*COV* in nanowire, bulk, and FD SOI MOSFETs.

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Chapter 6

Conclusions

In this thesis, fabrication, and physics of silicon nanowire FETs have been extensively studied to overcome the limitations of conventional VLSI technology. On the base of split C-V method measurement, experimental and theoretical investigations of carrier mobility characteristics in silicon nanowires are described systematically. It is found that surface orientation plays the key role that determinates the mobility modulation in nanowires, as well as the surface roughness. And also, it is experimentally found that within-device variability of not only V_{TH} but also that of DIBL and COV is suppressed in intrinsic channel nanowire FETs owing to the non intentionally doped channel and the absence of gate work-function variability. The intrinsic channel silicon nanowire MOSFET is promising for a future scaled device structure in terms of not only the short channel effect suppression but also the variability suppression.

The main results obtained in the thesis are summarized as follows.

In Chapter 3, carrier mobility in [100]- and [110]- direction NWs on (100)- oriented SOI is fabricated and characterized. The electron and hole mobility in "single" nanowire FETs is directly extracted from split C-V measurement for the first time. It is found that, mobility of nanowires on (100) SOI decreases monotonically as narrowing nanowire width due to serious process-induced roughness in narrower nanowires. It is found that hole mobility in [110]-direction silicon nanowires is higher than (100) universal curve even in a single nanowire FET, which originates from the effect of (110) side surface with high hole mobility. It indicates that surface orientation

plays a key role in nanowire mobility.

In Chapter 4, low temperature measurements were performed with [110]- direction NWs on (100) SOI to investigate the scattering mechanisms in tri-gate silicon nanowire. Surface roughness limited mobility and phonon limited mobility are analyzed. The Phonon momentum and Fermi momentum competition phenomenon in phonon limited mobility is observed in nanowire mobility behaviors below 100 K. The phonon scattering has little nanowire width dependence and nanowire width dependence of surface roughness limited mobility can addressed the mobility degradation in our tri-gate nanowire MOSFETs to the surface roughness scattering. The Mobility degradation mechanisms in NW FETs are analyzed with an α-factor model. It is found that, the serious process-induced roughness on the side surface is the main source of mobility degradation in tri-gate silicon nanowire pFETs.

In Chapter 5, variability behavior in nanowires MOSFETs are investigated by statistic analysis. The origins of variabilities in MOSFETs are also discussed in detail. It is experimentally found that within-device variability of not only V_{TH} but also those of DIBL and COV is suppressed in intrinsic channel nanowire FETs owing to the non intentionally doped channel and the absence of gate work-function variability.

In conclusion, the results obtained in this thesis show important information on the carrier mobility and variability characteristics in silicon nanowire MOSFETs, which are promising for a future scaled device structure in terms of not only the short channel effect suppression but also the performance enhancement and variability suppression.

Appendix

Fabrication Process

The top-down SNWTs can be viewed as 'narrow-channel' SOI MOSFETs realized by using a 'top-down' approach. Different from planar SOI FETs, the channel widths of SNWTs are lithography- defined and comparable to the Si body thicknesses, so the gate stacks are allowed to wrap around the wire channels to realize multi-gate or gate-all-around FETs, which offer better gate control than planar MOSFETs. In current experimental, the wire dimensions (i.e., Si body thickness and width) could be smaller than 10nm. With the top-down approaches, nanowire devices with different gate structures, different cross sections and also different channel directions are fabricated for investigation. In the fabrication process, thermal oxidation, dry etching and wet etching are utilized to create nanoscale nanowires by shrinking the dimension of SOI channel down to 10nm in either width or height. With the thermal oxidation, ultra-narrow nanowires can be achieved after long time oxidation, because the stress induced by the thermal oxidation will stop the further oxidation in nanoscale structure. With the dry etching, the nanowire pattern can be transferred from the EB resist or photo resist to Si (or SOI, Si on Insulator). With the wet etching, nanowire width can be modified with SC1 isotropic wet etching and TMAH anisotropic etching. Therefore in the fabrication process of silicon nanowire, after transferring the nanowire to Si layer, wet etching is used to control the nanowire width and height, and thermal oxidation will be performed for gate insulation layer together with further reduction in nanowire width.

A.1 Fabrication Process Flow of Tri-Gate Silicon Nanowire MOSFETs

In this work, we have fabricated tri-gate structure silicon naowire MOSFETs on the (100) SOI substrate, with the widely used "top-down approach" method in traditional CMOS process. The starting materials for each fabrication are p-type UNIBOND SOI wafer without intentional doping. Since the nanowire channels are not doped in the fabrication processes, the channel doping concentration is given by the initial doping concentration, which is nearly intrinsic.

An important problem in this silicon nanowire MOSFETs is the parasitic resistance of source and drain region. A thin SOI layer in source and drain region cannot be fully doped by the ion implantation process, resulting in severely large resistance. In order to avoid the serious parasitic resistance of source drain region, an additional LOCOS process was utilized to recess the channel region in advance. After that, the fabrication of tri-gate silicon nanowire MOSFETs was carried on with the nanowire channel at the recessed region.

As shown in the Fig. A.1, the first step of the device fabrication process is thinning (100) SOI to a prerequisite thickness by repeated thermal oxidation and buffered HF (BHF) etching, and then thermal oxidation was performed once again to form a SiO_2 mask. Laser exposure and buffered HF (BHF) wet etching are used to form trench between source and drain SiO_2 mesa masks.[Fig. A.1(a)] This SiO_2 mask is used to define the drain and source area by protecting the underneath SOI layer from etching steps in the following process steps to fabricate the silicon nanowire array, meanwhile the trench width between drain and source defines the length of the later fabricated silicon nanowires.

After the trench is made, Electron beam lithography (EBL) was performed to define multiple nanowires, and the spacing between the nanowires was 500 nm. To avoid the EB proximity effect at the joint between the nanowire channel and the source/drain, a nanowire pattern of 60 um

length was drawn across the trench. [Fig. A.1(b)] The final nanowire channel length is defined by the width of trench, which is 5~50 μm in our devices.

After dry etching, with the protection of the SiO2 mask and EB resist (HSQ), the source/drain and channels were fabricated simultaneously [Fig. A.1(c)]. Then, the tri-gate structure was achieved after RIE dry etching, and SC1 isotropic wet etching was performed to decrease the size of nanowires until the required width and height was reached. [Fig. A.1(d)]. Schematics of the top-view and three-dimensional structures are shown in Figs. A.1(e) and A.1(f), respectively. After SC1 narrowing, gate thermal oxidation and poly-silicon deposition were performed sequentially [Fig. 2.7(g)], and the following processes were similar to the normal CMOS process.

For tri-gate structure nanowire MOSFETs, parallel 1~100 nanowires were fabricated to achieve accurate gate-channel capacitance measurement. And we also compared devices containing nanowires of different lengths to obtain the intrinsic mobility characteristics.

In this appendix, aiming at carrier mobility measurements with high accuracy, fabrication process of Tri-Gate structure nanowire MOSFETs on SOI substrate are described in detail. Detailed conditions for the fabrication processes are shown in the following table.

The thickness data of SOI and oxide is determined by ellipsometry measurement. Directed measurement of the final NW height has not been performed, because of the small size of nanowire, which is impossible to be measured with the elliposometer. The final gate oxide thickness, NW height and width is estimated from the measurements of the reference dummy samples in each step. And the estimation is validated by cross section SEM observation in advance.

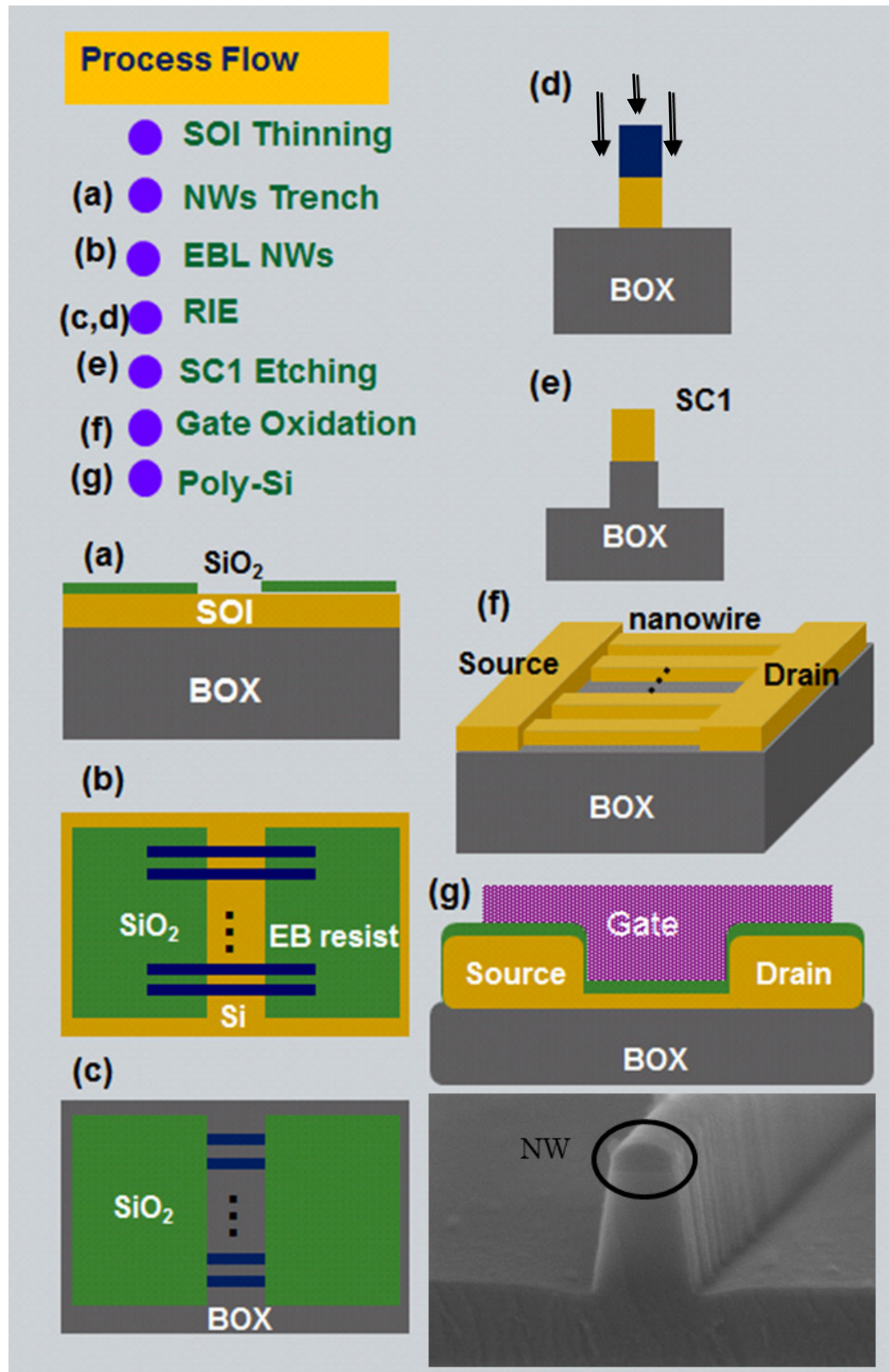

Fig. A.1. Main fabrication process flow of Tri-Gate nanowire nMOSFET.
(a) Formed mesa area after BHF wet etching; (b) nanowire pattern by EB lithography; (c) box layer is exposed after dry etching; (d) RIE etching to remove resist and form tri-gate structure; (e) SC1 etching to reduce W_{NW} and H_{NW} (f) gate oxidation and 3D structure after removing SiO2 mask and EB resist; (g) cross section after gate poly-Si deposition; (h) SEM image of fabricated tri-gate Si nanowire.

Table I. Flow and detailed conditions of the fabrication process of Tri-Gate Silicon Nanowire MOSFETs.

#	Process	Conditions	Thickness
1	Dicing Wafer cleaning Numbering	6 inch UNIBOND SOI wafer (p-type, (100), 10 ~ 20 Ωcm) → 2 cm × 1.5 cm Buffered HF (BHF) 1min. NH_4OH : H_2O_2 : H_2O = 1 : 1 : 6 (SC1) 75 ~ 80 deg. 10 min. BHF 1min. H_2SO_4 : H_2O_2 = 3 : 1 (SPM) 110 ~ 130 deg. 10 min. numbering BHF 1min. SPM 110 ~ 130 deg. 10 min.	SOI 100 nm / BOX 200 nm
2	SOI thinning Pre-cleaning	 HF : H_2O = 1 : 100 (DHF) 90 sec. SPM 110 ~ 130 deg. 10 min. DHF 90 sec.	
3	Ellipsometry	Measure SOI thickness	SOI 85 ~ 90 nm
4	Mark area Laser lithography	 HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
5	SOI etching	Helicon Etcher (step2: 5 sec., step3: 35 sec., step4: 0 sec., Recipe: Poly-Masumi)	
6	BOX removal	BHF 3 min.	
7	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	

8	Mark Laser lithography	HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 38CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
9	Mark etching	Helicon Etcher (step2: 0 sec., step3: 400 sec., step4: 0 sec., Recipe: Mark-Harata)	
10	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
11	Nitride deposition	Vertical CVD #1 (SiH_2Cl_2 20 sccm, NH_3 80 sccm, 33 Pa, 780 deg., 25 min.)	Nitride ~ 80 nm
12	LOCOS window Laser lithography	HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
13	Nitride etching	DFR etcher (step2: 35 sec., Recipe: SiN_CONT)	
14	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
15	Pre-cleaning	DHF 90 sec. SPM 110 ~ 130 deg. 10 min. DHF 90 sec.	
16	LOCOS Dry oxidation	O_2 : 1.0 l/min. 1100 deg. 30 min.	
17	Nitride removal	BHF 20 sec. H_3PO_4 180 deg. 12 min.	

18	LOCOS removal	BHF 2 min. SPM 110 ~ 130 deg. 10min.	Un-Recessed SOI ~ 85 nm Recessed SOI ~ 40 nm
19	SOI thinning Pre-cleaning Dry oxidation Oxide thinning	 DHF 90 sec. SPM 110 ~ 130 deg. 10 min. DHF 90 sec. O_2 : 1.0 l/min 1000 deg. 27 min. BHF 1 min	 Un-Recessed SOI 65 ~ 85 nm Recessed SOI 15 ~ 40 nm
20	Mesa oxidation Dry oxidation	 O_2 : 1.0 l/min. 1000 deg. 12 min.	Mesa oxide ~20nm Un-Recessed SOI 55 ~ 75 nm Recessed SOI 5 ~ 30 nm
21	Mesa mask Laser lithography	 HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
22	Mesa etching	BHF 30 sec.	
23	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
24	EB lithography Spin coating Pre-baking Exposure Development	FOx-15 : MIBK = 1 : 2 4000 rpm 40 sec. prebake 120 deg. 2 min. Area dose : 750 $\mu C/cm^2$ (for wire channel) Area dose : 300 $\mu C/cm^2$ (for mesa) Beam current : 100 pA Acceleration voltage : 50 keV NMD-3 60 sec. Post-baking 100 deg. 15 min.	

25	Channel formation RIE etching	Helicon Etcher (step2: 5 sec., step3: 5 ~ 30 sec., step4: 0 sec., Recipe: Poly-Masumi)	
26	Resist removal	DFR etcher (step2: 50 sec., Recipe: SiO_2-MIYAJI2) SPM 110 ~ 130 deg. 10 min.	
27	Wire narrowing	SC1 75 ~ 80 deg. 30 ~ 60 min.	
28	Gate oxide Thermal oxidation	DHF 90 sec. SPM 110 ~ 130 deg. 10 min. DHF 90 sec. O_2 : 1.0 l/min 1000 deg. 5 min.	Thermal oxide ~ 10 nm
29	Poly-Si deposition	Vertical CVD #1 (SiH_4 250sccm, 33 Pa, 580 deg., 45 min.)	Poly-Si 200 ~ 300 nm
30	Gate patterning Laser lithography	HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
31	Gate etching	Helicon Etcher (step2: 5 sec., step3: 105 sec., step4: 30 sec., Recipe: Poly-Masumi)	
32	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
33	P-mask patterning Laser lithography	HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
34	Ion implantation	BF_2^+ Acceleration voltage : 35 keV Dose : 3×10^{15} cm^{-2}	

35	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
36	N-mask patterning Laser lithography	 HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
37	Ion implantation	P^+ Acceleration voltage : 35 keV Dose : 3×10^{15} cm^{-2}	
38	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
39	Cleaning	SPM 110 ~ 130 deg. 10 min. SPM 110 ~ 130 deg. 10 min. SPM 110 ~ 130 deg. 10 min.	
40	Passivation oxide deposition	SPM 110 ~ 130 deg. 10 min. Vertical CVD #2 (SiH_4 : 15 sccm, O_2 : 60 sccm, 33 Pa, 400 deg., 180 min.)	Oxide 300 ~ 500 nm
41	Annealing N_2 annealing H_2 annealing	SPM 110 ~ 130 deg. 10 min N_2 : 1.0 l/min 950 deg. 20 min H_2 : 100 sccm, N_2 : 1.0 l/min 430 deg. 25 min	
42	Contact hole Laser lithography	 HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
43	Contact hole Etching	 BHF 3 ~ 6 min	
44	Resist removal	Acetone 5-10 min. SPM 110 ~ 130 deg. 10 min.	
45	Native oxide		

	removal	DHF 2 min.	
46	Al evaporation		Al 400 nm
47	Al electrode Laser lithography	HMDS 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 2min. AZ1500 20CP 500 rpm 5sec., 6000 rpm 60 sec., prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. develop Postbake 110 deg., 10 min.	
48	Al etching	Al etchant 45 ~ 50 °C 1 min.	
49	Resist removal	Acetone 5-10 min.	

List of Publications and Presentations

Journal Articles

[1] Ke Mao, Tomoko Mizutani, Anil Kumar, Takuya Saraya, and Toshiro Hiramoto, "Suppression of Within-Device Variability in Intrinsic Channel Tri-Gate Silicon Nanowire Metal–Oxide–Semiconductor Field-Effect Transistors", Japanese Journal of Applied Physics, Vol.51, No.2, February, 2012.

[2] Ke Mao, Takuya Saraya, and Toshiro Hiramoto, "Direct Measurement of Carrier Mobility in Intrinsic Channel Tri-Gate Single Silicon Nanowire MOSFETs", To be submitted to Japanese Journal of Applied Physics.

[3] Ke Mao, Takuya Saraya, and Toshiro Hiramoto. "Effects of Side Surface Roughness on Mobility Behaviors in Tri-Gate Silicon Nanowire MOSFETs", To be submitted to Japanese Journal of Applied Physics.

Presentations at International Conferences

[1] Ke Mao, Tomoko Mizutani, Anil Kumar, Takuya Saraya, and Toshiro Hiramoto. "Extremely Small Within-Device Variability in Intrinsic Channel Tri-Gate Silicon Nanowire MOSFETs", in International Conference on Solid State Devices and Materials (SSDM), Nagoya, 2011.

[2] Ke Mao, Takuya Saraya, and Toshiro Hiramoto. "Extraction of Carrier Mobility in Intrinsic Channel Tri-Gate Single Silicon Nanowire MOSFETs", accepted for oral presentation in International Conference on Solid State Devices and Materials (SSDM), Kyoto, 2012.

[3] Ke Mao, Takuya Saraya, and Toshiro Hiramoto. " The impact of Side Surface Roughness on Carrier Mobility in Tri-Gate Silicon Nanowire MOSFETs", accepted for oral presentation in

International Conference on Solid State Devices and Materials (SSDM), Kyoto, 2012.

Presentations at Domestic Conferences

[1] Ke Mao, Tomoko Mizutani, Anil Kumar, Takuya Saraya, and Toshiro Hiramoto. ”シリコンナノワイヤ MOSFET における Vth, DIBL および電流立上り電圧のデバイス内ばらつき”, 2012 年春季応用物理学会、東京、2012 年 3 月.

[2] Ke Mao, Takuya Saraya, and Toshiro Hiramoto. ”単一シリコンナノワイヤチャネルトランジスタのキャリア移動度測定”, 2012 年秋季応用物理学会、愛媛、2012 年 9 月(発表予定).