Sub-0.5V Extremely Low Power Logic Circuits

（電源電圧 **0.5V** 以下の極低電力ロジック回路に関する研究）

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Supervisor: Professor Makoto Takamiya

安福　正

Tadashi Yasufuku

DEPARTMENT OF ELECTRICAL ENGINEERING AND INFORMATION SYSTEMS,
THE UNIVERSITY OF TOKYO
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Abstract

Possibility for realization of sub-0.5V extremely low power logic circuits is investigated in this thesis. Transistor variations at low power supply voltage degrade the operation of logic circuits. Thus, the effects of transistor variations are investigated at low V_{DD} and countermeasures against them are proposed in the thesis.

Reduction of power supply voltage (V_{DD}) is an effective method for achieving ultra low power logic circuits since active power is proportional to V_{DD}^2 and leakage power is proportional to V_{DD}. Although circuits exhibit slower speeds at low supply voltage, low voltage operation of logic circuits remains attractive for energy-constrained systems. Besides, when V_{DD} is near/below the threshold voltage (V_{TH}) of transistors, logic circuits operate most efficiently. In this way, lowering power supply voltage achieves low power and energy efficient operation. Transistor variations, however, inhibit lowering V_{DD}, because the sensitivity of circuits to transistor variations drastically increases under reduced V_{DD}. The main obstacles for low voltage operation of logic circuits are function errors and delay variations of logic circuits, because one function error at a single logic gate is considered as the function error of whole circuits and the delay variations makes the design of logic circuits more difficult at low V_{DD}. These problems must be dealt with properly in the design of low voltage logic circuits. Thus, the purpose of the thesis is to reveal the effect of these two problems on logic circuits and propose countermeasures to achieve sub-0.5V extremely low power logic circuits.

At first, function error of logic gates is discussed in 65nm CMOS. Function errors

prevent lowering V_{DD} of logic circuits. The minimum operating voltage (V_{DDmin}) is defined as the minimum power supply voltage when the circuits operate without function errors. V_{DDmin} increases with the number of logic gates and CMOS technology down-scaling. Thus, reducing V_{DDmin} of logic circuits is important to achieve extremely low voltage logic circuits. The determinant factors of V_{DDmin} in logic circuits are investigated, and the design criteria to reduce V_{DDmin} are presented. V_{DDmin} consists of $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$. $V_{DDmin(RAND)}$ which is random component of V_{DDmin} depends on the random variation of threshold voltage of transistors and the number of stages of logic gates, while $V_{DDmin(SYS)}$ which is systematic component of V_{DDmin} is determined by the balance of nMOS and pMOS and is minimized when the logic threshold voltage is equal to half V_{DD}. Therefore, $V_{DDmin(RAND)}$ is reduced by increasing width of nMOS and width of pMOS, while $V_{DDmin(SYS)}$ is minimized by optimizing W_P/W_N at a design stage. The body-biasing is effective to compensate for the increase of $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation. The optimal body-biasing minimizes $V_{DDmin(SYS)}$ and the forward body biasing decreases $V_{DDmin(RAND)}$. In the measurement, V_{DDmin} is successfully reduced by 45mV from 193mV to 148mV by the forward body biasing.

Next, the effect of delay variations on logic circuits is explored in 65nm CMOS. Delay variations of logic gates make it difficult for logic gate paths to meet timing constraints. If enough setup timing margins are considered, operation frequency decreases. By contrast, to meet hold time constraint, hold compensation buffers are inserted into logic gate paths. Therefore, the within-die delay variation dependence on V_{DD} in several types of design under tests (DUT's) is measured with a proposed

circuit. The proposed circuit emulates a real logic path because DUT's are inserted between F/F's and F/F-related delays are included in the delay measurement. The main focus of the measurement is dependence of the logic circuits on the methodology of physical layout. Although, layout of logic circuits is usually designed by automatically using place and route (P&R) tools, the effect of the auto P&R layout on delay variation is not clear at low voltage. Thus, DUT delay dependence on methodology of physical layout is investigated. The measurement result reveals that relative delay variation difference (=sigma/average) between the manual layout and the P&R layout rapidly decreases from 1.56% to 0.07% with reducing V_{DD} from 1.2V to 0.4V, because the random delay variations due to the random transistor variations dominate total delay variations at low V_{DD}. This result indicates that low voltage logic circuits designed by P&R tools do not raise delay variations at low V_{DD}.

Finally, in order to achieve ultra low V_{DD} logic circuits, a post-fabrication dual V_{DD} control (PDVC) of multiple voltage domains is proposed. Reducing V_{DDmin} at a design phase is difficult because V_{DDmin} is mainly determined by random variations of transistors. Furthermore, only one functional error of logic gates increases V_{DDmin} of a whole logic circuit. Therefore, in order to reduce V_{DDmin}, V_{DD} must be controlled with multiple domains. In the proposed PDVC, the layout of the whole logic circuit is divided into many domains regardless of the functional blocks. The V_{DD} of each domain is independently selected from high V_{DD} (V_{DDH}) and low V_{DD} (V_{DDL}). PDVC is applied to a DES CODEC's circuit fabricated in 65nm CMOS. The layout of DES CODEC's is generated by P&R tools and divided into 64 V_{DD}

domains. V_{DDH} or V_{DDL} is applied to each domain and the selection of V_{DD}'s is performed based on multiple built-in self tests. V_{DDH} is selected in V_{DDmin}-critical domains, while V_{DDL} is selected in V_{DDmin}-non-critical domains. As a result, a maximum 24% power reduction was measured with the proposed PDVC at 300kHz, V_{DDH} =437mV, and V_{DDL}=397mV.

The results of the thesis, which includes investigation on and countermeasures against V_{DDmin} and delay variation, is useful to realize sub-0.5V extremely low power logic circuits for future LSI applications.

Acknowledgement

I would like to extend my sincere appreciation to my supervisor, Associate Professor Makoto Takamiya for his invaluable guidance throughout my study at the University of Tokyo. His creative vision and constructive ideas have been crucial to the success of this research. Professor Takayasu Sakurai went out of his way to advise me during the course of this research. I would like to thank Professor Toshiro Hiramoto, Professor Shuichi Sakai, Associate Professor Makoto Ikeda, and Associate Professor Toru Nakura for serving on my qualifying examination committee. Many thanks go to Dr. Koichi Ishida and Dr. Hiroshi Fuketa for their support and fruitful discussions. Mr. Katsuyuki Ikeuchi and Mr. Po-hung Chen are acknowledged for the stimulating discussions. I would like to thank all the members of Sakurai laboratory, Takamiya laboratory and ELP laboratory for their supports. Besides, I am very thankful for continual support from my family. Lastly, I would like to thank the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo. Part of chapter 2 and 4 was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO). Part of chapter 3 was carried out as a part of the next-generation circuit architecture technical development program supported by METI and STARC.

Table of Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1 Motivation and goal

LSI's market is widely spreading thanks to scaling of transistors. LSI's are not only applied to servers and PC's, but also applied to mobile devices such as smart phones. Besides, Application of LSI's to sensor network and human health care devices gathers attention recently. Because such devices are energy constrained, power reduction of LSI's are inevitable. To reduce energy consumption of logic circuits, lowering power supply voltage (V_{DD}) is a compelling approach, because power of logic circuits is expressed as below.

$$P = \alpha C V_{DD}^{\ 2} f + I_{LEAK} V_{DD} \qquad (1\text{-}1)$$

where α denotes activity rate of logic circuit, C denotes capacitance of a circuit, f denotes operation frequency and I_{LEAK} denotes leak current of a circuit. Although circuits exhibit slower speeds at low supply voltages, the trade-off between power and operation frequency remain attractive for energy-constrained systems. Figure 1-1 shows simulated dependence of delay, power and PD product on V_{DD}. PD product is correspond to energy consumption per cycle. The left axis is normalized power and delay. The right axis is normalized PD product. Power decreases according to V_{DD} scaling, on the other hand, delay increases according to V_{DD} scaling. Thus, PD product has a minimum point. In this case, energy is minimized at 0.3V. Although minimum energy point varies according to activity rate of a circuit, energy is generally minimized around 0.2V to 0.4V. In this way, low voltage operation of logic circuits is attractive to energy constrained applications.

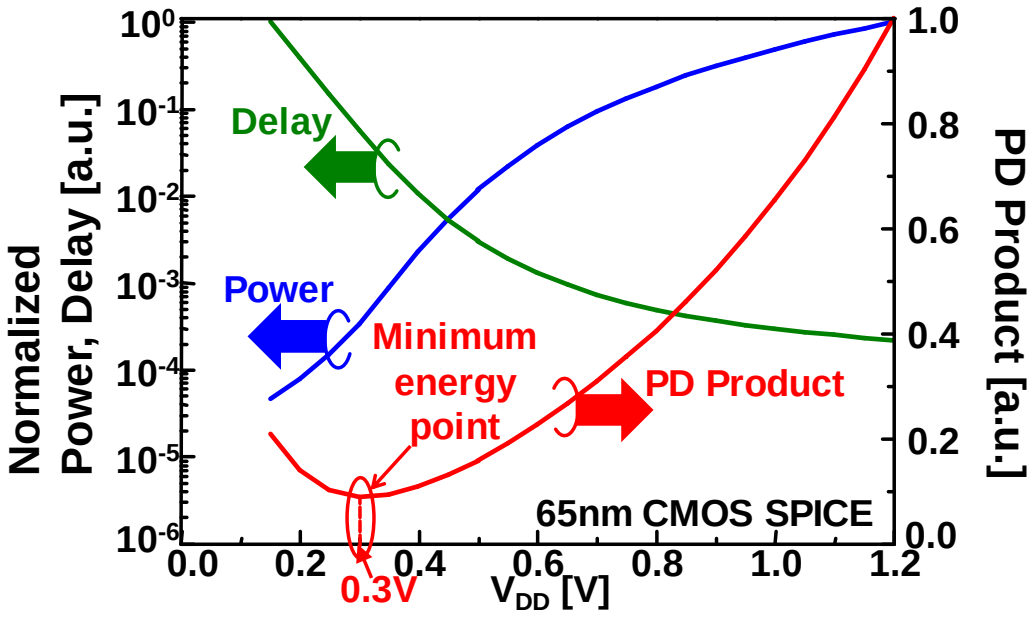


Figure 1-1. Simulated dependence of normalized power, delay and PD product on V_{DD}.

1.2 Obstacles for reducing V_{DD} of logic circuits

Although reduction of V_{DD} shows high energy efficiency, transistor variation dramatically increases according to V_{DD} scaling. Figure 1-2 shows the variation of Ids measured from 8192 nMOS's [1]. At ultra low V_{DD}, transistor current varies significantly. The variation of transistors causes function error and timing error in logic circuits. This makes it difficult to operate logic circuits normally. For example, Figure 1-3 shows the function error of logic circuits [2]. The waveform is a simulated output voltage of a 5-stage ring oscillator consisted of inverters. Output waveform attenuates with reduction of V_{DD}, and then stops. The voltage when oscillation stops is called V_{DDmin}. V_{DDmin} is the unavoidable lower limit for logic circuits. Thus analysis on V_{DDmin} should be conducted, and design method to reduce VDDmin must be revealed.

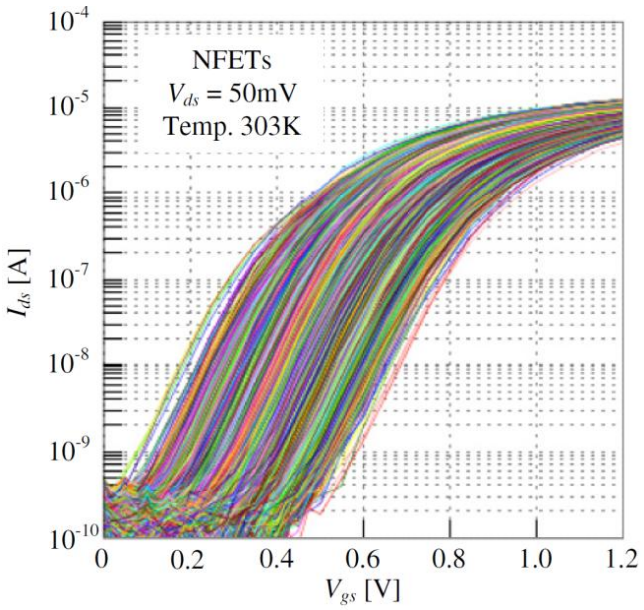


Figure 1-2. Variation of I_{ds}-V_{gs} curves from 8192 nMOS's. [1]

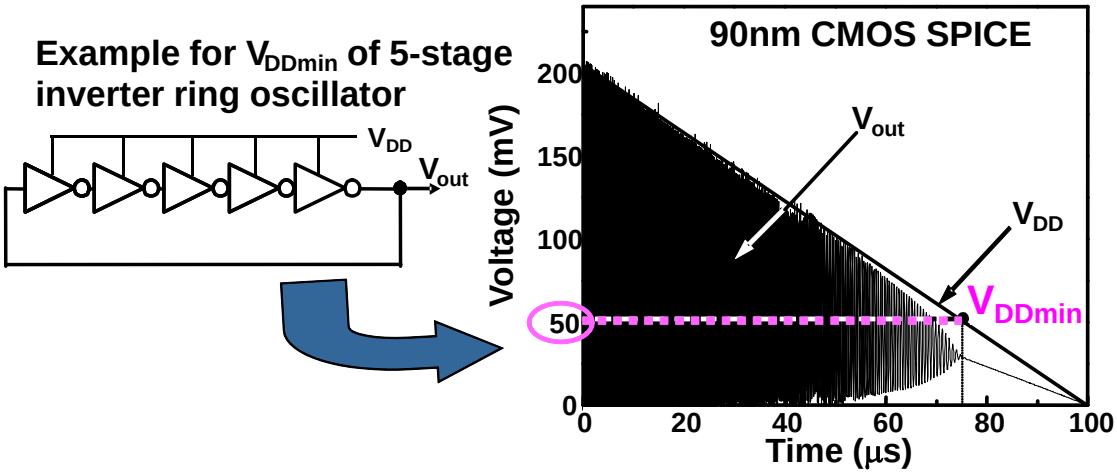


Figure 1-3 Example of V_{DDmin} for a ring oscillator with 5-stage inverters.

Delay variation of logic gates is also major problems to reduce V_{DD}. Figure 1-4 shows simulated dependence of relative delay variation of 100stage inverter chain on V_{DD}. Relative delay variation at 0.3V is more than 10 times larger than relative delay variation at 1.2V. Because design of logic circuits is made based on timing constraint, delay variation should also be investigated.

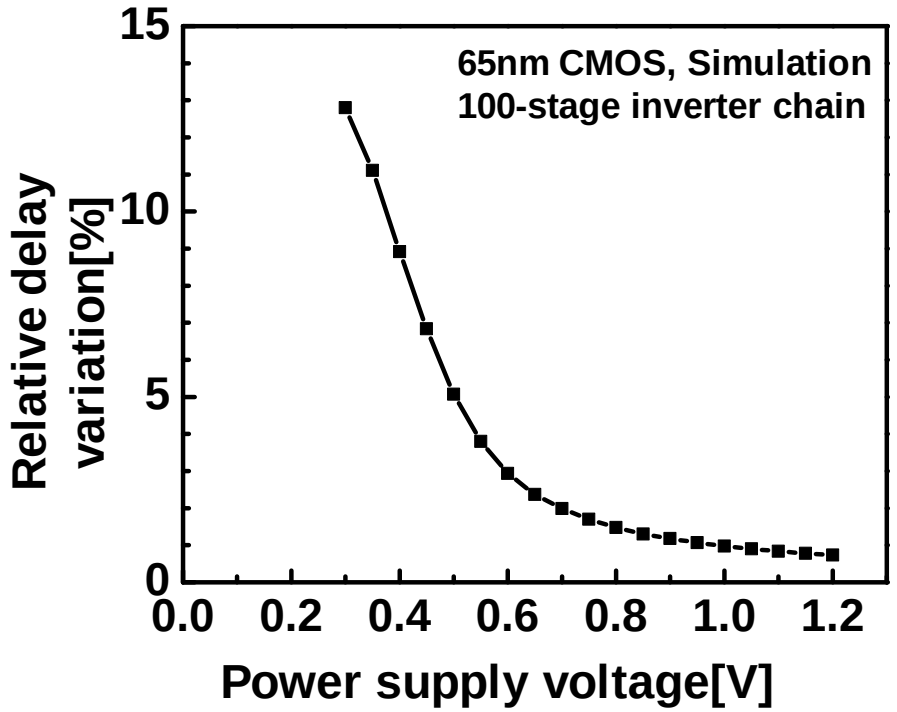


Figure 1-4. Simulated relative delay variation on V_{DD} in 65-nm CMOS process.

1.3 Thesis organization

This thesis is organized into 5 chapters. In chapter 2, determinant factors of V_{DDmin} are investigated. V_{DDmin} is divided into $V_{DDmin(SYS)}$ which is systematic component of V_{DDmin} and $V_{DDmin(RAND)}$ which is random component of V_{DDmin}. $V_{DDmin(SYS)}$ is determined by balance of nMOS and pMOS. $V_{DDmin(RAND)}$ is determined by variations of transistors. The design guide to reduce Both $V_{DDmin(sys)}$ and $V_{DDmin(RAND)}$ is investigated and is applied to general logic circuits. Optimization of F/F is also discussed. In chapter 3, the effect of delay variations on logic circuits is explored. A circuit which emulates a real logic path is proposed to measure delay variation of real logic paths. The main focus of the measurement is dependence of the logic circuits on the methodology of physical layout. The effect

of the auto place and route layout on delay variation is discussed. In chapter 4, to mitigate V_{DDmin} of logic circuits, a post-fabrication dual V_{DD} control of multiple voltage domains is proposed. In the proposed method, the layout of the whole logic circuit is divided into many domains regardless of the functional blocks. V_{DD} applied to each domain is optimized after fabrication using a proposed optimization algorithm. Conclusions of the thesis are made in chapter 5.

References

[1] T. Tsunomura, A. Nishida, and T. Hiramoto, "Verification of Threshold Voltage Variation Properties in Scaled Transistors with Ultra Large-Scale Device Matrix Array Test Element Group", Japanese Journal of Applied Physics, Vol. 48, No. 12, 124505, December, 2009.

[2] T. Niiyama, P. Zhe, K. Ishida, M. Murakata, M. Takamiya, and T. Sakurai, "Increasing Minimum Operating Voltage (V_{DDmin}) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega-Stage Ring Oscillators," International Symposium on Low Power Electronics and Design (ISLPED), pp. 117-122, Aug. 2008.

Chapter 2
Analysis and reduction of minimum operating voltage of logic circuits

2.1 Minimum operating voltage of logic circuits

Reduction of power supply voltage (V_{DD}) is an effective method for achieving ultra low power logic circuits since active power is proportional to V_{DD}^2 and leakage power is proportional to V_{DD}. Thus, many works have been carried out on logic circuits operating at low V_{DD} [1-2]. V_{DD} scaling is, however, obstructed by the minimum operating voltage (V_{DDmin}) [3] of CMOS logic gates. V_{DDmin} is the minimum power supply voltage when the circuits operate without function errors. V_{DDmin} increases with the number of logic gates and CMOS technology down-scaling. Thus, reducing V_{DDmin} of logic circuits is important to achieve ultra low voltage (V_{DD} < 0.4V) logic circuits. Previously, there were no design guides to reduce V_{DDmin} of circuits since the determinant factors of V_{DDmin} were not clarified. In this paper the determinant factors of V_{DDmin} in logic circuits are investigated, and the design criteria to reduce V_{DDmin} are presented. Also, temperature dependency of V_{DDmin} is measured, revealing for the first time, that the V_{DDmin} under the worst condition depends on the gate counts of logic circuits.

2.2 Test chip design

Figure 2-1 (a) and (b) show schematic diagrams of the inverter and 2 input NAND (2NAND) chains of which the V_{DDmin} are measured. The inverter chain has 10001 (10k) stages of inverters and has monitoring ports branching out from the

11th stage, 101st stage and so on. The NAND chain has 100001 (100k) stages of 2NANDs with similar ports. Figure 2-1 (c) shows a detailed schematic diagram of the inverters used in the inverter chain of Figure 2-1 (a). The body-bias voltages of both the nMOS transistors ($V_{bs(nMOS)}$) and the pMOS transistors ($V_{bs(pMOS)}$) can be controlled. Note that when $V_{bs(nMOS)}$ is positive the nMOS transistors are forward biased, whereas when $V_{bs(pMOS)}$ is positive the pMOS transistors are reverse biased. The gate lengths of all transistors are fixed to the minimum of the process, and W_N and W_P are the gate widths of the nMOS and pMOS transistors, respectively.

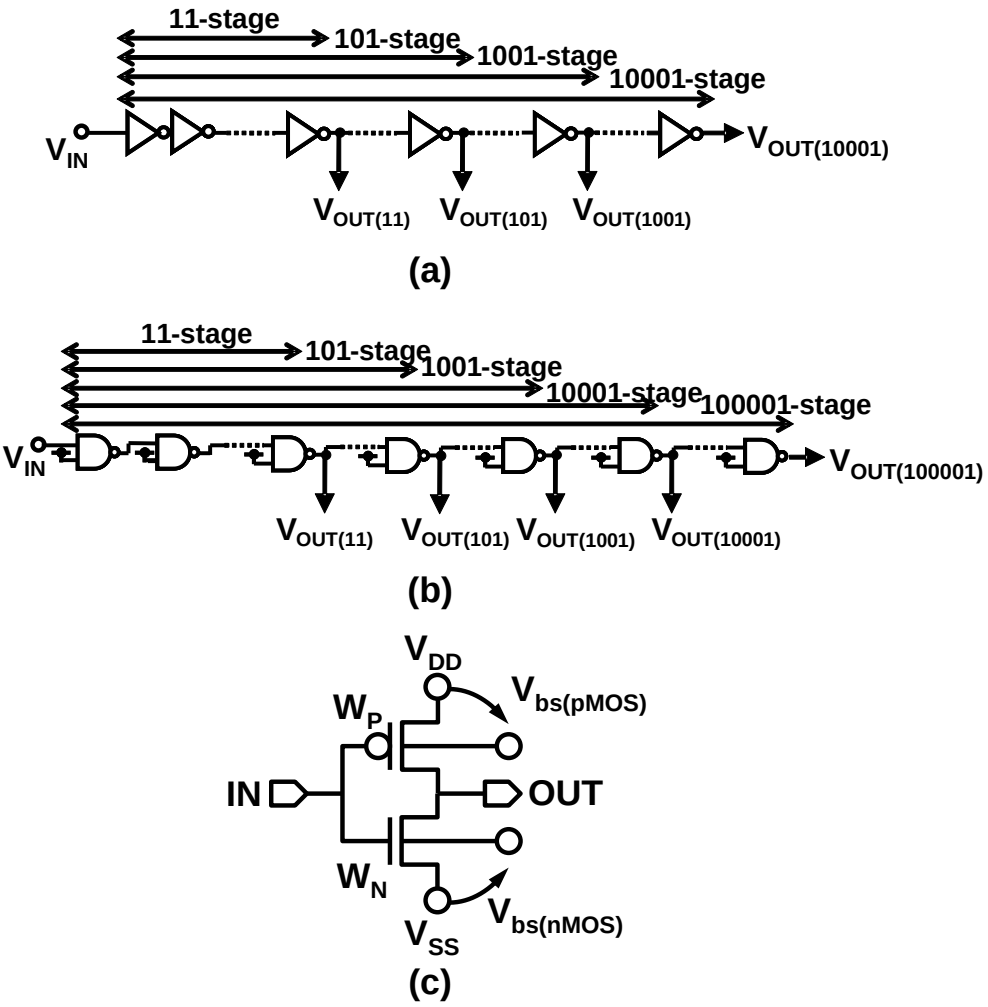


Figure 2-1. Schematic diagram of fabricated chains to measure V_{DDmin}. (a) Inverter chain. (b) 2 input NAND (2NAND) chain. (c) Inverter used in the chain in (a).

Figure 2-2 shows the layout and chip micrograph of the test chip of the 2NAND chain. Both the inverter chain and the 2NAND chain circuits are fabricated in a 65nm CMOS process occupying 0.4mm x 0.6mm, and 1mm x 0.8mm, respectively.

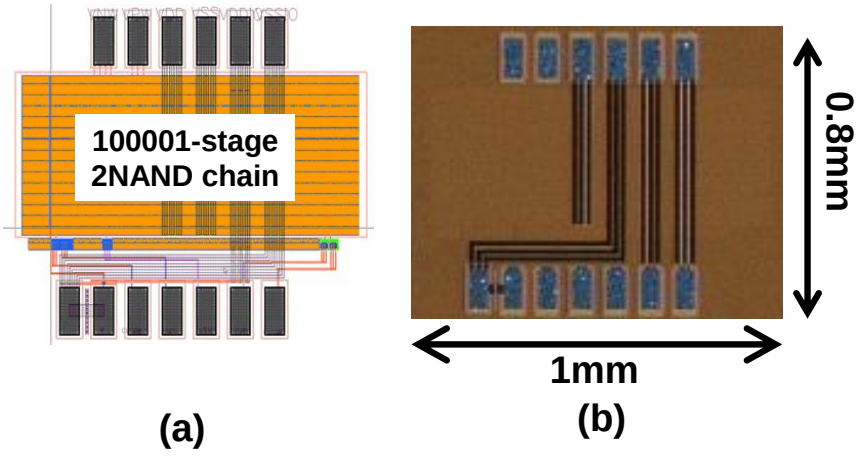


Figure 2-2. Test chip of 2NAND chain fabricated in 65-nm CMOS. (a) Layout. (b) Chip micrograph.

2.3 Experimental results

2.3.1 Determinant factors of V_{DDmin}

Figure 2-3 shows measured and simulated dependence of V_{DDmin} on the number of stages in the inverter and 2NAND chains. The average V_{DDmin} in the measured 17 dies for 2NAND and 20 dies for inverter is shown. Monte Carlo SPICE simulation includes within-die random threshold voltage (V_{TH}) variations and the number of trials of the Monte Carlo simulation is 100 times. Figure 2-3 indicates that V_{DDmin} increases as the number of stages increases. Note that the simulations are executed only up to 1k stages due to the simulation time constraint. Since the simulated results agree with the measurements in Figure 2-3, various simulations are conducted to clarify determinant factors of V_{DDmin} in the rest of this paper.

A closed-form expression of the V_{DDmin} described in [4] is shown as,

$$V_{DDmin} = \frac{\sigma_{pn}}{a}\sqrt{\ln\left(\frac{N}{b}\right)} + c \qquad (2\text{-}1)$$

$$\sigma_{pn} = \sqrt{\sigma_p^{\,2} + \sigma_n^{\,2}} \qquad (2\text{-}2)$$

where N is the number of stages, σ_p (σ_n) is the standard deviation of within-die V_{TH} variations of pMOS (nMOS), a is a constant determined by DIBL coefficient, b is a constant determined by yield, and c denotes the balance of the strength of nMOS and pMOS. The standard deviation (σ) of V_{TH} variation can be expressed as noted in [5],

$$\sigma = \frac{A_{VT}}{\sqrt{LW}}, \qquad (2\text{-}3)$$

where A_{VT} is Pelgrom coefficient, L is the gate length, and W is the gate width.

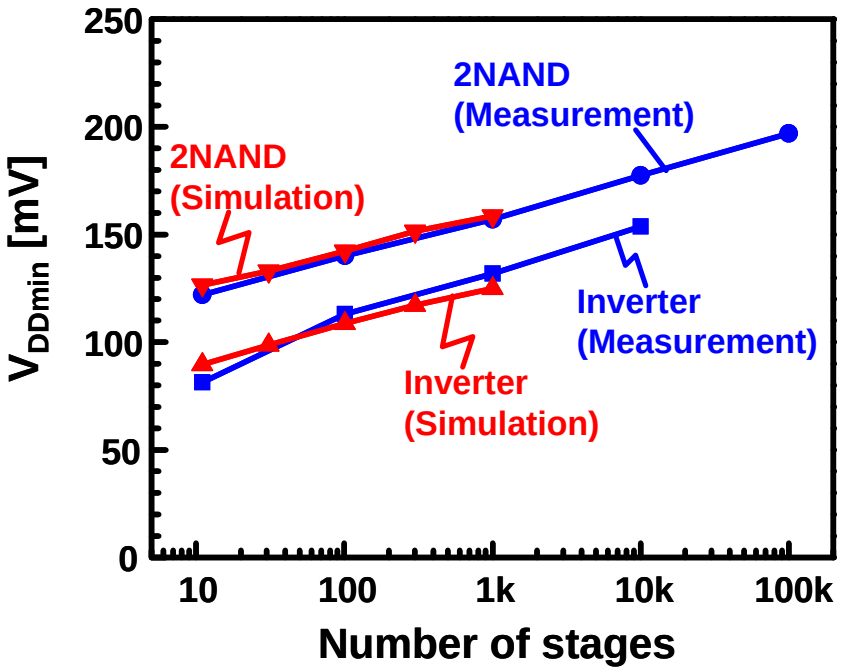


Figure 2-3. Measured and simulated dependence of V_{DDmin} on number of stages in inverter and 2NAND chains.

By using Equation (2-1), determinant factors of V_{DDmin} are investigated in this paper. Figure 2-4 shows the simulated dependence of V_{DDmin} on the number of stages in the inverter chain with and without random V_{TH} variation. V_{DDmin} consists of the following two components; the systematic component ($V_{DDmin(SYS)}$), and the random variation component ($V_{DDmin(RAND)}$). $V_{DDmin(SYS)}$ is obtained by simulations without within-die V_{TH} variation represented as the lower line, while $V_{DDmin(RAND)}$ is defined as the difference between two lines in Figure 2-4. While $V_{DDmin(RAND)}$ depends on the number of stages, $V_{DDmin(SYS)}$ does not. Therefore, $V_{DDmin(RAND)}$ corresponds to the first term in Equation (2-1) and $V_{DDmin(SYS)}$ corresponds to the second term (=*c*) in Equation (2-1). $V_{DDmin(RAND)}$ depends on the random V_{TH} variation and the number of stages of logic gates, while $V_{DDmin(SYS)}$ is determined by the balance of nMOS and pMOS.

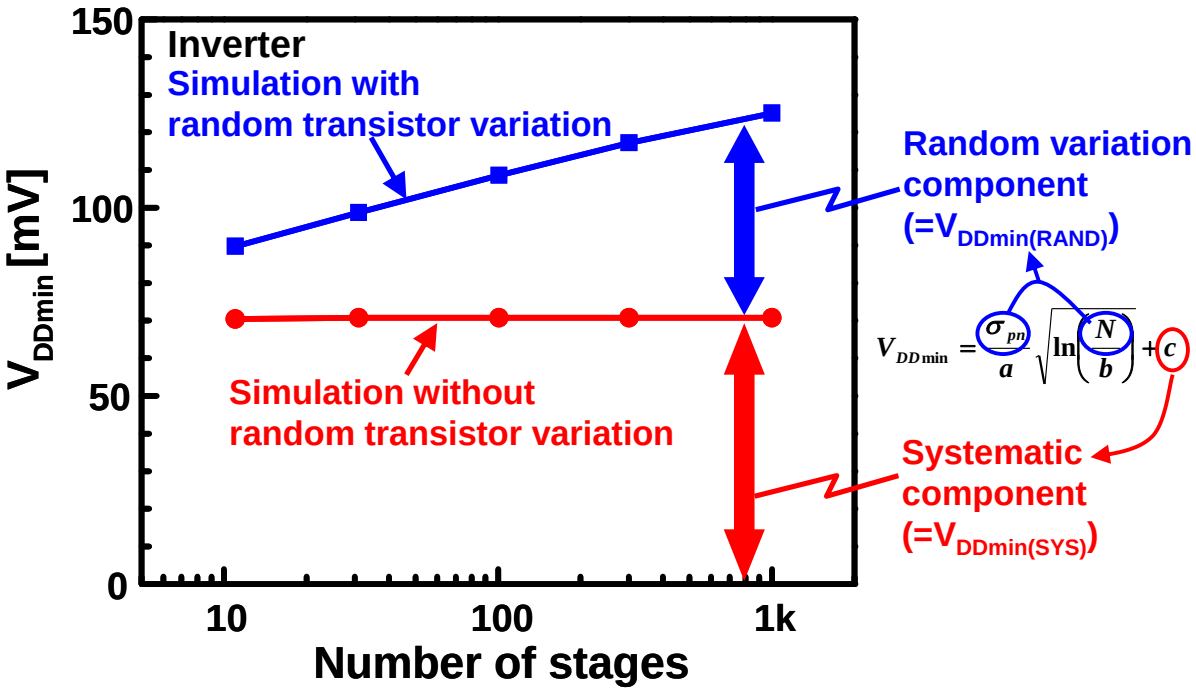


Figure 2-4. Simulated dependence of V_{DDmin} on number of stages in inverter chain with and without random V_{TH} variation.

2.3.2. Gate sizing to reduce V_{DDmin}

In order to examine the dependence of V_{DDmin} on the balance of the drive strength of nMOS and pMOS, Monte Carlo simulations for the 101-stage inverter chain are conducted with various V_{TH} of pMOS to change the balance. Figure 2-5 shows the simulated dependence of V_{DDmin} of the inverter chain on V_{TH} shift of pMOS (ΔV_{TP}) with and without random V_{TH} variation. In this simulation, ΔV_{TP} is shifted by changing the parameter in SPICE. $V_{DDmin(SYS)}$ depends on ΔV_{TP} and is minimum at ΔV_{TP}=30mV, where nMOS and pMOS are balanced. On the other hand, $V_{DDmin(RAND)}$ is constant, because σ of within-die V_{TH} variation does not depend on ΔV_{TP}. This result indicates that $V_{DDmin(SYS)}$ is determined by the balance of nMOS and pMOS, which is predicted by Equation (2-1).

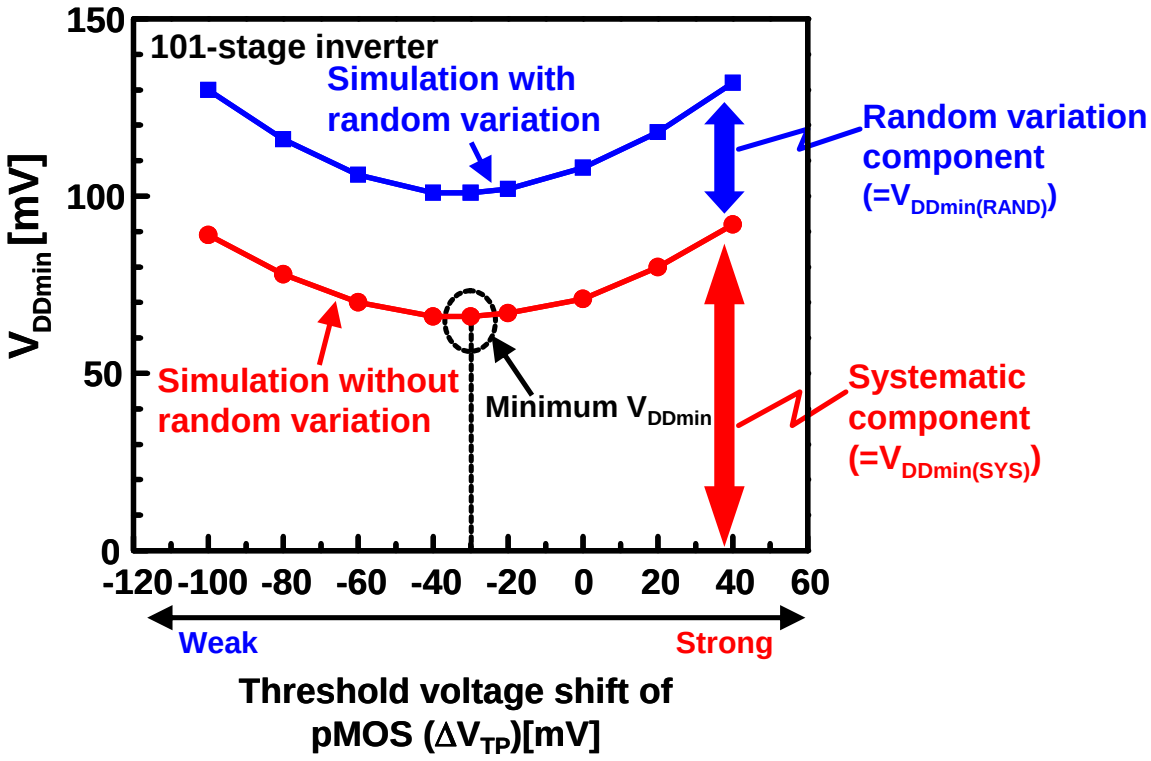


Figure 2-5. Simulated dependence of V_{DDmin} of inverter chain on V_{TH} shift of pMOS (ΔV_{TP}) with and without random V_{TH} variation.

In [6], $V_{DDmin(SYS)}$ of subthreshold circuits is minimized by tuning the logic threshold voltage to half V_{DD}. To confirm the effect of this tuning, the dependence of the normalized logic threshold voltage on ΔV_{TP} at different V_{DD} is simulated without random V_{TH} variation as shown in Figure 2-6. The definition of the logic threshold voltage is shown in the inset of Figure 2-6. The logic threshold voltage is normalized by each V_{DD}. When the logic threshold voltage is equal to half V_{DD} at each V_{DD}, ΔV_{TP} is -30mV, where the minimum V_{DDmin} is achieved as shown in Figure 2-5. This result indicates that $V_{DDmin(SYS)}$ is minimized when the logic threshold voltage is equal to half V_{DD}.

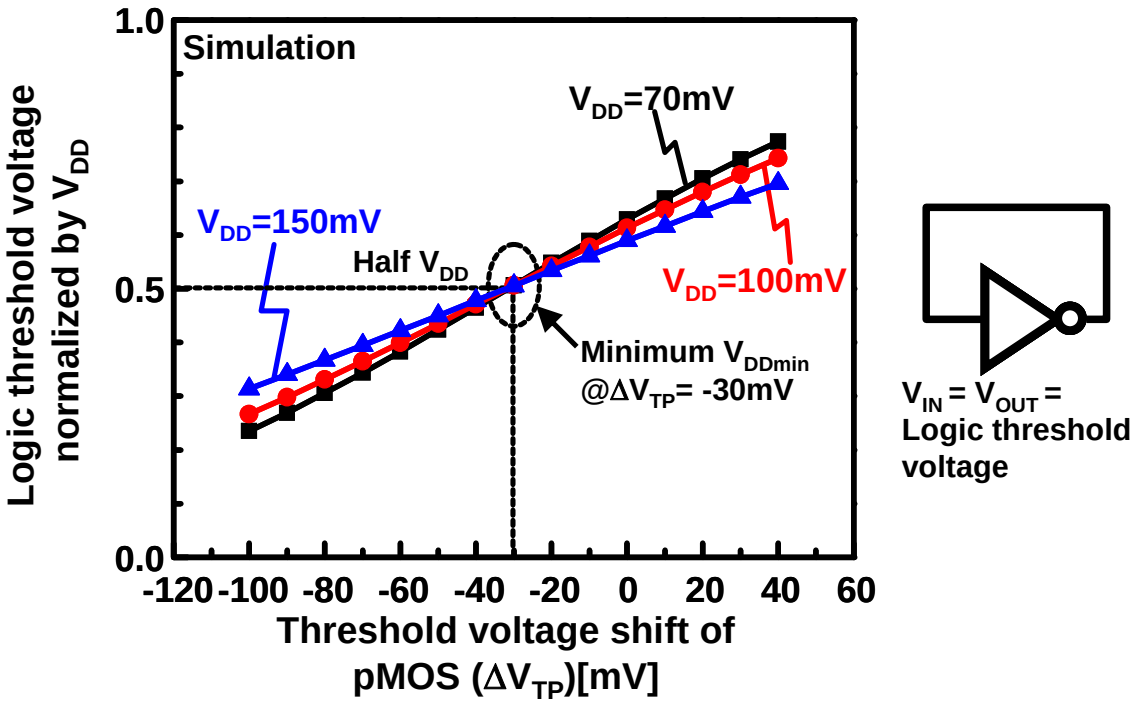


Figure 2-6. Simulated dependence of normalized logic threshold voltage on ΔV_{TP} at different V_{DD} without random V_{TH} variation.

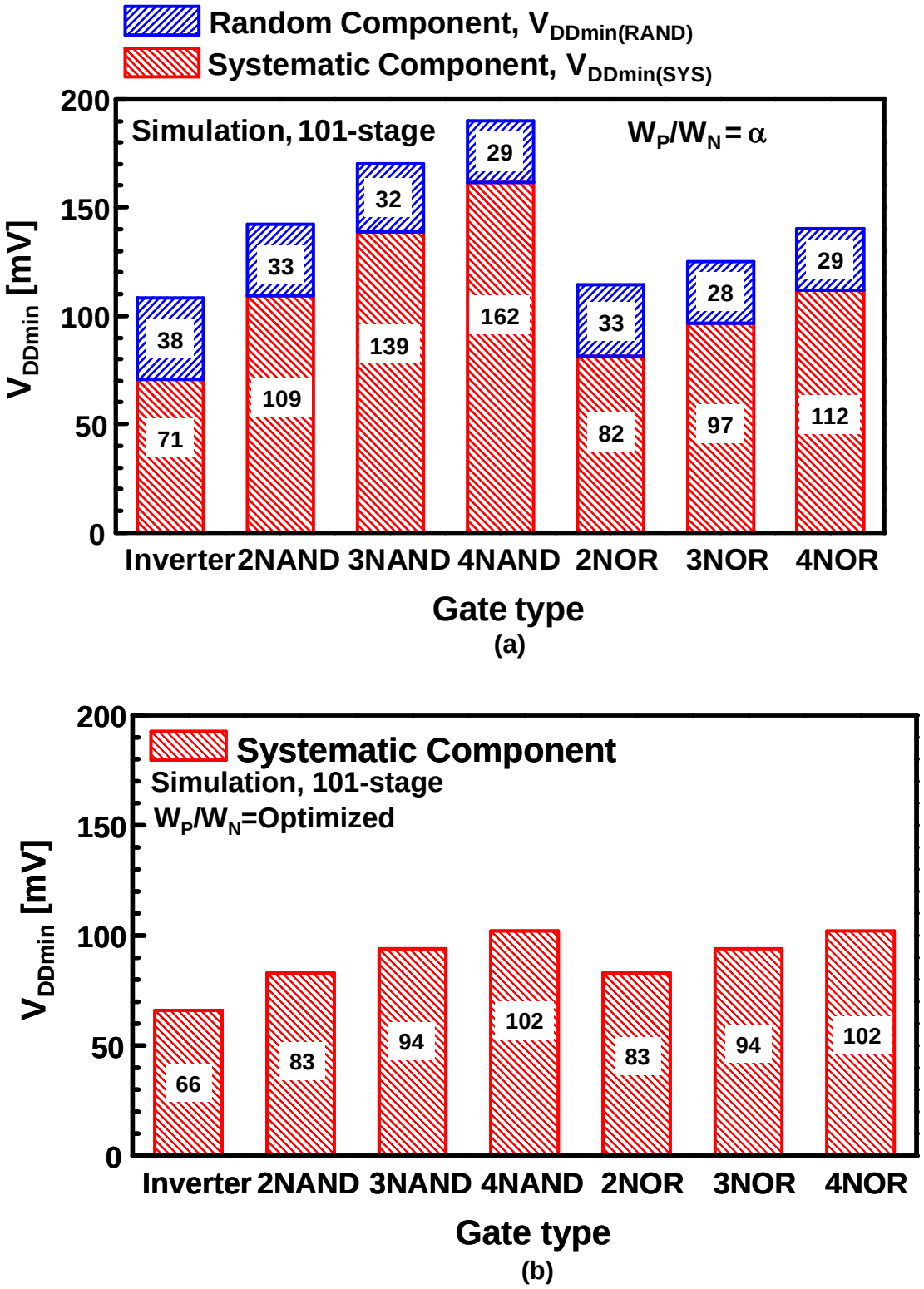


Figure 2-7. Simulated dependence of V_{DDmin} of 7 types of 101-stage chains with different logic gates. (a) W_P/W_N of all logic gates is constant . (b) W_P/W_N of each logic gate is optimized as shown in Fig. 8.

Figure 2-7 (a) shows the simulated dependence of V_{DDmin} of 7 types of 101-stage chains with different logic gates. W_P/W_N of all logic gates is constant which is defined as α in Figure 2-7 (a) and all logic gates operate as an inverter, i.e. one of the inputs of each logic gate is connected to the output of the previous stage and other inputs are tied to V_{DD} or V_{SS} in NAND and NOR gates, respectively. As shown in Figure 2-7 (a), V_{DDmin} of each logic gate is divided into $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$. $V_{DDmin(SYS)}$ increases as the number of inputs of the logic gates increases (e.g. 4NAND and 4NOR), because stacking and paralleling transistors worsen the balance of the strength of nMOS and pMOS and hence the logic threshold voltages deviate from half V_{DD}. In contrast, $V_{DDmin(RAND)}$ decreases as the number of inputs of the logic gates increases, because stacking and paralleling transistors decreases the transistor variations.

Logic threshold voltages, however, can be tuned to half V_{DD} by changing the gate size (W_P/W_N) in each logic gate at a design stage. Figure 2-8 shows the simulated dependence of normalized logic threshold voltage on the normalized W_P/W_N. for 7 types of logic gates. For example, in 4NAND gate, when W_P/W_N is 0.11 α, the logic threshold voltage is half V_{DD}, which means that W_N of 4NAND must be 8.8 W_P to minimize $V_{DDmin(SYS)}$. When too large or small W_P/W_N is not acceptable due to the area constraint, the logic gates with a lot of inputs (e.g. 4NAND and 4NOR) should not be used in the design of subthreshold logic circuits. Figure 2-7 (b) shows the simulated dependence of $V_{DDmin(SYS)}$ of 7 types of 101-stage chains with different logic gates when W_P/W_N of each logic gate is optimized to have the logic threshold voltage of half V_{DD} as shown in Figure 2-8. For example, in 4NAND gate,

$V_{DDmin(SYS)}$ can be reduced from 162mV to 102mV by optimizing W_P/W_N. as shown in Figure 2-7 (a) and (b). $V_{DDmin(SYS)}$ in Figure 2-7 (b) increases with increasing number of inputs of the logic gates, because the inverter gain is degrade in stacked transistors. It is noted that $V_{DDmin(SYS)}$'s of the number of inputs of the logic gates (e.g. 2NAND and 2NOR) are the same, because the number of the stacked transistors is the same.

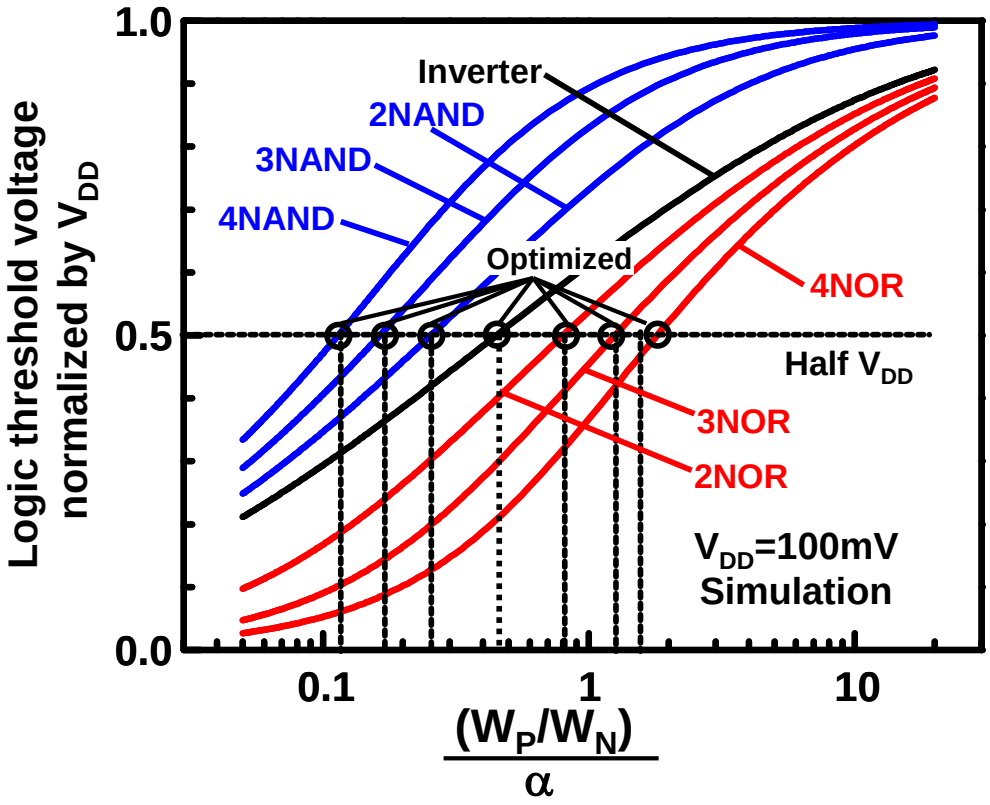


Figure 2-8. Simulated dependence of normalized logic threshold voltage on normalized W_P/W_N for 7 types of logic gates.

While $V_{DDmin(SYS)}$ is minimized by optimizing W_P/W_N, $V_{DDmin(RAND)}$ is reduced by increasing W_N and W_P. Figure 2-9 shows the simulated dependence of V_{DDmin} on the number of stages in the inverter chain with 3 types of gate width. The gate widths of

nMOS and pMOS in "x2 inverter" are two times larger than those in "x1 inverter." W_P/W_N is α in all the inverters. The gate width does not affect the balance of the strength of nMOS and pMOS. Therefore, $V_{DDmin(SYS)}$'s of the three types of gate chains is completely identical as illustrated in Figure 2-9. On the other hand, as the gate width increases, $V_{DDmin(RAND)}$ decreases, σ of within-die V_{TH} variation is reduced, which is expressed in Equation (2-2). Consequently, V_{DDmin} of the "x4 inverter" chain is the lowest.

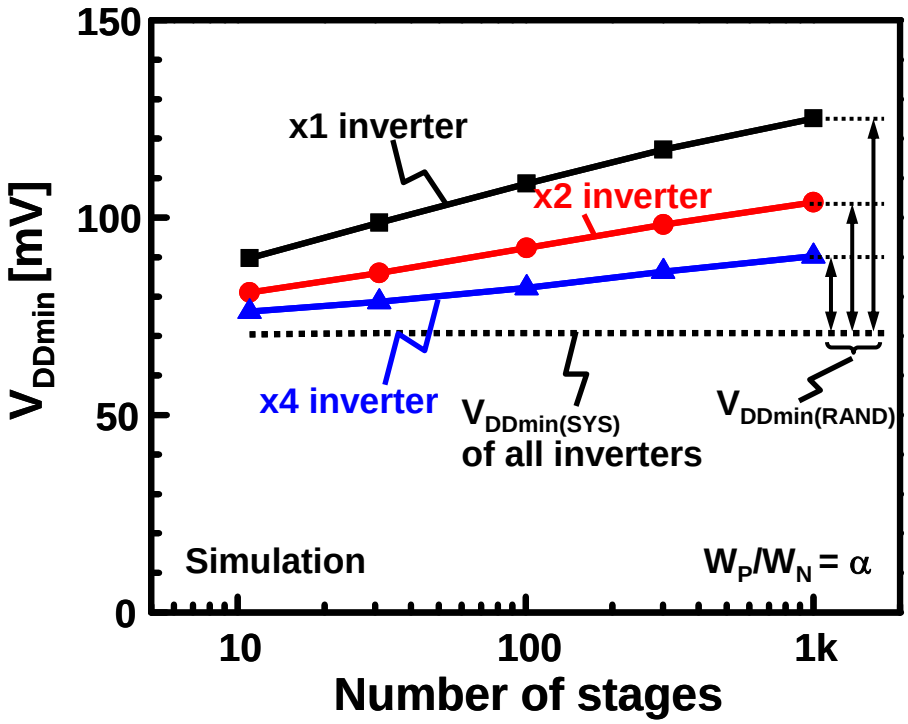


Figure 2-9. Simulated dependence of V_{DDmin} on number of stages in inverter chains with 3 types of gate width.

2.3.3. Body-biasing to reduce V_{DDmin}

Figure 2-10 shows measured dependence of V_{DDmin} on the number of stages in 2NAND chains in 2 wafers with different process corner. 17 dies in wafer 1 and 42 dies in wafer 2 are measured. The upper line is the same line depicted in Figure 2-3

and the lower line shows a different lot. These two lines are different, because the balance of nMOS and pMOS differs between the two lots due to die-to-die V_{TH} variation. In order to reduce such $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation, body-biasing is effective to compensate for the die-to-die V_{TH} variation. In this section, the effect of body-biasing is investigated.

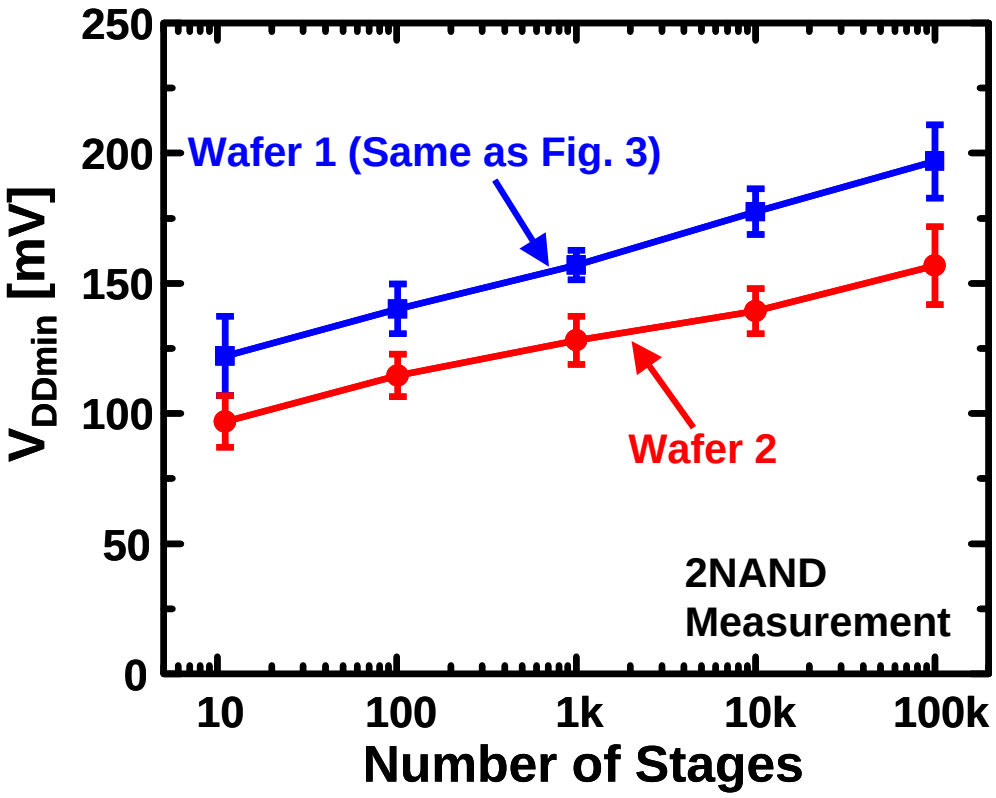


Figure 2-10. Measured dependence of V_{DDmin} on number of stages in 2NAND chains in 2 wafers with different process corner.

Figure 2-11 shows measured dependence of V_{DDmin} in a 100001 (100k)-stage 2NAND chain on the body bias voltage of nMOS and pMOS. When nMOS and pMOS are well-balanced, V_{DDmin} is low as shown in the optimal body bias line. In contrast, when nMOS and pMOS are unbalanced, V_{DDmin} increases. The initial V_{DDmin} is 189mV, when both body bias voltages are 0V. The lowest V_{DDmin} was

135mV at $V_{bs(NMOS)}$= 400mV and $V_{bs(PMOS)}$= -300mV. This indicates that balancing the nMOS and pMOS using body-biasing is effective to reduce $V_{DDmin(SYS)}$.

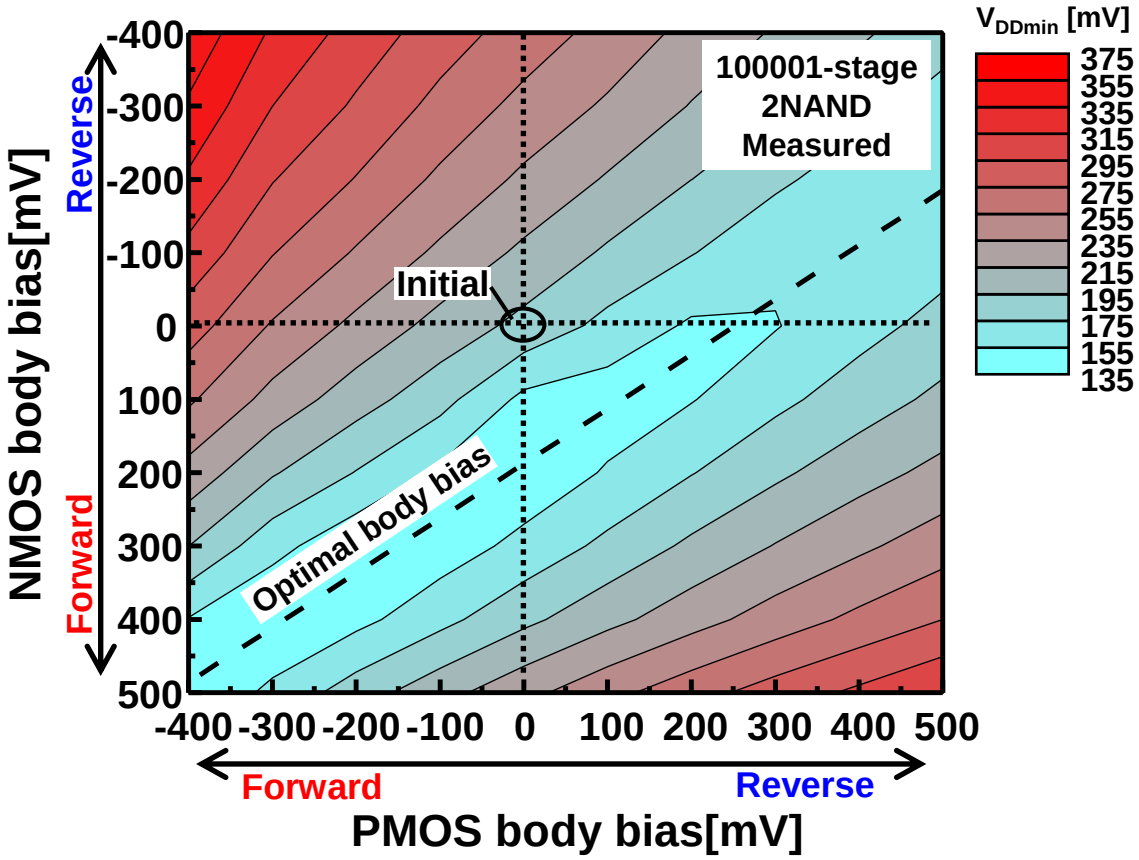


Figure 2-11. Measured dependence of V_{DDmin} in 100001-stage 2NAND chain on body bias of nMOS and pMOS.

Next, the feasibility of the post-fabrication compensation at unbalanced process corners is investigated with the 101-stage inverter chain. Figure 2-12 shows simulated $V_{DDmin(SYS)}$ with and without the compensation using pMOS body-biasing. The unbalanced process corner conditions are SF and FS. SF means slow nMOS (= high V_{TH}) and fast pMOS, whereas FS means fast nMOS (= low V_{TH}) and slow pMOS. TT means typical nMOS and pMOS, which is included as a reference. The compensation using pMOS body-biasing reduces $V_{DDmin(SYS)}$ by 88mV (from 154

mV to 66 mV) and 40mV (from 108 mV to 68 mV) in SF and FS conditions, respectively. The compensated $V_{DDmin(SYS)}$'s of the three process corners show almost same values, since the strength of pMOS and nMOS is well-balanced by body-biasing. Thus, the increase in $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation is compensated by the post-fabrication body-biasing.

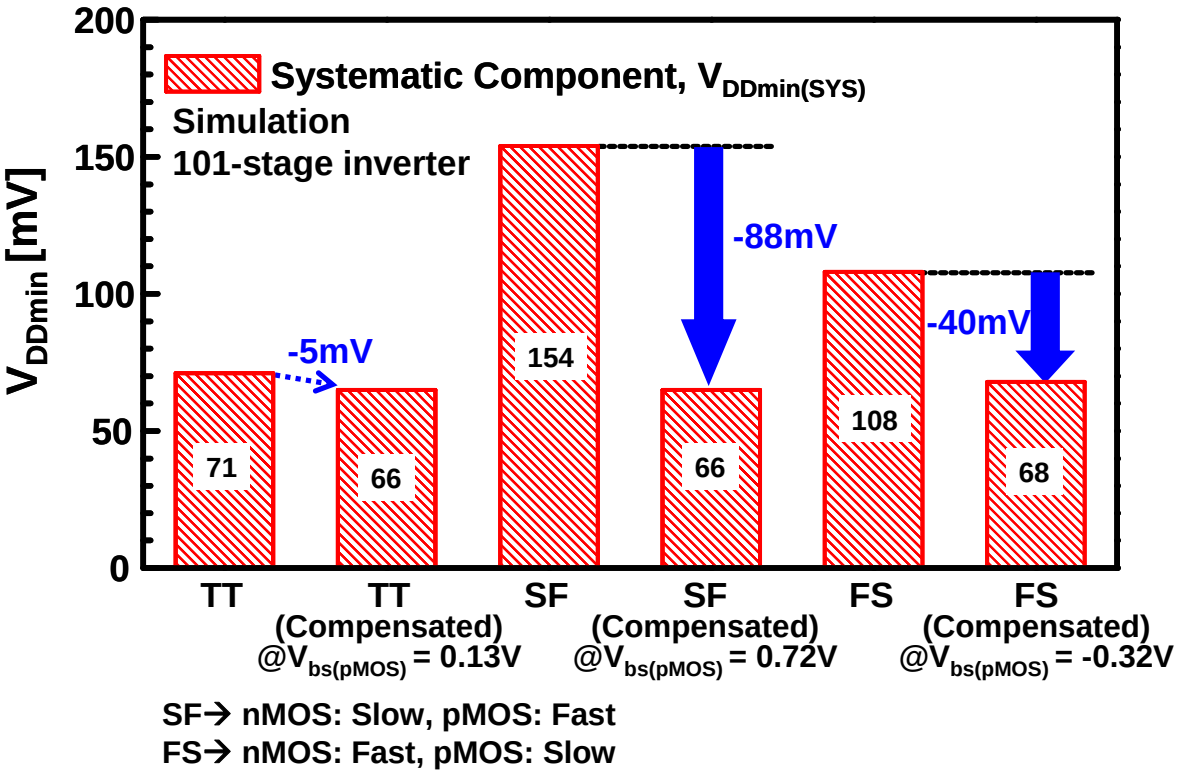


Figure 2-12. Simulated $V_{DDmin(SYS)}$ with and without the compensation using pMOS body-biasing in 101-stage inverter chain.

In addition, the body-biasing also affects $V_{DDmin(RAND)}$. Within-die V_{TH} variation is reduced by forward body biasing [7]. Tuning of both $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$ by the body-biasing is demonstrated in the measurement. Figure 2-13 shows measured dependence of V_{DDmin} on the number of stages in three body-bias conditions for the 2NAND chain. Table 2-1 summarizes the body bias conditions.

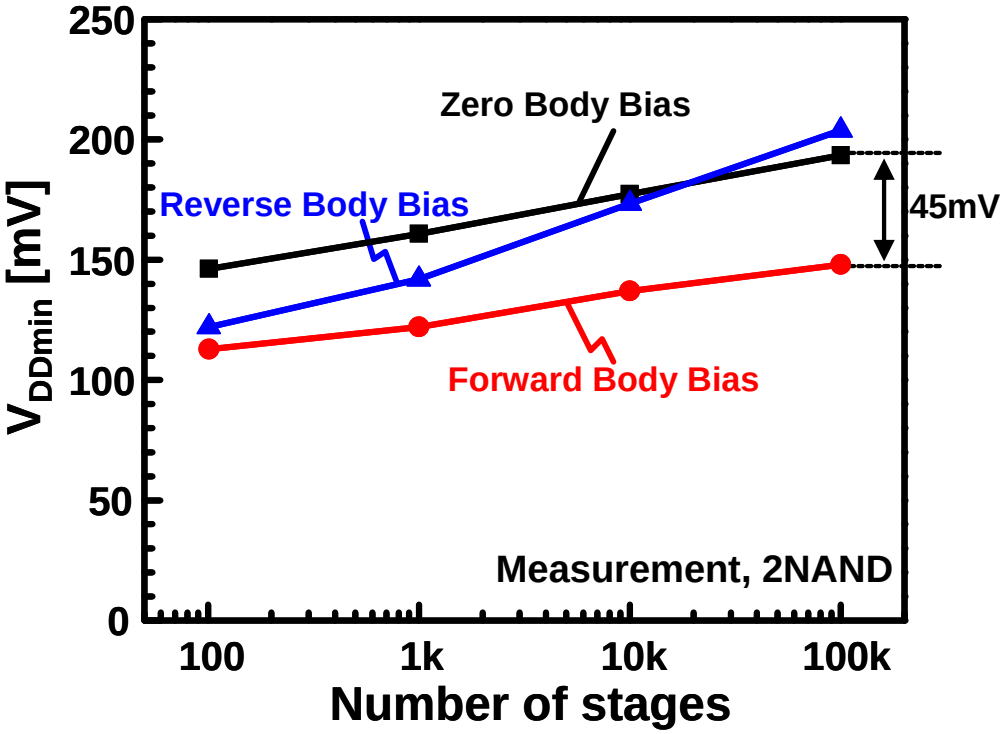


Figure 2-13. Measured dependence of V_{DDmin} on number of stages in three body-bias conditions in 2NAND chain.

Table 2-1. Body bias conditions used in Figure 2-13.

	NMOS Body Bias, $V_{bs(nMOS)}$	PMOS Body Bias, $V_{bs(pMOS)}$
Zero Body Bias	0V	0V
Forward Body Bias	0.1V	-0.25V
Reverse Body Bias	-1.0V	0.6V

Zero body bias is the initial condition and nMOS and pMOS are not balanced. On the other hand, the drive strength of pMOS and nMOS are balanced by optimizing forward body biasing or reverse body biasing as shown in Table 2-1. Figure 2-13 indicates that V_{DDmin} of both reverse and forward body bias at 101 stages is lower

than that of zero body bias, because $V_{DDmin(SYS)}$ is minimized by the optimal body biasing. It is noted that the gradient of the line shown in Figure 2-13 of reverse and forward body bias is different. The gradient of the reverse body bias is steep, while the gradient of the forward body bias is gentle, which indicates that $V_{DDmin(RAND)}$ is reduced by the forward body bias because within-die V_{TH} variation is reduced. For example, compared with the initial zero body bias, measured V_{DDmin} is reduced by 45mV from 193 mV to 148mV by forward body biasing at 100k stages. Thus, the optimal body-biasing minimizes $V_{DDmin(SYS)}$ and the forward body biasing decreases $V_{DDmin(RAND)}$.

2.3.4. Temperature dependence of V_{DDmin}

The temperature dependence of V_{DDmin} is discussed in this section. This is the first work to report the temperature dependence of V_{DDmin}. Figure 2-14 shows the measured dependence of V_{DDmin} on temperature in various inverter chains. The temperature dependence of V_{DDmin} varies with the number of stages of the chain. At 11-stage chain, V_{DDmin} increases by 10mV as temperature increases from -40˚C to 110˚C. This phenomenon is considered as a result of increase in $V_{DDmin(SYS)}$, since $V_{DDmin(SYS)}$ depends on the thermal voltage and the rise in temperature increases $V_{DDmin(SYS)}$ [4]. On the other hand, at 10001-stage chain, V_{DDmin} decreases by 25mV as temperature increases from -40˚C to 110˚C. This phenomenon implies that $V_{DDmin(RAND)}$ decreases as the temperature increases, because A_{VT} decreases with increasing temperature [8]. As a result, the worst (=highest) V_{DDmin} condition of logic circuits with small gate counts is high temperature, while the worst V_{DDmin}

condition of logic circuits with large gate counts is the worst at low temperature. Therefore, the temperature for the worst corner analysis for V_{DDmin} should be changed depending on the number of gate counts of logic circuits.

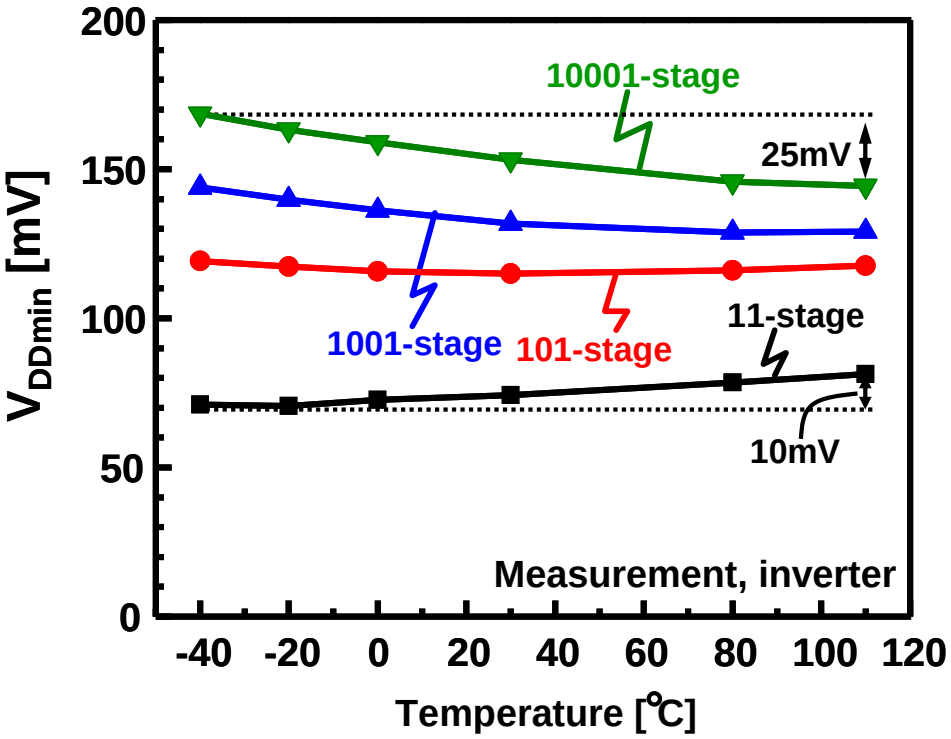


Figure 2-14. Measured dependence of V_{DDmin} on temperature in various inverter chains.

2.4 Reduction of random component of V_{DDmin}

In the previous section, determinant factors of V_{DDmin} are discussed. $V_{DDmin(SYS)}$ is minimized when the logic threshold voltage is equal to half V_{DD}. Increasing gate width of transistors reduces $V_{DDmin(RAND)}$. Increasing gate width, however, is not preferable to actual logic circuits, because it increases power consumption and area of logic circuits. Thus, optimization to reduce $V_{DDmin(RAND)}$ without increase in gate width is discussed in this section. Condition of the optimization is that total W of logic gates are constant. Namely,

$$W_P + W_N = W_{P0} + W_{N0} = Const. \quad (2\text{-}4)$$

$$W_P = W_{P0} - x \quad (2\text{-}5)$$

$$W_N = W_{N0} + x \quad (2\text{-}6)$$

where, W_N (W_P) is gate width of nMOS (pMOS), W_{N0} (W_{P0}) is initial gate width of nMOS (pMOS), and *x* is difference from initial value. Under the condition, area and power consumption will not vary. Figure 2-15 shows simulated dependence of V_{DDmin} of 101-stage inverter and normalized σ_{pn} on x.σ_{pn} is normalized by σ_{pn0} which is calculated from W_{P0} and W_{N0}. $V_{DDmin(SYS)}$ varies because balance of nMOS and pMOS changes according to *x* as discussed in previous section. $V_{DDmin(RAND)}$ in Figure 2-15 also varies according to *x* although $V_{DDmin(RAND)}$ in Figure 2-5 xx does not depend on threshold voltage of pMOS. This is explained by the difference of σ_{pn} at each point as shown Figure 2-15. When σ_{pn} is large, $V_{DDmin(RAND)}$ is also large.

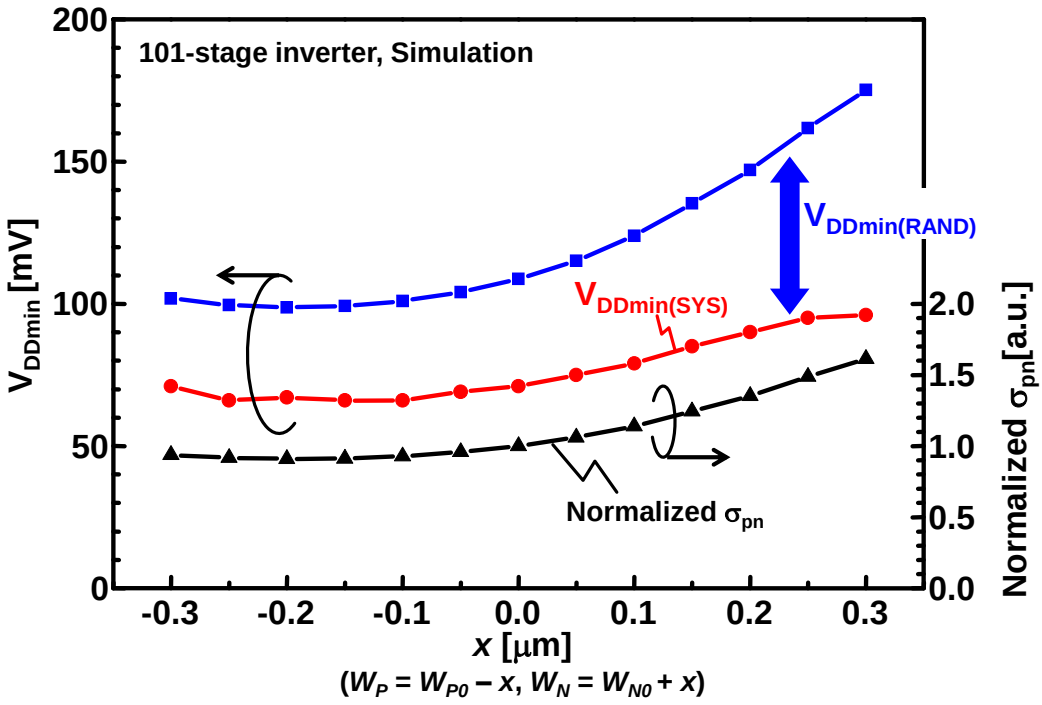


Figure 2-15. Simulated dependence of V_{DDmin} of 101-stageinverter and normalized σ_{pn} on *x*

Figure 2-16 shows the dependence of $V_{DDmin(RAND)}$ of inverter, 2NAND and 2NOR on normalized σ_{pn} when $W_P + W_N$ is constant. σ_{pn} for 2NAND and 2NOR with W_P and W_N is assumed to be equal to σ_{pn} of inverter with W_P and W_N [4]. $V_{DDmin(RAND)}$ in the figure is proportional to σ_{pn}. Thus, $V_{DDmin(RAND)}$ is minimized when σ_{pn} is minimized. Gate width which minimizes σ_{pn} is calculated as shown below.

Minimize $\sqrt{\sigma_n^2 + \sigma_p^2}$, i.e. minimize $\sigma_n^2 + \sigma_p^2$ under the condition where $W_P + W_N = C = Const.$

$$\sigma_p^2 + \sigma_n^2 = \frac{A_{VTP}^2}{LW_P} + \frac{A_{VTN}^2}{LW_N}$$
$$= \frac{1}{L}\left(\frac{A_{VTP}^2}{W_P} - \frac{A_{VTN}^2}{C - W_P} \right) \qquad (2\text{-}7)$$

The derivative of equation (2-7) is below.

$$\frac{1}{L} \cdot \frac{\{(A_{VTN} - A_{VTP})W_P + C \cdot A_{VTP}\}\{(A_{VTN} + A_{VTP})W_P - C \cdot A_{VTP}\}}{W_P^2 (W_P - C)^2}$$

Therefore, σ_{pn} is minimized. Under this condition,

$$W_N = \frac{A_{VTN} \cdot C}{A_{VTP} + A_{VTN}}, \quad W_P = \frac{A_{VTP} \cdot C}{A_{VTP} + A_{VTN}} \qquad (2\text{-}8)$$

Because $V_{DDmin(RAND)}$ increases when difference between W_N (W_P) and the optimal W_N (W_P) is large, an unbalanced pair of W_N and W_P is not acceptable to reduce $V_{DDmin(RAND)}$.

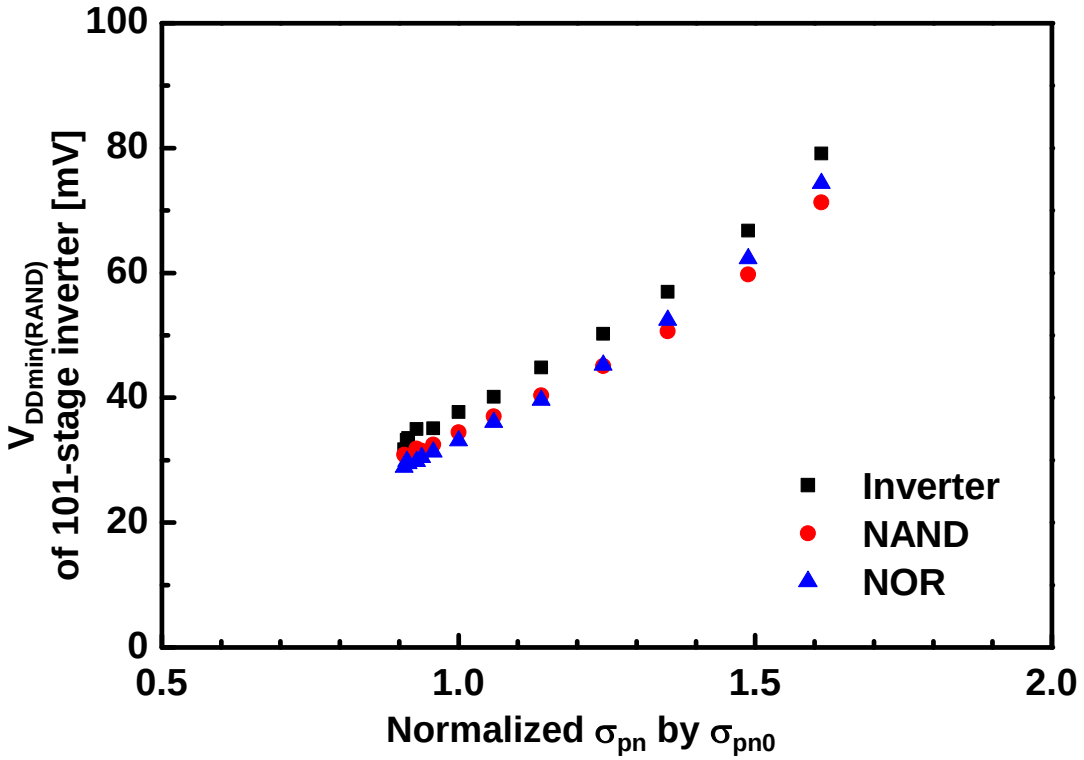


Figure 2-16. Dependence of $V_{DDmin(RAND)}$ of inverter, 2NAND and 2NOR on normalized σ_{pn}

2.5. Reduction of V_{DDmin} of general logic circuits

In this section, reduction of V_{DDmin} for general logic circuits is investigated based on the results so far. As the representative of general logic circuits, arithmetic logic unit (ALU) is adopted. Figure 2-17 shows the block diagram of ALU of which the V_{DDmin} is simulated. Number of bit counts of input is 3 and the ALU has the 8 functions controlled by F. The functions include add, subtract, divide, multiply, residue, bitwise AND, bitwise OR and bitwise EX-OR as shown Table 2-1.

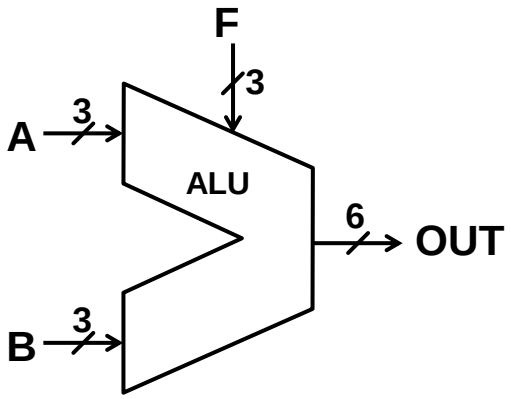


Figure 2-17. Schematic diagram of 3-bit arithmetic logic unit to simulate VDDmin.

Table 2-2. Function of ALU shown in Figure 2-17

F		
0	+	(Add)
1	-	(Subtract)
2	/	(Divide)
3	%	(Multiply)
4	*	(Residue)
5	&	(Bitwise AND)
6	|	(Bitwise OR)
7	^	(Bitwise EX-OR)

The ALU is synthesized from RTL using commercial synthesis tool. Synthesis is executed under the 3 conditions which are named standard synthesis, 2-input synthesis and 3-input synthesis respectively. Standard synthesis uses all logic gates in a standard cell library. This is included as a reference of V_{DDmin} without optimization. 2-input synthesis utilizes inverter, 2NAND and 2NOR. 3-input synthesis utilize inverter, 2NAND, 2NOR, 3NAND and 3NOR. Table 2-3 shows the statistics of gate counts after the synthesis. In case of standard synthesis, the half of

all gates are consisted of inverter, 2NAND and 2NOR and the others are consisted of other gates such as EX-OR and and-or-invert gates. Total gate counts of 2-input synthesis and 3-input synthesis is approximately doubled compared to standard synthesis because complex gates are excluded. The total area of 2-input synthesis and 3-input synthesis also increase.

Table 2-3. Statistics of gate counts for 3 synthesis types.

Statistics of gate counts

Synthesis condition	Standard	2-input	3-input
Inverter	26	47	57
2NAND	16	82	76
3NAND	0	0	12
2NOR	12	79	59
3NOR	0	0	1
Other gate	51	0	0
Total gate	105	218	205
Area	1	1.44	1.40

Synthesis type

Standard: Synthesis with all gates in library
2-input: Synthesis with Inverter, 2NAND, 2NOR
3-input: Synthesis with Inverter, 2NAND, 3NAND, 2NOR, 3NOR

Next, to reduce V_{DDmin}, inverter, 2NAND, 2NOR, 3NAND, 3NOR used in 2-input synthesis and 3-input synthesis are optimized in two ways. Table 2-4 summarizes the method for optimizations. $W_{N(INV)}$ ($W_{P(INV)}$) denotes gate width of nMOS (pMOS) of inverters, and gate width of other gates are named by same naming rules. Each of two optimizations is conducted under the condition that total gate width in each logic gate is constant in order not to increase power and area. In optimization

A, only gate width of the inverter is optimized to adjust logic threshold voltage to half V_{DD}. The gate width of the inverter is applied to the other gates. Namely, $V_{DDmin(SYS)}$ of inverter is minimized but $V_{DDmin(SYS)}$ of NAND and NOR is not minimized. In optimization B, all gates are optimized respectively to minimize $V_{DDmin(SYS)}$ of each gate. Thus, gate width differs according to gate type. Optimization A is easier than optimization B as to design and layout because all gates has same W_N and W_P.

Table 2-4. Summary of optimization method for logic gates in ALU.

Standard (Std.)	**Standard cells without no change**
Optimization A (Opt. A)	**$W_{N(INV)}$, $W_{P(INV)}$ are optimized and applied to all other gates.**
	$W_{N(INV)} = W_{N(2NAND)} = W_{N(2NOR)} = \ldots.$ **$W_{P(INV)} = W_{P(2NAND)} = W_{P(2NOR)} = \ldots.$**
Optimization B (Opt. B)	**W_N, W_P of each gate is optimized respectively.**
	$W_{N(INV)} \neq W_{N(2NAND)} \neq W_{N(2NOR)} \neq \ldots.$ **$W_{P(INV)} \neq W_{P(2NAND)} \neq W_{P(2NOR)} \neq \ldots.$**

Condition:
$W_{N(INV)} + W_{P(INV)} = W_{N(2NAND)} + W_{P(2NAND)} = W_{N(2NOR)} + W_{P(2NOR)} = \ldots. = Const.$
$(= W_{N0} + W_{P0})$

Figure 2-18 explains the definition of V_{DDmin}. V_{DDmin} is derived from DC analysis with Monte Carlo simulation. DC analysis is conducted for all possible inputs (i.e. $2^3 \times 2^3 \times 2^3 = 512$ patterns) and the number of trials for Monte Carlo simulation is 100 times. When any output in 6 outputs cross half V_{DD}, the voltage is defined as the V_{DDmin} of an input pattern in a trial shown in Figure 2-18. Simulation is conducted in the same manner by changing input pattern with 512 times. The V_{DDmin}

of a Monte Carlo trial is defined as the maximum value from V_{DDmin} of 512-input patterns because ALU does not operate correctly below the voltage. Same simulation is conducted in other Monte Carlo trials. Finally, The V_{DDmin} of ALU is calculated from averaging all V_{DDmin} of all Monte Carlo trials. $V_{DDmin(SYS)}$ is also simulated in the same way without variation of transistors.

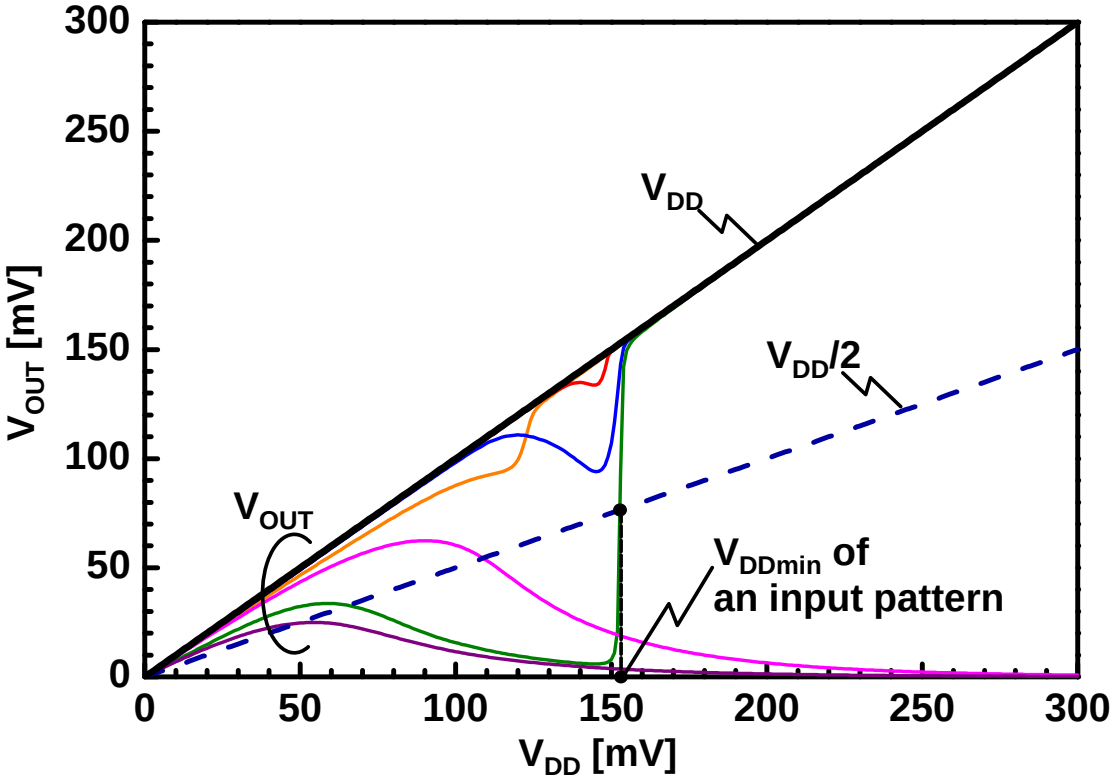


Figure 2-18. Definition for V_{DDmin} of an input pattern.

Figure 2-19 shows the simulated dependence of V_{DDmin} on all synthesis and optimization patterns. V_{DDmin} of 2-input synthesis and 3-input synthesis decreases compared to standard synthesis. $V_{DDmin(SYS)}$ of optimization B is smallest because all gates are optimized individually. Although total V_{DDmin} of optimization B is smallest in the optimization, $V_{DDmin(RAND)}$ of optimization B increases compared to

optimization A because the pair of W_P and W_N is unbalanced from the optimal point shown in equation (2-8). This means that total V_{DDmin} of optimization B exceeds total V_{DDmin} of optimization A when number of gate counts in logic circuits increases. Thus, the best design to reduce V_{DDmin} of large scale circuits is optimization A. Compared to $V_{DDmin(RAND)}$ of 2-input synthesis with optimization A, $V_{DDmin(RAND)}$ of 3-input synthesis with optimization A decreased by 6mV. Therefore, whether 2-input synthesis or 3-input synthesis is applied should be determined by circuit size. Figure 2-20 (a) and (b) shows histogram of V_{DDmin} for 2-input synthesis and 3-input synthesis. Standard deviation of each optimization is also shown. Actual operation voltage is determined by the average and sigma to meet required yield.

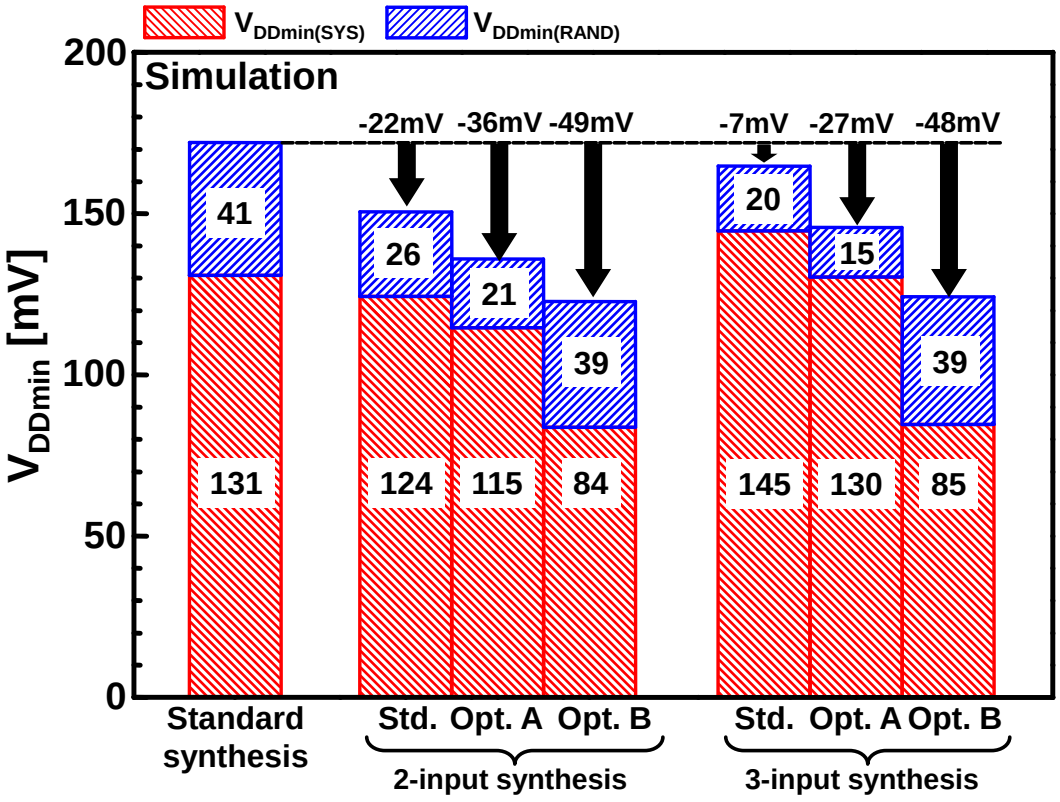
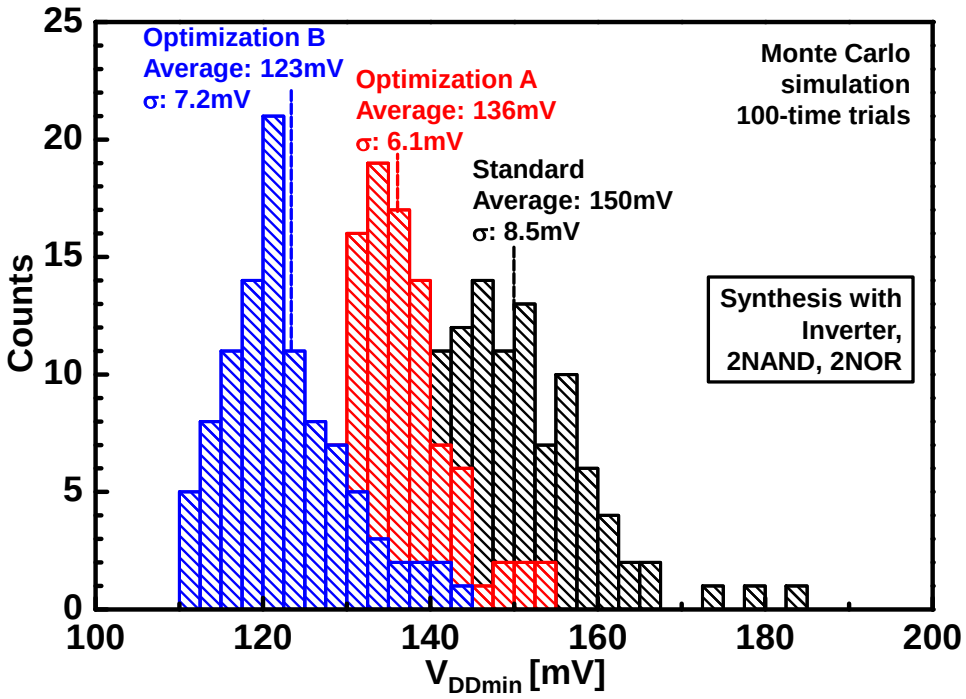
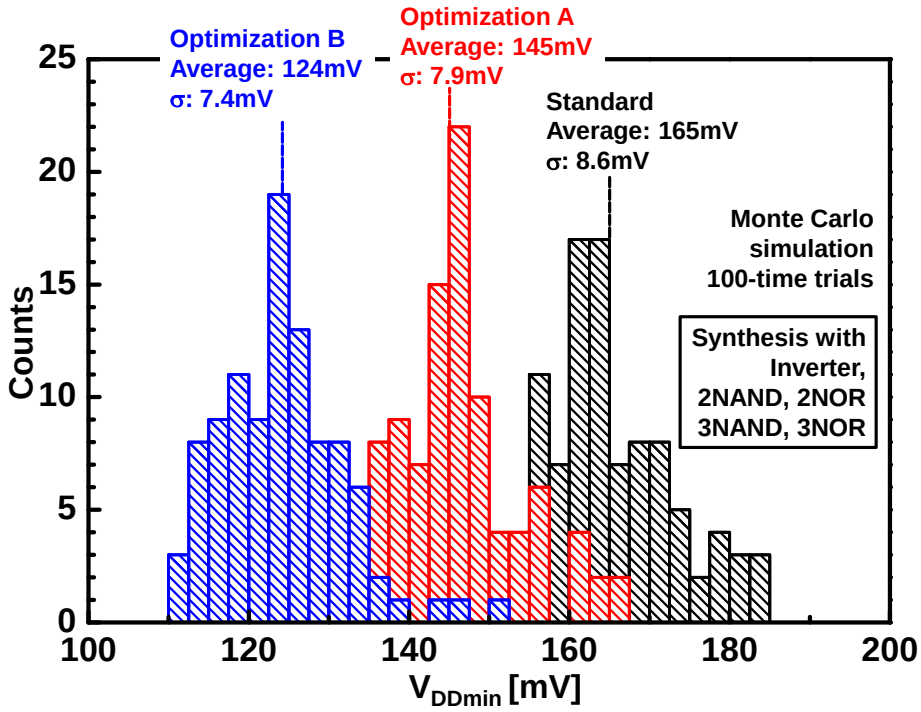


Figure 2-19. Simulated dependence of V_{DDmin} of all synthesis and optimization pattern. Standard synthesis is added as a reference.



(a)



(b)

Figure 2-20. Simulated histogram of V_{DDmin} for 2 types of optimization and standard

2.6. Optimization of F/F

In this section optimization of F/F is discussed. Figure 2-21 (a) shows schematic diagram of F/F chain to measure V_{DDmin}. The number of stage of F/F is 16 stages to 4096 stages for measurement and 10, 30, 100 stages for simulation. V_{DDmin} is defined as V_{DD} where the output of F/F is stopped. Figure 2-21 (b) illustrates the schematic of F/F. Master and slave has a same circuit. Measurement and simulation is conducted using these circuits.

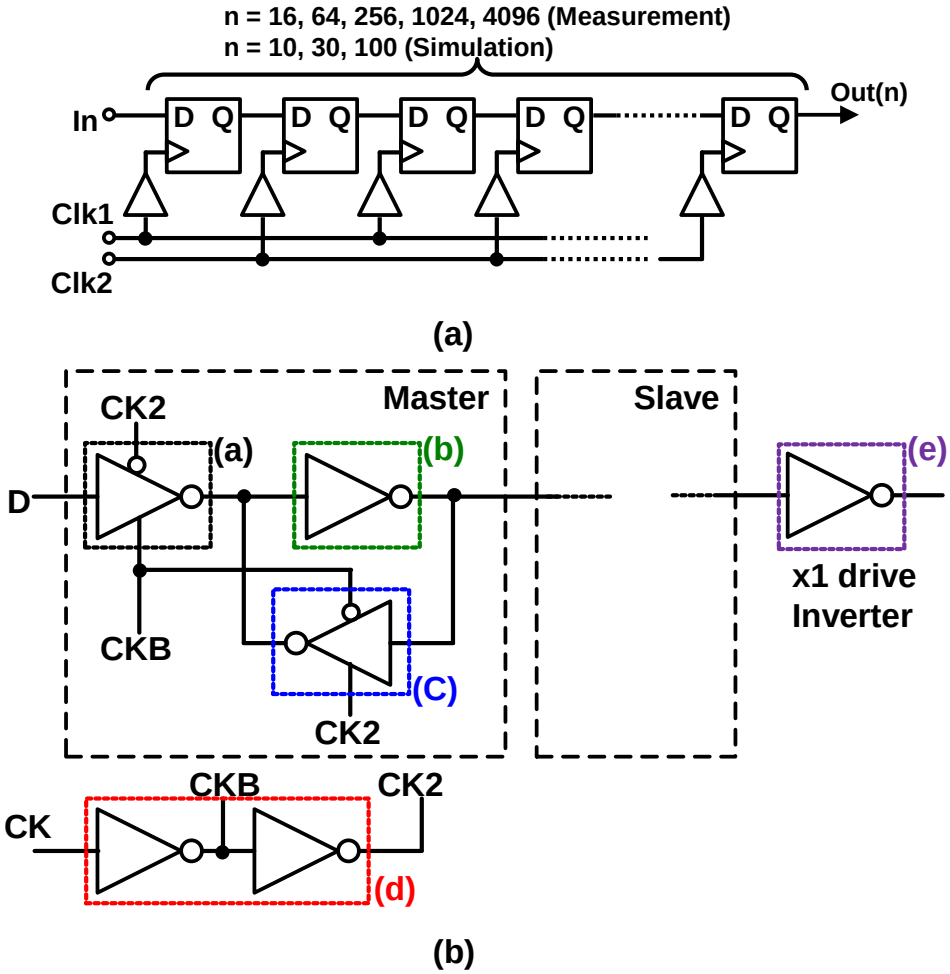


Figure 2-21. Schematic diagram of F/F to measure and simulate VDDmin. (a) Chain circuit of F/F from 16 to 4096 stages for measurement and 10 to 100 stages for simulation. (b) Schematic diagram of F/F.

Figure 2-22 shows measured and simulated dependence of V_{DDmin} on number of stages in F/F and inverter. Measured V_{DDmin} of F/F is 3-times greater than that of inverter. Thus, to achieve low voltage logic circuits, reducing V_{DDmin} of F/F is inevitable. Simulation of F/F up to 100 stages is conducted by using same circuit. Black line is the simulation with default value of threshold voltage of transistors. This line does not correspond to measurement result because threshold voltage of measured dies is not typical condition. Thus, by fitting threshold voltage of pMOS and nMOS, the simulation result is fitted to the measurement result. Since the simulated results agree with the measurement, optimization of F/F by simulation is conducted. Default value of threshold voltage is used at the optimization.

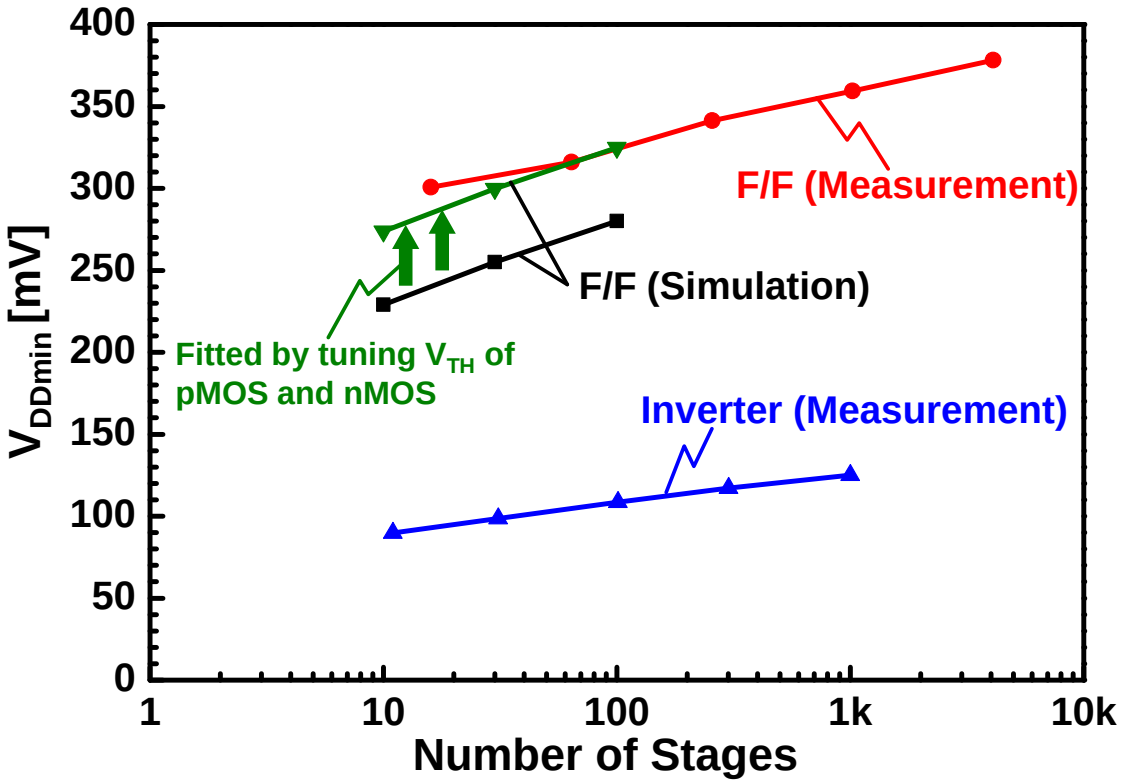


Figure 2-22. Simulated and measured dependence of VDDmin for F/F and inverter on number of stages.

At first, to reduce $V_{DDmin(SYS)}$ logic threshold voltage of each gate in the F/F is tuned to half V_{DD}. Total gate width of F/F is not changed in this optimization. Table 2-5 shows V_{DDmin} of standard and optimized F/F. Total V_{DDmin} of optimized F/F is reduced by 66mV from 230mV and $V_{DDmin(SYS)}$ of optimized F/F is reduced by 70mV from 170mV.

Table 2-5. VDDmin of standard F/F and optimized F/F.

	Standard F/F	Optimized F/F
V_{DDmin} [mV]	230	164 (-66)
$V_{DDmin(SYS)}$ [mV]	170	100 (-70)
$V_{DDmin(RAND)}$ [mV]	60	64 (+4)

$V_{DDmin(RAND)}$, however, does not changed because total gate width does not varied. Thus, to reduce $V_{DDmin(RAND)}$, sensitivity analysis to investigate which parts of F/F mainly affect on $V_{DDmin(RAND)}$ is conducted. F/F is divided into 5 parts according to its function and denoted as (a)-(e) as shown in Figure 2-21. (a), (b) and (c) is also applied to the gate which has the same function in the slave latch. When sensitivity of $V_{DDmin(RAND)}$ for (a) is investigated, transistor variations are included only for (a), and transistor variations of the other parts are not included. Same simulation is conducted for the other parts. Note that $V_{DDmin(SYS)}$ is constant because transistor size is not chanced. Figure 2-23 shows the result of sensitivity analysis. This figure shows latch part of (b) and (c) mainly affect the $V_{DDmin(RAND)}$. On the other hand, other parts such as clock buffer and output driver slightly affect on $V_{DDmin(RAND)}$. Thus, transistor size of latch parts of the F/F should be upsized to reduce $V_{DDmin(RAND)}$. Figure 2-24 shows the effect of upsizing latch on V_{DDmin}. By upsizing

transistor width in latch parts $V_{DDmin(RAND)}$ decreases by 8mV. $V_{DDmin(SYS)}$ also decreased because contention between (a) and (c) is mitigated.

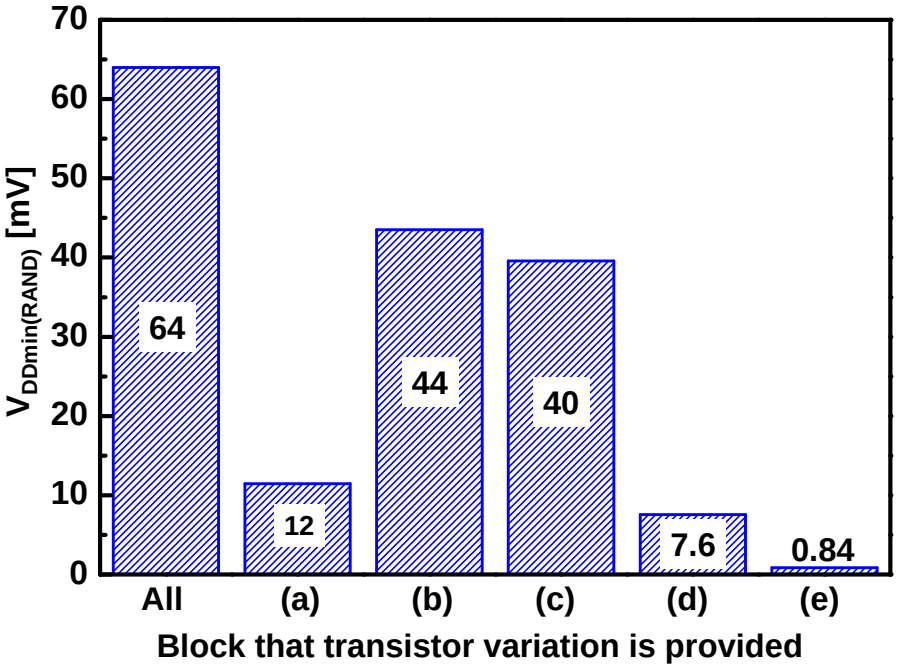


Figure 2-23. $V_{DDmin(RAND)}$ at sensitivity analysis for each part

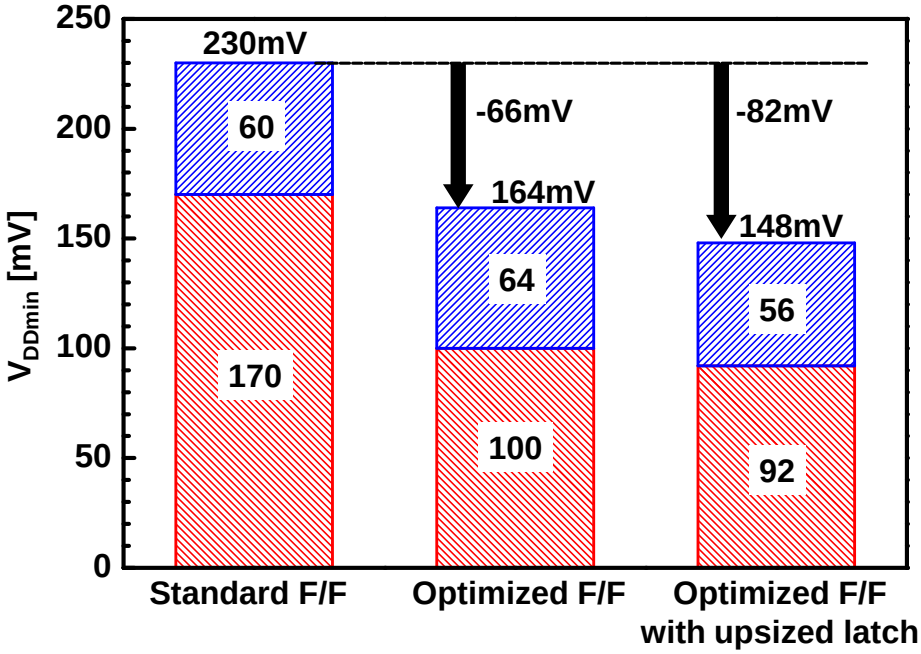


Figure 2-24. V_{DDmin} of standard F/F, optimized F/F and optimized F/F with upsized latch.

Reduction of $V_{DDmin(RAND)}$ is expanded when the number of F/F increases. Figure 2-25 shows simulated dependence of V_{DDmin} on number of F/F stages. Simulation is executed up to 100 stages and the result is extrapolated up to 1k stages based on Equation (2-1). This figure shows that difference between optimized F/F and optimized F/F with upsized latch increases at large scale circuit. Thus, optimized F/F with upsized latch reduces V_{DDmin} in large scale circuits.

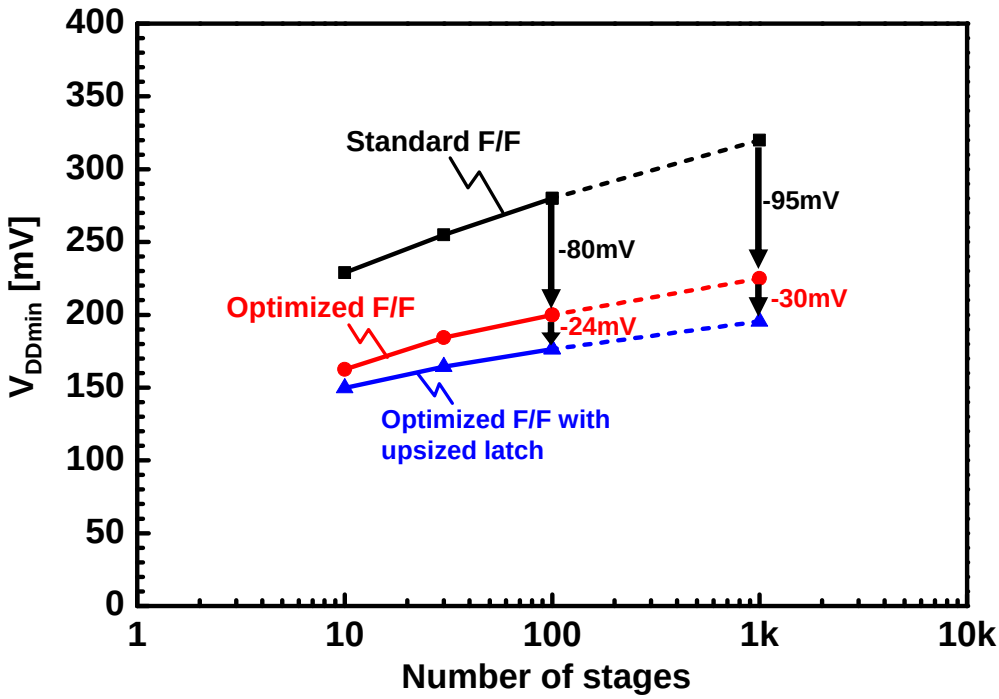


Figure 2-25. Simulated and extrapolated V_{DDmin} on number of stages up to 1k stages for standard F/F, optimized F/F and optimized F/F with upsized latch.

Table 2-6 summarizes the key features. The total gate width of optimized F/F does not change and, the total gate width of optimized F/F with upsized latch is 1.22 times larger than standard F/F. Power and Clock to Q delay at 1.2V and 0.3V is also simulated. Clock frequency to simulate power of F/F's is determined by oscillation frequency at each voltage of a ring oscillator which consists of F.O. 4 inverters.

Activity rate of F/F is 1. Power of optimized F/F almost does not change because total gate width is constant. On the other hand, power of F/F with upsized latch increases proportional to upsized gate width. Clock to Q delay of both optimization increases by x1.26 or x1.27.

Table 2-6. Summary of key features of 3types of F/F's

	Standard F/F	Optimized F/F	Optimized F/F with upsized latch
$V_{DDmin(SYS)}$ [mV]	170	100	92
V_{DDmin} [mV]			
@100stage	280	200	176
@1000stage	320	225	195
Total gate width	1	1	1.22
Power*			
@ 1.2V	1	1.05	1.25
@ 0.3V	1	0.98	1.16
Clock to Q delay			
@ 1.2V	1	1.26	1.27
@ 0.3V	1	1.27	1.26

*** Clock frequency is determined by delay of F.O. 4 inverter, and activation rate is 1.**

$V_{DDmin(SYS)}$ of F/F is reduced from 170mV to 100mV by tuning logic threshold voltage of each gate to half V_{DD} and $V_{DDmin(RAND)}$ of F/F is reduced from 64mV to 56mV by upsizing gate width of latch. At the 1k stages, V_{DDmin} of optimized F/F is 225mV and V_{DDmin} of optimized F/F with upsized latch is 195mV. These are 95mV and 125mV reduction compared to standard F/F. Thus, Optimization of F/F is necessary to achieve low voltage logic circuit because V_{DDmin} of F/F without optimization is much higher than that of combinational logic circuits.

2.7 Summary

Determinant factors of V_{DDmin} of CMOS logic gates are investigated and a design guide to reduce V_{DDmin} is shown by measurements and SPICE simulations of logic-gate chains in 65nm CMOS. V_{DDmin} consists of $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$. $V_{DDmin(RAND)}$ depends on the random V_{TH} variation and the number of stages of logic gates, while $V_{DDmin(SYS)}$ is determined by the balance of nMOS and pMOS and is minimized when the logic threshold voltage is equal to half V_{DD}. Therefore, $V_{DDmin(RAND)}$ is reduced by increasing W_N and W_P, while $V_{DDmin(SYS)}$ is minimized by optimizing W_P/W_N at a design stage. The body-biasing is effective to compensate for the increase of $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation. The optimal body-biasing minimizes $V_{DDmin(SYS)}$ and the forward body biasing decreases $V_{DDmin(RAND)}$. In the measurement of V_{DDmin} of 100k-stage 2NAND chain, V_{DDmin} is successfully reduced by 45mV from 193mV to 148mV by the forward body biasing. The temperature dependence of V_{DDmin} is measured for the first time. The worst (=highest) V_{DDmin} condition of logic circuits with small gate counts is high temperature, while the worst V_{DDmin} condition of logic circuits with large gate counts is low temperature. Therefore, the temperature for the worst corner analysis for V_{DDmin} should be changed depending on the number of gate counts of logic circuits. V_{DDmin} of general circuits and F/F's is also discussed based on the design guide to reduce V_{DDmin}. Reducing V_{DDmin} for general logic circuits constraining the total gate width per logic gate constant is also discussed. Although optimization of each gate reduces $V_{DDmin(SYS)}$, $V_{DDmin(RAND)}$ increases because of unbalanced pair of gate width of nMOS and pMOS. Thus, the best way to reduce V_{DDmin} of large scale

logic circuits is to optimize the gate width of inverter and apply it to other gates. $V_{DDmin(SYS)}$ of F/F is reduced from 170mV to 100mV by tuning logic threshold voltage of each gate to half V_{DD}. $V_{DDmin(RAND)}$ of F/F's is reduced from 64mV to 56mV by upsizing gate width of latch. V_{DDmin} of 1k-stage F/F chain could be reduced by 95mV and 125mV for optimized F/F and optimized F/F with upsized latch respectively.

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Chapter 3
Analysis of delay variation

3.1. Introduction

Reduction of power supply voltage (V_{DD}) is an effective method for achieving ultra low power logic circuits. Power consumption of CMOS logic circuits is determined by equation (3-1),

$$P = \alpha f C V_{DD}^{2} + I_{LEAK} V_{DD} \qquad (3\text{-}1)$$

where P shows power consumption, α shows an activity factor, f shows clock frequency, C shows the capacitance, and I_{LEAK} shows leakage current. From this equation, it proves that lowering V_{DD} is the most effective way to reduce power consumption of LSI's and the maximum energy efficiency is achieved at low V_{DD} (e.g., 340mV [1]). Thus, many works have been carried out on the low V_{DD} operation of logic circuits [1]-[4].

Transistor variation is, however, more pronounced at low V_{DD} [2]. This means that the design of logic circuit becomes more difficult at low V_{DD} because the transistor variation makes it difficult for logic gate paths to meet timing constraint. If enough setup time margins are considered, operation frequency lowers. By contrast, to meet hold time constraint, hold compensation buffer is inserted into logic gate paths. Therefore, investigating logic gate path delay variation is very important.

Logic gate delay is usually measured using ring oscillators [5]-[8]. Gate delay is calculated from oscillation frequency of ring oscillators. This method, however, is not good for logic testers because the logic testers are not suitable for measuring analog data

like ring oscillator's frequency. In addition, ring oscillator does not emulate real logic gates because it does not include flip-flops (F/F's)-related delays such as the clock-to-Q delay and the setup delay. In order to solve the problems, this paper proposes a tester-friendly all digital circuits to measure the dependence of within-die delay variations on V_{DD} down to 0.4V. The logic gate path delay is easily measured by changing the clock frequency. The circuit also emulates a real logic path because device under tests (DUT's) are inserted between F/F's and F/F-related delays are included in the delay measurement. This paper discusses within-die delay variation dependence on V_{DD} and several kinds of DUT's.

DUT delay dependence of the logic circuits on physical layout is also important because layout of logic circuits is usually designed by automatically using place and route (P&R) tools. In such case, interconnect capacitance is much larger than that with the manual layout. The effect of the auto place and route layout on gate delay variation is not apparent at the low voltage. This effect is also investigated in this paper.

Section 3-2 presents proposed tester-friendly all digital delay measurement circuits, and explains the operation and method of measuring logic gate delay. Section 3-3 shows the experimental results. The delay variation dependence on logic gate type is discussed. Comparison between manual layout and auto P&R is also investigated. Section 3-4 concludes this paper.

3.2. Tester-friendly all digital delay measurement circuit

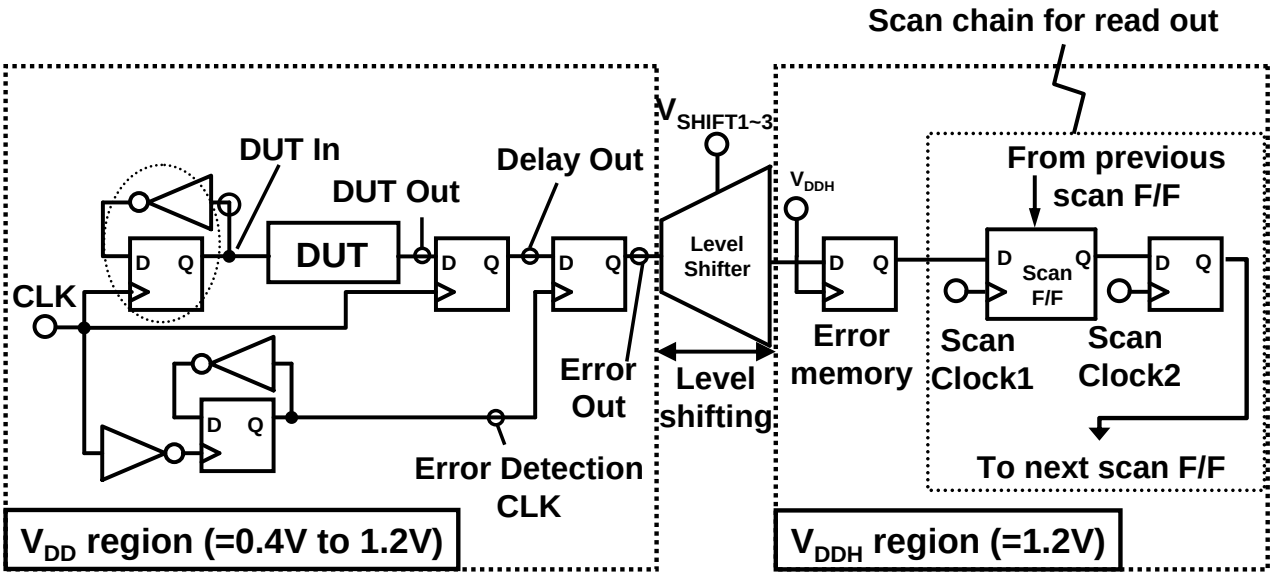
Figure 3-1 (a) shows the one unit of proposed tester-friendly all digital delay measurement circuit. This circuit is friendly to digital tester because an input of this

circuit is only clock signal, and the output of the circuit is digital serial out. DUT delay is measured by sweeping clock frequency. This feature is suitable for digital tester which can change frequency easily. DUT is inserted between two F/F's and F/F-related delays are included in the delay measurement. The left part of schematic diagram is V_{DD} region (= 0.4V to 1.2V), and the right side is V_{DDH} region (= 1.2V). DUT is placed in V_{DD} region. Delay of one DUT is measured by this unit. In the V_{DDH} region, error memory and scan chain for reading results is placed.

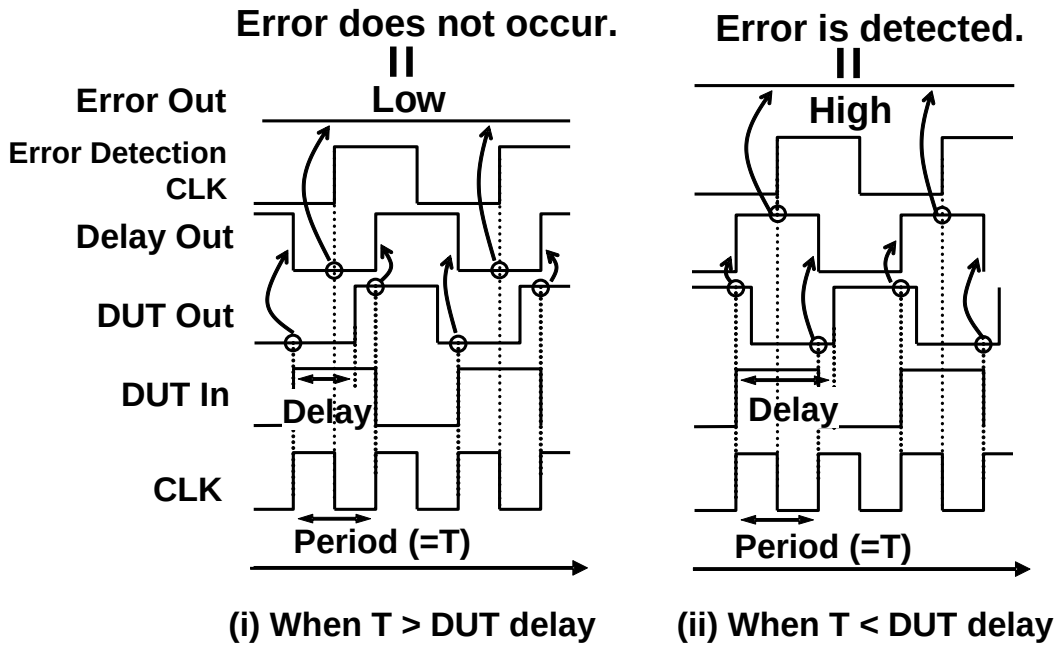
Figure 3-1 (b) shows a timing chart of delay measurement circuit. All F/F's are initialized by resetting their memory before starting measurement. Input of DUT is made from clock. Output of DUT is fetched by clock. When the DUT delay is shorter than clock period (T), an error does not occur. In contrast, when the DUT delay is longer than T, an error is detected and Error Out signal changes from low to high. Error Out signal is converted to V_{DDH} level by the level shifter and is stored in an error memory. If error occurs at least once, error memory stores high level. Output of this error memory can easily read using scan chain. In this way, DUT delay is measured digitally and the tester-friendly measurement is achieved.

Figure 3-2 shows the schematic diagram of the level shifter in Figure 3-1 (a). When V_{DD} is very low, false operation of level shifter can occur because of transistor variation. To ensure correct operation, the level shifter is consisted of 4-stage level shifters, and 3 types of voltages (V_{SHIFT1}, V_{SHIFT2} and V_{SHIFT3}) are supplied only for the level shifters. As shown in Figure 3-2, The first stage level shifter has large gate width to mitigate transistor variation. Figure 3-3 shows a block diagram of a test chip and chip micrograph. The die size is 1500μm x 490μm and is fabricated by 65nm standard CMOS process.

The test chip has two types of DUT's and each DUT type is consisted of 128 delay measurement units shown in Figure 3-1 (a). This enables to measure within-die delay variation from 128 DUT's.



(a)



(b)

Figure 3-1. Schematic and timing chart of proposed tester-friendly all digital delay measurement circuit. (a) Schematic diagram. (b) Timing chart.

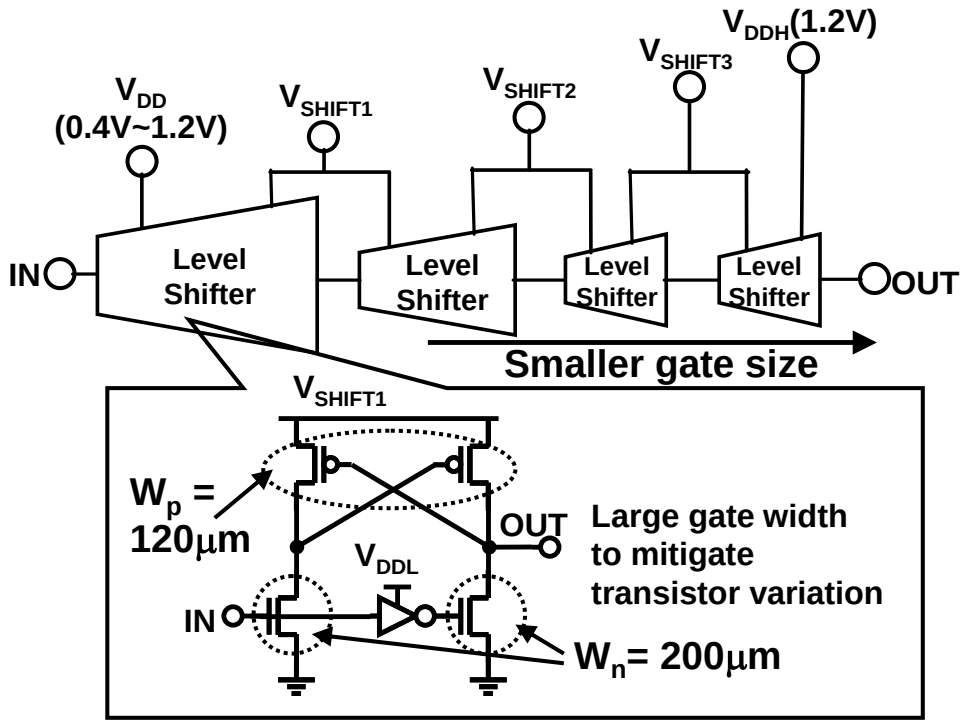


Figure 3-2. Schematic diagram of level shifter in Figure 1(a).

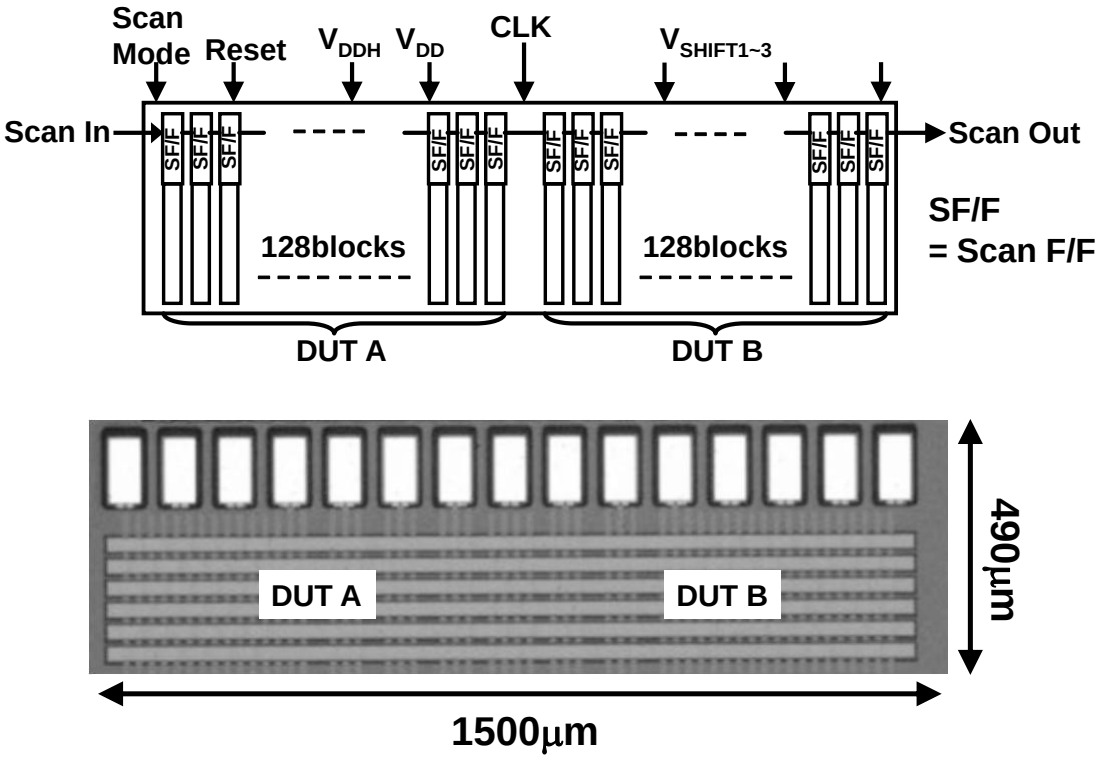


Figure 3-3. Block diagram of test chip and chip micrograph.

Figure 3-4 explains a method to measure the dependence of within-die delay variations on V_{DD} down to 0.4V. Figure 3-4 (a) shows error count dependence on clock period at single V_{DD}. Figure 3-4 (a) is measured by sweeping clock period. Figure 3-4 (b) shows a histogram of DUT delay which is obtained by differentiating Figure 3-4 (a). The standard deviation (σ) of DUT's at single power supply voltage is calculated from the histogram. Figure 3-4 (c) shows dependence of σ of delay on V_{DD} which is acquired by sweeping V_{DD} in Figure 3-4 (a) and (b).

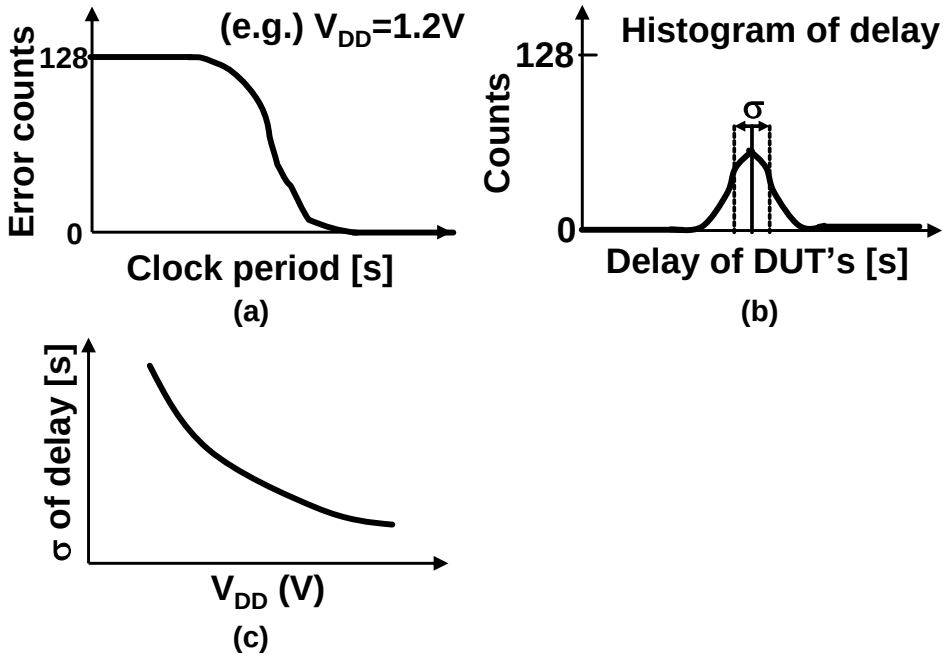


Figure 3-4. Method to measure dependence of within-die delay variations on V_{DD}. (a) Error count dependence on clock period at single V_{DD}. (b) Histogram of DUT delay. (c) Dependence of sigma of delay on V_{DD}.

Various types of DUT's are implemented to survey dependence of DUT delay on gate type, gate width, and layout method. Table 3-1 summarizes implemented DUT types. Each DUT includes 100 stages. Regarding the gate type, x1 size inverter and x1 size NAND are compared. Regarding the gate width, x0.5 size inverter and x1 size inverter

are compared. Regarding the layout method, the layout of x0.5 size inverter is designed using auto place and route tool, and compared with using the manual layout.

Table 3-1. Implemented DUT types.

Gate type	Size	Layout
Inverter	x0.5	Manual (Regular)
Inverter	x0.5	Auto P&R (Irregular)
Inverter	x1	Manual (Regular)
NAND	x1	Manual (Regular)

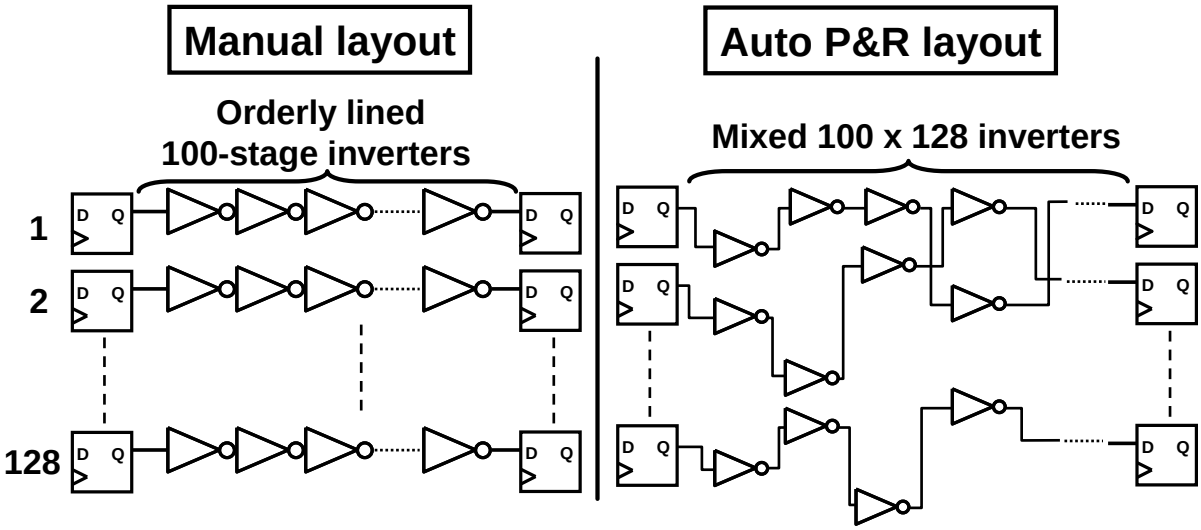


Figure 3-5. Schematic of manual layout and auto place and route layout.

Figure 3-5 shows a schematic of manual layout and auto place and route layout. In case of the manual layout, 128 paths of 100-stage inverters are in a line and the layout is regular. Meanwhile, 100 x 128 inverters are shuffled in the auto place and route layout. Table 3-2 compares key features of the manual layout and the auto place and route layout. In case of manual layout, interconnect delay is small and there is no systematic variation of interconnect because all paths have the same interconnect capacitance and resistance.

On the other hand, auto place and route has large interconnect delay and systematic variation of interconnect. Both manual layout and auto place and route have random variation of transistors.

Table 3-2. Key features of manual layout and auto place and route layout.

	Manual layout	Auto P&R layout
Random variation of transistors	w/	w/
Systematic variation of interconnection	w/o	w/
Interconnection delay	small	large

3.3. Experimental results

3.3.1. Measured dependence of within-die delay variations on V_{DD}

Figure 3-6 (a) shows the measured histogram of within-die DUT delay at V_{DD}=1.2V. NAND has largest delay because it has two stacked nMOSFET's. The auto place and route x0.5 inverter has larger delay than manual layout x0.5 inverter because of large interconnect capacitance. The auto place and route x0.5 inverter has the largest variation of DUT delay because of large interconnect variation. Figure 3-6 (b) shows the measured histogram of DUT delay at V_{DD}=0.4V. By comparing Figure 3-6 (a) and (b), DUT delay at 0.4V is larger and the delay variation at 0.4V are larger those at 1.2V. At 0.4V, the difference of delay variation between the manual layout and the auto place and route layout is reduced compared with that at 1.2V.

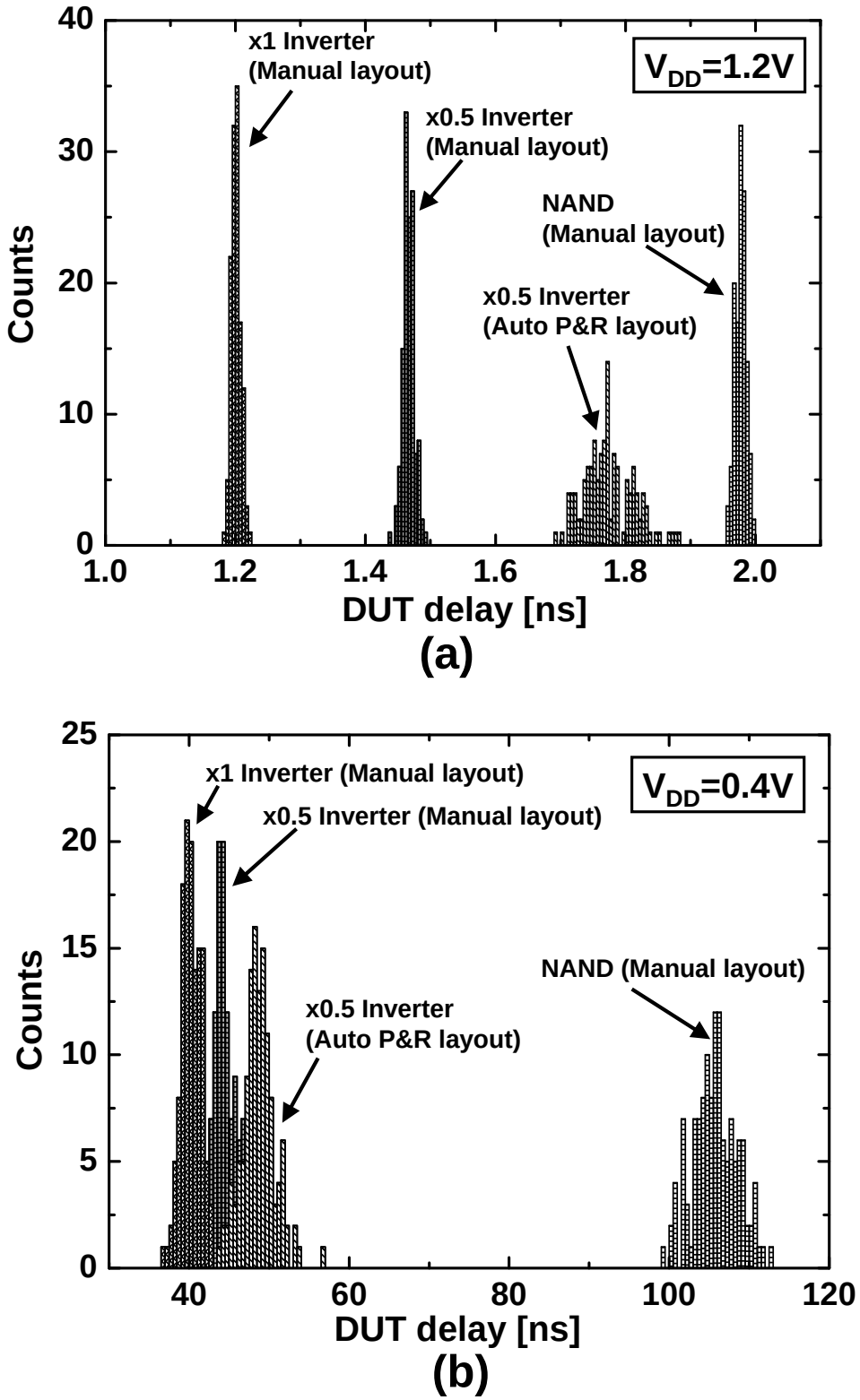


Figure 3-6. Measured histogram of within-die DUT delay. (a) V_{DD}=1.2V. (b) V_{DD}=0.4V.

Figure 3-7 shows the dependence of average DUT delay on V_{DD}. This shows average DUT delay (μ) increases with lowering V_{DD}. The delay of the manual layout inverter is always smaller than that of the auto place and route layout because of the difference of interconnect capacitance. The x1 inverter is the fastest due to its high current drivability. Figure 3-8 shows the measured dependence of standard deviation (σ) of DUT delay on V_{DD}. Although the difference of σ between the auto place and route layout and other gates is large at high V_{DD}, the difference reduces as V_{DD} is reduced. This comparison, however, is not fair because these DUT's have different delay. To fairly compare delay variation, relative delay variation derived from dividing σ by μ is introduced.

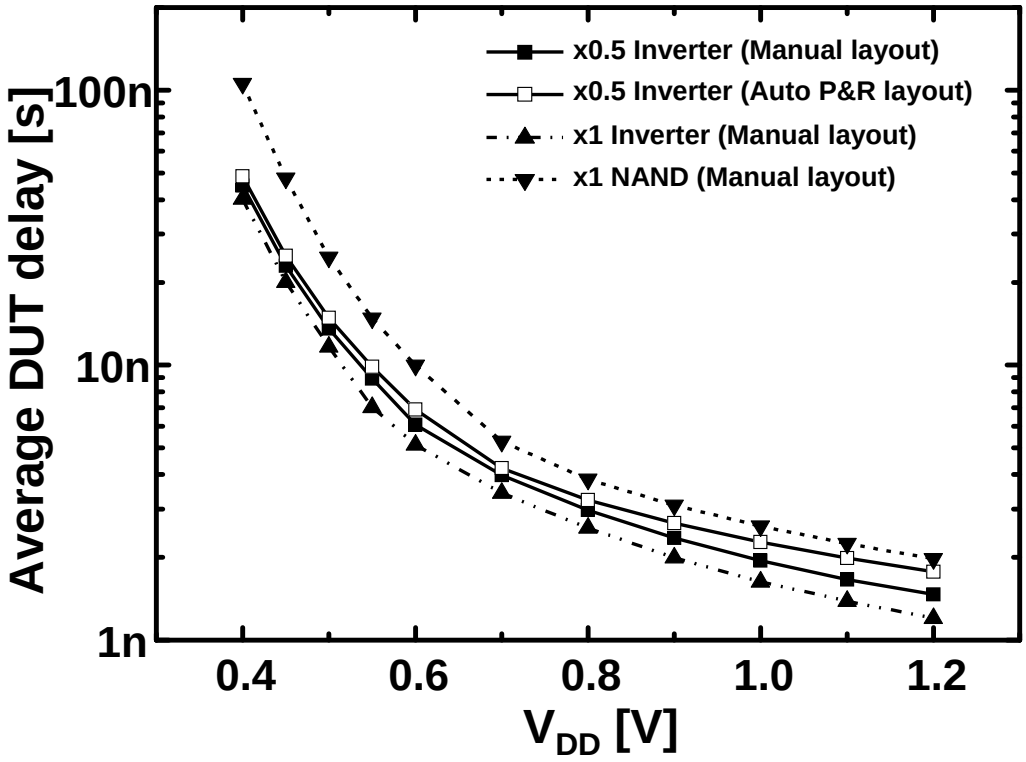


Figure 3-7. Dependence of average DUT delay on V_{DD}.

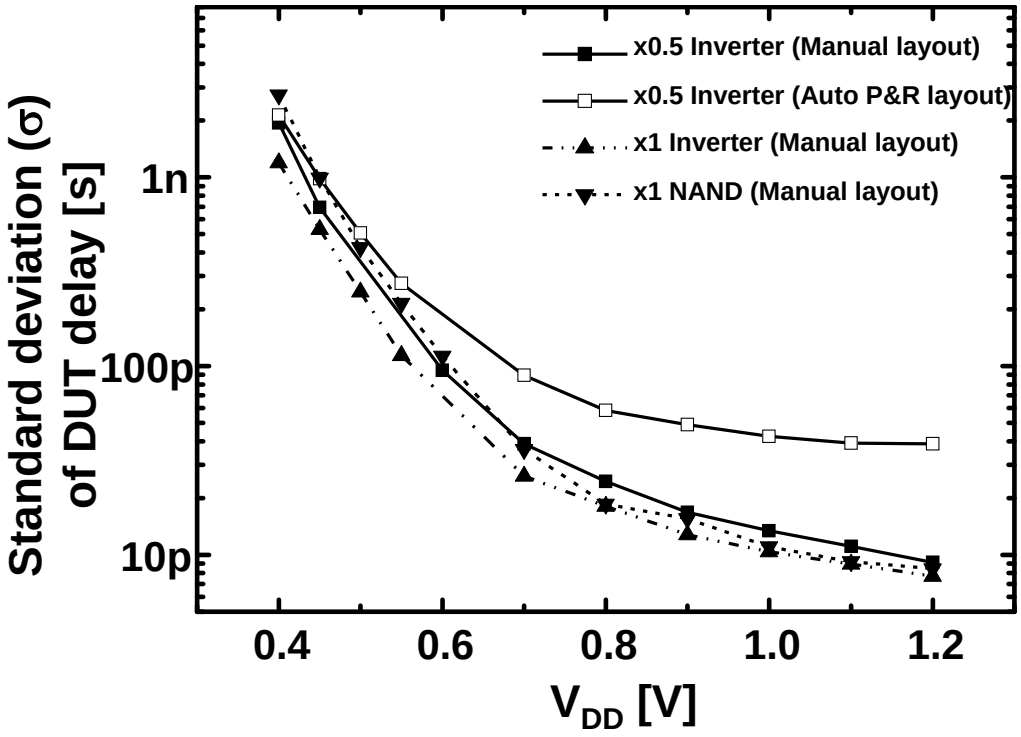


Figure 3-8. Measured dependence of standard deviation (s) of DUT delay on V_{DD}.

Figure 3-9 shows the measured dependence of relative delay variation (σ/μ) on V_{DD}. This shows that the difference of relative delay variation between manual layout and auto P&R decreases from 1.56% to 0.07% when reducing V_{DD} from 1.2V to 0.4V. This effect is explained by the following equations. Regarding manual layout, average delay (μ_M), standard deviation (σ_M) and relative delay variation (σ_M/μ_M) is expressed as Equations (3-2) - (3-4),

$$\mu_M = R_T \cdot C_T \tag{3-2}$$

$$\sigma_M = R_T \cdot \Delta C_T + \Delta R_T \cdot C_T \tag{3-3}$$

$$\frac{\sigma_M}{\mu_M} = \frac{\Delta C_T}{C_T} + \frac{\Delta R_T}{R_T} \tag{3-4}$$

where R_T is resistance of transistor, ΔR_T is standard deviation of R_T, C_T is transistor capacitance, and ΔC_T is standard deviation of C_T. The resistance and capacitance of the interconnect are ignored in Equation (3-2). Regarding auto P&R layout, Average (μ_A), Standard deviation (σ_A) and relative delay variation (σ_A/μ_A) of manual layout is expressed as (3-5) - (3-6),

$$\mu_A = R_T \cdot (C_T + C_I) \quad (3\text{-}5)$$

$$\sigma_A = R_T \cdot (\Delta C_T + \Delta C_I) + \Delta R_T \cdot (C_T + C_I) \quad (3\text{-}6)$$

$$\frac{\sigma_A}{\mu_A} = \frac{\Delta C_T + \Delta C_I}{C_T + C_I} + \frac{\Delta R_T}{R_T} \quad (3\text{-}7)$$

where C_I is capacitance of interconnection and ΔC_I is standard deviation of C_I. The resistance of the interconnect is ignored in Equation (3-5). In (3-5) and (3-7), $\Delta R_T/R_T$ term dominants σ_M/μ_M and σ_A/μ_A at low V_{DD}, the transistor variation is larger than the interconnect length variation at low V_{DD}. In this way, the difference of relative delay variation becomes small in low V_{DD} region.

In Figure 6, NAND has the smallest σ/μ, because the total gate size is the largest in four types of DUT's. More specifically, NAND consists of 4 transistors and other gates have 2 transistors. It also proved that σ/μ of x1 inverter is smaller than x0.5 manual layout inverter, because transistor variation is proportional to $1/\sqrt{LW}$ [6].

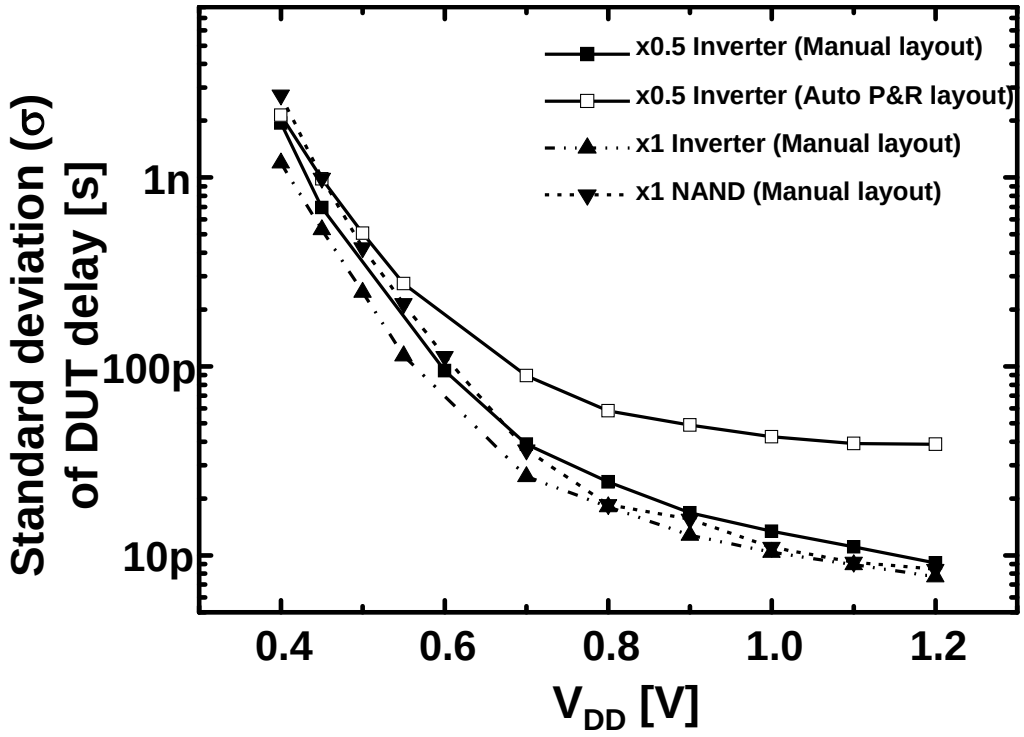


Figure 3-9. Measured dependence of standard deviation (s) of DUT delay on V_{DD}.

3.3.2. Delay variation difference between manual layout and auto place and route layout

In order to investigate the delay variation difference between the regular manual layout and the auto place and route layout, Figure 3-10 shows the measured spatial within-die DUT delay distributions normalized by the average DUT delay. This figure also shows the measured histogram of normalized DUT delay. Figure 3-10 (a) shows the manual layout inverter and Figure 3-10 (b) shows for the auto place and route layout inverter. In Figure 3-10 (a), DUT delay has only random variations caused by the random transistor variations. The magnitude of the DUT delay variation at 0.4V is larger than that at 1.2V. Figure 3-10 (b) shows that center location has larger delay than the both ends. This is caused by systematic variation of interconnect in the auto place and route layout.

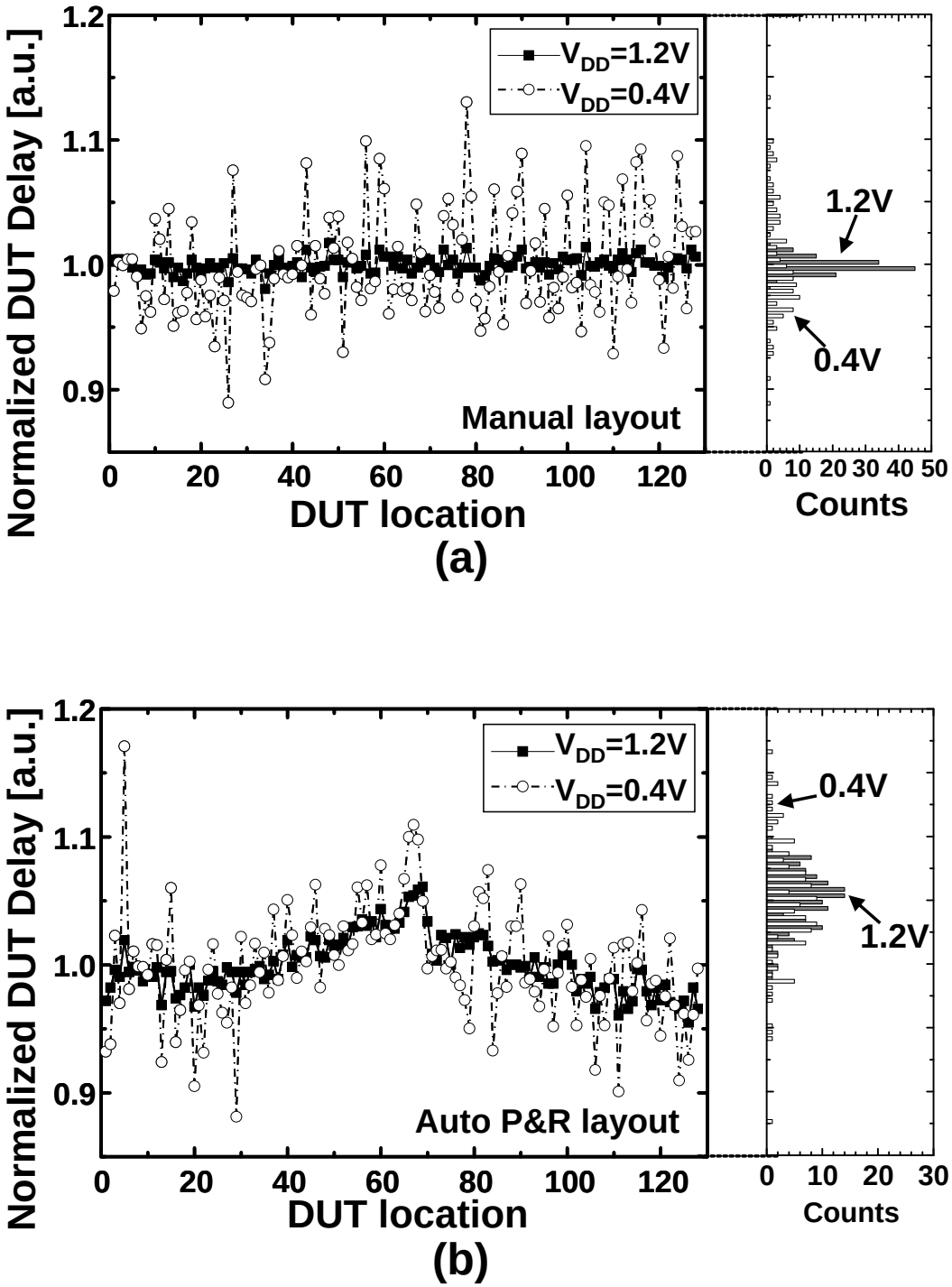


Figure 3-10. Measured spatial within-die DUT delay distributions normalized by the average DUT delay at 1.2V and 0.4V. (a) Manual layout. (b) Auto place and route layout.

Figure 3-11 shows the measured spatial within-die DUT delay distributions for two chips at 0.4V. DUT is the manual layout inverter. This proves that the variation of manual layout inverter is only caused by the random transistor variations because the two lines in Figure 3-11 have no correlation. Figure 3-12 shows the measured and simulated spatial within-die DUT delay distributions at 1.2V. DUT is the auto place and route layout inverter. The simulated results are obtained by Monte Carlo SPICE simulation after LPE. The systematic spatial delay distribution is similar between the measured and simulated results, which proves that the longer delay at center location is caused by the systematic variation of interconnect in the auto place and route layout.

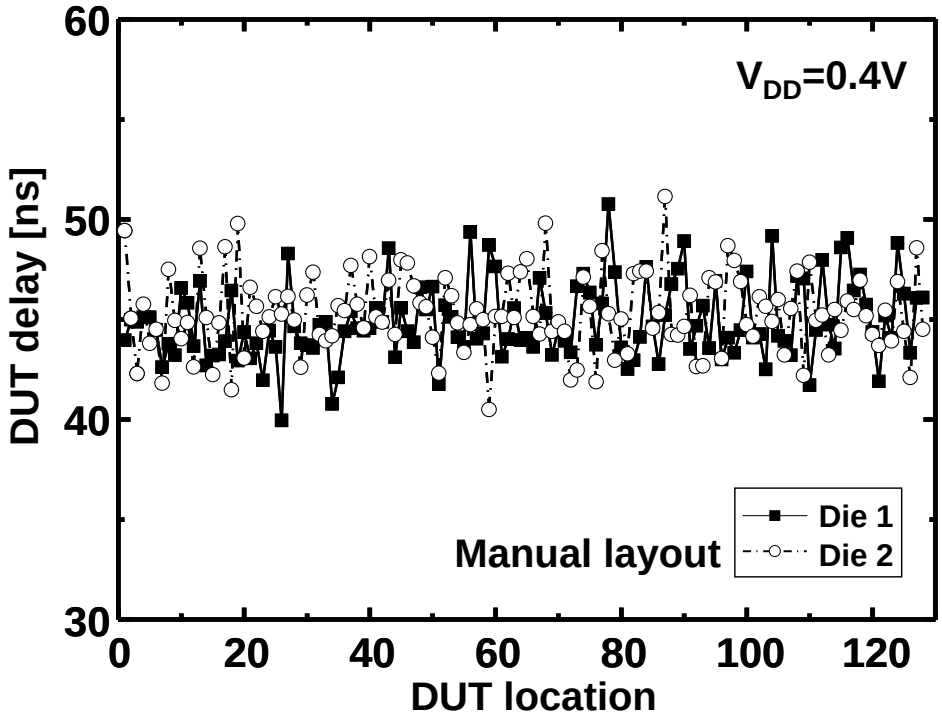


Figure 3-11. Measured spatial within-die DUT delay distributions of manual layout for two chips at 0.4V.

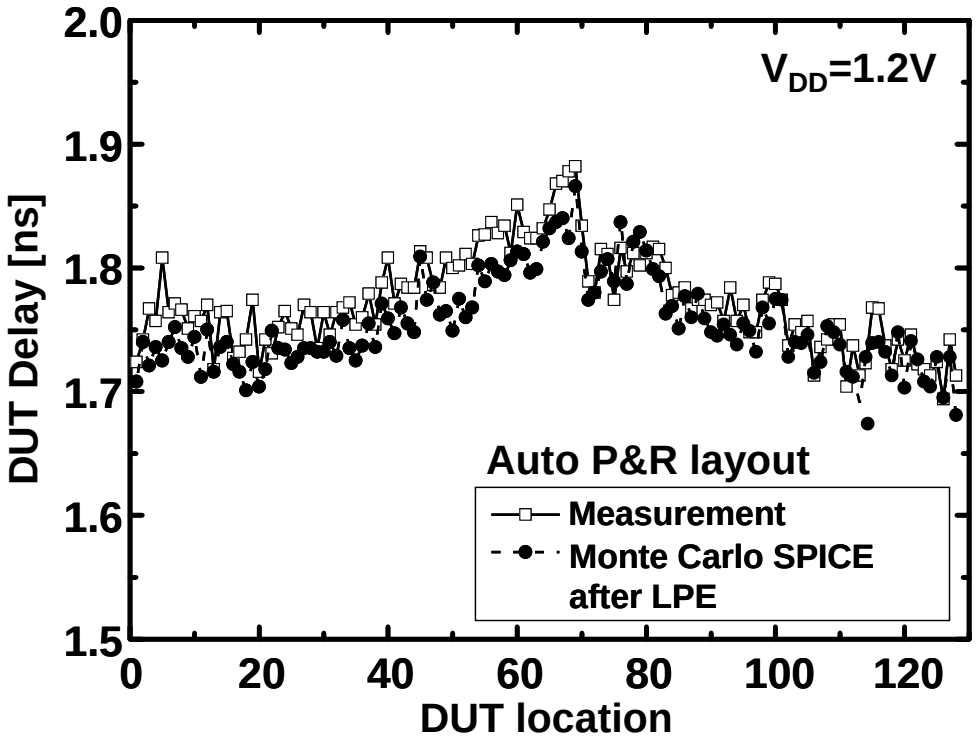


Figure 3-12. Measured and simulated spacial within-die DUT delay distributions of auto P&R layout at 1.2V

3.4. Summary

The tester friendly all digital circuits to measure the dependence of within-die delay variations on V_{DD} down to 0.4V is proposed. The logic path delay including the clock-to-Q delay and the setup delay of F/F's is easily measured by changing the clock frequency using the tester.

The V_{DD} dependence of the within-die delay variation difference between the regular manual layout and the auto place and route (P&R) layout is investigated and measured for the first time. The relative delay ($=\sigma/\mu$) variation difference between the manual layout and the P&R layout at 1.2V is large (1.56%), because the systematic delay variations due to interconnect length variations is larger than the random delay variations

due to the random transistor variations. In contrast, the difference at 0.4V is very small (0.07%), because the random delay variations increased with the reduced V_{DD} and dominate total delay variations.

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Chapter 4

Post fabrication dual power supply voltage control

4.1. Introduction

Reduction of the power supply voltage (V_{DD}) is an effective method for achieving ultra low power logic circuits since the active power and the leakage power depend on V_{DD}. Thus, many works have been carried out on the low V_{DD} operation of logic circuits [1-2]. The V_{DD} scaling is, however, limited by the minimum operating voltage (V_{DDmin}) of CMOS logic gates. V_{DDmin} is a minimum power supply voltage when the circuits operate without function errors [3-4]. The dependence of V_{DDmin} of flip-flop (F/F), NAND, and NOR gates on the number of logic gates is investigated. Figure 4-1 (a) shows a schematic diagram of a 2-input NAND chain for the V_{DDmin} measurement. The NAND chain has outputs from the 11th stage to the 10001th stage. Figure 4-1 (b) is a schematic diagram of a F/F chain. V_{DDmin} is defined as V_{DD} where the output of F/F is stopped. Figure 4-2 shows the measured dependence of V_{DDmin} of F/F, NAND, and NOR gates on the number of stages in 65nm CMOS. Measurement of V_{DDmin} is conducted with slow clock (1kHz). V_{DDmin} increases as the number of stages increases. V_{DDmin} of F/F is much higher than that of NAND and NOR gates. For example, V_{DDmin} of F/F is 378mV at 4096 stages. This result indicates that V_{DD} scaling below 400mV in large scale processors with 10M to 100M logic gates is difficult, because V_{DDmin} of 10M to 100M logic gates is above 400mV.

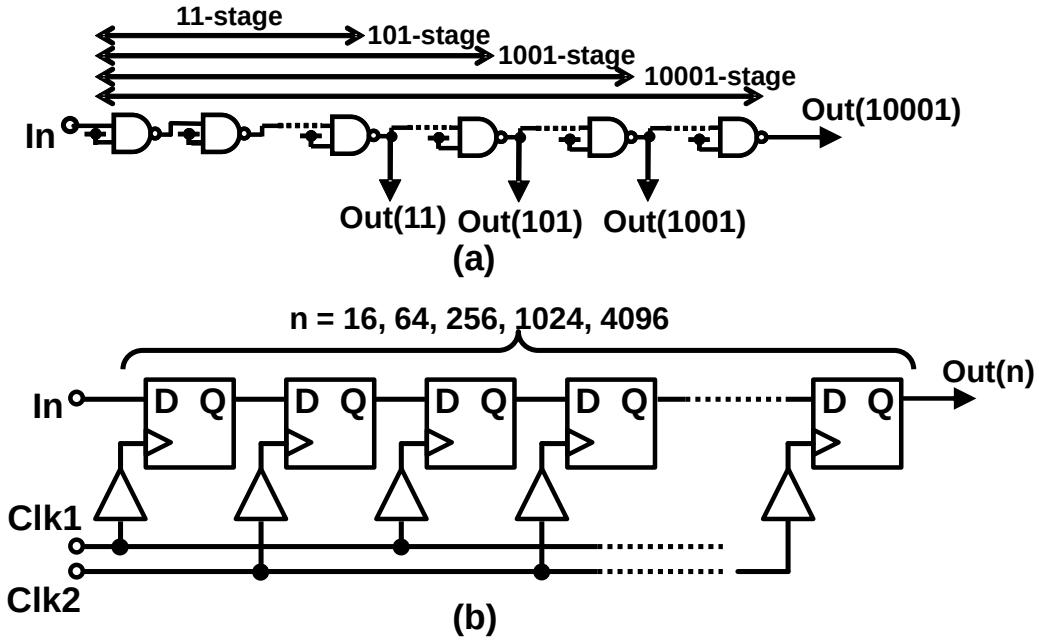


Figure 4-1. Schematic diagram of chain circuits to measure V_{DDmin} fabricated in 65nm CMOS. (a) 2-input NAND chain. (b) F/F chain.

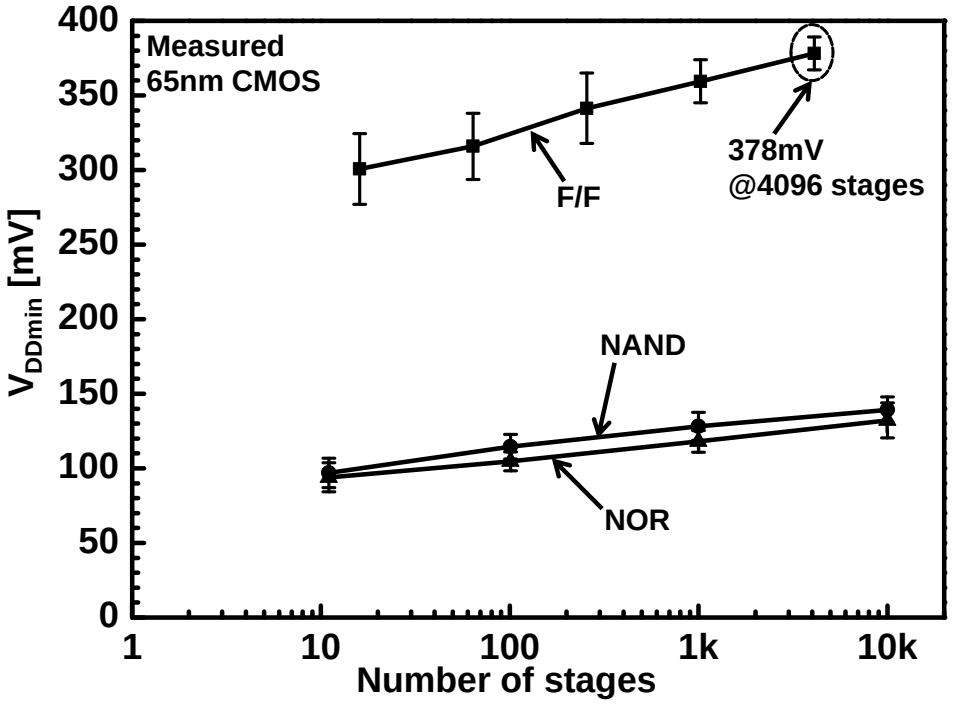


Figure 4-2. Measured dependence of V_{DDmin} on number of stages in F/F, NAND and NOR.

In order to achieve ultra low V_{DD} logic circuits, a new solution to exceed the V_{DDmin} limit is required. Reducing V_{DDmin} at a design phase, however, is difficult because V_{DDmin} is mainly determined by random variations of the threshold voltage of transistors [5]. Furthermore, only one functional error of F/F or logic gates increases V_{DDmin} of a whole logic circuit. Therefore, in order to reduce V_{DDmin}, V_{DD} must be controlled with multiple domains. The conventional fine-grained V_{DD} control at design phase [6] cannot solve the V_{DDmin} problem, because the position of the logic gate with the highest (=worst) V_{DDmin} is random. Thus, to achieve low power logic circuits with ultra low V_{DD}, a post-fabrication dual supply voltage control (PDVC) for fine-grained V_{DD} domains is proposed in this paper. PDVC reduces the power consumption of logic circuits effectively by reducing V_{DD} below V_{DDmin}.

Section 4.2 shows test circuits divided into 64 V_{DD} domains for PDVC. Area penalty of PDVC is also discussed. Section 4.3 presents experimental results. The power reduction by reducing V_{DD} below V_{DDmin} with the proposed PDVC is also discussed. Section 4.4 concludes this paper.

4.2. Proposed Post-Fabrication Dual Supply Voltage Control (PDVC)

Figure 4-3 illustrates a difference between a conventional dual V_{DD} control and PDVC. In the conventional dual V_{DD} control, V_{DD} is common within a functional block and is independently controlled in each block. In addition, level shifters are inserted between functional blocks with different V_{DD}'s. In contrast, in the proposed PDVC, the layout of the whole logic circuit is divided into many domains regardless of the functional blocks. Although the layout of PDVC has connections between

different voltage domains, level shifters are not inserted, because the leakage current between different V_{DD} domains is negligible when the difference of V_{DD1} and V_{DD2} is small. In the conventional dual V_{DD} control, V_{DD} of large functional blocks cannot be reduced, because the probability of the existence of F/F's with high V_{DDmin} within the functional block increases. On the other hand, V_{DD} is reduced below V_{DDmin} by the proposed PDVC, because V_{DD} of domains which does not include bad F/F's (namely F/F's with high V_{DDmin}) is reduced. [7] also shows a within-functional-block fine-grained adaptive dual V_{DD} control. In [7], V_{DD} is controlled by the setup error prediction signals generated by canary F/F's. The V_{DD} control in [7], however, cannot reduce average V_{DD} below V_{DDmin}, because the canary F/F's also have function errors due to its V_{DDmin}. Therefore, the proposed PDVC is required in V_{DDmin}-limited ultra low voltage logic circuits.

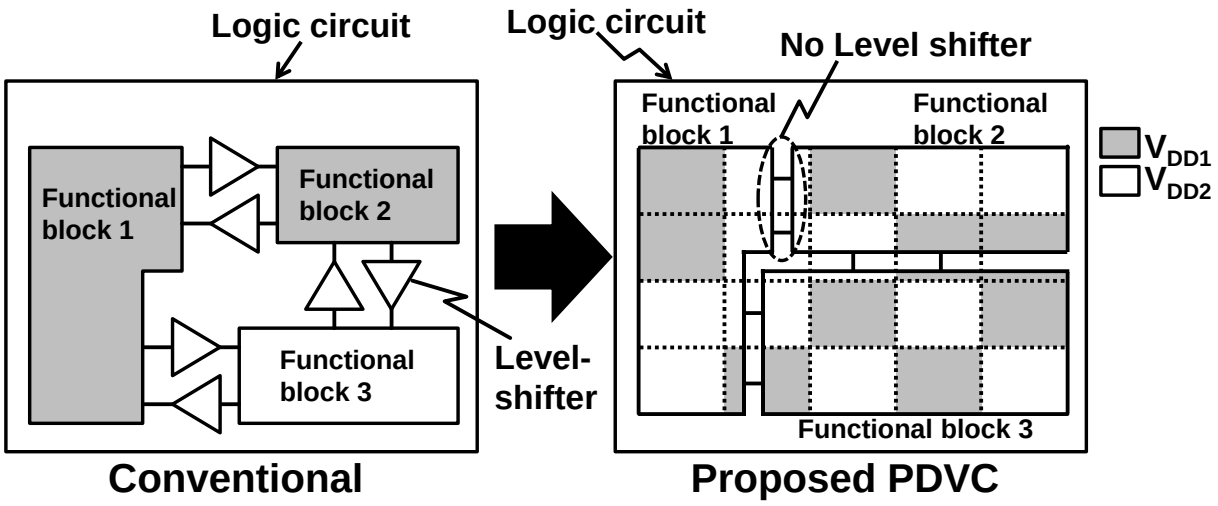
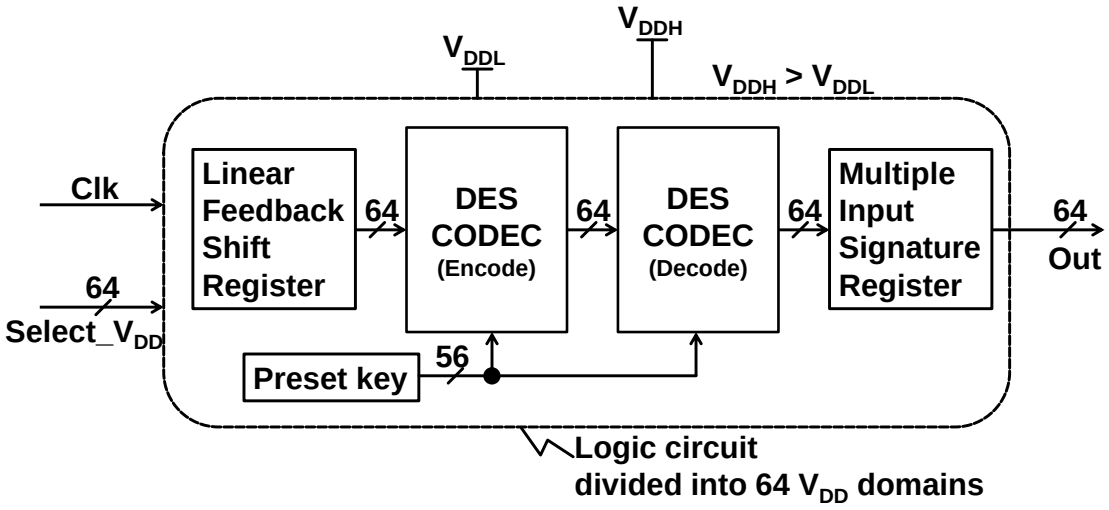


Figure 4-3. Comparison between conventional and proposed dual V_{DD} control.

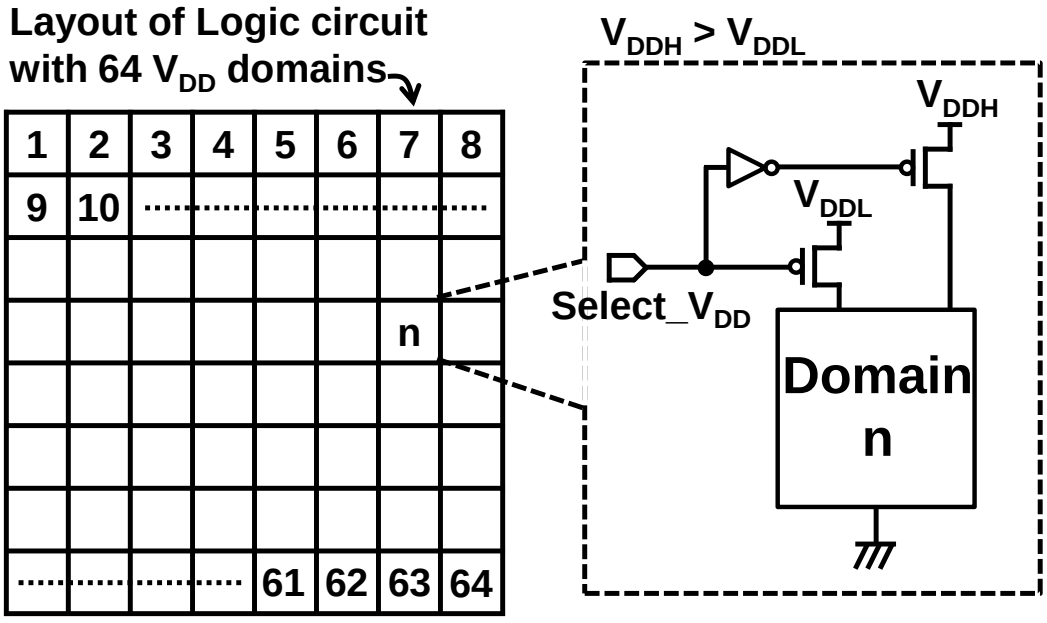
Figure 4-4 (a) shows a block diagram of the fabricated logic circuit to demonstrate the proposed PDVC. The core circuits are series-connected 64-bit data

encryption standard codec's (DES CODEC's). These DES CODEC's execute an encryption and a decryption based on the preset key. The inputs of DES CODEC's are generated by a 64-bit linear feedback shift register, and the outputs are compressed by a 64-bit multiple input signature register (MISR). The outputs of MISR are read using a scan chain and the result is compared to expectation vectors. The logic circuit in Figure 4-4 (a) is divided into 64 V_{DD} domains without relations to its function as shown in Figure 4-3. Figure 4-4 (b) shows a schematic of a layout of the logic circuit with 64 V_{DD} domains. A schematic diagram of domain *n* is also shown. The circuit is divided into 8 x 8 domains and each domain size is the same. Each domain has 2 power switches to select high V_{DD} (V_{DDH}) or low V_{DD} (V_{DDL}). The power switches are domain-by-domain controlled by Select_V_{DD} signal from a tester. Figure 4-5 shows a die micrograph and a layout of the fabricated logic circuit (DES CODEC's) in 65-nm CMOS. The layout with 64 V_{DD} domains was designed using a commercial auto P&R tool. The die size is 960μm x 1260μm. The core area of DES CODEC's with 64 V_{DD} domains is 516μm x 516μm. Each domain size is 54μm x 63.2μm including 2 power switches. The domain size is smaller than that of [7] (100μm x 100μm). The area overhead of the 2 power switches is 7%. Compared with a conventional single V_{DD} design with a power switch for the power gating, however, the area overhead due to an additional power switch in PDVC is 3.5%. The area overhead due to the separation between 64 V_{DD} domains is negligible. The fabricated logic circuit (DES CODEC's) includes 110,045 gates and 4,123 F/F's. As shown in Figure 4-2, V_{DDmin} of this circuit is determined by F/F's instead of combinational circuits and will be around 400mV, because V_{DDmin} of F/F's with

4096 stages is 378mV.



(a)



(b)

Figure 4-4 (a) Block diagram of test circuit divided into 64 V_{DD} domains. (b) Schematic of layout of logic circuit with 64 V_{DD} domains and schematic diagram of domain n.

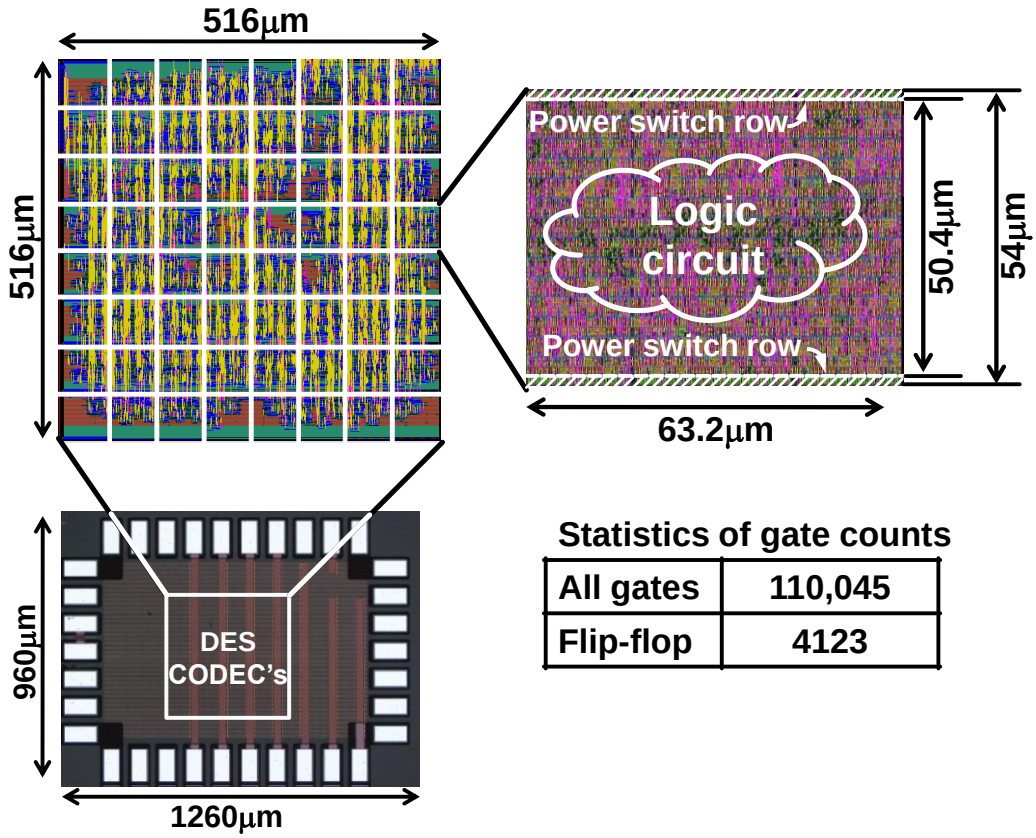


Figure 4-5. Die micrograph and and layout of the DES CODEC's fabricated in 65-nm CMOS.

4.3. Experimental Results

Figure 4-6 shows measured shmoo plot of the fabricated DES CODEC's from 0.4V to 1.2V. In this measurement, single V_{DD} is provided to all 64 domains. Maximum operating frequency of the circuit is 630MHz at 1.2V. The maximum operating frequency decreases as V_{DD} is reduced. V_{DDmin} of the DES CODEC's is 450mV, because the DES CODEC's has function errors below 400mV at any clock frequencies. In this paper, the clock frequency for the V_{DDmin} measurement is fixed to 300kHz. Table 4-1 summarizes measured V_{DDmin} of 10 dies in ascending order. Minimum and maximum V_{DDmin} in 10 dies are 399mV and 437mV, respectively.

Although V_{DDmin} varies between die to die, it is difficult to measure V_{DDmin} of all fabricated dies in terms of a test cost. The highest (=worst) V_{DDmin}, however, can be calculated [5]. Thus, V_{DDH} is fixed to V_{DDmin} of the worst die (437mV, in this case).

Table 4-1. Measured V_{DDmin} of 10 dies

Die #	V_{DDmin} [mV]
1	399
2	404
3	424
4	424
5	426
6	430
7	431
8	433
9	435
10	437

Low

High

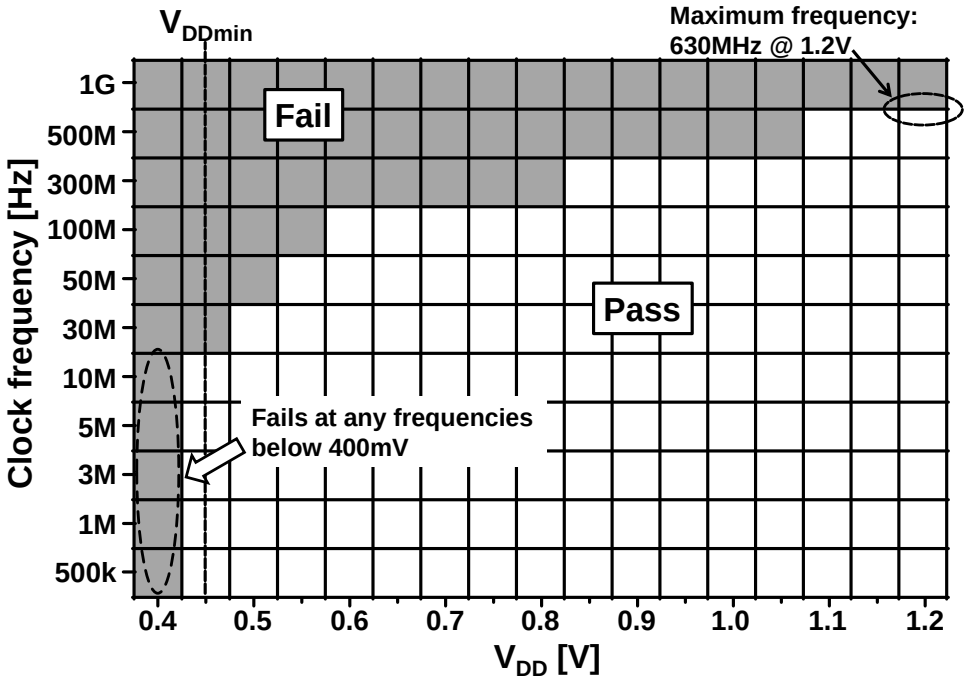


Figure 4-6. Shmoo plot of fabricated DES CODEC's.

Figure 4-7 shows a flow chart of an algorithm used for PDVC. V_{DDH} is selected in V_{DDmin}-critical domains, while V_{DDL} is selected in V_{DDmin}-non-critical domains. A post-fabrication die-to-die dual V_{DD} selection is inevitable, because the domains where V_{DDmin} is high are determined by random transistor variations and the selection of V_{DDH} or V_{DDL} in each domain is different between dies. In order to minimize the power of the DES CODEC's, the number of V_{DDL} domains should be maximized, because both the dynamic and leakage power of a domain is reduced by changing from V_{DDH} to V_{DDL}. Thus, an algorithm to efficiently find out V_{DDL} ($<V_{DDmin}$ of each die) domains is required to shorten testing time.

Explanation of the algorithm is shown in (i)-(v), where n (=100) is the maximum number of iterations, i is a current iteration count, c (<1) is a constant, w (<1) is a weighting coefficient, k is the number of domains used from a failed domain list, and a is an initial number (>1).

(i) V_{DD} of all domains are assigned to V_{DDH}. The voltage of V_{DDH} is determined by the highest (=worst) V_{DDmin} across dies. Next, the voltage of V_{DDL} is determined. Optimal V_{DDL} in this algorithm will be discussed in Figure 4-9.

(ii) Domains with V_{DDH} are selected and changed to V_{DDL} domain, and built-in test is executed. Prior V_{DDL} domains are not selected, because F/F's with high V_{DDmin} are not included in the domain.

(a) The number of domains to be selected is calculated. Only V_{DDH} domains are selected in this step (ii). The number is ac^i. When iteration count is small, larger

number of domains is selected to reduce power consumption rapidly. In contrast, when iteration count is large, 1 domain is changed to approach optimal solution.

(b) Transition probability of each domain is calculated based on a failed domain list and *w*. Latest *k* domains are selected from the failed domain list. The failed domain list saves past failed domains in the built-in self test. The past failed domains have a high possibility of including logic gates with high V_{DDmin}.

(c) Domains are randomly selected by the transition probability ratio calculated in (b). The selected V_{DDH} domains are changed to V_{DDL} domains.

(iii) Built-in self test is executed.

(iv) When the test is passed, adopt new set of V_{DD}. When the test is failed, discard changes and add failed domains to the failed domain list.

(v) Increment *i*. While $i < n$, return to (ii).

Please note that a measurement of the power consumption is not required in this algorithm. This is important because this algorithm has a potential to be embedded in the circuits.

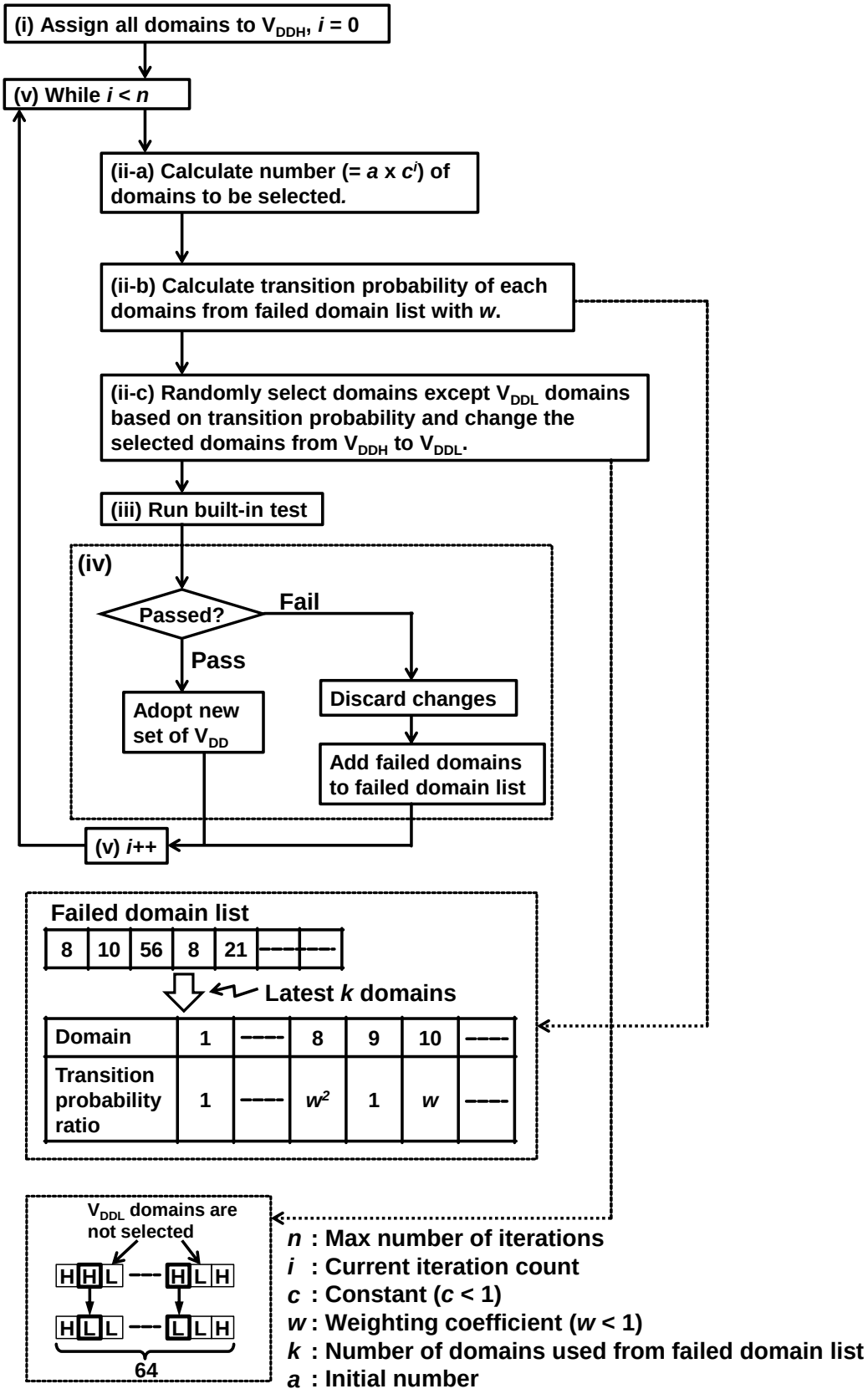


Figure 4-7. Flow chart of algorithm for PDVC.

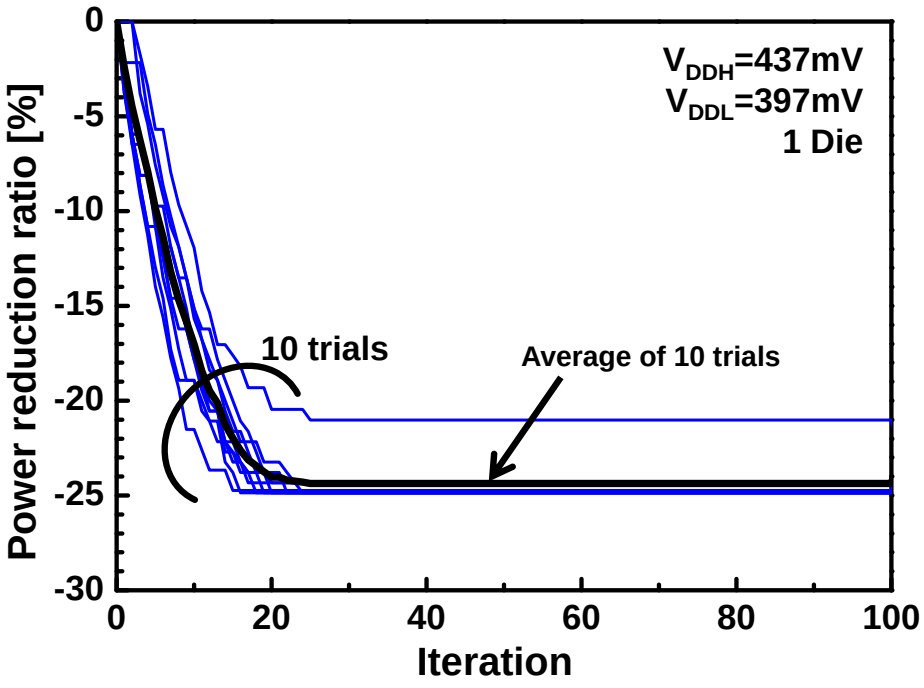
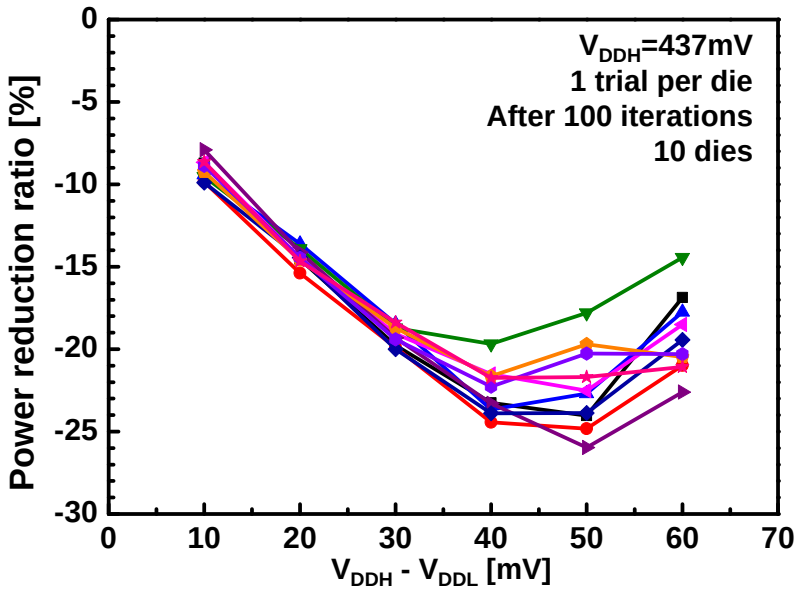


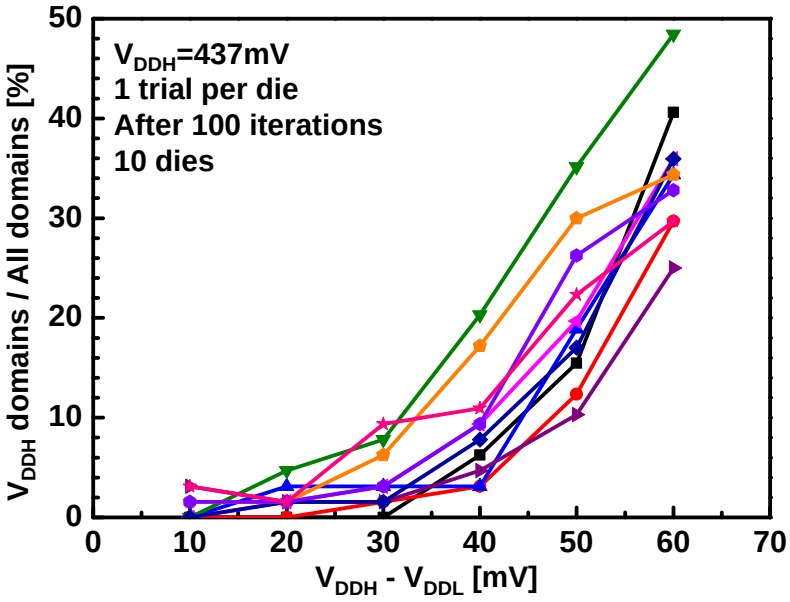
Figure 4-8. Measured dependence of power reduction ratio on iteration counts in one die.

Figure 4-8 shows the measured dependence of power reduction ratio on the number of iterations. 10 trials are executed for 1 die. These 10 lines take different routes, because the algorithm randomly selects domains. Power reduction of a chip is defined as average of 10 trials. In this case, the power reduction ratio after 100 iterations is 24%. In order to determine an optimal V_{DDL}, Figure 4-9 (a) shows the measured dependence of power reduction ratio on the voltage difference between V_{DDH} and V_{DDL} after 100 iterations in 10 dies. When V_{DDH} - V_{DDL} is 40mV or 50mV, the power reduction ratio is maximized. In this paper, V_{DDH} - V_{DDL} of 40mV is used, because the variation of the power reduction ratio at 50mV is larger than that of 40mV. Figure 4-9 (b) shows the measured dependence of the percentage of V_{DDH} domains on V_{DDH} - V_{DDL}. With increasing V_{DDH} - V_{DDL}, the percentage of V_{DDH}

domains increases, while the power consumption of V_{DDL} domains decreases. This is the reason why the power reduction ratio is maximized at V_{DDH} - V_{DDL} of 40mV or 50mV in Figure 4-9 (a).



(a)



(b)

Figure 4-9. (a) Measured dependence of power reduction ratio on $V_{DDH} - V_{DDL}$. (b) Dependence of percentage of V_{DDH} domains on V_{DDH} - V_{DDL}.

Figure 4-10 shows the measured dependence of the power reduction ratio on the number of iterations in 10 dies. Each line denotes average of 10 trials in each die. V_{DDH} is 437mV and V_{DDL} is 397mV. The power is reduced by 6.7% to 17% at 10 iterations, 14% to 24% at 30 iterations, and 20% to 24% at 100 iterations. As the number of iterations increase, the power reduction ratio also increases. When the test cost of the 100 iterations is not acceptable, the 10 iterations or the 30 iterations will be a reasonable choice.

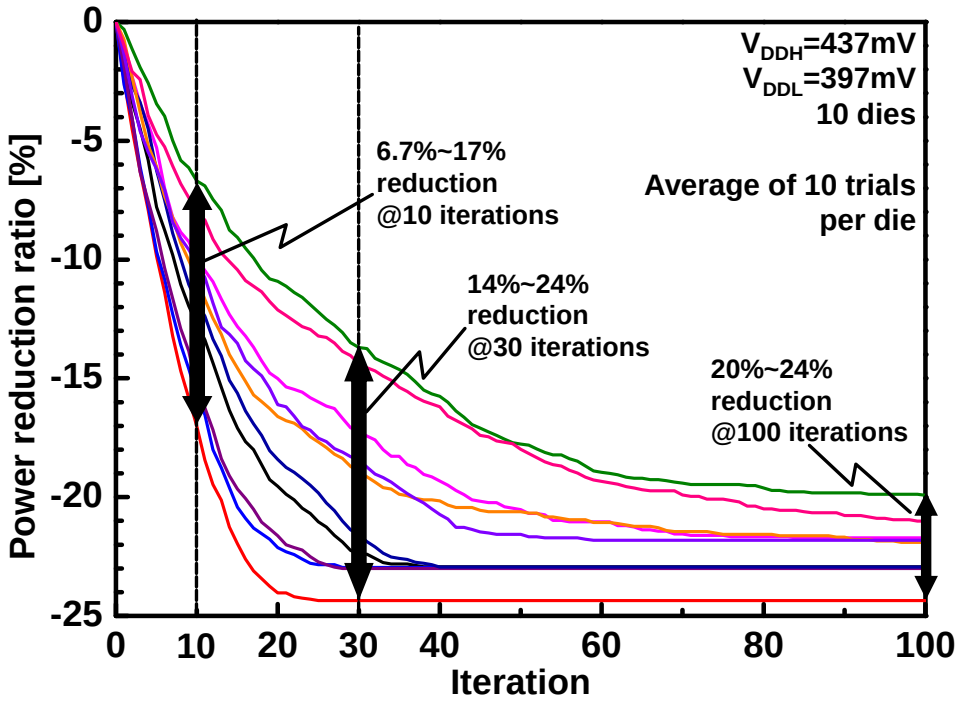


Figure 4-10. Measured dependence of average power reduction ratio on iteration counts in 10 dies.

In order to investigate the distribution of V_{DDH} and V_{DDL} in 64 V_{DD} domains and to check the stability of the convergence of the proposed algorithm in Figure 4-7, Figure 4-11 shows the measured maps of the probability of V_{DDH} in 64 V_{DD} domains for 10 dies. 10 trials are performed to measure the probability of V_{DDH} per die. In 64

V_{DD} domains of each die, the probability of V_{DDH} is nearly 0% or 100%, which indicates that the proposed algorithm is stable. The maps for 10 dies have no strong correlations. In order to check the random and systematic components in the distribution of V_{DDH} and V_{DDL} in 64 V_{DD} domains, Figure 4-12 shows the average of 10 maps in Figure 4-11. The probability of V_{DDH} across 10 dies is less than 40%, which indicates that the position of F/F's with high V_{DDmin} is almost random and the die-to-die PDVC is required to achieve the low power logic circuits with ultra low V_{DD}.

Table 4-2 summarizes the key features of the fabricated DES CODEC's. Power reduction up to 24% is achieved by the proposed PDVC.

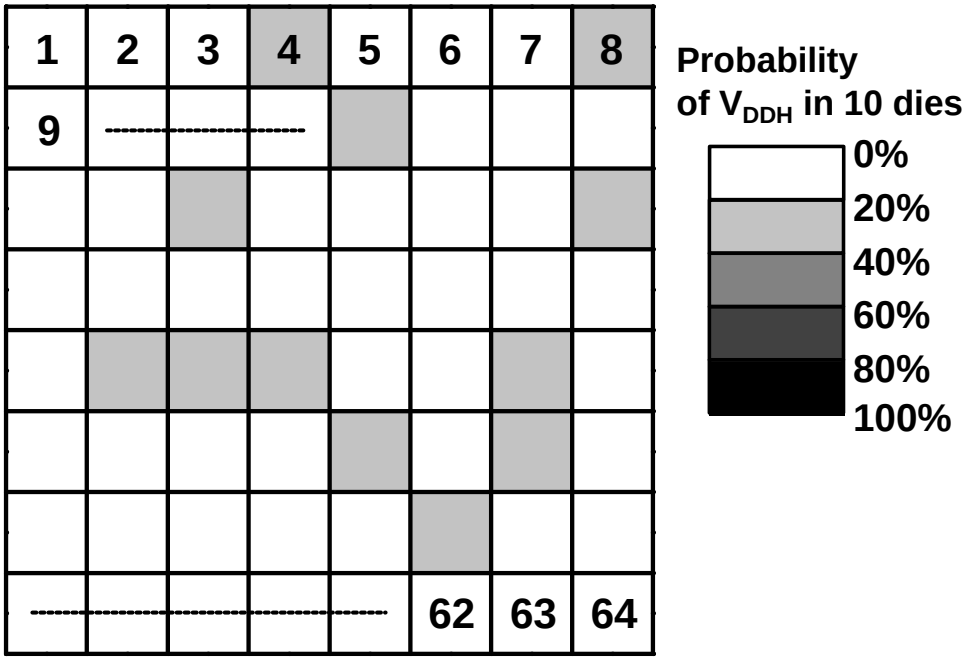


Figure 4-11. Averaged probability map of V_{DDH} in 10 dies

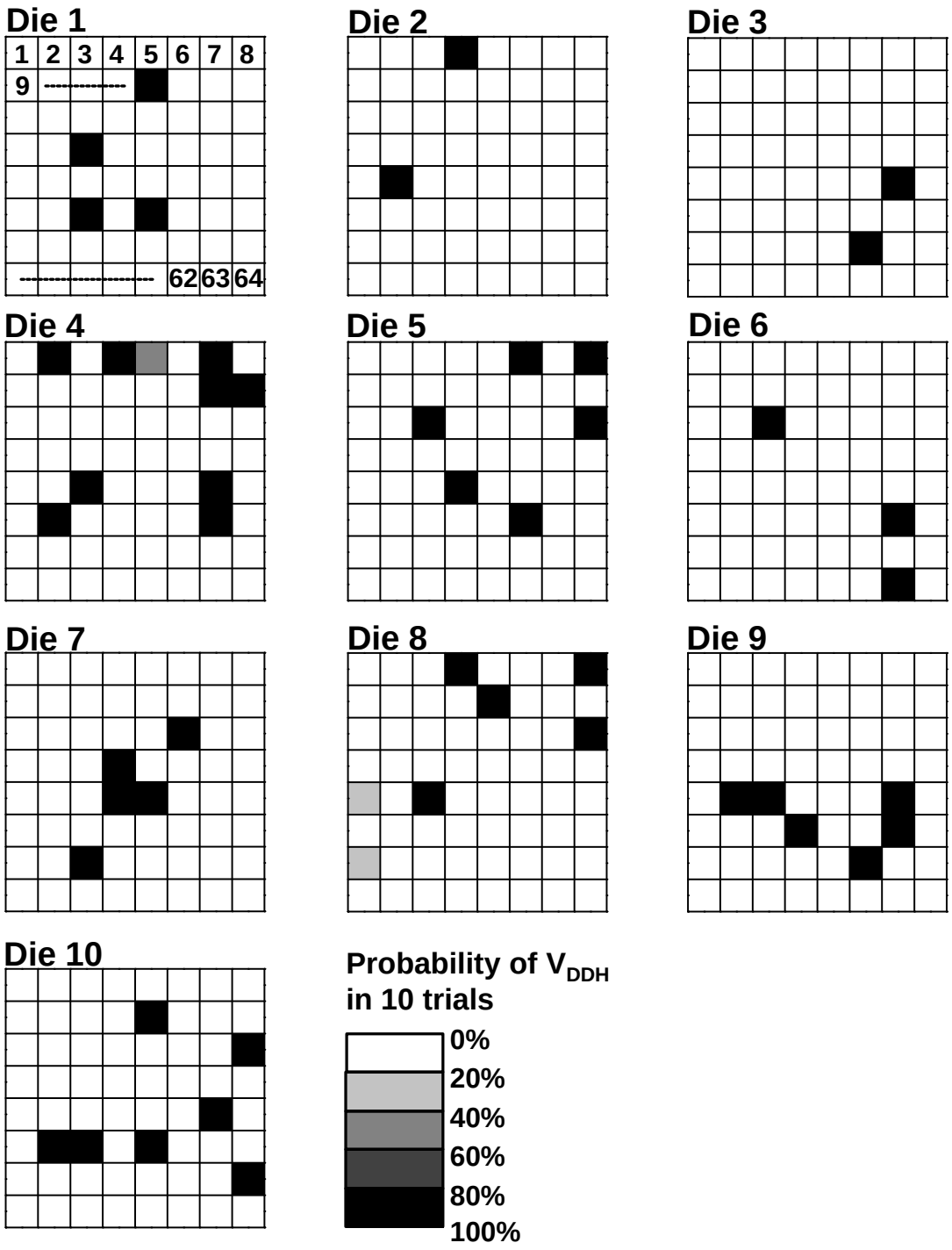


Figure 4-12. Probability map of V_{DDH} of 10 dies in 10 trials

Table 4-2. Summary of key features.

Technology	**65nm CMOS**
Clock frequency for V_{DDmin}	**300kHz**
Core area	**516μm x 516μm**
Average power	
Before PDVC	**18.4μW**
After PDVC	**14.3μW**
Power reduction by PDVC	**6.7% ~ 17%@10 iterations**
	14% ~ 24% @30 iterations
	20% ~ 24% @100 iterations

4.4. Summary

A post-fabrication dual supply voltage control (PDVC) of multiple voltage domains is proposed for a V_{DDmin}-limited ultra low voltage logic circuits. PDVC effectively reduces an average V_{DD} below V_{DDmin}, thereby reducing the power consumption of logic circuits. PDVC is applied to the DES CODEC's circuit fabricated in 65nm CMOS. The layout of the DES CODEC's is divided into 64 V_{DD} domains and each domain size is 54μm x 63.2μm. The area penalty of PDVC is 3.5%. A maximum 24% power reduction at 30 iterations was measured with the proposed PDVC at 300kHz, V_{DDH} =437mV, and V_{DDL}=397mV.

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Chapter 5
Conclusion

This thesis investigates the effect of transistor variations on the operation of logic circuits under low power supply voltage, and proposes countermeasures to achieve sub-0.5V, extremely low power logic circuits.

In chapter 2, determinant factors and reduction of V_{DDmin} of CMOS logic gates are investigated and a design guide to reduce V_{DDmin} is shown by measurements and SPICE simulations of logic-gate chains in 65nm CMOS. V_{DDmin} consists of $V_{DDmin(SYS)}$ and $V_{DDmin(RAND)}$. $V_{DDmin(RAND)}$ depends on the random V_{TH} variation and the number of stages of logic gates, while $V_{DDmin(SYS)}$ is determined by the balance of nMOS and pMOS and is minimized when the logic threshold voltage is equal to half V_{DD}. Therefore, $V_{DDmin(RAND)}$ is reduced by increasing W_N and W_P, while $V_{DDmin(SYS)}$ is minimized by optimizing W_P/W_N at a design stage. The body-biasing is effective to compensate for the increase of $V_{DDmin(SYS)}$ due to the die-to-die V_{TH} variation. The optimal body-biasing minimizes $V_{DDmin(SYS)}$ and the forward body biasing decreases $V_{DDmin(RAND)}$. In the measurement of V_{DDmin} of 100k-stage 2NAND chain, V_{DDmin} is successfully reduced by 45mV from 193mV to 148mV by the forward body biasing. The temperature dependence of V_{DDmin} is measured for the first time. The worst (=highest) V_{DDmin} condition of logic circuits with small gate counts is high temperature, while the worst V_{DDmin} condition of logic circuits with large gate counts is low temperature. Therefore, the temperature for the worst corner analysis for V_{DDmin} should be changed depending on the number of gate counts of logic circuits. Reducing V_{DDmin} for general logic circuits

constraining the total gate width per logic gate constant is also discussed. Although optimization of each gate reduces $V_{DDmin(SYS)}$, $V_{DDmin(RAND)}$ increases because of unbalanced pair of gate width of nMOS and pMOS. Thus, the best way to reduce V_{DDmin} of large scale logic circuits is to optimize the gate width of inverter and apply it to other gates. $V_{DDmin(SYS)}$ of F/F is reduced from 170mV to 100mV by tuning logic threshold voltage of each gate to half V_{DD}. $V_{DDmin(RAND)}$ of F/F's is reduced from 64mV to 56mV by upsizing gate width of latch. V_{DDmin} of 1k-stage F/F chain could be reduced by 95mV and 125mV for optimized F/F and optimized F/F with upsized latch respectively.

In chapter 3, the tester friendly all digital circuits to measure the dependence of within-die delay variations on V_{DD} down to 0.4V is proposed. The logic path delay including the clock-to-Q delay and the setup delay of F/F's is easily measured by changing the clock frequency using the tester. The V_{DD} dependence of the within-die delay variation difference between the regular manual layout and the auto place and route (P&R) layout is investigated and measured for the first time. The relative delay ($=\sigma/\mu$) variation difference between the manual layout and the P&R layout at 1.2V is large (1.56%), because the systematic delay variations due to interconnect length variations is larger than the random delay variations due to the random transistor variations. In contrast, the difference at 0.4V is very small (0.07%), because the random delay variations increased with the reduced V_{DD} and dominate total delay variations.

In Chapter 4, A post-fabrication dual supply voltage control (PDVC) of multiple voltage domains is proposed for a V_{DDmin}-limited ultra low voltage logic circuits. PDVC effectively reduces an average V_{DD} below V_{DDmin}, thereby reducing the power

consumption of logic circuits. PDVC is applied to the DES CODEC's circuit fabricated in 65nm CMOS. The layout of the DES CODEC's is divided into 64 V_{DD} domains and each domain size is 54μm x 63.2μm. The area penalty of PDVC is 3.5%. A maximum 24% power reduction at 30 iterations was measured with the proposed PDVC at 300kHz, V_{DDH} =437mV, and V_{DDL}=397mV.

The results of the thesis, which includes investigation on and countermeasures against V_{DDmin} and delay variation, is useful to realize sub-0.5V extremely low power logic circuits for future LSI's applications.

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