Master's thesis

1×N Nyquist-sampling optical phased-array silicon switches with improved extinction ratio

消光比改善に向けた１×Ｎナイキストサンプル光フェーズアレイシリコンスイッチ

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Contents

Chapter 1

Background and Motivation

1.1 Increasing Data Traffic

During the past few years, the amount of information data traffic has increased drastically. Annual global IP traffic will surpass the zettabyte (1000 exabytes) threshold in 2016. Global IP traffic will reach 1.1 zettabytes per year or 91.3 exabytes (one billion gigabytes) per month in 2016. By 2018, global IP traffic will reach 1.6 zettabytes per year, or 131.6 exabytes per month. Global IP traffic has increased more than fivefold in the past 5 years, and will increase threefold over the next 5 years. Overall, IP traffic will grow at a compound annual growth rate (CAGR) of 21 percent from 2013 to 2018. Even crucially, busy-hour Internet traffic is growing more rapidly than average Internet traffic. Busy-hour (or the busiest 60-minute period in a day) Internet traffic increased 32 percent in 2013, compared with 25 percent growth in average traffic. Busy-hour Internet traffic will increase by a factor of 3.4 between 2013 and 2018, while average Internet traffic will increase 2.8-fold. Busy-hour Internet traffic will reach 1.0 petabits per second (Pbps) by 2018, the equivalent of 335 million people streaming a high-definition (HD) video continuously [1].

As figure 1.1 shows, the overall total IP traffic of the global network is expected to grow up to 132 exabytes per month by 2018, up from 51 exabytes per month in 2013, a CAGR of 21 percent. Total Internet traffic has experienced dramatic growth the past two decades. More than twenty years ago, in 1992, global Internet networks carried approximately 100 GB of traffic per day. Ten years later, in 2002, global Internet traffic amounted to 100 gigabytes per second (GBps). In 2012, global Internet traffic reached 12,000 GBps. Table 1 provides a view of the historical benchmarks for total Internet traffic.

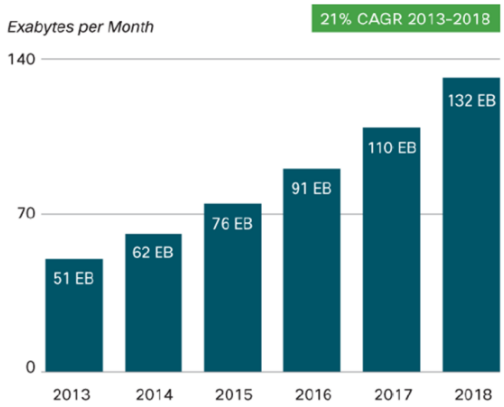


Figure 1.1 Cisco VNI forecasts 132 Exabytes per month

Per capita IP and Internet traffic growth has followed a similarly steep growth curve over the past decade. Globally, IP traffic will reach 17 GB per capita by 2018, up from 7 GB per capita in 2013, and Internet traffic will reach 14 GB per capita by 2018, up from 5 GB per capita in 2013. Not long ago, in 2008, per capita Internet traffic was 1 GB per month. In 2000, per capita Internet traffic was 10 megabytes (MB) per month. The high speed increasing IP traffic and its high power consumption has been a critical issue to be solved in the 21st century [2].

Year	Global Internet Traffic
1992	100 GB per Day
1997	100 GB per Hour
2002	100 GBps
2007	2000 GBps
2013	28,875 GBps
2018	50,000 GBps

Source: Cisco VNI, 2014

Table 1

1.2 Datacenter Network

1.2.1 Datacenter in Cloud Computing

Cloud computing has recently emerged as a new paradigm for hosting and delivering services over the Internet. Today's cloud computing architecture can be divided into 4 layers: the hardware/datacenter layer, the infrastructure layer, the

platform layer and the application layer, as shown in Figure 1.2.1. We could see that the hardware layer is responsible for managing the physical resources of the cloud, including physical servers, routers, switches, power and cooling systems. In practice, the hardware layer is typically implemented in data centers. A data center usually contains thousands of servers that are organized in racks and interconnected through switches, routers or other fabrics. Typical issues at hardware layer include hardware configuration, fault tolerance, traffic management, power and cooling resource management [3]. Data center, which is home to the computation power and storage, is central to cloud computing and contains thousands of devices like servers, switches and routers. Proper planning of this network architecture is critical, as it will heavily influence applications performance and throughput in such a distributed computing environment. Further, scalability and resiliency features need to be carefully considered. It plays an important role in today's Internet communication system, which combines local computers to upper side Internet servers. However, high power cost is the largest recurring problem, especially when it was entering the ZB era of the data traffic in datacenters, the power consumption of the global datacenters has already reached more than 330 billion kWh in 2007 [4]. If we assume that each byte of traffic is traversing over the Internet, 10^6 bytes (1MB) of data communications are being generated within one, or more datacenters [5].

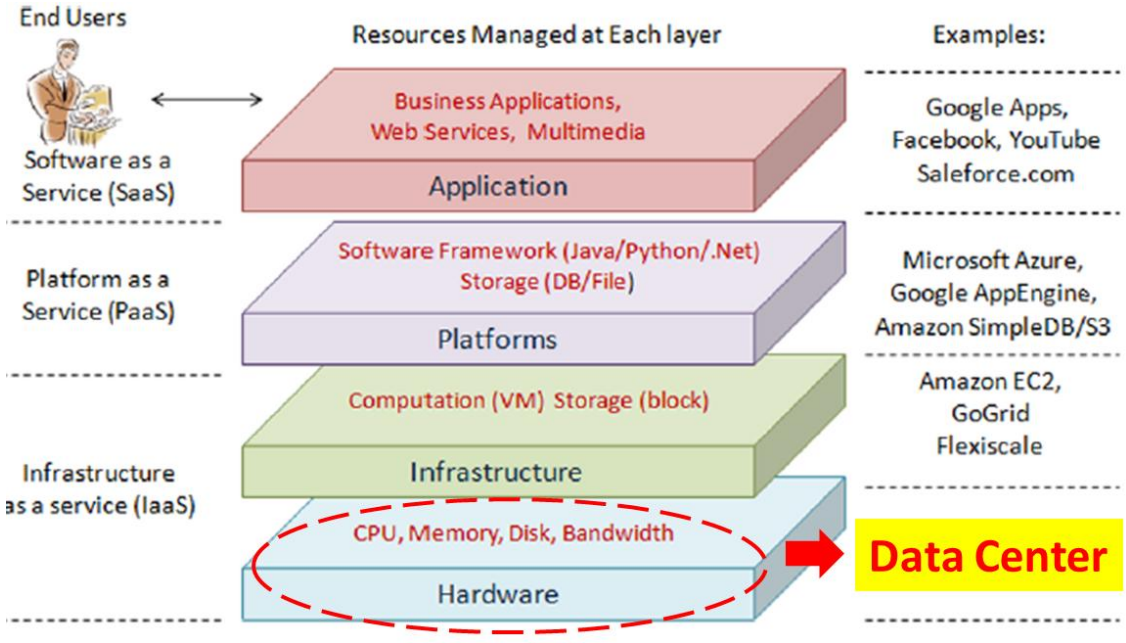


Figure 1.2.1

1.2.2 Conventional Datacenter

In the datacenter, an aggregated switch is first connected to the access switch, and then arrange into each racks to the servers as shown in Figure 1.2.2. Notice that a large-scale datacenter is consist of either one or several rooms, such kind of connection requires significant numbers of links. Within the given power budget and bandwidth limitation, it is hard to combine all the nodes with cables due to the high power consumption. Thus, new technique is required for breakthrough this barrier [6].

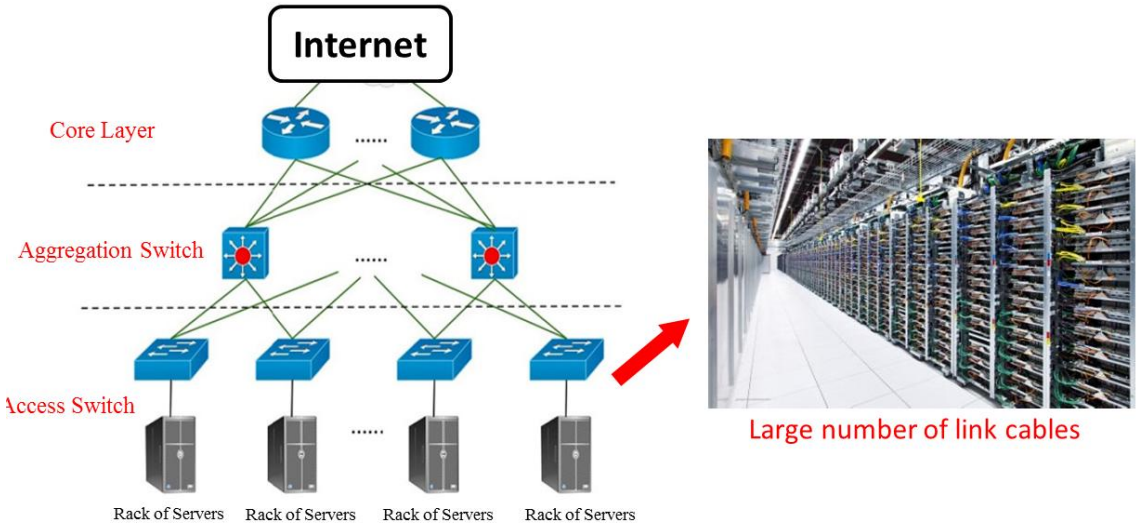


Figure 1.2.2 datacenter network infrastructure

Moreover, figure 1.2.3 shows typical electronic switches used in the datacenter. The traditional electronic switch, which controls the signal path, is facing crucial challenges in terms of power consumption and latency for the intra-datacenter network. Most of the cross-connects that are currently used in networks use an electrical core for switching where the optical signals are first converted to electrical signals, which are then switched by electrical means and finally converted back to optical signals. This type of switching is referred to as O/E/O switching. This approach features a number of disadvantages. First, the switching speed of electronics cannot keep up with the capacity of optics. Electronic asynchronous transfer mode (ATM) switches and Internet protocol (IP) routers can be used to switch data using the individual channels within a WDM link, but this approach implies that tens or hundreds of switch interfaces must be used to terminate a single link with a large number of channels. Second, O/E/O switching is neither data-rate nor data-format transparent. When the data rate increases, the expensive transceivers and electrical switch core have to be replaced. Such O/E/O

conversion in multiple switching nodes, which is not necessary for the transmission itself, leads to additional power consumption and latency on current datacenters. Since the O/E and E/O conversion at both sides of electrical switch, it also requires the multiplexer and demultiplexer (MUX/DEMUX) circuits at input and output nodes respectively which are used for adjust the level of bit rates from the range in transport system to the range in the electronic switch and backwards.

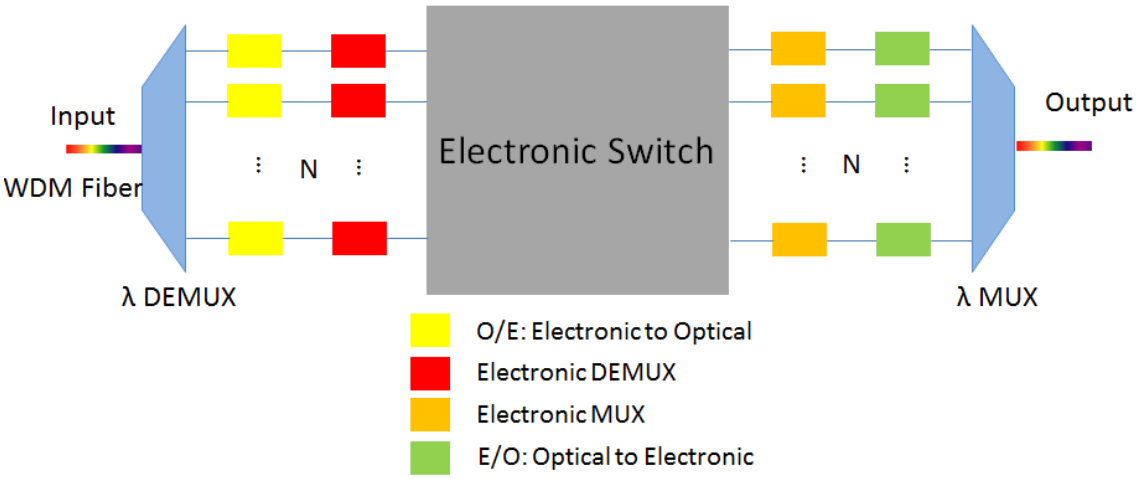


Figure 1.2.3 Electronic Switch

1.3 Optical Switching Network

1.3.1 Scheme of Optical Switch

All-optical switching technology was proposed recent year to solve the potential power consumption problem. Instead of electrical interconnection, optical cables can carry large amounts of information over the distance between servers with much smaller cable size and higher density of connections due to the time division multiplexing (TDM) and wavelength division multiplexing (WDM). Optical switching network can provide ultra-high bandwidth at short reconfiguration time for various types of transmission. Figure1.3.1 shows the scheme of optical switch, the all-optical switching technology provides optical bypass interconnection at every switch nodes, whereas the optical path experiences multiple O/E/O conversions in electronic switches as discussed before. Consequently, the all-optical switching configuration is expected as a potential technology to significantly reduce the overall power consumption of the datacenter networks by over 75% [7]. From the benefit of using all-optical approaches in optical switching without electronic switches, there have been proposed several datacenter

network architectures. Optical switching has provided a viable path toward the realization of photonic networks, as it has shown possibility on lowering the latency, reducing the power consumption and increasing the bandwidth.

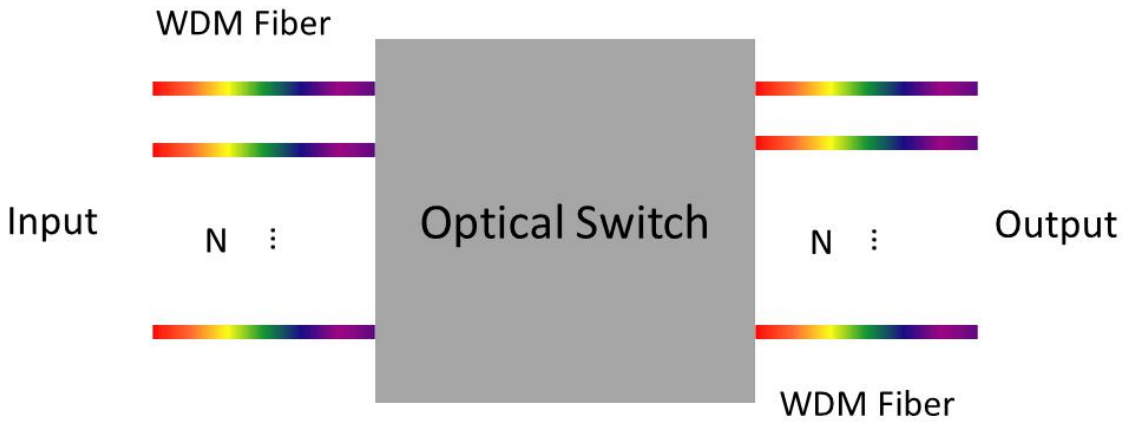


Figure 1.3.1 Scheme of Optical Switch

1.3.2 Required Properties of Optical Switch

There are several characteristics to evaluate the performance of the optical switch, such as switching speed, extinction ratio, insertion loss, cross talk and polarization-dependent loss. The definitions of these characteristics are given below [8].

Switching speed:

Switching speed is one of the most important parameters, which is defined as the time it takes for the switching reconfiguration from one state to the other (off to on or on to off). This reconfiguration time cannot be avoided and should be as short as possible. With the transmitted packet size over kilobytes, even close to 1 Tb/s in the future, the switching time had better to be in the order of a few nanoseconds.

Extinction ratio (ON-OFF switches):

It is the ratio of the output optical power in the on-state to the power in the off-state. It (r_e) could be given by

$$r_e = \frac{P_{on}}{P_{off}}$$

where the P_{on} is the power level in the on state, and P_{off} is the power level in the off-state. Since crosstalk causes penalty at each switching stage, lower extinction ratio may limit

the number of switching hops. The extinction ratio should be as large as possible

.

Insertion loss:

Insertion loss is the power loss because of the presence of the switch. This loss is an undesirable feature as the dynamic range of the signals in the network will be increased by it. Minimization the insertion loss for switches with large number of ports is difficult, but it should be as small as possible since power consumption of the device is strongly dependent on it.

Polarization dependent loss (PDL):

PDL is the deviation in losses between two states of polarization. Low PDL is required for real application of optical switches. As polarization-dependent devices need to be adjusted by polarization controlling components, which are difficult to be integrated with other devices. On the other side, low PDL is quite necessary when using in the high-bit-rate optical networking systems which employing the polarization division multiplexing (PDM) to double the spectral efficiency.

Other parameters also need to be taken into account including reliability, power consumption, scalability, temperature resistance. By optimization the design and structure of the device, it is possible to improve the performance of the optical switch, but some pay-off should be considered at the same time.

1.4 Present state of Si Optical Switch

Several kinds of optical switch have been proposed in recent years. However, each of them has some disadvantages on performance which limits the further real application. Here two kinds of silicon optical switch are shown and discussed.

1.4.1 Thermo-Optical 8×8 split-and-select optical switch

Fig. 1.4.1 shows the configuration and the fabricated chip photograph of an 8×8 split-and-select type optical switch, where eight 1×8 splitters and eight 1×8 selectors are connected in a full mesh manner. Optical circuit including 152 TO-MZ switch elements was formed within a chip size of 12mm×16mm. Thermo-optical (TO) switch elements are used for integrated optical circuits for optical path switches. Fig 1.4.1 inset shows a schematic of TO switch elements based on Mach-Zehnder (MZ) structure using silicon

optical waveguides. Rib waveguides with a silicon thickness of 1.5um are used. On one arm of the MZ structure, there is a TO phase shifter, where a refractive index is changed by applying a current to a heater placed. By using this heater current as a path selection signal, an optical path in the TO-MZ switch element is switched between the bar and the cross port. Curves of TE and TM polarization light transmission show little difference. Polarization independent switching with an extinction ratio of about 25dB is obtained. The turn-on heating power is 38mW and response time within 15us. Devices based on silicon rib waveguides were fabricated on an 8-inch SOI wafer with a silicon thickness of 1.5um with 248-nm lithography. The role of the 1×8 selector is to set up one light path while blocking the other 7 paths with high extinction ratio. The gate part is composed of 1×1 switch elements, which are turned off in the absence of current. The selector part is composed of 2×1 switch elements in which the path to the bar port is blocked in the absence of current. This scheme of blocking light paths by cascaded switch elements without applying the heater current is quite useful for high extinction ratio independently of ambient temperature.

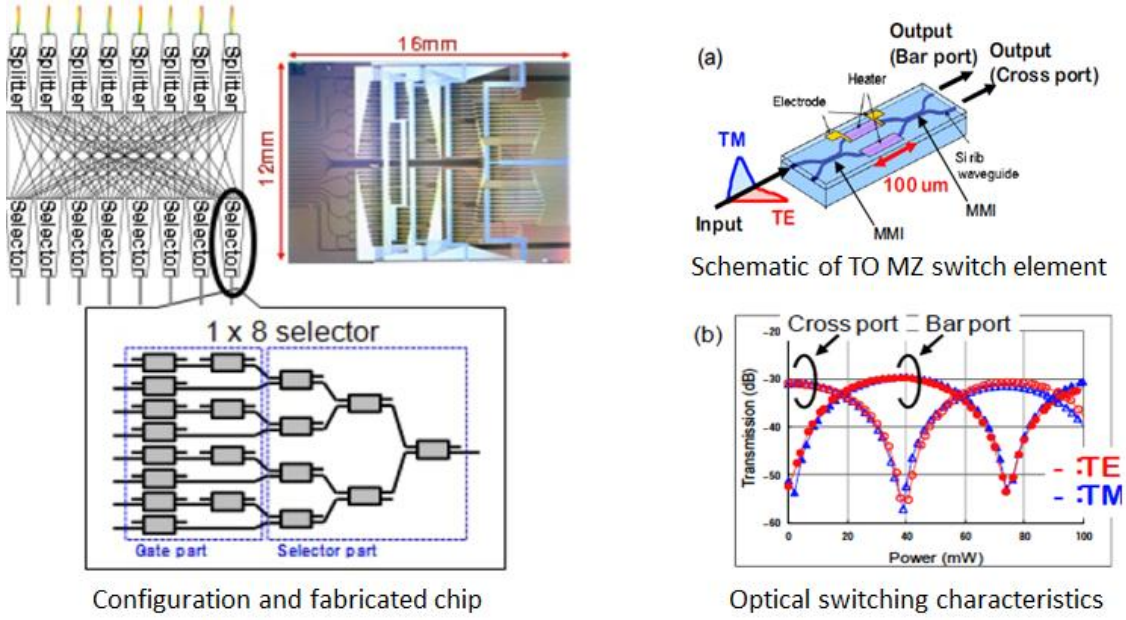


Figure 1.4.1

Figure 1.4.2(a) shows the measured transmission spectra representing the turn-on and turn-off states of each path in the 8×8 switch. Polarization independent switching with a high extinction ratio over 40dB in a wide wavelength range over 50nm has been confirmed. Temperature dependence of the switching characteristics is also evaluated. As shown in Fig 1.4.2 (b), transmission spectra at different temperatures in the range

from 0℃ to 75℃ and confirmed no degradation in the extinction ratio within this temperature ranges [9].

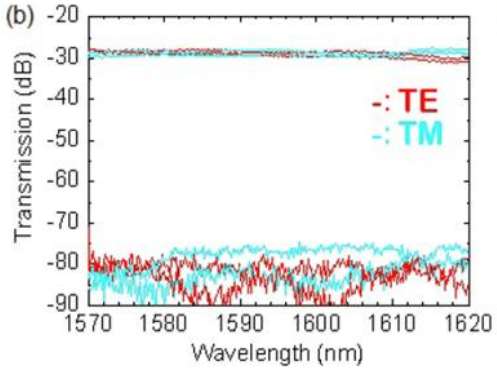


Figure 1.4.2 (a)

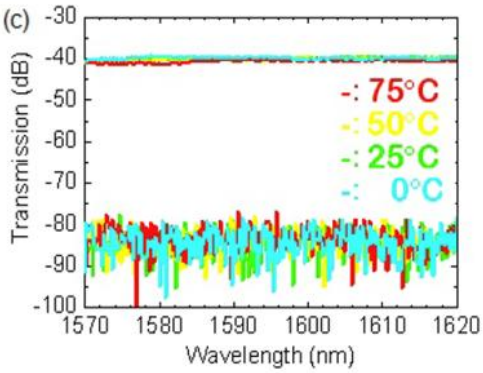


Figure 1.4.2(b)

This TO 8×8 split-and-select optical switch performs as wavelength independence with high extinction ratio and temperature stability. However, the basic structure of the device determines limitation with large number of output ports.

1.4.2 1×8 silicon photonic switch based on optical phased array

The layout of the 1×8 optical phased-array silicon switch is designed based on the previous studies on phased-array technology. The waveguide width is designed to be 600 nm at the thermo-optic phase-shifters and 500 nm elsewhere. 14 phase shifters are employed and selected the length of the star couplers to be 36 μm to minimize the optical loss while achieving sufficient extinction ratio. The heater length in each thermo-optic phase shifter is set to 400 μm. From 2D cross-sectional thermal simulation, we calculate the heat distribution around the phase shifter, and decide the spacing between two neighboring arrays to be 30μm. To further suppress thermal crosstalk, we introduce heat-insulating grooves with the width of 10 μm and the depth of 1μm between the heaters. Fig. 1.4.3 shows the photograph of the fabricated 1 × 8 silicon optical switch and dynamic switching characteristics.

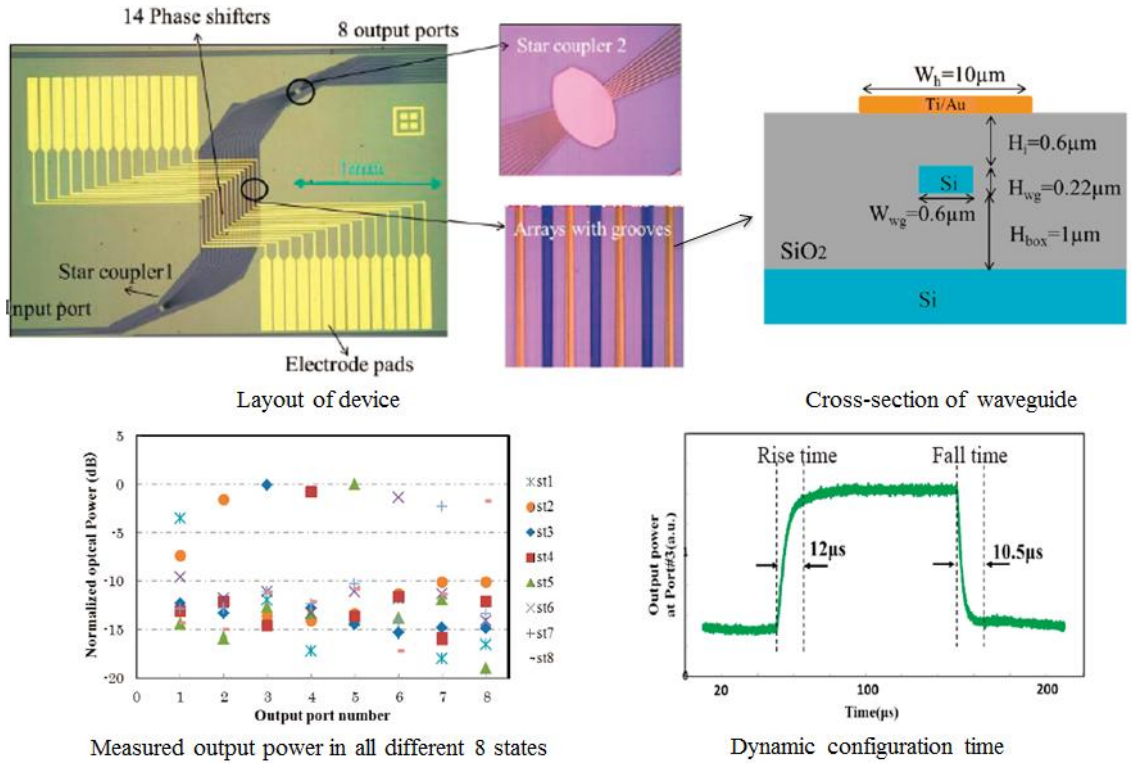


Figure 1.4.3

The footprint of the entire optical switch, including all the electrode pads, is 1.9 mm × 2.8 mm. The extinction ratio at the port #2, #3, #4, #5 is over 10 dB. The fiber-to-fiber loss ranges from 43.2 dB to 46.8 dB. The propagation loss of the silicon waveguide is measured to be 0.8dB/mm. The average total power consumed in all 14 phase shifters is 155mW.The configuration time: rise time and the fall time (between 10% and 90%) are 12.0 μs and 10.5 μs, respectively [10].

Although the switching behavior has been confirmed, with limited ratio between the numbers of array to number of output ports, the extinction ratio is insufficient practical applications.

1.4.3 Ultra-compact 8×8 strictly-non-blocking Si-wire PILOSS switch

A waveguide-based integrated $N \times N$ optical switch can be formed by using a certain number of 2 × 2 element switches. Each of the element switches in an $N \times N$

switch is set to either OFF or ON state by changing the applied electric power. Proper design can make the element switch 'normally' OFF (the switch with no electric power applied is in OFF state). Therefore, the total power consumption of an $N \times N$ switch is determined by the number of the element switches in ON state. One standard $N \times N$ switch topology is called a path-independent insertion-loss (PILOSS) topology in which the switch consists of the matrix of 2 × 2 element switches. In the PILOSS topology, light always passes through N element switches and $N-1$ intersections, thus experiences the equal attenuation for all the N^2 ways of paths. The number of ON state element switches is N in the PILOSS topology.

The 8 × 8 PILOSS switch chip was fabricated by using *e*-beam lithography and CMOS compatible process. Figure 1.4.4(a) is a microscope image of the fabricated PILOSS switch chip including 64 Mach-Zehnder (MZ) switches and 49 intersections. The Si-wire waveguide is 430-nm wide and 220-nm high, buried by SiO2 cladding. The 3-dB splitter/combiner of the MZ switch is a directional coupler (DC), which is designed for the transverse-magnetic (TM) mode that provides a larger fabrication tolerance than the transverse-electric mode case. Each arm of the MZ switch has a thermo-optic phase-shifter with a TiN heater. The footprint of the PILOSS switch is 3.5 × 2.4 mm^2. The heaters were controlled through an external heater driver. Optical fiber arrays were butt-coupled to the waveguide chip through the spot-size converters (SSCs) fabricated at the edges of the chip. The coupling loss between the SSC and fiber was estimated to be 3.6 dB/facet from fiber-to-fiber insertion loss (10.4 dB) and propagation loss (3.2 dB/cm × 1.0cm = 3.2 dB) of a reference Si-wire waveguide on the same chip [11].

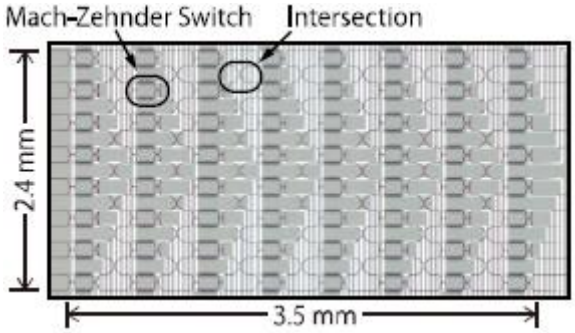


Figure 1.4.4(a): Microscope image of fabricated Si PILOSS switch chip

The on-chip loss is 6.5 ± 1.0 dB, and the crosstalk is around −23.1 dB. It also showed successful switching of the digital-coherent 43-Gbps QPSK signal. Although the wavelength and polarization dependence of the PILOSS switch are yet issues to be solved, these results demonstrate that the Si-wire based PILOSS switch can be a good

candidate for the high-port-count strictly-non-blocking matrix switch in the integrated form.

1.5 Outline of Thesis

This thesis focuses on the performance improvement of 1×N optical phased-array silicon switch, especially extinction ratio, using newly proposed Nyquist-sampling technology. The thesis begins from the demand for optical switch which has been proposed to solve the high power consumption on conventional datacenter. In chapter 2, the general information of Nyquist-sampling phased-array silicon switch is introduced, including the principle, advantages and numerical simulation result on the performance for large scalability. Chapter 3 demonstrates analytical simulation and the design of the device. The design rule for each part of the device is explained in details and optimization of each parameter is discussed. Chapter 4 shows the fabrication of the device. Process flow and conditions for each process is introduced. At last, chapter 5 presents the measurement result and discussion. The evaluation of device performance is shown with potential implementation for future improvement.

Chapter 2

Nyquist-sampling 1×N optical Phased-array Switch on Si platform

2.1 Photonic Integrated Circuits on Si platform

2.1.1 Photonic Integrated Circuits

Over the last 50 years, Moore's Law has been proved to be true that the number of components on semiconductor is increasing fast as doubled every two years. The idea of photonic integration, which was first proposed in 1969, is the technology of packing multiple photonic devices on a single chip [12]. Today, the photonic integrated circuit (PIC) technology plays a critical role in the t communication system in terms of its low cost, smaller footprint, power reduction and simplified complexity. In spite of these advantages and the quite long history of the idea, the level of progress in photonic integration has been much slower than electronic integration, which has been limited within few hundreds devices on a chip. It is believed that PIC technology is a promising solution for the next generation high-capacity required communication market.

2.1.2 Advantages of Optical Switch on Silicon platform

Optical devices on PICs are usually integrated in a planar platform with optical waveguides connected. PICs are sometimes referred as planar lightwave circuits (PLC) which have been fabricated with a variety of material systems, including silica on silicon (Si) [13], Lithium Niobate ($LiNbO_3$) [14], Silicon on Insulator (SOI) [15], and III-V component semiconductors [16]. The comparison among different materials and the reason why silicon platform is promising for the further application is shown below.

III-V component semiconductor

III-V component semiconductor is one of the best materials for light sources. It provides the integration for most of the optical functions required in the 1310nm and 1550nm telecom wavelength windows. It also performs good properties on integration technology that passive functional devices such as AWG, VOA and switches could be integrated with active functional devices on one InP chip. Moreover, multiple quantum well (MQW), defined as growing hetero-structures of compound semiconductors, has improved the performance of laser, amplifiers and electro-absorption devices which utilize the quantum confined stark effect (QCSE) [17]. Even though InP is advanced on integration technology, it has larger propagation loss than Silicon-based waveguides. Commercial PIC has several advantages such as reduction of the number of components coupling and packaging steps, which leads to better reliability, lower power consumption and smaller footprint. However, the maximum InP substrate size available today is 4 inches which limits its scalability on InP-based PICs [18].

Lithium Niobate

Lithium Niobate ($LiNbO_3$), which is transparent in the visible spectral range, performs excellent on electro-optic, acousto-optic and nonlinear optic properties. However, it could not be used to implement active components, such as lasers and detectors. Moreover, the typical electrode length of $LiNbO_3$ modulator is on centimeter orders which is much larger compared with other material-based modulators. Thus, $LiNbO_3$ shows less promising on integration for practical application and its complex process requirements either limits its possibility in large scale PIC [19].

Silicon

Silicon is the second most abundant element in our planet. Today, Si has not only been the dominant host material for electronic integrated circuits (IC), but also has shown the promise as a platform material for future large-scale PICs. Due to its low cost and suitability for high volume manufacturing, Silica-based PICs has been widely adopted for the Fiber-To-The-Home market [20].

Silicon Photonics is receiving much interest because it enables the use of well-developed Si processing technologies as well as Si substrates that are cheaper than the compound semiconductor (GaAs or InP) substrates to fabricate a broad range of optical devices. Silicon photonics creates many possibilities such as photonic integration on Si substrates, monolithic integration of both electronic and photonic devices, and optical interconnection between electronic devices, and optical

interconnection between electronic logic circuits on large-scale integrations. Whilst the performances which have been achieved are typically still inferior to those of more traditional photonic materials, they surpass the more moderate requirements of the short reach data links. Testament to this is the emergence of products based upon silicon photonics to the market. The real advantage of silicon photonics is the low manufacturing costs. A large number of devices can be fabricated on large wafers with high yield in a similar manner to fabrication within the CMOS electronics industry. Silicon photonic devices are now being demonstrated on 300mm wafers with enhancements in performance reported owing to the superior process tools available for this wafer generation.

Moreover, Silicon Photonics, which is utilizing Si itself as a waveguide by employing Si-on-insulator (SOI) infrastructure, has become popular recently. SOI provides solutions for nano-structuring of PIC, because of its high refractive index contrast between Si (3.4) and SiO2 (1.45). SOI waveguides can provide very small waveguide width (in general 0.4um~1um) and also small bending radius (even less than 10um). To date silicon photonic devices have been fabricated using SOI wafers where the buried oxide and silicon over layer provide a natural low loss guiding system. SOI based wire waveguides below 1dB/cm have been demonstrated and their potential for integration with CMOS circuitry and process compatibility make SOI an attractive material for electronic-photonic convergence. Although it is difficult to implement high performance active devices on Si, such as laser, modulator and detectors, due to its indirect bandgap, many of the building blocks required to form a functional silicon photonic circuit have been demonstrated. Hybrid-integration has been expected to implement better performance PICs by bonding III-V on SOI wafers [21].

2.2 Overview of Phased-array Optical Switch

2.2.1 Conventional structure of optical switch

There are two kinds of switching types, distinguished by the achievable switching function: blocking and non-blocking. The non-blocking architecture is capable of realizing every interconnection path between the inputs and the outputs, as each port can be operated individually without considerations of other ports state. On the other hand, if there are some interconnection paths that cannot be realized due to the certain state of other ports, the switch is defined as blocking. As discussed in this thesis, we will talk about the non-blocking switches, which is more promising for the application.

Three typical structures used in the conventional optical switches are presented below and their drawbacks are also discussed.

Crossbar (Wide-sense non-blocking)

Without requiring any existing connection to be rerouted, if any input can be connected to any certain idle output, a switch is defined as wide-sense non-blocking. Certain routing algorithms help such structure to perform without blocking. As Figure 2.2.1(a) shown, an N×N crossbar switch is made of n^2 2×2 switches. Assume the shortest path length is 1, the longest path length will be 2n-1. As the switch port n increases, the number of required switch elements and the longest path length increase with a significantly large rate. This is the main drawback of the crossbar architecture; even the switch can be fabricated without any crossovers.

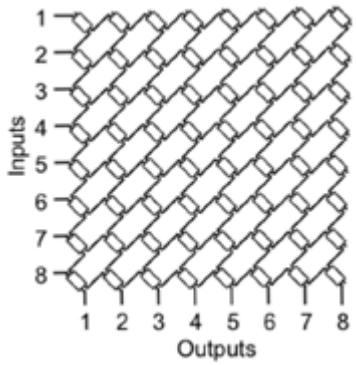


Figure 2.2.1(a): Crossbar 8×8 switch architecture

Beneš (Rearrangeable non-blocking)

Rearrangeable non-blocking switch refers to which requires rerouting of connections to realize the non-blocking property. It is so called rearrangeable, since the path of a pair of expected ports may have to be changed or rearranged when some other pairs of port initiates the connection. So each connection involves extra control complexity, which may even cause disruption of connections. Beneš switch, which based on rearrangeable non-blocking architecture, is one of the most efficient switch architectures contributed to the reduction in the number of switches using cascaded 2×2 switches as a building block. Fig 2.2.1(b) shows the typical Beneš architecture. For constructing a N×N switch, $(n/2)(2\log_2 n-1)$ 2×2 switch nodes are required. The path length is always same in this structure, which goes through $(2\log_2 n-1)$ 2×2 switches. This structure hopefully reduced number of switch nodes and the path length, while its control complexity may comes to be a big issue with increasing N.

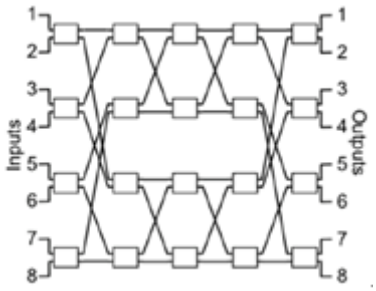


Figure 2.2.1(b): Beneš 8×8 switch architecture

Spanke (Strictly non-blocking)

A strictly non-blocking switch can make a connection between any idle input and any idle output regardless of how previous connections have already been made. Strictly non-blocking architecture is considered as the most suitable for building large-scale switches. Spanke architecture is a typical example for strictly non-blocking. N×N spanke switch is made of n 1×N switches and n 1×N switches as shown in Fig 2.2.1(c). In total, there are 2n switches elements required. The path length is all identical which equals to 2. Comparing with other schemes, spanke switch provides the least number of switch elements and shortest path length for implementing N×N switch. Morevover, it has been demonstrated recently in the literature [22]. With analytical and numerical approaches, the performance of spanke architecture (strictly non-blocking) architecture is much better in terms of throughput and latency than the Beneš (rearrangeable non-blocking) architecture. However, the drawback of conventional spanke architecture is that it requires a number of waveguide crossovers, making it difficult for large scale integration.

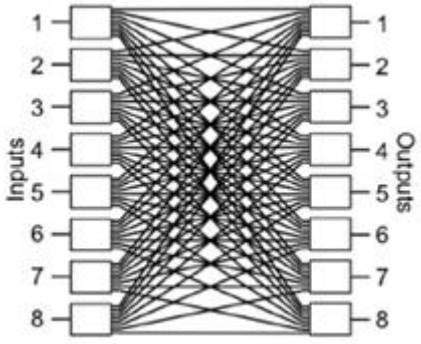


Figure 2.2.1(c): Spanke 8×8 switch architecture

In conclusion, the conventional crossbar and tree structures are is cascading several 1 × 2 or 2 × 2 switches to building an N ×N switch matrix. Cascading a large number of

this type of switches, however, faces difficulties in terms of the optical insertion loss and footprint. Among the conventional architecture, the spanker architecture performs best in reduction of required elements and path length. However, the conventional three structures have disadvantages and limitations on real application for large scale integrated circuits. Thus, new optimized structure is demanded which should perform better, especially available for large scalability.

2.2.2 Integrated optical phased-array switch

Phased-array technology was first proposed in microwave systems to provide high performance and directional flexibility. Phased-array is used for controlling the spatial distribution of electromagnetic waves through phase conditions of an array of signals, which is mainly used on antenna systems, optical beam deflectors, optical multiplexers/demultiplexers and optical switches.

Phased-array was proposed by Karl Ferdinand Braun in 1905 to improve the directivity of radio waves [23]. A phased array is a system that controls the spatial distribution of electromagnetic waves through phase conditions of an array of signals. Arrayed antennas operating at radio frequencies have been the major application of phased arrays up to now. With phased-array in antenna systems, it is available to achieve reinforced signal in certain direction by controlling the relative phases of respective signals. Analogue to optical domain, it is proved possible to construct optical path selectivity system by employing phase shifter arrays and varieties of researches have been done since then. The optical phased arrays have been used to overcome the limitations of mechanical beam steering, and to be used in optical sensor systems including laser radar [24]. These devices utilized guided-wave phase shifters and free-space optics to implement optical beam steering. Arrayed waveguide grating (AWG) multiplexer/demultiplexer, developed in 1991 [25], has been the most widespread optical phased-array device so far. Compared with previous beam steering devices, AWGs are completely integrated. Both the input signal distribution and the phase-controlled signals interference are both realized by employing star couplers. A linear phase slope is maintained by gradually changing length of arrayed waveguides. Since the effective phase difference depends on the wavelength, signals at different wavelengths are separated at the output. Now AWG technology has been widely used as mature devices with hundreds of channels in networks. Then researchers have focused on more possibilities of phased-array technology. In 1992, the first phased-array device referred as an optical switch utilized AlGaAs/GaAs guided-wave phase shifters and slab

waveguides for integrated beam steering to nine output ports [26]. In 1998, Fluck proposed thermo-optic 1×8 SiO_2 phased-array switch. In recent years, integrated 1×N and 8×8 phased-array switches on InP platform have been successfully demonstrated by Tanemura, Murat and Kwack [27]. Also, a 1×8 phased-array switch on Si platform was proposed by Chen in 2013 [10].

As shown schematically in Fig. 2.2.2(a), integrated optical phased-array switching is accomplished by distributing the optical signal to multiple waveguides using a passive splitter, controlling the phase conditions of individual waveguide modes via phase shifters, and generating the interference of these signals using another passive coupler. This principle can be extended to large numbers of outputs by increasing the number of phase shifters without the necessity of increasing the number of switching stages substantially [28].

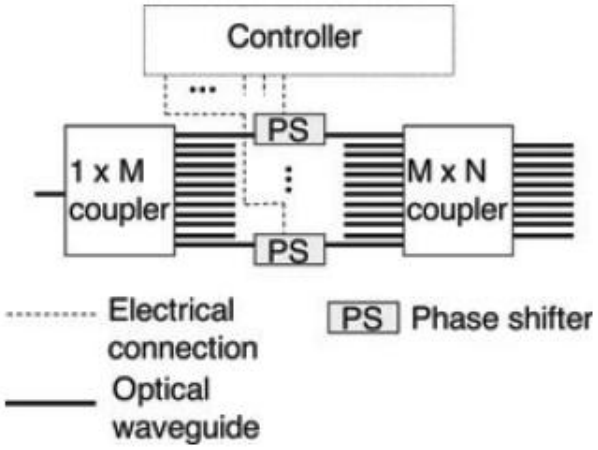


Figure 2.2.2(a)

The basic operation of single-stage switching is possible by forming a linear distribution of optical phase (with modulo 2π) in the arrayed waveguides. The deflection angle at the output star coupler depends on the slope of this distribution, which makes electro-optical switching possible.

Star couplers are employed for the 1 ×M/M×N passive couplers due to their advantages such as simple design and high fabrication tolerance. Fig 2.2.2(b) shows the scheme of star coupler.

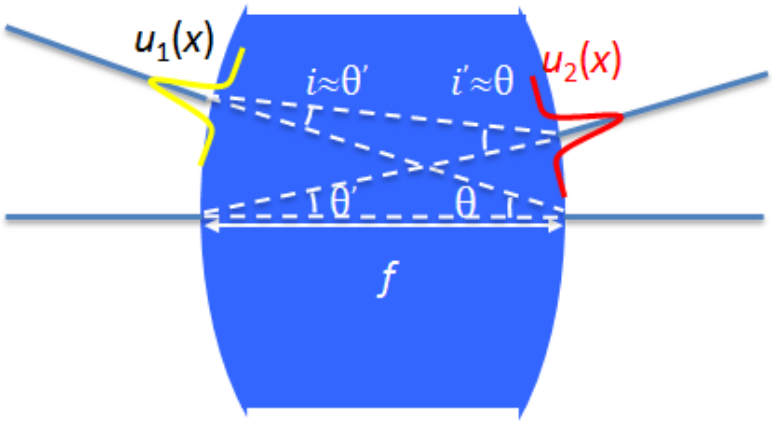


Figure 2.2.2(b): scheme of star coupler

As long as the inequality (1) is valid, Fraunhofer diffraction approximations could be used.

$$L \gg \frac{\pi w^2}{4\lambda} \tag{1}$$

Notice that in Fig 2.2.2(b) the angle of i' at the upper output port, within the paraxial approximation, with the coordinate θ at center port of output plane, and a similar property applies to i. In the other word, over the aperture of the receiving element the incident wave is approximately a circular wave originating from the center port of the input plane. Thus, the amplitude transmittance to the certain output port under the Fraunhofer approximation is given as [29]

$$\eta(\theta,\theta') = \sqrt{\frac{k}{2\pi f}} \cdot \int u_1(x)\exp(jkx\theta')dx \cdot \int u_2(x)\exp(jkx\theta)dx \cdot \exp(-jkf\theta\theta') \tag{2}$$

where $u_1(x)$ and $u_2(x)$ are the mode field profiles of the radiating and receiving waveguides respectively; θ and θ' are the input port angle and output angle respectively; k is the propagation constant at the star coupler region; f is the star coupler length; the last term of the equation $\exp(-jkf\theta\theta')$ is the phase shift applied at the phase shifter.

In this case, the transmittance of the conventional phased-array switch, ignoring the propagation loss and excess losses at the phase shifters, the amplitude transmittance to the output port is express as

$$T_n = \sum_{m=1}^{M} \eta(0,\theta_m)\cdot\eta(\theta_m,\theta_n)\cdot\exp(\phi_m) \tag{3}$$

where θ_m and θ_n are the angular coordinates the phased-array port and output port

respectively and ϕ_m is equal to the $\exp(-jkf\theta\theta')$ as applied phase shift at the m th phase shifter [13]. Fig.2.2.2 (c) shows the mode profile at each plane corresponding to the conventional phased-array switch.

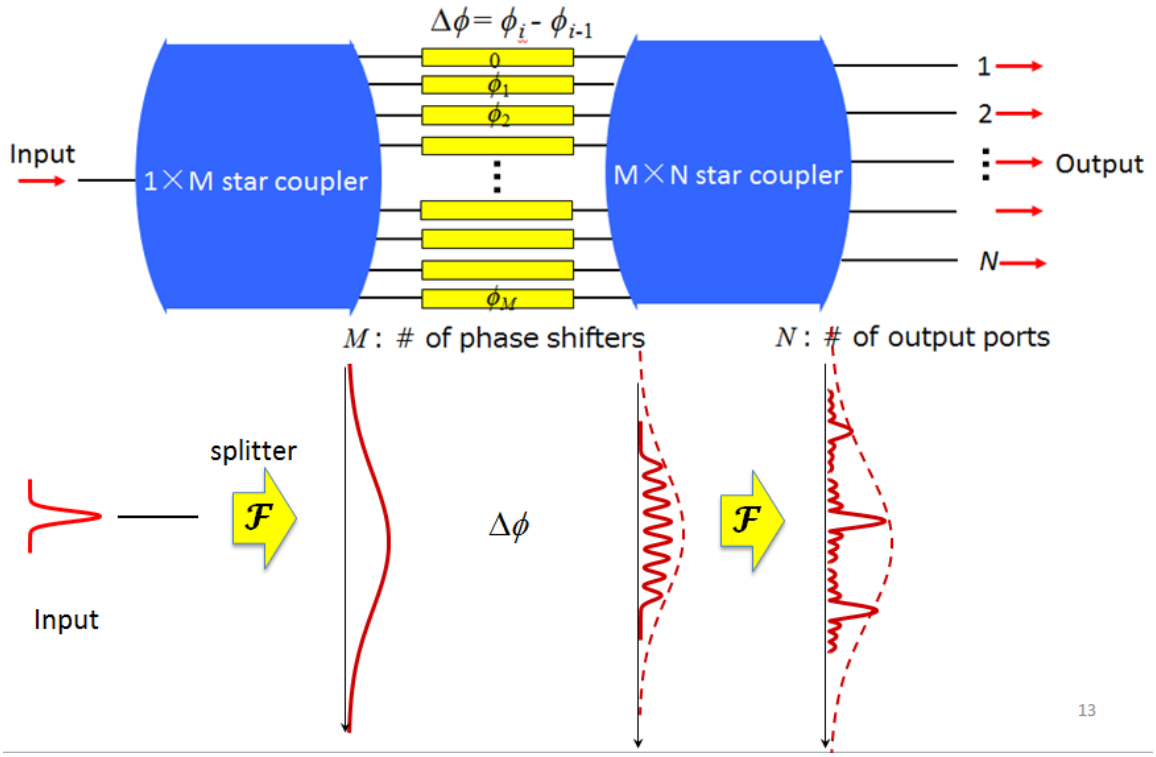


Figure 2.2.2(c): Mode profile changes at different planes of phased-array switch

By calculating Eq.(3) for various combinations of N, M, and f, the minimum M required to realize the given switching property could be estimated as M/N≈1.5. However, for large scalability, better performance of previous designed optical phased-array silicon switch, with limited M/N, is expected to be improved, especially on the extinction ratio. Now, new themes combined with phased-array technology is under investigated for further performance improvement on 1×N and N×N optical switches on Si platform.

2.3 Analytical explanation of Nyquist-sampling Phased-array Switch

As the property of phased-array switch we have discussed in chapter 2.2.2, in order to improve the extinction ratio with limited M/N ratio, it is necessary to reduce or avoid

the intersymbol interference. In telecommunication, intersymbol interference (ISI) is a form of distortion of a signal in which one symbol interferes with subsequent symbols. This is an unwanted phenomenon as the previous symbols have similar effect as noise, thus making the communication less reliable. ISI is usually caused by multipath propagation or the inherent non-linear frequency response of a channel causing successive symbols to "blur" together. The presence of ISI in the system introduces errors in the decision device at the receiver output. Therefore, in the design of the transmitting and receiving filters, the objective is to minimize the effects of ISI, and thereby deliver the digital data to its destination with the smallest error rate possible. The expected output mode profile is shown in Fig 2.2.3(a), in which adjusts the positions of the N output ports to the respective nodes of the sinc function.

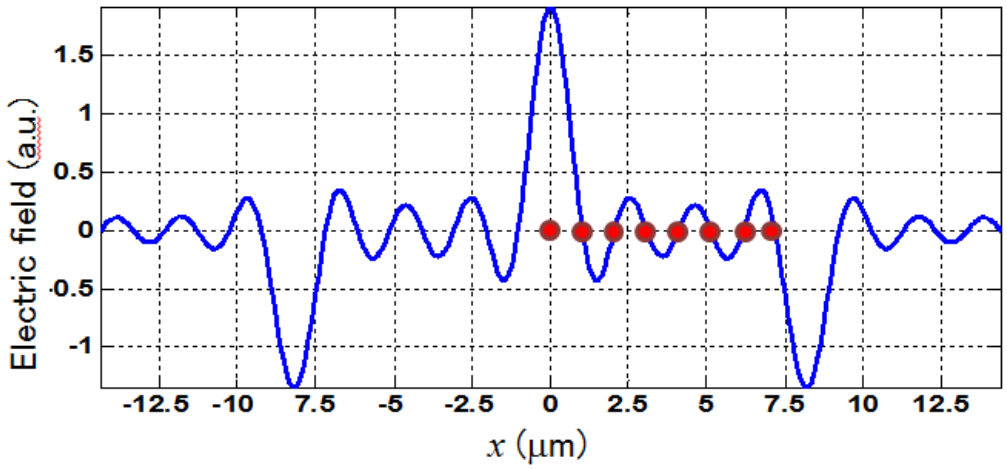


Figure 2.3.1: Expected mode profile at the output plane
with output ports set on the red nodes of the sinc function

As we discussed in the previous chapter, the output mode profile could be derived with Fourier transform of input mode profile. Thus, through shaping the input mode profile, we can get the expected output profile. Noticing that this sinc function just meets the Nyquist criterion which is described as:

$$h(nx) = \begin{cases} 1; & n = 0 \\ 0; & n \neq 0 \end{cases} \tag{4}$$

The Nyquist theorem says that this is equivalent to:

$$\frac{1}{Cx}\sum_{k=-\infty}^{+\infty} H\left(f - \frac{k}{x}\right) = 1 \quad \forall f \tag{5}$$

where $h(x)$ is the field distribution at the output plane of the star coupler, $H(f)$ is the field envelop at the input plane of the star coupler.

So we only need to shape an input mode profile to meet the Eq. (5) at the input plane. Then the raised cosine just fits the requirement which is represented as

$$H(f)=\begin{cases} T, & |f|\le \frac{1-\beta}{2T} \\ \frac{T}{2}\left[1+\cos\left(\frac{\pi T}{\beta}\left[|f|-\frac{1-\beta}{2T}\right]\right)\right], & \frac{1-\beta}{2T}<|f|\le\frac{1+\beta}{2T} \\ 0, & otherwise \end{cases}$$

$$0\le\beta\le 1 \tag{6}$$

The Fig.2.3.2 and Fig.2.3.3 show the mode profile of raised cosine and its Fourier transform respectively.

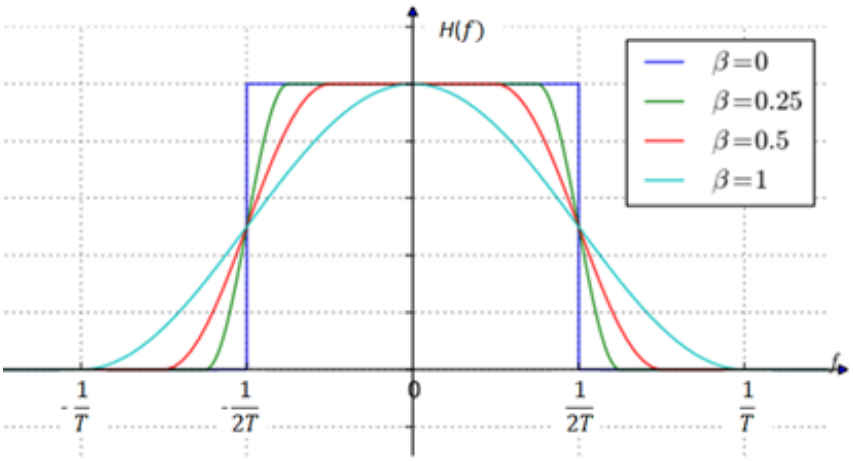


Figure 2.3.2: Mode profile of raised cosine with different β

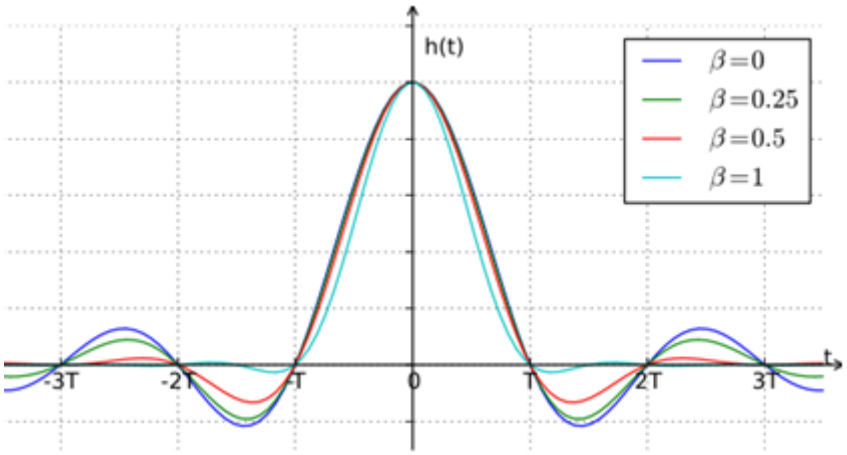


Fig2.3.3: Mode profile of raised cosine after Fourier transforms with different β

Then the field envelop at the input plane of the star coupler could be set as Fig 2.3.3 However, the intercept on the x axis determines the width of the field envelop, which also related to the number of the phase shifters. In this case, it is obvious that when

$\beta = 0$, the square shape function has the smallest intercept. So we choose the square shape field envelop in our design. And it is much easier to realize the square shape with identical field at all the phase shifters. To ensure the identical field property, cascaded 3dB couplers are employed, which is convenient on design and fabrication.

The structure of Nyquist-sampling phased-array 1×*N* switch is shown in Fig. 2.3.4. Instead of the first star coupler used in the previous phased-array switches, it utilizes one 1×*M* splitter. As a result, input light is split into *M* arrayed phase shifters with an equal power distribution, which then generates sinc-function field profile at the output of the *M*×*N* star coupler. By adjusting the positions of the *N* output ports to the respective nodes of the sinc function as shown in Fig. 2.3.4 inset (i.e., by Nyquist-sampling), we could suppress the power leakage to the undesired output ports and thus achieve high ER even with a limited *M*/*N* ratio.

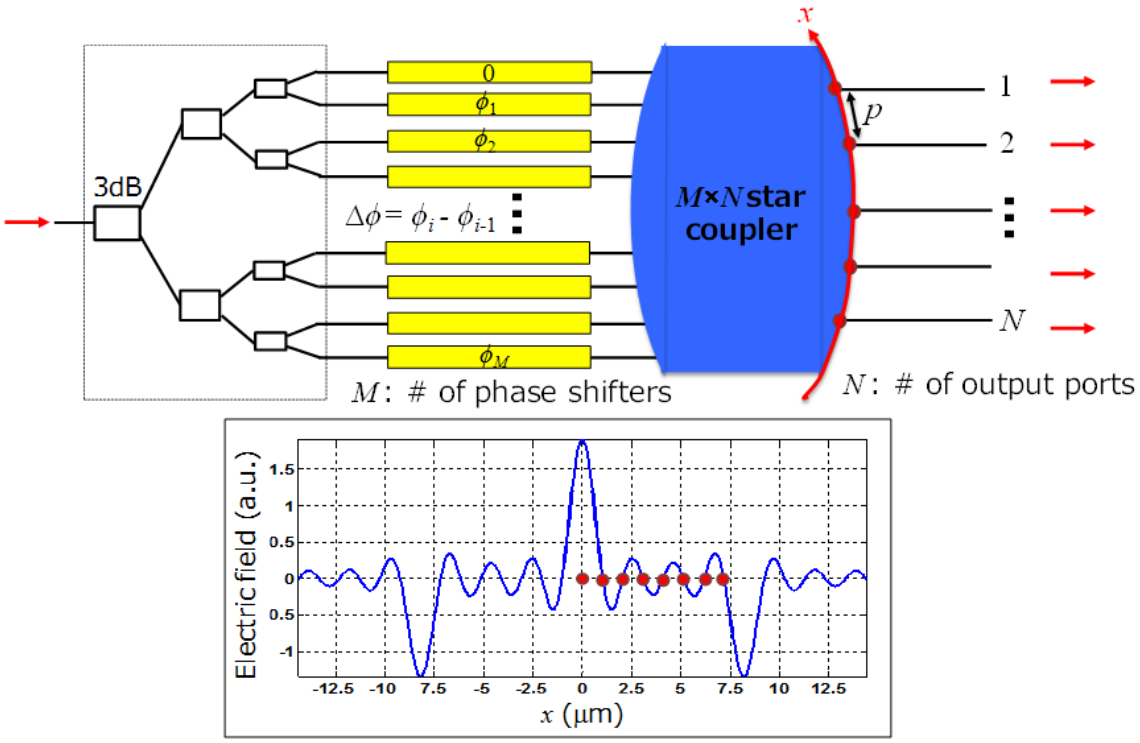


Figure 2.3.4: Structure of Nyquist-sampling phased array switch and its intensity profile at the star coupler output (inset).

Chapter 3

Analytical Simulation and Design of Device

The 1×N Nyquist-sampling phased-array silicon switch presented here is an entirely monolithically integrated semiconductor photonic device consists of one splitter part, arrays of phase shifters, one star coupler and output waveguides. All the waveguides in the array region between the splitter and star coupler are exactly same in length, which is the reason of the antisymmetrical design. Otherwise, If the light path of each array is not equal, the device becomes highly wavelength dependent similar with a tunable AWG. Each phase shifter at the center of the arrayed waveguides is used to manipulate the phase condition of individual waveguide mode respectively. Star coupler is a passive optical device that couples multiple optical waveguide modes at one plane with the modes at the other plane. These phase-controlled signals diffract in the star coupler, whose output plane embodies the output waveguides. The optical mode pattern at the output plane depends on the phase conditions of array modes through interference. The basic single-port switching condition is satisfied by forming a linear phase slope in the array, analogous to beam steering in antenna arrays and optical phased arrays. Moreover, arbitrary distribution of optical modes at the output plane could be achieved through controlling the phase and amplitude conditions of arrayed signals with a modification of the device.

Analytical simulation result and the related design of device are presented in this chapter in details.

3.1 Analytical Simulation

The principle of Nyquist-sampling phased-array optical switch has been introduced in the chapter 2. Based on this principle, in this chapter, we present some analytical simulation with Matlab platform including the comparison between two kinds of switch,

the influence on different output position and star coupler length, and possibility for large N scalability.

Comparison on 1×N Nyquist-sampling and conventional optical phased-array switch

Compared with the conventional 1×N phased-array optical switch, our design employing the Nyquist-sampling technique and is expected to provide better performance, especially on extinction ratio. Simulation results between the two different designs are presented in this chapter.

In our simulation, we take 1×7 switch as an example, which is also used for our real fabrication. Fig. 3.1.1 shows the calculated characteristics of 1×7 switches with the previous structure using a star coupler as the splitter and Fig. 3.1.2 shows the proposed Nyquist-sampling structure using cascaded 3dB couplers as the splitter. The transmittance to the respective output ports is plotted as a function of the applied phase difference $\Delta\phi$ between the adjacent phase shifters. In both cases, we assume a silicon nanowire switch with waveguide width = 0.5μm, M×N star coupler length = 15μm, and M = 8.

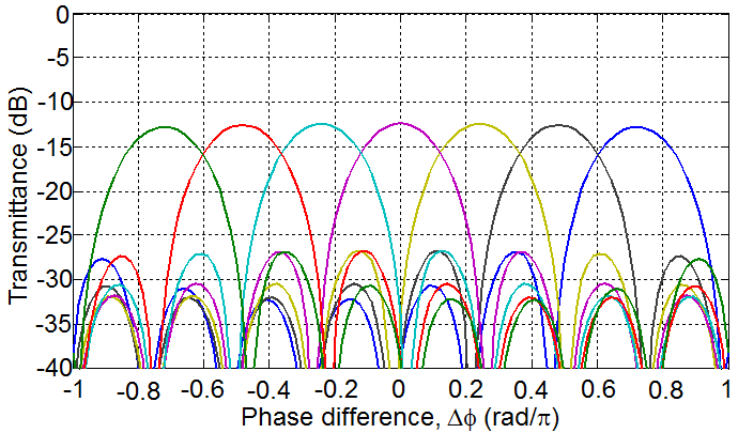


Figure 3.1.1: Transmittance of previous 1×7 phased-array switch

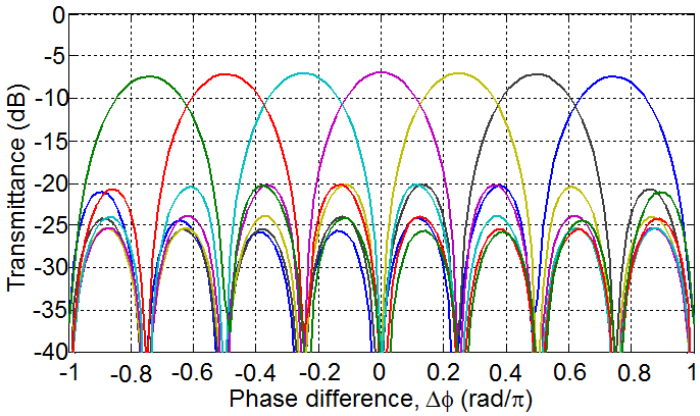


Figure 3.1.2: Transmittance of 1×7 Nyquist-sampling phased-array switch

The extinction ratio (ER) of previous design can be 17.2dB for the worst port, while the ER of Nyquist-sampling design is improved to 26.4dB. It shows that with Nyquist-sampling switch presents better performance on ER with same M/N ratio; In other words, it could reach the required ER with less M/N ratio.

Extinction ratio dependence on different output pitch of Nyquist-sampling switch

Based on the Nyquist-sampling theory, it is necessary to set the output ports of star coupler at certain positions. Fig. 3.1.3 shows the ER of 1×7 Nyquist-sampling switch with M=8 for different output pitches. Both the best ER of the ports and worst ER of the ports for each case are shown as the red and green lines respectively.

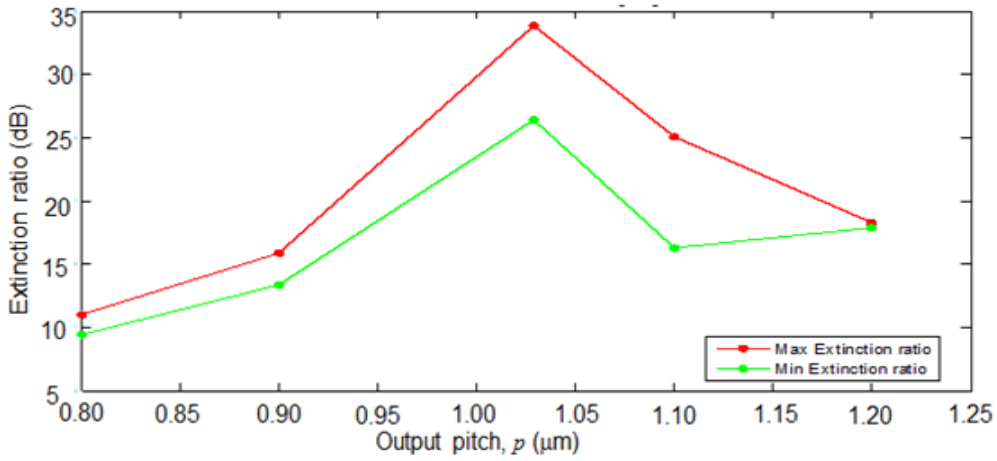


Figure 3.1.3: Dependence of extinction ratio on output port pitch of 1×7 Nyquist-sampling switch

The x axis is corresponded to the output pitch and y axis is corresponded to the ER.

The output pitch is set from 0.80μm to 1.20μm with 0.1μm step. As it is shown that when the output pitch is p = 1.03μm, corresponding to the Nyquist-sampling condition, we obtain the highest ER. This result also indicates that it is important to adjust the output ports to meet the condition.

Extinction ratio of Nyquist-sampling switch with different star coupler length

Based on the characteristic of phased-array switch, the length of star coupler also has influence on the ER. Fig. 3.1.4 shows the dependence of extinction ratio on different star coupler length for 1×7 Nyquist-sampling switch.

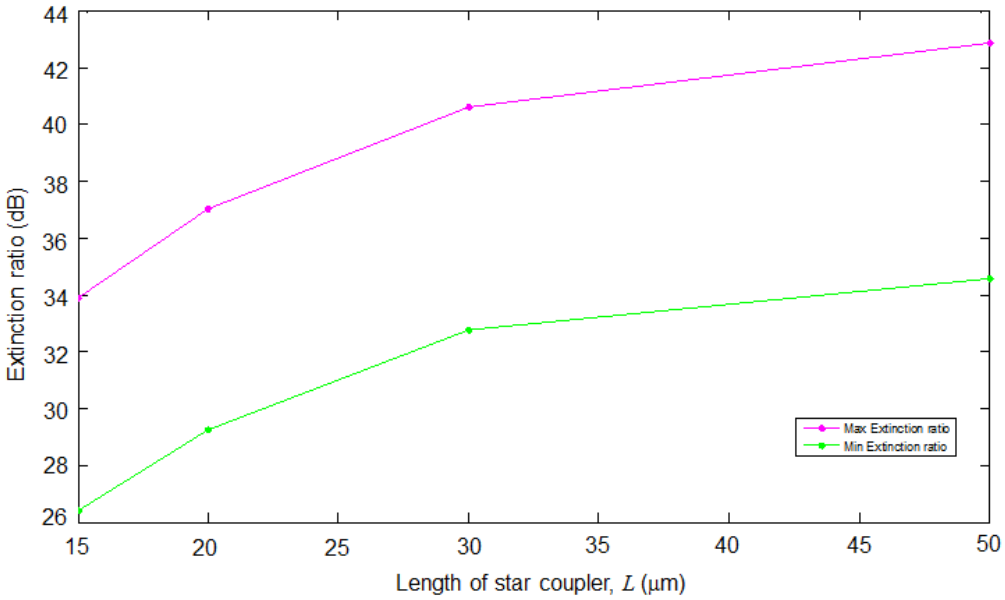


Figure 3.1.4: Dependence of extinction ratio on length of star coupler of 1×7 Nyquist-sampling switch

The length of star coupler changes from 15μm to 50μm. With optimized output position under Nyquist-sampling condition, ER increases with larger length of star coupler. However, larger star coupler will increase the power loss and the footprint of device.

Extinction ratio of Nyquist-sampling switch with large N

In order to make sure that Nyquist-sampling switch could get high ER with limited M/N ratio. Fig. 3.1.5 shows the characterization of 1×15 Nyquist-sampling phased array switch (waveguide width = 0.5 μm, star coupler length = 50 μm) with M = 16.

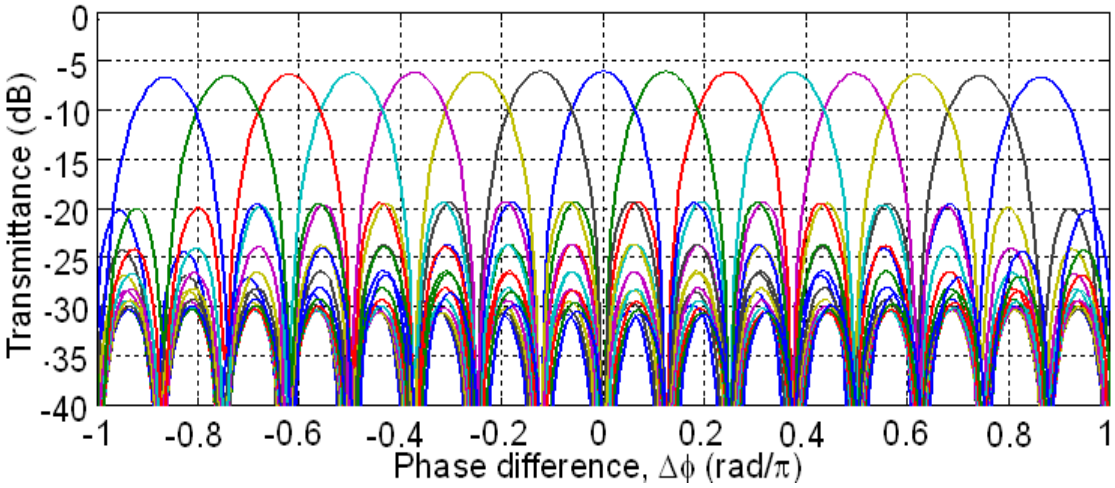


Figure 3.1.5: Characteristic of 1×15 Nyquist-sampling Switch with 16 phase shifters

ER larger than 23.1 dB is obtained with M/N = 1.07. The reduced number of phase shifters would effectively shrink the device footprint and reduce the overall power consumption as well as complexity of the driver circuit. As a result, Nyquist-sampling phased-array switch provides better performance on large scalability with small M/N≈ 1.07 compared with conventional design M/N=1.5.

3.2 Design of Nyquist-sampling Phased-array Switch

The layout design determines several characteristics of device such as insertion loss, extinction ratio, power consumption and footprint. As explained in previous chapter, some compromise is required to balance the performance of the device. Thus, further optimization is available for better performance.

The design parameters which are the most effective on the switch characteristics are the width of waveguides at the intersections with the star coupler, the length of star couplers, the number of arrayed waveguides, array pitch and the output pitch. The layout of 1×N Nyquist-sampling phased-array switch is mainly consist of four parts as cascaded-3dB splitter, phase shifter array, star coupler and extra waveguides. Each of them has its design requirement and principle. Here we presented our design of 1×7 Nyquist-sampling phased-array switch. The explanation is given in details below.

Wavelength independent asymmetrical structure

The device is wavelength independent, so it requires that path length of each array

waveguides should be same and leads to the asymmetric of the device. Fig.3.2.1 shows the asymmetric structure of device which is 1mm×1mm.

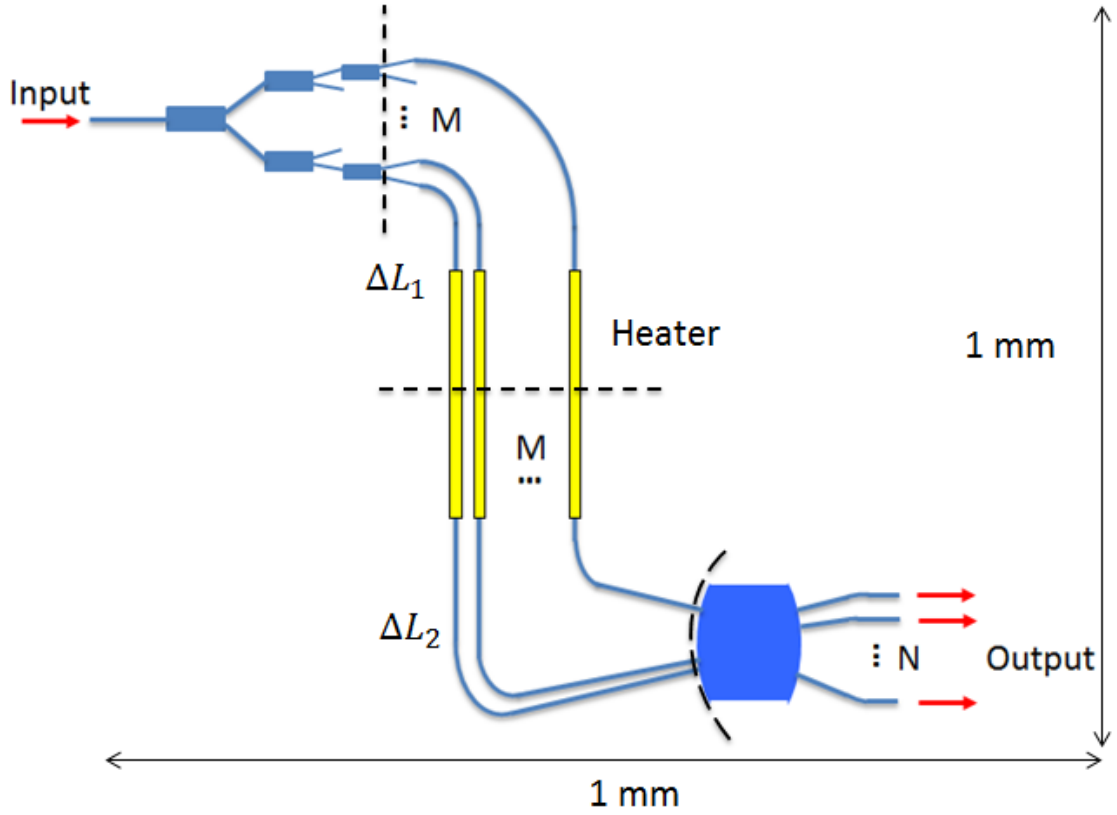


Figure 3.2.1: Layout of 1×N Nyquist-sampling switch

Since the symmetric structure of cascaded 3dB coupler, the path from input port to the output plane of splitter is same. To design all the path length identical, only the path between output plane of splitter and output plane of star coupler need to be considered. We divide the path into two parts at the middle of the straight waveguide. As shown in figure, ΔL_1 refers to the length difference for each path of the upper part and ΔL_2 refers to the length difference of the lower part. Then the wavelength independent condition could be given as

$$\Delta L_1 + \Delta L_2 = 0 \qquad (3\text{-}1)$$

ΔL_1 is introduced by the bending part with different radius; ΔL_2 is introduced by the low straight part and bending structure. With mathematic calculation for both parts, it is easy to fit the Eq. (3-1) with proper length of each parameter.

Cascaded-3dB Splitter

In order to split the input light into arrayed waveguides identically, a cascaded-3dB splitter is employed. The power distribution performance through this splitter is rather important, since it determines the mode profile at the output plane as discussed in chapter 2.

Fig 3.2.2 shows the layout of cascaded-3dB splitter and 3dB coupler element. At each node, same 3dB coupler element divided the input power into two identical ones. At last, the input power splits into M arrayed waveguides with phase shifters. Since it is directly connected to the arrayed waveguides, the pitch between adjacent ports (p_1) should be all same and equals to the pitch between arrayed phase shifters.

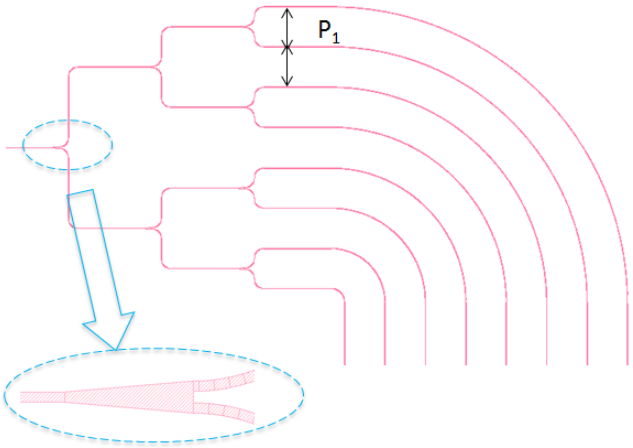


Figure 3.2.3(a): cascaded 3dB splitter

Fig 3.2.3(a) shows the characteristic of taper-structure presented by BeamProp simulation. It is proved that the power distribution at two output ports is equal through such taper-structure 3dB coupler. However, with input waveguide width=0.4μm, output waveguide width =1.25μm, taper end width=5μm, the power at each output of 3dB coupler is about 30%, which is bit far from expected 50%.

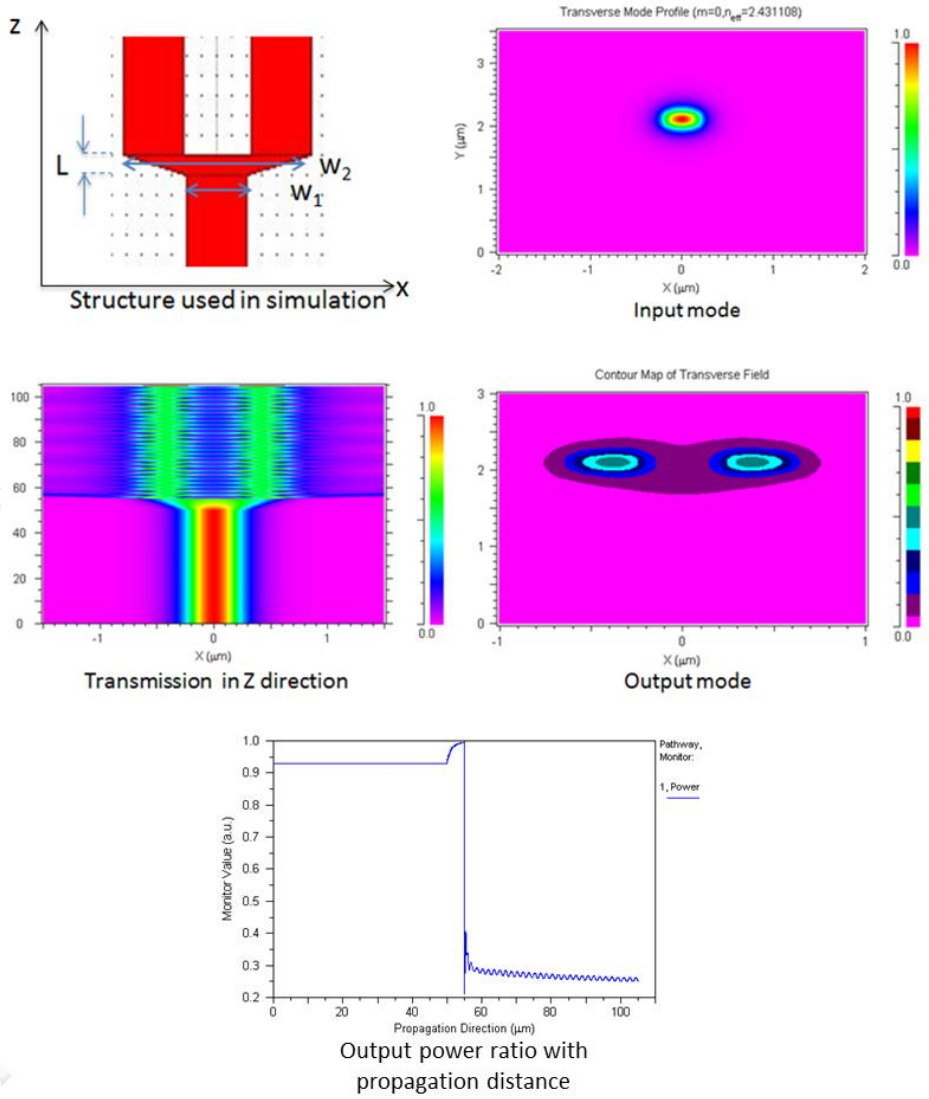


Figure 3.2.3(a): characteristic of taper-structure coupler

Fig 3.2.3(b) shows the characteristic of directly bending connected structure. With the same equal distribution property, the directly connected structure provides higher output power ratio with same parameter.

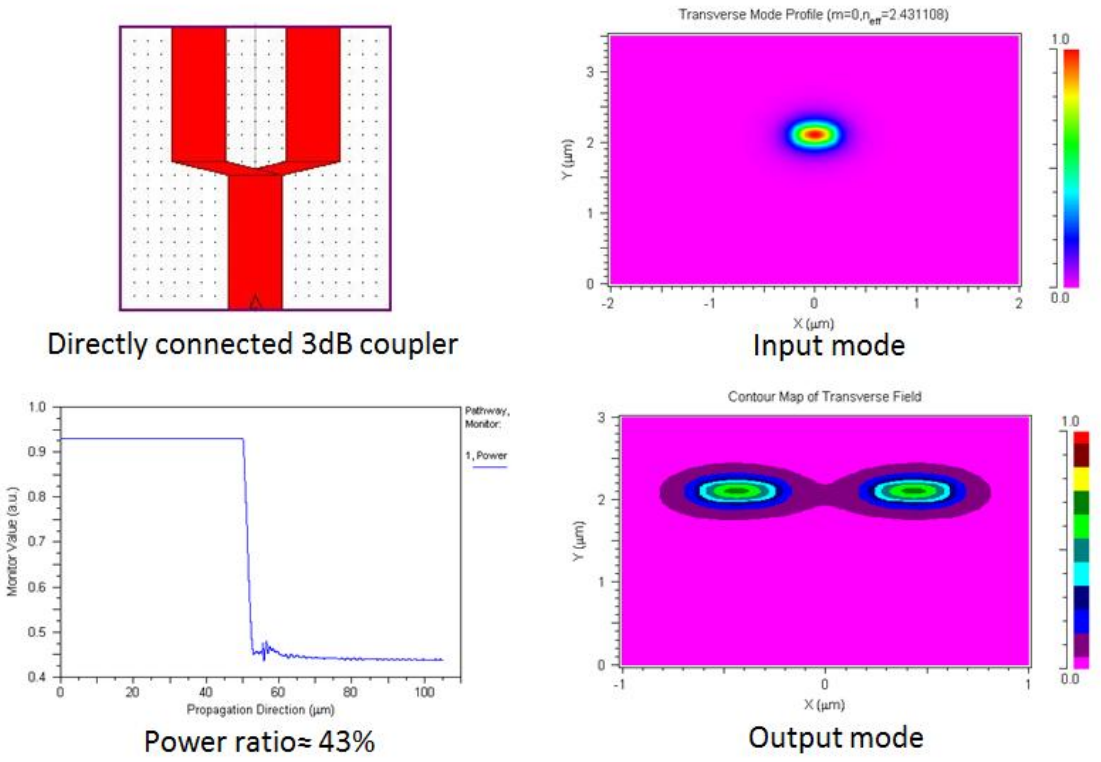


Fig 3.2.3(b): characteristic of directly connected 3dB coupler

However, as this research is mainly focused on the possibility of extinction ratio improvement, 3dB coupler elements only need to provide identical power distribution. Due to the process limitation, it is not easy to fabricate directly connected 3dB coupler, so the taper-structure coupler is chosen which is much easier to be fabricated. Moreover, cascaded tree structure is only employed with perform better stability and easy fabrication. Considering the large footprint limitation caused by this structure on scalability, other integrated couplers which can also provide equal distributed power with large number of output could be taken into place to shrink the size of splitter, if necessary.

Thermo-optics phase shifter

The optical switches based on thermo-optic (TO) effect are very attractive due to their simplicity and flexibility. The thermo-optic effect refers to the variation of the refractive index of a heated dielectric material. The thin-film heater is utilized to change

the refractive index and propagation characteristic of waveguide. Consequently, get a phase shift and output image changed [30]. The phase shift is controlled as given,

$$\Delta\emptyset = \frac{2\pi}{\lambda} \cdot \Delta n \cdot L \tag{3-2}$$

where Δn is the change of refractive index, L is the length of heater. Δn could be derived as

$$\Delta n = \frac{dn}{dT} \cdot \Delta T \tag{3-3}$$

where $\frac{dn}{dT}$ is referred to thermo-efficiency, which depends on the temperature.

Since the thermo-optic phase shifter design is same with the previous phased-array switch, here we just use the same length of phase shifters as L_h=400μm.

Waveguide heater and electrode

Since the high refractive index contrast between Si (3.47) and SiO2 (1.45), silicon-on-insulator (SOI) waveguides can have very small waveguide width (<1μm) and also small bending radius (~10μm). In our case, we use mesa type waveguides. The silicon core width=0.5μm/0.4μm at junctions/others, and height=0.26μm, with 0.6μm thick SiO2 covered and 1μm thick box layer underneath as shown in Fig. 3.2.4.

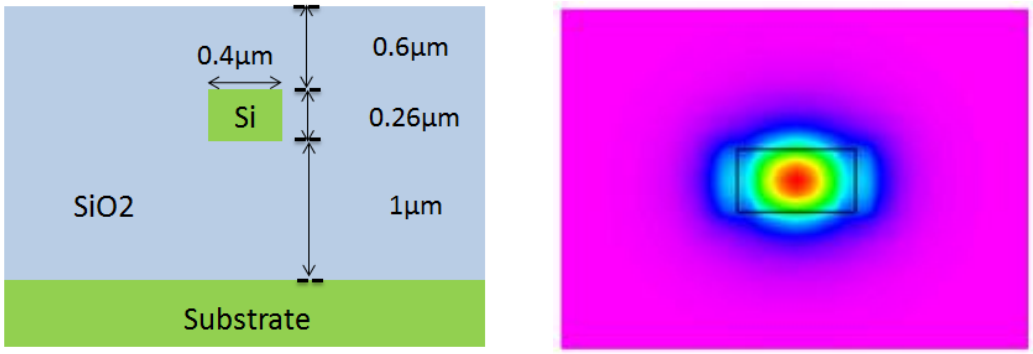


Figure 3.2.4: Cross-section of waveguide

With effective refractive index method, we could get the n_{eff} = 2.88 as shown in Fig. 3.2.5.

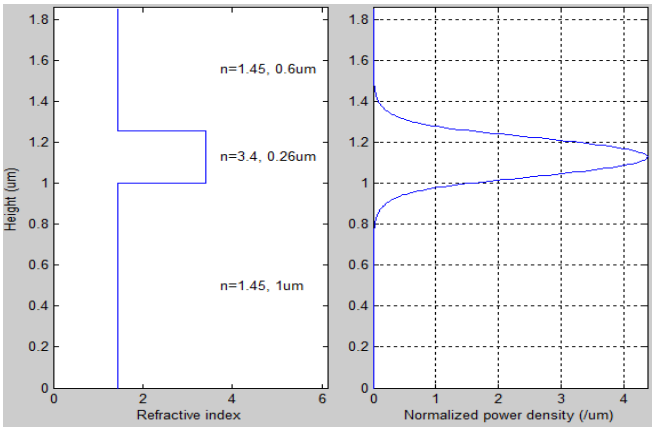


Figure 3.2.5: effective refractive index calculation

Heater and electrode

For the heater and electrode parts, since we use thermo-optics to change the refractive index of waveguide which related to the main power consumption of device. In order to improve the power efficiency, heat isolation trenches are employed to reduce the influence on adjacent arrays and to help achieve good heat conduction. Based on the analysis finished by our previous lab member, width of isolation trenches between adjacent phase shifters and the pitch between adjacent phase shifters determines the performance of heat conduction. The heater material is Titanium, which performs good attachment on SiO_2 surface and high resistance 420nΩ·m. Fig. 3.2.6 shows the cross-section of phase array waveguide with heater covered. The width of the heat isolation trench W_t = 10μm, thickness of trench = 1μm; width of heater W_h =5μm, thickness H_h = 0.1μm; pitch between adjacent phase shifters G = 30μm.

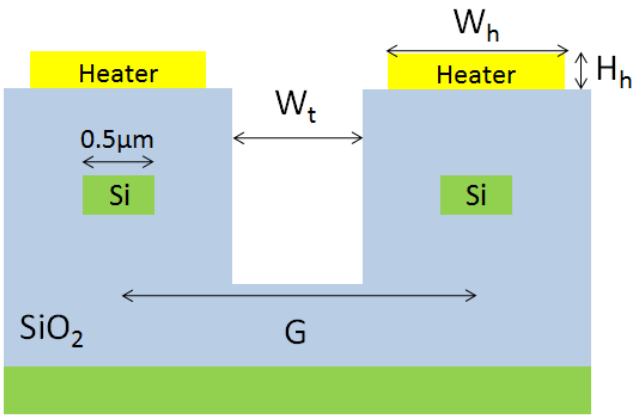


Figure 3.2.6: Cross-section of phase array waveguides

Fig. 3.2.7 shows the top view and cross-section of heater and electrode. The heater in our design use only 0.1μm thick Titanium without Au on it, which is different from previous design and provides larger resistance to help improve the power efficiency. The electrode is same with the previous structure, which is consist of 0.1μm thick Titanium to ensure the attachment between 0.7μm thick Au and SiO_2 underneath.

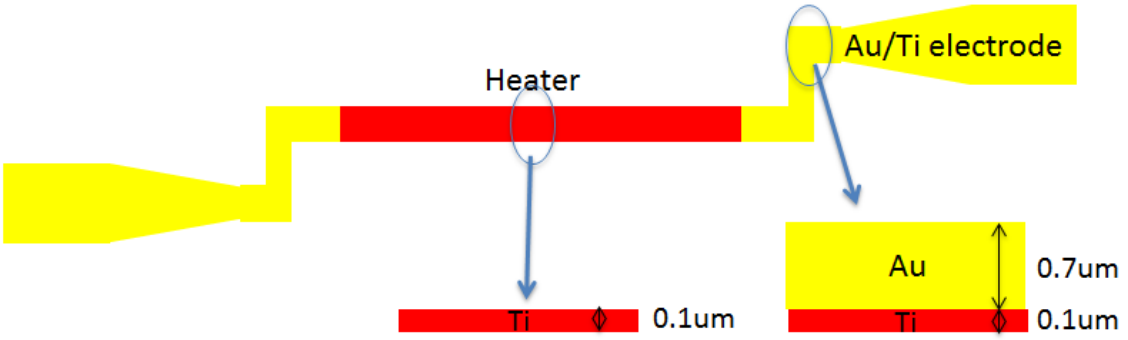


Figure 3.2.7: top view and cross-section of heater/electrode

Star coupler

As explained before, star coupler is used to generate interference of the phased controlled input light to achieve the beam steering and port selection. Based on the Nyquist criterion, we set the output ports at certain sinc function nodes with proper number of phase shifters (M) to meet our requirement of extinction ratio improvement. Another requirement is that the waveguides of the output plane should not cover a total length wider than the FSR, which avoids multiple waveguides receiving light from different diffraction modes. Also, the pitch of the waveguides at the input plane of star coupler affects the FSR inversely proportional.

In conclusion, the star coupler length, array and output pitches, and the number of arrayed waveguides are not independent parameters and their values have to be optimized depending on the design priorities. In our case, we set the parameters as pitch of input at star coupler (p_{in}) = 1μm, pitch of output at star coupler (p_{out}) = 1μm, length of star coupler (L_f) = 15μm, width of waveguide at input/output ports (w_{in}/w_{out}) = 0.5μm as shown in Fig. 3.2.8.

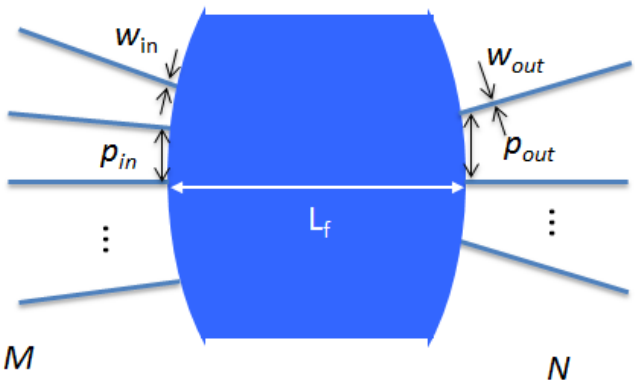


Figure 3.2.8: parameters of star coupler

3.3 Conclusion

In this chapter, the analytical simulation and design of the device have been introduced. The relatively optimized parameter is shown in the Table 3.1 below.

Parameters	Length (μm)	Description
W_{wg} , H_{wg}	0.4/0.5 , 0.26	Silicon core : width and height
L_f	15	Length of star coupler
p_{in} , p_{out}	1 , 1	Pitch of input and output waveguides at star coupler
G	30	Pitch between adjacent phase shifters
L_h	400	Length of phase shifter
W_t , H_t	10 , 1	Heat isolation trench: width and height
W_H , H_H	5 , 0.1	Heater (Ti): width and thickness
H_{Ti} , H_{Au}	0.1 , 0.7	Electrode: thickness of Ti and Au

Table 3.1: parameters of 1×7 Nyquist-sampling phased-array optical switch

Fig. 3.3 shows the layout of final device, with different layers: silicon waveguide layer (red), isolation trench layer (purple), heater layer (dark blue), electrode (light blue).

The size of the waveguide part is 0.8mm×1mm, the full size of the device including electrodes is 1.5mm×1.5mm.

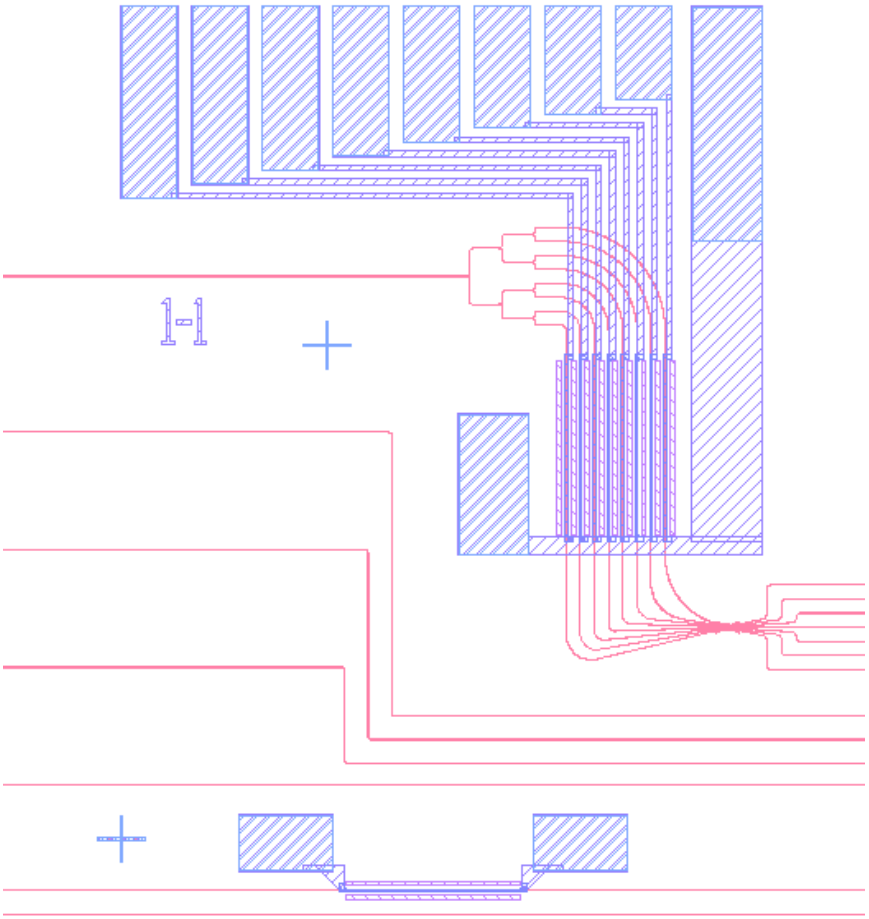


Figure 3.3: Layout of device with different layers

Chapter 4

Fabrication of Device

In this chapter, the process flow and the condition are introduced. The device is fabricated on the SOI substrate, with EB writing, SiO_2 sputtering, dry etching, wet etching, photolithography and metal deposition. The condition and fabrication result of each process is introduced in details.

4.1 Process Flow

The device process flow is shown in Figure 4.1.1.

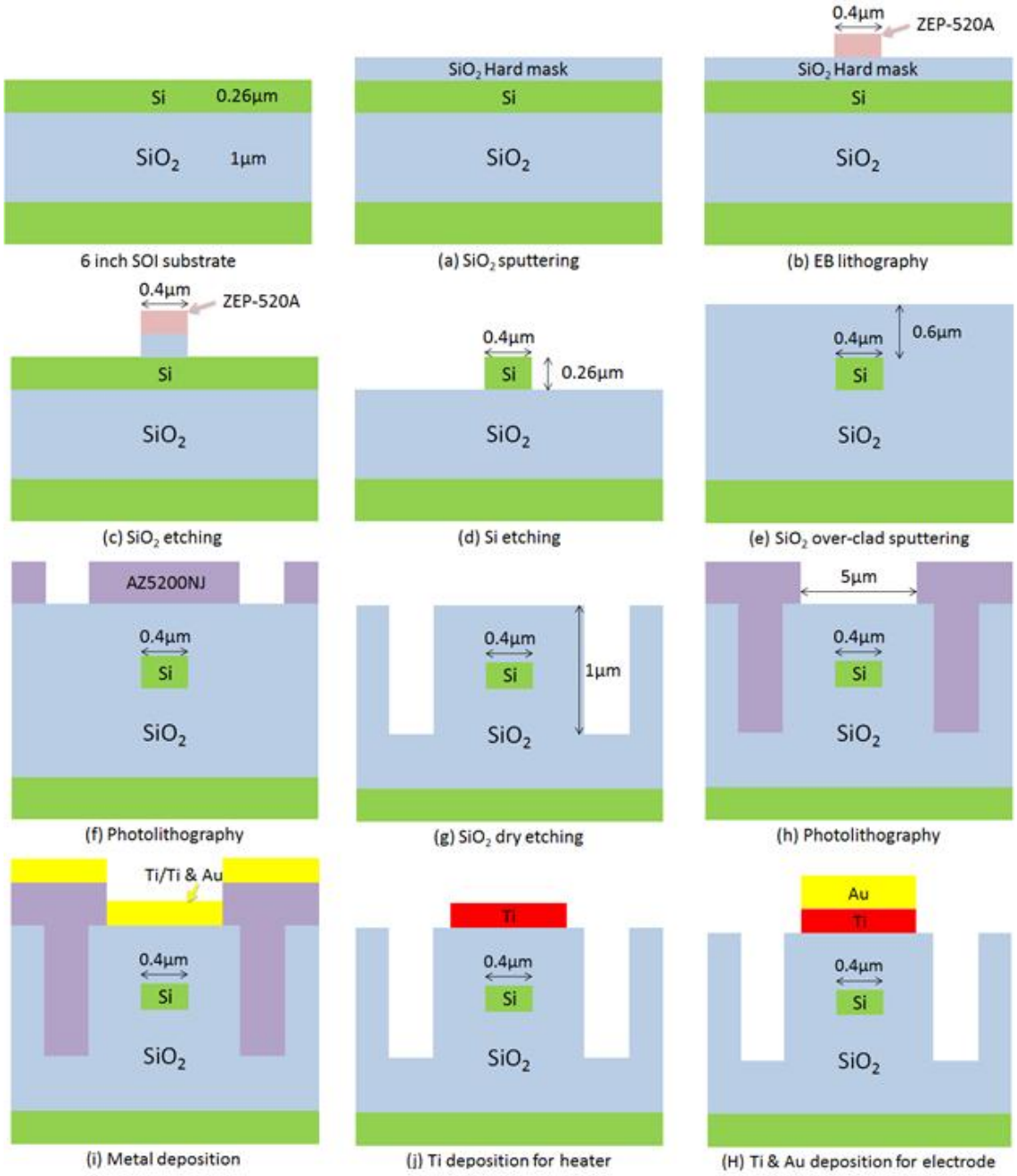


Figure 4.1.1: Process flow

Process (h) and (i) should be done twice to deposit different metal layer for heater and electrode respectively.

4.2 Fabrication Condition & Results

Cleaning and Dicing

Here we use 6 inch SOI wafer as substrate to fabricate the device. First, the wafer is divided into 3cm × 3cm chips by dicer. Then we use piranha (H_2SO_4:H_2O_2=3:1) to clean the chips for 10mins with hotplate temperature 170°C in order to remove particles and dusts on the SOI surface.

SiO_2 Sputtering

We use Anelva Sputter to do the SiO_2 sputtering on the SOI chips. With power source 200W for 30mins, in which the sputter rate is about 6nm/mins, the thickness of the sputtered SiO_2 layer is measured to be around 180nm~200nm by Dektak profiler. The detail condition is shown in Table 4.1.1.

Target	Power source	Pressure	Gas flow	Time	Sputter rate
SiO_2	200W	0.5Pa	Ar@12sccm	30mins	6~7nm/min

Table 2: condition for SiO_2 Sputtering

EB writing

We use negative EB resist ZEP-520 as the EB resist for the EB writing, which means that most of the areas on the chip is shot by the electron beams. Since the rather small dimension waveguides of device (smallest width=0.4μm, bending radius=7μm), the waveguide is fragile (some narrow parts of waveguide will miss or flow away) when do the EB writing directly. The EB writing result without optimization as shown in Figure 4.1.2(a)(b), some parts of waveguides are missing or dislocation. The bending part and narrow part is more sensitive than that the straight part and wide part in the same condition.

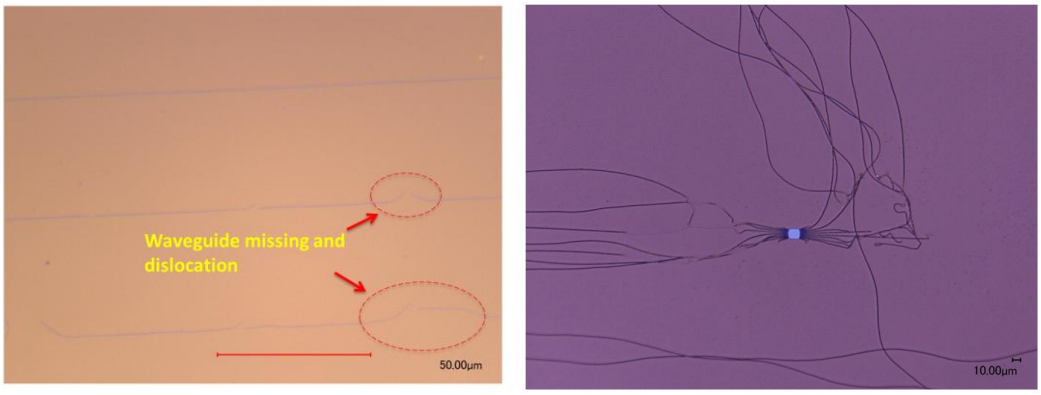


Figure 5.1.2(a)(b): waveguides are missing and dislocated in two times EB writing

Thus, in order to get well written waveguides, shrinking the beam shot areas is necessary. Fig 4.1.3 shows the strategy used in the EB pattern. By employing additional cover (red shadow parts in the figure) on the blank parts, the area exposed to the electron beam shot is tremendously reduced. To ensure that adding parts would not affect the device performance, the pitch between the cover area and device is larger than 5μm.

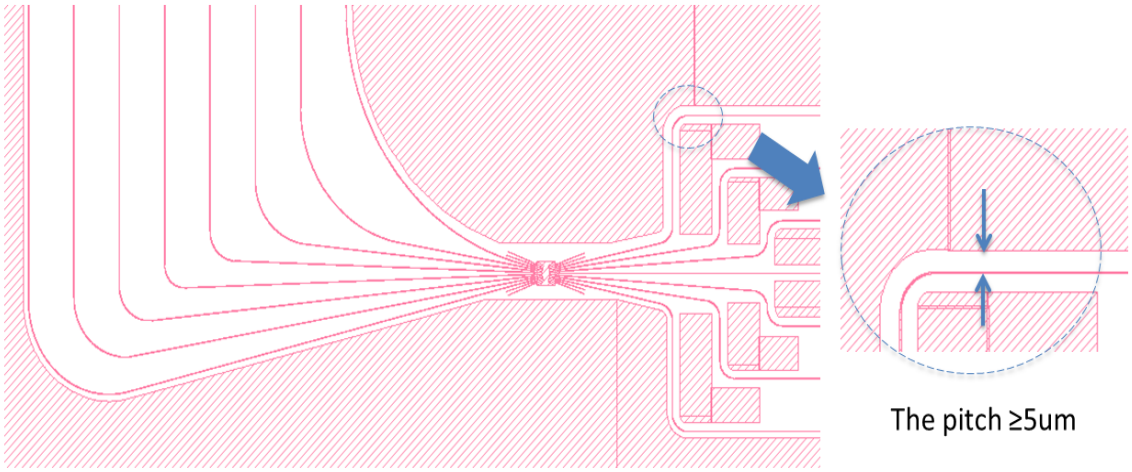


Figure 4.1.3: modified EB pattern with cover on blank part

The spin coating recipe is shown below in Table 4.1.2. OAP primer is for better contact between SiO_2 layer and ZEP-520 resist. Espacer is necessary for better conductivity, since the SiO_2 itself is not good conductor for electrons.

	OAP (Primer)	ZEP-520A	エスペーサー (Espacer)
Spincoat speed	3000rpm	4000rpm	3000rpm
Coating time	30s	60s	60s
Bake temperature	110℃	180℃	110℃
Bake time	60s	5~10mins	10mins

Table 4.1.2:spincoating recipe for EB writing

The dose count for EB writing should be in the range from 104μc/cm^2 to 110μc/cm^2. After writing the pattern, development is required to remove the waste part. Before doing the development, it is necessary to wash off the espacer with water. Then put the sample in ZED-N50 for 1min, adding several seconds if not enough. Use IPA to rinse for 1min. And the final EB writing pattern is shown in Figure 4.1.4.

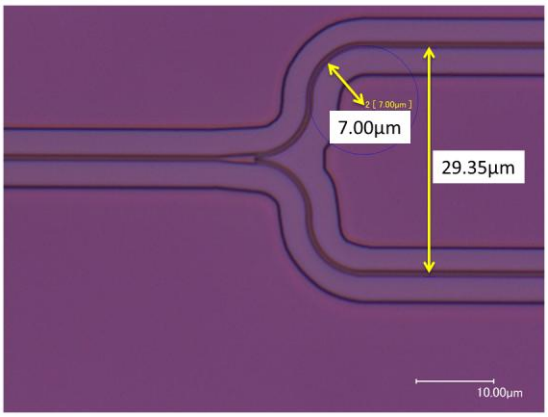


Figure 4.1.4(a): waveguide with the smallest bending radius=7μm

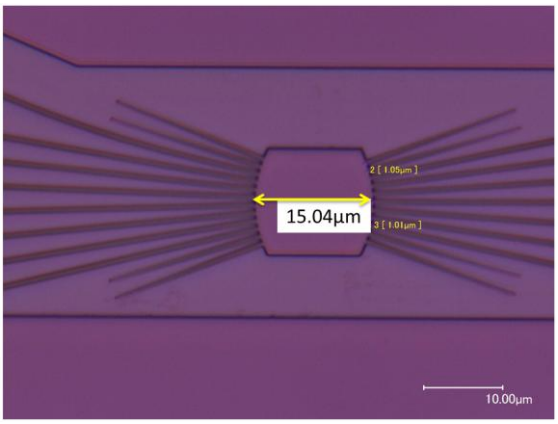


Figure 4.1.4(b): star coupler with 15.04μm

Dry etching

Dry etching is required twice. First, use CHF_3 to etch the SiO_2 layer. Then use O_2 to do the ashing in order to remove the EB resist. At last, use Cl_2 to etch the Si layer. The etching condition is shown in the Table 4.1.3. The etching rate is about 25nm/min for SiO_2 and 145nm/min for Si.

	SiO_2 etching	Ashing	Si etching
Gas pressure	1.00pa	5.00pa	2.00pa
Source power	60W	200W	200W
Bias power	25W	0	40W
O_2 flow rate	0	10.00sccm	0
Ar flow rate	5.00sccm	0	0
CHF_3 flow rate	5.00sccm	0	0
Cl_2 flow rate	0	0	8sccm
Etching rate	25~30nm/min	—	140~150nm/min
Time	14mins	10mins	2.5mins

Table 4.1.3: etching condition

Fig 4.1.5(a)(b) and (c) show the top view and cross-section from scanning electron microscope (SEM) image of device after SiO_2 layer etching. The previous two figures show that the EB writing part is rather successful, even the narrowest is OK. From fig (c), we could see that the vertical level and roughness of SiO_2 etching is acceptable.

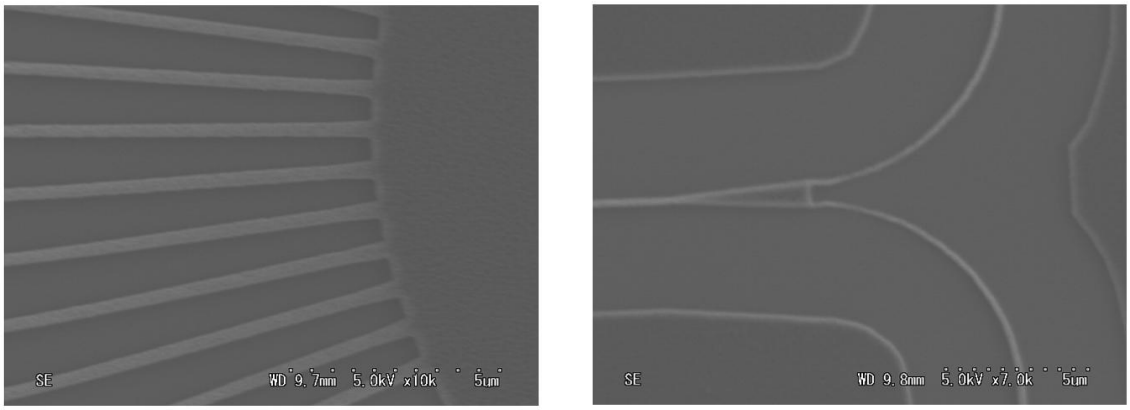


Figure 4.1.6(a)(b): top view at input of star coupler after SiO_2 etching

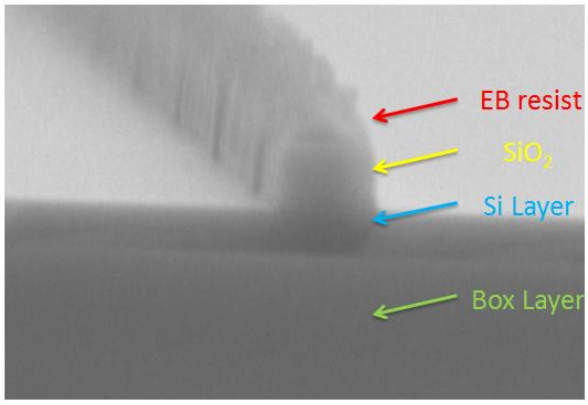


Figure 4.1.5(c): cross-section of waveguide after SiO2 etching

Fig 4.1.6(a) and (b)(c) respectively show the top view and cross-section from SEM image of device after ashing and Cl_2 etching. Considering the roughness and verticality, these figures indicate that the etching condition of Cl_2 is suitable for the desirable mesa silicon waveguides.

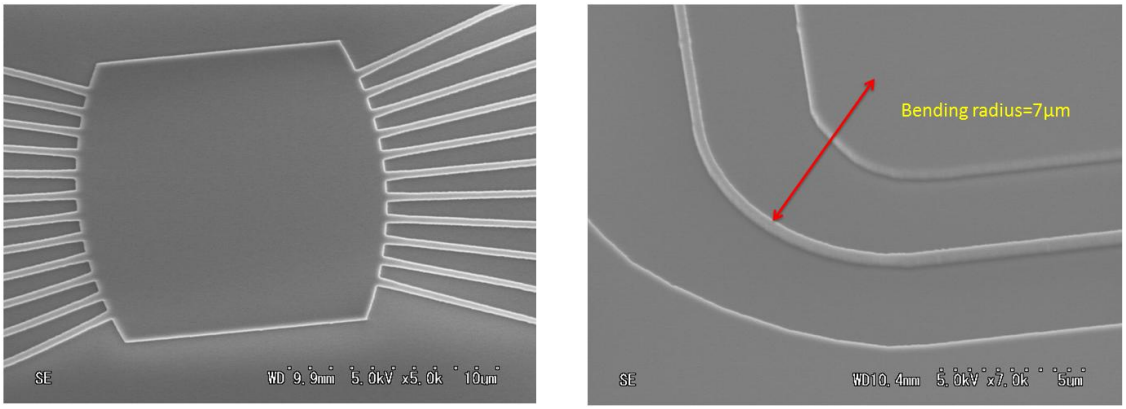


Figure 4.1.6(a)(b): top view of star coupler and bending & straight waveguide after ashing and Si etching

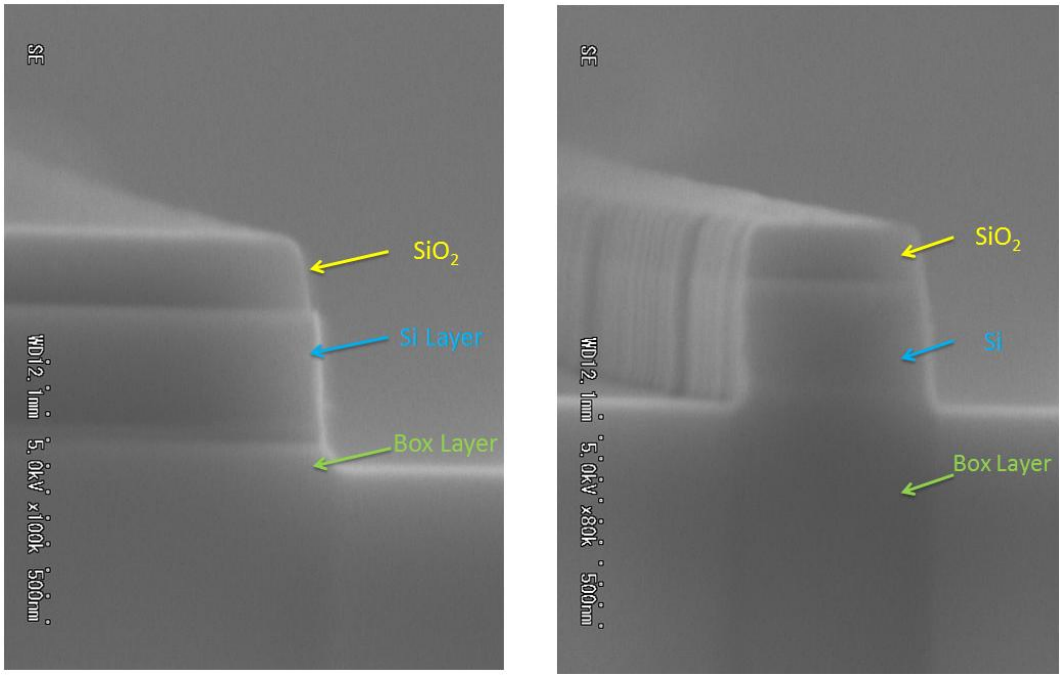


Figure 4.1.6(c)(d): cross-section of waveguide after ashing and Si etching

Wet etching

In order to remove the remaining SiO_2 hard mask on the top of Si waveguide, we put the sample into BHF for 10s. Another cleaning process may be required, if there are particles on the surface.

Another SiO_2 Sputtering

One more time sputter SiO_2 is required in the same condition shown in Table 4.1.1, with only difference the time is 90min. Then the sputtered SiO_2 cover layer thickness is about 600nm.

Photolithography

In order to etch trenches between phased-array waveguides to improve the heat isolation, we do the photolithography with photomask to set the expected position for SiO_2 etching. Here we use AZ5200NJ which is positive photo-resist. The steps in details are listed below:

(a) Spincoating: 500rpm for 5s and 4000rpm for 40s
(b) Prebake on hotplate at 90℃ for 70s
(c) Exposure with photo-mask for 1s
(d) Postbake on hotplate at 120℃ for 2mins

(e) Exposure without photo-mask for 7s
(f) Development in NMD3 for 1min and rinse in water for more than 1min

SiO_2 Dry etching for isolation trench

SiO_2 dry etching, in the same condition as mentioned above, is required to etch the isolation trench. The etching time is roughly 40mins for 1um trench thickness.

Then use acetone and IPA to remove the photo-resist on the sample. Another cleaning process would be added, if necessary.

Heater metal deposition

We first use AZ5200NJ as photo-resist in the same steps mentioned above to do the photolithography. Then with EB evaporator, we deposit 100nm thick and 5um width Ti on the top of the arrayed waveguides as heaters. The deposition rate had better to be smaller than 0.2nm/s to ensure the quality of deposit metal.

Then do the liftoff in acetone solvent at 70℃ for more than 10mins. Another 2mins in Ultrasonic cleaner is required to remove all the waste particles on the sample. Use IPA to rinse again.

Electrode metal deposition

Similar with heater metal deposition, after photolithography we deposit 100nm thick Ti and 700nm thick Au as electrodes for the device. The Au deposition rate could be faster but no more than 0.5nm/s. Then do the liftoff again.

4.3 Discussion and Conclusion on Fabrication

During the whole process flow, the EB writing process is the most fundamental and important one, since it decides the shape and quality of all the waveguide parts. The quality of coated resists, which determined by the condition of spincoating, bake time and resist itself, had better to be checked with microscope after each of them is finished. Dose count should not be smaller than 100μc/cm^2, otherwise cannot get sufficient exposure. The development time, in general, is about 1min, but sometimes 2mins are required.

For the dry etching, it is important to control the gas flow to ensure the verticality and roughness of the waveguide. As the several trials during experiment, take Si etching as an example, it seems that the more Cl_2 gas flow, the waveguide tends to more like inverted-trapezoid; On the contrary, less gas flow leads to closer as trapezoid. And

another point is that since the etching mechanism is based on selectivity for different materials, it is necessary to make sure thickness of mask is enough for sufficient etching requirement.

As to the photolithography and metal deposition, it mainly depends on the operation by the users. The process requires accurate alignment within several micrometers, which is not easy to be achieved due to the limitation of machine and users deviation. Thus, enough offset should be considered when we design the pattern of the device.

Moreover, compared with previous design, we employed different metal layer for heater and electrode. Only 100nm thick Titanium is deposited as heater, which provides higher resistance than Titanium covered with Au structure. As a result, it helps reduce the required applying power on each phase shifters to get the same performance.

The final fabricated device is shown in Fig. 4.3 and Fig. 4.4.

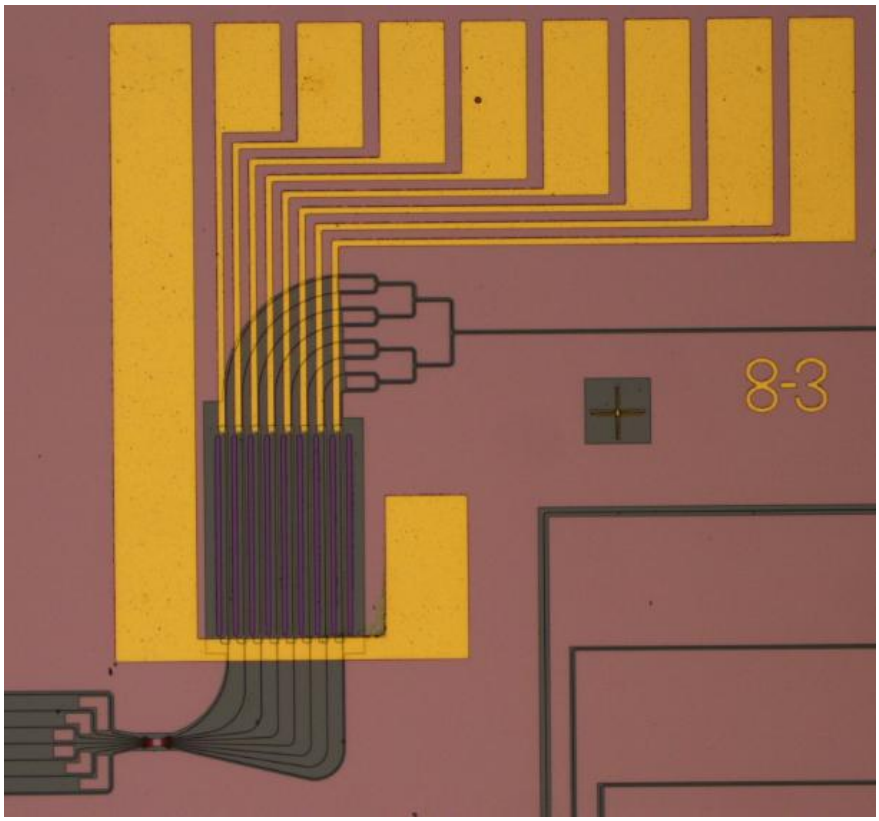


Figure 4.3: photo of Final device

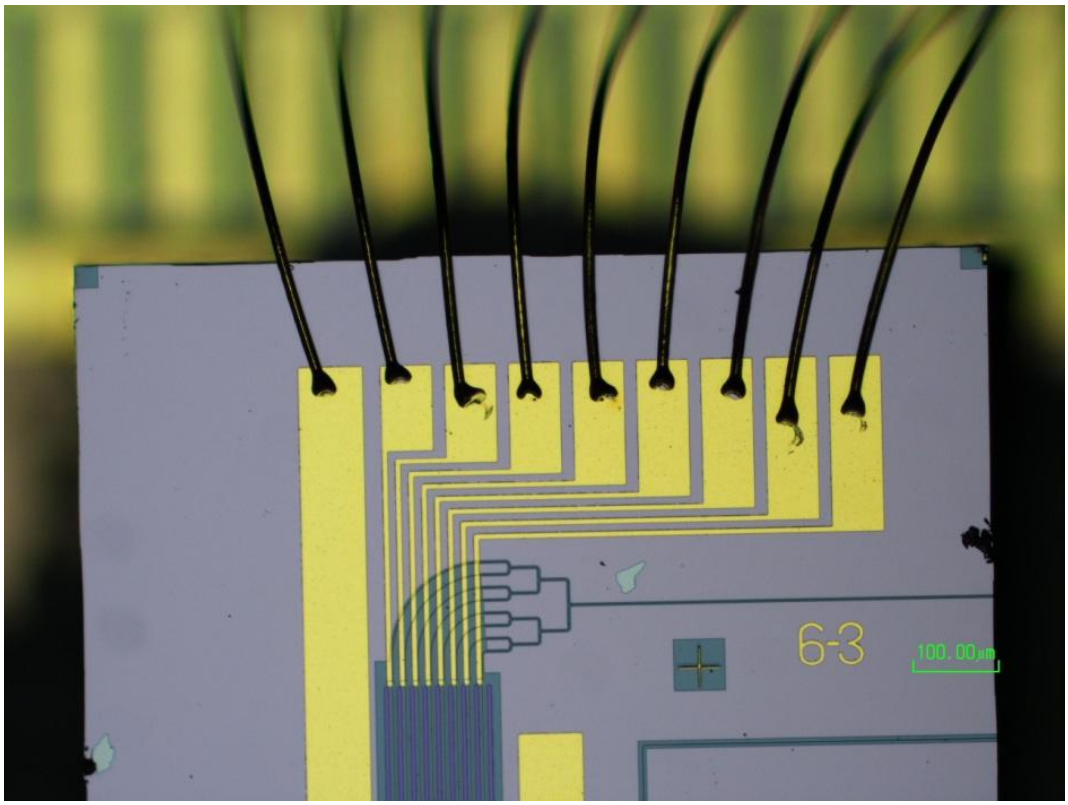


Figure 4.4: Photo of final device after wire bonding

Chapter 5

Measurement and Evaluation of Device

In the previous chapter, we have finished fabricated 1×7 Nyquist-sampling optical phased-array silicon switch. In this chapter, characteristic of the device is presented and discussed. First, the waveguide performance including propagation loss and coupling loss is evaluated. Then the phase shifters are measured with I/V curve and working condition. At last, with proper applied voltage for each switching condition, the performance of switching is evaluated.

5.1 Evaluation of Si waveguide

Fig. 5.1.1 shows the experiment setup for optical and optoelectronic measurements. A tunable laser emitting around the wavelength of 1550 nm was used as the light source. A variable optical attenuator (VOA) was used to control the optical power at the input. The polarization state of light at the input of the chip was controlled by using a polarization controller. The light was transmitted between these components via single mode fibers (SMF). The light was coupled to and from the chip by end-coupling to the cleaved waveguide facets. To obtain a lower coupling loss, a special fiber with a lens attached at the tip (lensed fiber) was employed. The fibers were maintained a focal distance away from the facets.

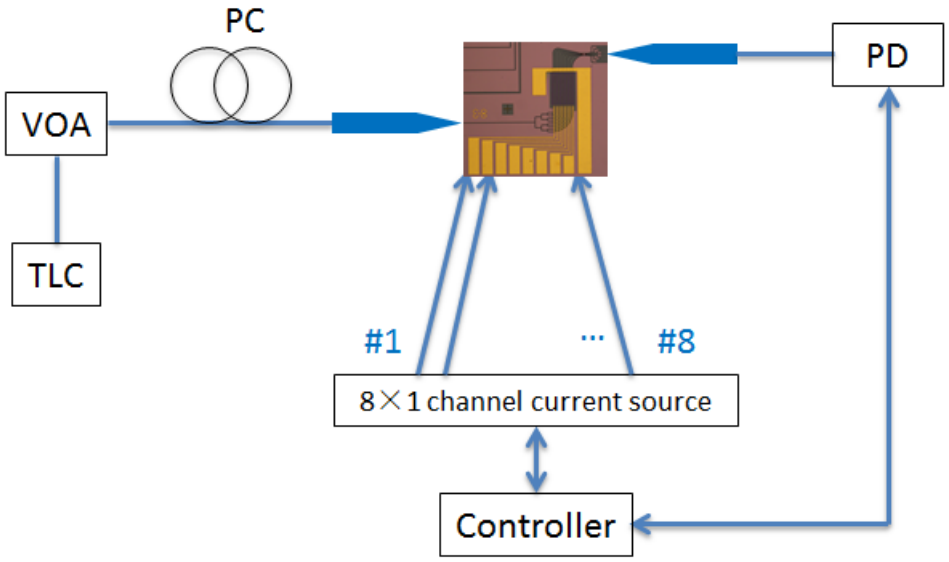


Figure 5.1.1: Optical measurement system of 1×7 switch.
TLC: tunable laser controller, VOA: variable optical attenuator,
PC: polarization controller, PD: photodetector

Fig.5.1.2 shows the dependence of propagation loss in different length dummy waveguides. The propagation loss is about 5.25dB/mm, coupling loss is 13.5dB.

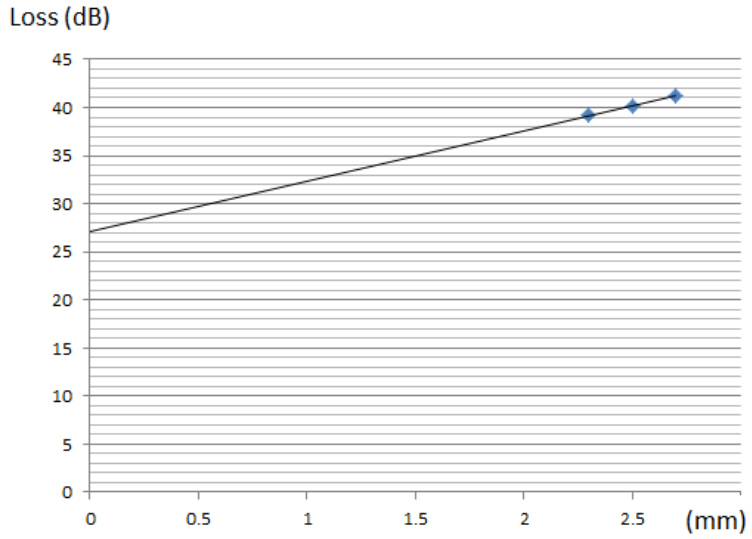


Fig. 5.1.2: Dependence of loss on different waveguide length

5.2 Evaluation of Heater

The characteristic of heater plays an important role for the final performance, since it determines the phase control by thermo-optics. Here the measurement of heater resistance is presented. Fig. 5.2 shows the I/V curve of phase shifter #7.

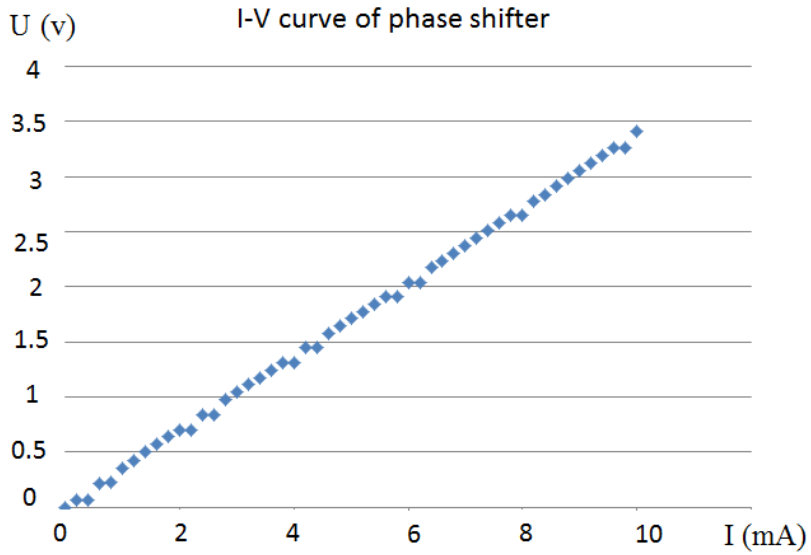


Figure 5.2: I-V curve of phase shifter

Since in our design we employed only 100nm thick Titanium as heater, the resistance is about 350Ω，which is larger than the previous design. Thus, we could get the 2π-phase modulation with lower applied power.

5.3 Characteristic of switching

First of all, in order to measure the switching performance, it is necessary to achieve the most appropriate condition of phase shifters for each port respectively. Fig. 5.3.1 shows the measurement strategy.

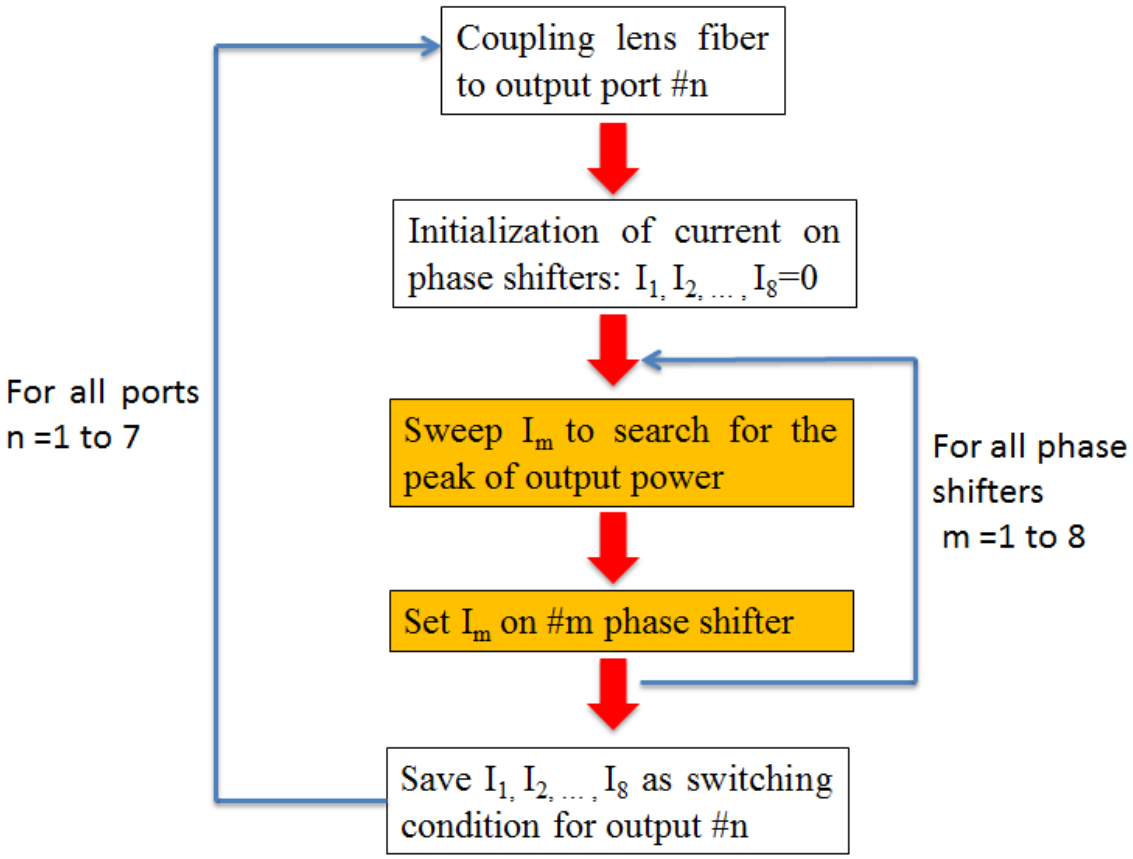


Figure 5.3.1: Algorithm for optimization for switching conditions of 1×7 Nyquist-sampling phased-array switch with number of array 8

As shown in the Fig. 5.3.1, we set each output port to the lens fiber to search for the condition respectively. For each port, the sweep current increases from 0 to find the peak of output power and set corresponding current I_m to each phase shifters. Then save all the I_m as the switching condition for certain port. At last, we could get the switching conditions for all the output ports. Fig. 5.3.2 shows an example of searching I_2 for output port #7.

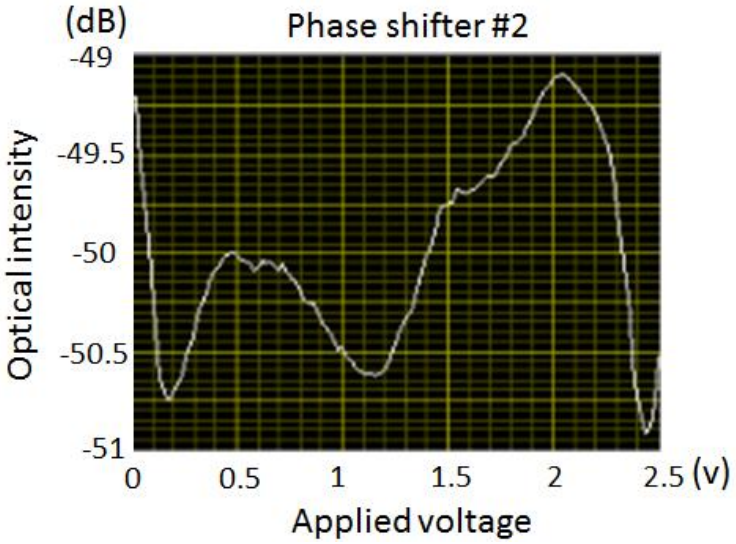


Figure 5.3.2

By scanning applied voltage within 2.5V, 2π-phase modulation was achieved with power consumption 17.9mW.

5.4 Conclusion

Several passive device characteristic and heater condition has been measured and presented.

The propagation loss is bit large. It may cause by the etching condition. Further measurement should be finished to make sure the reason.

Compared with Ti/Au structure heater, only Ti layer provides larger resistance and reduces the applied power for 2π-modulation within 2.5V and power consumption about 17.9mW.

However, the extinction ratio of all the ports still needs to be measure, which is not finished yet. Also, the dynamic characteristic of switch could be obtained at the same time.

Chapter 6

Conclusion

Large-scale integrated optical switches with broad optical bandwidth and high extinction ratio are of particular importance in the future optical-packet switching networks and high-performance computing systems. Among several approaches, we have developed monolithically integrated 1×N Nyquist-sampling phased-array optical switch on silicon platform. Compared with other kinds of switch, our design has advantages in terms of relatively small footprint and broadband operation. Also, we use Nyquist-sampling technique to reduce the number of phase shifters to achieve high extinction ratio, which is a great improvement from previous phased-array optical switch.

The analytical simulation on the performance of Nyquist-sampling phased array switch has been presented including comparison with previous design, ER dependence on output pitch and star coupler length, and possibility for large scalability with limited M/N ratio.

We have successfully fabricated out 1×7 Nyquist-sampling phased-array optical switch on SOI substrate. The fabrication condition and result have been discussed and demonstrated. From the observation, each part of the device, especially the smallest bending radius and star coupler, has been confirmed to be fine. Although some of the process conditions are strict due to the small dimension of the device, we have utilized varieties of methods to overcome all of them.

For the measurement, since the tight schedule, only some passive characteristic of device and phase shifters controlling are presented. Further measurement on extinction ratio and dynamic characteristic are required to be finished. So far, the measurement result has fit our design and theoretical analysis, it is promising to have sufficient data to support our idea.

In the future, the possibility of N×N Nyquist-sampling phased-array switch on Si platform requires to be investigated. The high performance of integrated optical switch on Si will actually contribute a lot to the future data communication. Thus, it is really promising the further the research on this novel design.

List of publication

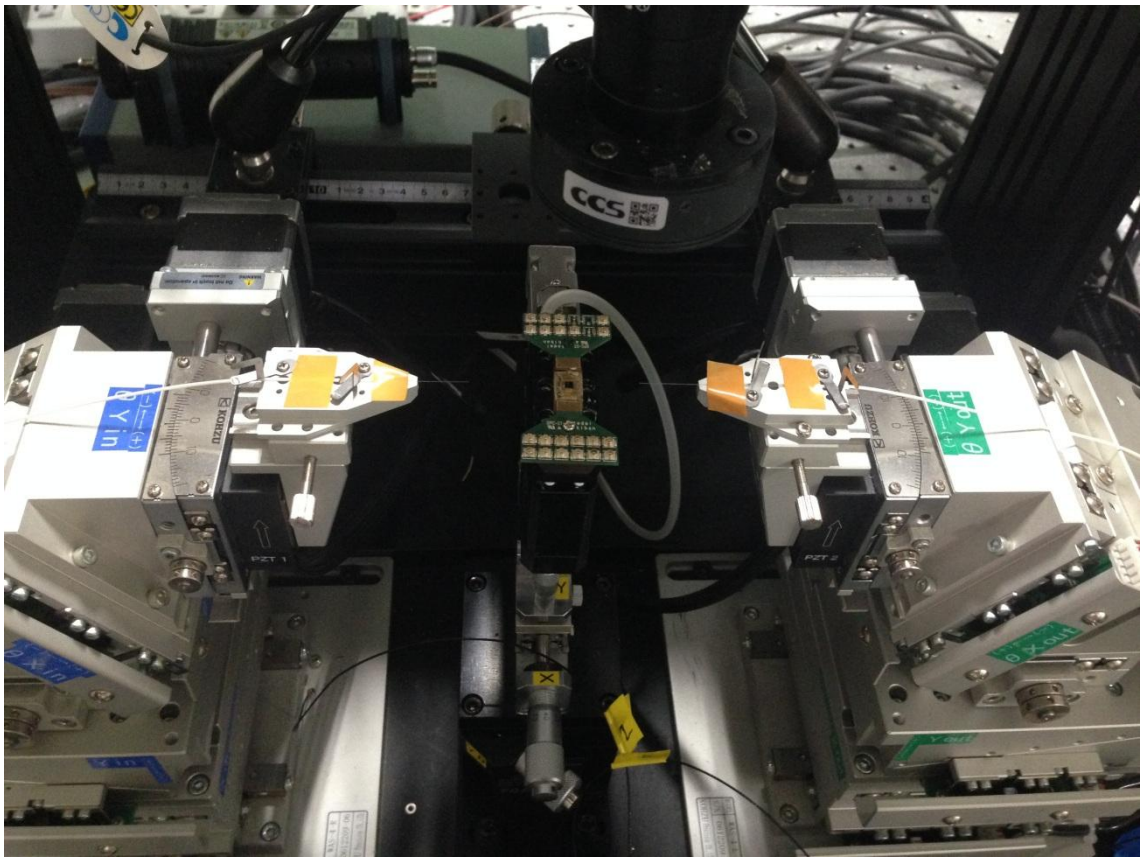
[1] Ming Cui, Takuo Tanemura, and Yoshiaki Nakano, “1×N Nyquist-sampling Phased-Array Switch for Extinction Ratio Improvement,” IEICE, 2014 Sep (Accepted)

Appendix

1. Equipment used in the experiment

EB writer: ADVANTEST F5112　(VDEC)
　　CRESTEC CABL-9200TFTN
Spin coater: MIKASA 1H-D7
Dry etcher: ANELVA L-201D
Photolithography: Karl Suss MJB3
EB evaporator (Au/Ti): ULVAC UEP-2000
Sputter（SiO2）: ULVAC MNS-2000RF
8×2 Channel current source: ILX Lightwave LDC-3908
Laser source: Agilent 8163B
Wave generator: WaveFactory WF 1966 2CH
Oscilloscope: Tektronix DPO4104

2. Measurement setup



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