論文の内容の要旨

Integrated Optical Matrix Switches and Buffers Based on InP Phased-Array Technology

（InPフェーズドアレイ技術による
集積光マトリクススイッチと光バッファに関する研究）

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During the past few years, many new applications of Internet have been developed, such as cloud computing, social networking, and video streaming. In order to provide cloud-based for data-intensive services warehouse scale datacenters (DCs), which consists of over 100,000 servers, are being built across the world. In these DCs, servers arranged in each rack are first connected to the top-of-rack (TOR) switch and this is then uplinked to the cluster switches to provide interconnection between the racks. With the increasing data-rate of the aggregated signal inside these cluster switches, the existing electronic packet switches are facing more and more challenges in terms of power consumption and latency for the intra-DC network. Furthermore, this bottleneck is likely to be extended into the inter-DC network in the foreseeable future. Multiple DCs communicate through the public networks to perform periodic data mirroring and backup. This means that the public network has to share the network resources and has to reconcile huge inter-DC traffic demands, on top of the yearly increased total data traffic growth. To distribute and process the large amounts of data across the entire public network, the energy consumption at the core routers is also becoming the bottleneck in scaling up the data capacity. These significant increments of data flows demand the implementation of larger bandwidth and lower latency communication network with lower power consumption.

Optical interconnection has been spotlighted as a key technology to overcoming the bottleneck of the communication bandwidth and power consumption over for the several decades. It has been deployed in not only long-range communication at the public communication network, but also short-range communication such as interconnecting between server racks in DCs. However, the data switching at cores and clusters are still being transferred by electrical packet switches, which need several optical/electronical/optical (O/E/O) conversions.

Optical switching technologies have potential that can significantly reduce the power consumption and solve thermal dissipation problems on switching elements by electing the O/E/O conversion. Several hybrid electrical/optical switch architectures for intra-DC network have been proposed and it is presented by micro-electro-mechanical switch (MEMS) based optical circuit switching (OCS) technology. Yet, the relatively slow (10s of ms) reconfiguration time of MEMS based switching cannot accommodate the indeterminate burst traffic of heterogeneous DC applications.

Optical packet switching (OPS) network, on the other hand, can provide ultra-high bandwidth at nanosecond-scale reconfiguration time for various types of traffic. There are two essential components for constructing OPS network. One is a N×N optical matrix switch that distributes the signal by interconnecting between desired ports momently. The other is a variable optical buffer, which is essential to resolve contention and congestion of colliding packets, which are having a same destination port.

In order to substantiate the OPS with ultra-fast switching time, high-speed large-scale optical matrix switches are attracting renewed interest. Several monolithically integrated InP photonic switches have been demonstrated based on different approaches such as semiconductor optical amplifier (SOA)-based gate switches and arrayed waveguide grating (AWG)-based switches. However, those approaches are not suitable to implement all following three criteria, scale up port count (scalable), reduce the latency (strictly non-blocking architecture), and handle high-bit-rate (transparent to various data formats), which are important to improve the throughput of the OPS network. The lack of practical variable optical buffers is also an issue, which has disturbed the implementation of OPS. To achieve the variable optical buffer, a high-speed 1×N optical switch and N delay lines of different length are needed.

This dissertation focuses on defining feasibility of the OPS router, which consists of a high-speed transparent N×N optical switch matrix and a variable optical buffer. A phased-array scheme was adapted as a basic switching principle to form a strictly non-blocking scalable switch design, which can be employed as a large-scale switch matrix and a distributing component of the variable buffer architecture for OPS router.

The world's first novel strictly non-blocking WDM-transparent 8×8 photonic switch is demonstrated, which is monolithically integrated on an InP chip. The switch consists of a central large slab region and phased-array antennas (PAAs) attached on both the input and output sides. Each PAA consists of one star coupler and 12 phase shifters to achieve sufficient beam-steering/collecting performance. By tuning the phase shifters, arbitrary combination of the input and output ports can be dynamically interconnected at the central slab. This scheme offers strictly non-blocking (or wide-sense non-blocking) switching, since each port is controlled independently by the setting of other ports. Moreover, there is no waveguide crossing on the entire device, which should provide a significant advantage over the other schemes in terms of scaling the number of port. With an appropriate design of the array shape, optical path length difference can be minimized to achieve nearly wavelength-insensitive operation across the C-band.

The switch contains 192 phase shifters, 96 waveguides array attached at the each side of the central slab, 16 star couplers, and a number of other passive waveguides. The complete matrix switch, including the bonding electrode pads, fits in a footprint of 14.3 × 7.2 mm^2. The entire chip has an identical epitaxial structure of p-i-n InP/InGaAsP heterojunction. The guiding layer is 500-nm-thick undoped bulk InGaAsP, having a photoluminescence peak at 1.37-μm wavelengths to maximize the phase-shifter efficiency. Owing to the all-passive waveguide structure, the switch could be fabricated by a simple, low-cost and regrowth-free dry-etching device process.

The static switching experiment have done successfully with randomly selected several input and output ports. For all the ON-state switching cases, wavelength-dependent loss is kept within ±1.5 dB in the entire C-band (1530-1570 nm). At 1550 nm, we have obtained the extinction ratio of more than 25 dB (34 dB in the best case) and the on chip loss of around 28 dB (include the propagation loss of 18 dB/cm) that can be improved by at least 14.5 dB with an improved fabrication process. Dynamic operation switching was also demonstrated with reconfiguration time of less than 4.2 ns, which include the response time of the driver circuit.

The modulation format independence on wavelength division multiplexing (WDM) is very important to provide high-bit-rate throughput. Furthermore, it has been pointed out that the future DC networks would most likely employ commodity network interface cards with WDM (e.g., 10G×n) optical interfaces. To evaluate the WDM data format transparence of the InP phased-array 8×8 switch, error-free forwarding of 40-Gbps (10-Gbps×4Ch) WDM signal was demonstrated successfully with <2-dB power penalty.

We also have achieved the hybrid variable optical buffer module for intra-packet synchronization. Optical buffering has been one of the major technical challenges in realizing optical packet switching routers and interconnects. We have demonstrated a compact optical buffer module, comprising an InP 1×8 phased-array switch and a silica-based delay line circuit. The integrated delay line circuit is fabricated on the silica-based planar-lightwave circuit (PLC) platform, and has the ladder architecture for reducing the size. In addition, variable optical couplers (VOCs) are integrated to achieve effective power equalization. By using VOCs, we have effectively suppressed the power deviation within 1.2 dB without inducing noticeable excess losses. Tunable and uniform buffering of up to 21 ns is obtained with 3-ns temporal resolution.

In summary, this thesis comprises results of the research about high-speed large-capacity optical matrix switches and compact tunable optical buffers, demonstrated by experimental and theoretical approach. Especially the phased-array scheme has been focused as a key technology for realizing great switching properties required overcoming the current drawbacks. Although there exist several technical issues, which have prospect for the solution, this study confirms that scalable phased-array matrix switches and hybrid variable buffers have potential to implement the future OPS networks.