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Fabrication of SiO_2/4H-SiC (0001) interface with nearly ideal capacitance-voltage characteristics by thermal oxidation

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We fabricated SiO_2/4H-SiC (0001) metal-oxide-semiconductor capacitors with nearly ideal capacitance-voltage characteristics, simply by the control of thermal oxidation conditions which were selected based on thermodynamic and kinetic considerations of SiC oxidation. The interface with low interface defect state density $<10^{11}\,cm^{-2}\,eV^{-1}$ for the energy range of 0.1–0.4 eV below the conduction band of SiC was obtained by thermal oxidation at 1300 °C in a ramp-heating furnace with a short rise/fall time, followed by low temperature O_2 anneal at 800 °C.
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Silicon carbide (SiC) has attractive properties, such as high breakdown-field and high thermal conductivity, which are suitable for high-voltage power electronic devices with high energy-efficiency.[1,2] In addition, its ability to grow SiO_2 by thermal oxidation is one of the unique advantages of SiC over other wide-gap semiconductors. Among the typical polytypes of SiC (3C, 4H, and 6H), 4H-SiC is the most suitable polytype for electronic applications. However, thermal oxidation of SiC has been believed to induce significant amount of both interface defects[3] and near-interface traps,[4] which limit the inversion channel mobility of SiC metal-oxide-semiconductor (MOS) field effect transistors, as well as the performance reliability. For 6H-SiC surfaces, wet oxidation has been reported to suppress the formation of those defects, and the interface state density (D_{it}) is suppressed to $10^{11}\,cm^{-2}eV^{-1}$.[5,6] In contrast it does not work efficiently for 4H-SiC,[7,8] which is the most extensively investigated polytype of SiC, even though some reports indicate that pyrogenic oxidation improves the interface of 4H-SiC $(000\bar{1})$[9] For the reduction of the effects of those interface defects on 4H-SiC, various passivation techniques including annealing in NO.[10,11] and H_2[9,12] have been investigated. Among those techniques, $POCl_3$ treatment has been reported to work most effectively to D_{it},[11] though it does not contribute to improve the threshold voltage stability. For further reduction of D_{it}, we consider it is crucial to employ oxidation conditions suitable for the elimination of carbon-related byproducts from the interface because the carbon residues are the most possible origin of those defects on 4H-SiC.[3,4] In this study, we demonstrate the formation of SiO_2/4H-SiC (0001) interface with D_{it} less than $10^{11}\,cm^{-2}eV^{-1}$, simply by the control of thermal oxidation conditions without using those passivation techniques.

Thermal oxidation kinetics of SiC has been discussed by the modified Deal-Grove model,[13] where the generation and transport of CO are taken into account, in addition to the transport and consumption of O_2 at the interface of SiO_2/SiC. In this model, the overall reaction is expressed as

$$SiC + \frac{3}{2}O_2 \rightarrow SiO_2 + CO\uparrow. \quad (1)$$

This simple consideration tells us that the oxidation conditions to enhance an immediate out-diffusion of CO from the SiO_2/SiC interface are inevitably important. From the kinetic viewpoint, it would be better to limit the oxide thickness to enhance CO out-diffusion. We have already reported that the thickness region ~15 nm is thin enough for the interface-reaction-limited growth for the dry oxidation at 1100–1300 °C on 4H-SiC (0001).[14] In addition, from the thermodynamic viewpoint, we also need to select the oxidation temperature and the O_2 partial pressure (pO_2) suitable for the enhancement of CO ejection. For the interface-reaction-limited growth, it is reasonable to consider that the interface is in non-equilibrium state where the gaseous products are immediately removed away from the interface. Then, the reaction with the most negative free energy change (ΔG) would be dominant among the possible reactions between SiC and O_2.[15] For the ideal case, where the reaction described by Eq. (1) occurs in one step, the SiO_2 formation is accompanied with the direct formation of CO molecule from SiC. It is noticed that such reaction is predicted to give the most negative ΔG only in the limited range of temperature for a given pO_2. This is because carbon precipitation ($SiC + O_2 \rightarrow SiO_2 + C$) will be thermodynamically favored for low temperature region, whereas active oxidation ($SiC + O_2 \rightarrow SiO + CO$) will be dominant for high temperature region.[15] Taking into account the solubility limit of O_2 in SiO_2, $\sim 2.5 \times 10^{16}\,cm^{-3}$[16] for 1-atm O_2 at around 1200 °C, one may assume that the effective pO_2 at SiO_2/SiC interface is calculated to be $\sim 5 \times 10^2$ Pa for a oxidation in 1-atm pO_2 ambient. Then the temperature window for the ideal reaction in 1-atm O_2 is approximately estimated to be 1100 – 1400 °C. Actually, we have observed a high activation energy (~3.8 eV) of 4H-SiC (0001) oxidation at 1100 – 1300 °C in 1-atm O_2,[14] which is in good agreement

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with the calculated energy barrier for the direct CO ejection from the interface via carbonyl structure.[17]

4H-SiC (0001), Si face, wafers with $\sim 1 \times 10^{16}\,\mathrm{cm}^{-3}$ doped n-type epitaxial layers were cleaned in diluted HF, followed by the oxidation at 1100 and 1300 °C in 1-atm dry O_2 with the ramp-heating furnace. A short rise/fall time (>600 °C/min) was employed to minimize the unwanted additional oxidation at lower temperature where the carbon precipitation would be more pronounced. After the growth, some films were annealed additionally at 800 °C in O_2 for 30 min aiming for the reduction of interface defects. Such post-oxidation annealing (POA) in O_2 has been reported to work efficiently for the elimination of carbon residues and/or the annihilation of oxygen vacancies.[5] Note that 800 °C is sufficiently low temperature to neglect the additional growth of oxide in 30 min, which does not contribute to the interface deterioration by the oxidation at non-ideal temperature. The POA at high temperature in inert gas has been employed in some reports;[6,8,18] however, we avoided such POA conditions to suppress the possible formation of oxygen vacancies. This is because the window for the thermodynamically ideal reaction moves to lower temperature for lower pO_2, as is concluded from thermodynamic consideration.[15] The back-contact was formed by Ni evaporation followed by post-metallization anneal in N_2. Finally, Au electrodes were deposited as top-contact to form the MOS capacitors.

The bidirectional capacitance-voltage (C-V) characteristics measured with various frequencies from 1 kHz to 1 MHz are shown in Fig. 1 for the MOS capacitor fabricated with oxidation at 1300 °C and POA at 800 °C. The oxide thickness was determined to be ~14 nm by grazing incidence x-ray reflectivity. Not only the hysteresis but also the frequency dispersion of the C-V curves are well suppressed except for the depletion region where the effects of interface states appear slightly. The ideal C-V curve, calculated from Poisson's equation, is also shown in Fig. 1 as a broken line. For the calculation of the ideal curve, the oxide thickness, the doping density of substrate, and the flatband voltage (V_{FB}) were set to 13.5 nm, $1.5 \times 10^{16}\,\mathrm{cm}^{-3}$, and 1.7 V, respectively. Note that the ideal curve agrees well with the experimental high-frequency one at 1 MHz, which indicates the formation of interface with low density of interface defects. Especially, the good coincidence in accumulation region clearly shows that the effects of near-interface traps, which have been observed frequently in SiC MOS devices,[10,19,20] are well suppressed.

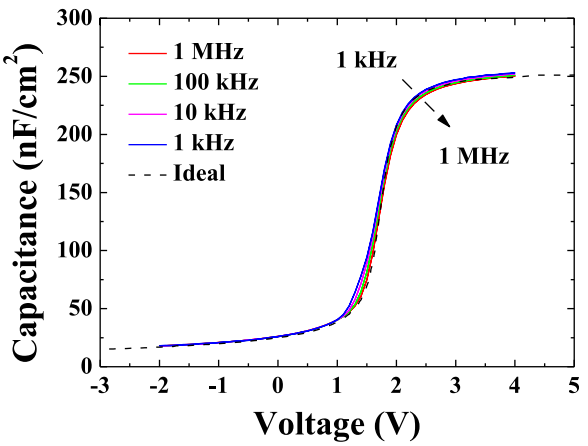

FIG. 1. Bidirectional C-V characteristics of the MOS capacitor ($T_{ox} \sim 14$ nm) fabricated by 1300 °C oxidation followed by POA at 800 °C in O_2. Measurement was conducted at various frequencies from 1 kHz to 1 MHz. Broken line shows the ideal C-V curve calculated by Poisson's equation.

The D_{it} values were estimated by the conductance method[21] assuming the equivalent circuit shown in Fig. 2(a). C_{ox} is the capacitances of gate oxide. G_p and C_P are the conductance and capacitance of SiC, respectively. Since the maximum value of G_p/ω, which was determined in the frequency range from 20 Hz to 2 MHz in our experimental condition, is directly related to the capacitance of interface traps, D_{it} is approximated as the following relationship:

$$D_{it} \cong \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max}, \tag{2}$$

where q and ω are the elementary charge and the angular frequency, respectively. Note that this method is quantitatively more accurate and reliable, as long as the MOS capacitors have nearly ideal C-V characteristics, than the high-low frequency method which is often employed in the analysis of SiC MOS capacitors.[10,11]

Before applying the conductance method, we determined series resistance (R_s) by the extrapolation of high-frequency limit of the real part of impedance measured in accumulation region. Then, R_s was removed from the measured impedance. The typical results of frequency dependence

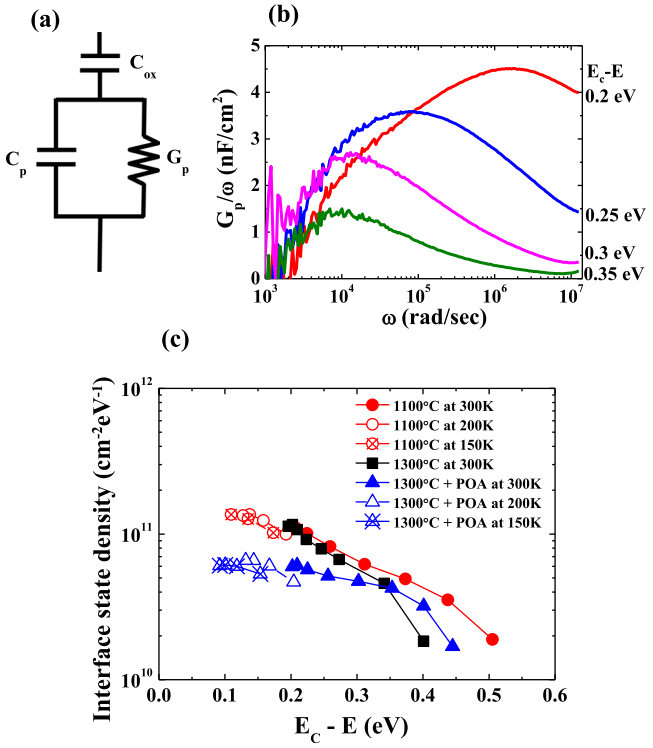

FIG. 2. (a) Equivalent circuit of MOS capacitors for conductance method. (b) Frequency dependence of G_p/ω measured at room temperature for the MOS capacitor fabricated by 1300 °C oxidation followed by POA at 800 °C in O_2. (c) Interface defect state density as a function of energy level below the conduction band, estimated from the peak values of G_p/ω measured at various temperatures from 150 – 300 K. The oxides grown at 1100 °C, 1300 °C, and 1300 °C + POA at 800 °C in O_2 are compared.

of G_p/ω are shown in Fig. 2(b). From the peaks, D_{it} values were determined at each gate voltage, and shown in Fig. 2(c) as a function of energy level with reference to the conduction band edge of SiC. The measurements were done not only at room temperature but also at 150 and 200 K to extend the energy range of the characterization toward the conduction band edge of SiC. As a result, for all the samples, we observed interface state density as low as $\sim 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ or less, which are lower than the reported values of as-oxidized films on 4H-SiC (0001).[20,22] In previous reports, it has been indicated that, for as-oxidized films on 4H-SiC(0001), D_{it} increases sharply to the values ranging from 10^{12} to $10^{13}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ near the conduction band edge.[20] We believe such significant improvement is attributable to the two factors: the limited oxide thickness to assure the removal of CO accumulation, and the oxidation with ramp-heating furnace which suppresses the unwanted low-temperature oxidation of the interface. Both 1100 °C- and 1300 °C-oxidized interfaces show $\sim 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ or less for the energy range of 0.1–0.4 eV below the conduction band edge of SiC. For 1300 °C oxidation, slightly lower D_{it} is suggested than that of 1100 °C oxidation for deep energy region. We speculate this might come from the fact that 1100 °C is closer to the lower limit of the temperature range for thermodynamically ideal reaction.

It should be noted that the best results were demonstrated by the oxidation at 1300 °C followed by the low-temperature POA at 800 °C in O_2 where $D_{it} < 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ was attained even 0.1 eV below the conduction band edge of SiC. This POA temperature is sufficiently low to neglect the additional oxidation of SiC at the interface, but expected to annihilate the defects at the interface or in the near-interface oxide. The oxidation temperature of 1300 °C is high enough to avoid the unwanted low-temperature mode as discussed above. On the other hand, oxidation at such a high temperature possibly induces oxygen vacancies, since it is suggested from the thermodynamic consideration that the generation of SiO would be enhanced at 1300 °C, which is close to the higher limit of the temperature range for the ideal reaction. Therefore, we speculate that the improvement by the low-temperature POA in O_2 should be mainly attributed to the annihilation of oxygen vacancies induced by high-temperature oxidation. The observed D_{it} after POA is even less than the best reported ones with NO- or P-passivated interfaces,[10,11] especially for the shallow energy levels which have influences on n-channel field effect transistor operations. These results indicate that appropriate selection of oxidation conditions is more effective for the reduction of D_{it} compared with the conventional passivation process employing NO. Further reduction of D_{it} would be expected by combining our process with those passivation techniques. It is reported that defects with very fast time constant were observed for SiC MOS capacitors, which are detected by the measurements at as high-frequency as 100 MHz and low temperature conductance method.[20,23] However, our samples did not show any additional peaks in our measurement range even at 150 K where the time constant is expected to become more than three orders longer than 300 K. This fact shows that there is no additional components called "very fast states"[23] in our samples. From these results, we can conclude that one of the best way to reduce the interface defect state density at SiO_2/4H-SiC (0001) is to control the thermal oxidation conditions.

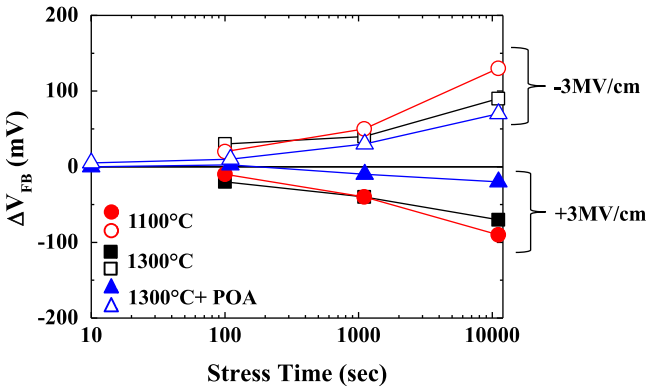

FIG. 3. Flatband voltage shifts of C-V curves of MOS capacitors by the application of constant electrical stress ±3 MV/cm at room temperature for 10^4 s.

The fact that $D_{it} < 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ is achievable simply by the thermal oxidation even without any passivation techniques, indicates that SiO_2/4H-SiC (0001) system is potentially favorable to form the interface with less dangling bonds. In general abrupt change of atomic arrangement induces significant strains at the oxide-semiconductor interfaces, which is one of the intrinsic driving forces to generate the interface defects. We have reported that near-interface structure of thermally grown oxides on 4H-SiC (0001), Si face, is less strained than that on $(000\bar{1})$, C face,[24] and even less than those on Si (001).[25,26] We believe that this advantage of 4H-SiC (0001) would be one of the reasons why only low density of interface state defects are intrinsically introduced at this interface.

Last but not least, the stability of V_{FB} against the electrical stress was investigated at room temperature. The constant voltage stress ±3 MV/cm was applied repeatedly and shift of V_{FB} was observed. The leakage current levels of the three samples were almost identical and less than $\sim 10^{-6}$ A/cm^2 for +3 MV/cm stress. They did not change significantly throughout the stress test. As shown in Fig. 3, it was found that POA at 800 °C was quite effective to suppress the stress-induced V_{FB} shift, which was well below 100 mV after 10^4 second stress. This shift is not so small but comparable to the typically reported results of well-passivated 4H-SiC MOS devices.[27] Our results seem to have the rooms for further improvement by optimization of POA conditions.

In conclusion, we demonstrated nearly ideal C-V characteristics for SiO_2/4H-SiC (0001) MOS capacitors, simply by the control of thermal oxidation conditions. The low interface defect state density, $<10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ for the energy range of 0.1–0.4 eV below the conduction band edge of SiC, was observed for the interface fabricated by thermal oxidation at 1300 °C, followed by POA at 800 °C. These results indicate that the interface with low interface defect density is achievable for 4H-SiC (0001) simply by thermal oxidation.

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