論文内容の要旨

論文題目　**Development of high electric field effect devices by using ultrathin oxide nanosheet**

（酸化物ナノシート超薄膜を用いた高電界効果素子の開発）

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1. Introduction

Carrier doping to semiconductors or insulators with the application of electric field by means of field effect transistor (FET) has been intensively studied to induce or modify various functionalities,[1] such as superconductivity[2] and room-temperature ferromagnetism.[3] In principle, FET is composed of trilayer structure, gate electrode/gate insulator/semiconductor. To apply a higher electric field for modulating a larger amount of carrier, a thinner gate insulator with high voltage endurance is required. However, thin gate insulators made of typical dielectric materials such as SiO_2 and high-k oxides often result in considerable leakage current[5] and/or reduced dielectric constant.[6]

Recently, several kinds of dielectric oxide nanosheets with the thicknesses of only about 1 nm and the lateral sizes of about several μm have been synthesized by exfoliating single crystals of a layered oxide.[4] It was reported that multi-layered densely packed dielectric oxide nanosheets maintained a large relative dielectric constant (ε_r) higher than 100 and a leakage current density lower than 10^{-7} A/cm^2 at a gate voltage of 1 V. Thus, these dielectric oxide nanosheets are promising materials as the gate insulators of FETs.

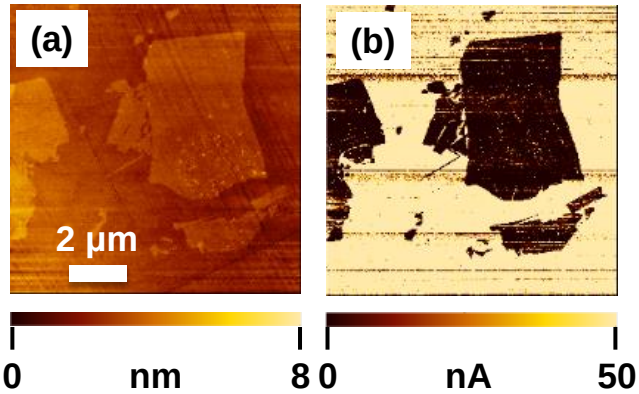

Figure 1. (a) Topological and (b) current images of a single $Ti_{0.87}O_2^{0.52-}$ dielectric nanosheet.

2. Experimental

The ultimate gate insulator is a single dielectric oxide nanosheet because the application of a small gate voltage will produce high electric field, leading to a large amount of carrier modulation, in principle. Thus, the dielectric and insulating properties of a single nanosheet are of strong interest.

[Observation of insulating property of a single nanosheet]

The insulating property of the single nanosheet was confirmed by current image mapping of the tip of atomic force microscope (AFM) / a single nanosheet / a conductive substrate geometry (Figure 1). However, in this geometry, the quantitative evaluation of insulating and dielectric properties is quite difficult because the electric field distribution is completely different from that of a planar capacitor in a practical device. Therefore, it is necessary to evaluate a single nanosheet as an insulator in a well-defined planar capacitor structure with sufficiently small electrodes.

[Capacitor with a single nanosheet insulator]

Au / a single $Ti_{0.87}O_2^{0.52-}$ nanosheet / Au planar micro-capacitors on an insulating $SrTiO_3$ (001) single crystal surface were fabricated in a clean room. Bottom electrodes were fabricated by electron beam lithography, electron beam evaporation, and lift off method. $Ti_{0.87}O_2^{0.52-}$ nanosheets were deposited on the bottom electrodes. Top electrodes were fabricated in the same manner as bottom electrodes. Figure 2(a) is the schematic diagram of final capacitor structure. Electrical measurements were performed in an electrically shielded prober system in vacuum (below 10^{-4} Pa) at room temperature.

[Top gate FET with nanosheet gate insulator]

Figure 2(b) shows a top gate FET structure. A $SrTiO_3$ (001) single crystal substrate with an atomically flat surface was used as a semiconductor channel. Ti/Au source and drain electrodes were fabricated by electron beam lithography, electron beam evaporation, and lift off method. The multi-layer films of nanosheets were fabricated by layer-by-layer assembly using the Langmuir-Blodgett (LB) method. Gate electrodes were fabricated in the same manner as bottom electrodes.

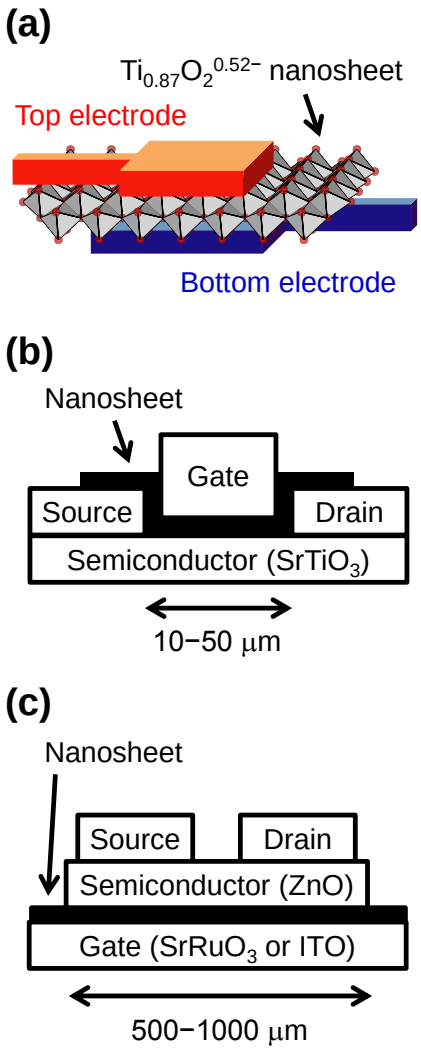

Figure 2. Structure of fabricated devices (a) capacitor (b) top gate FET (c) bottom gate FET.

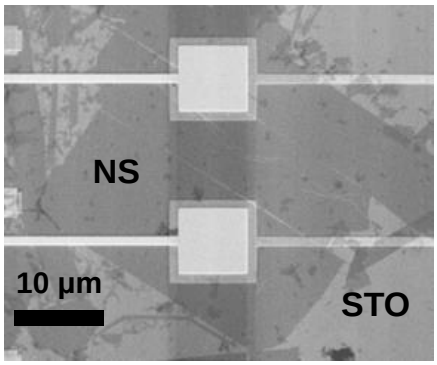

Figure 3. Magnified view of the micro-capacitors. Dark and light gray areas, except the electrodes, correspond to $Ti_{0.87}O_2^{0.52-}$ nanosheets (NS) and the $SrTiO_3$ (STO) surface, respectively.

[**Bottom gate FET with nanosheet gate insulator**]

Figure 2(c) shows a bottom gate FET structure. The multi-layer films of nanosheets were fabricated by layer-by-layer assembly using the LB method on atomically flat $SrRuO_3$ or indium-tin-oxide (ITO). On the multi-layer film, ZnO thin film was sputtered, followed by the fabrication of source and drain electrodes of silver paste.

3. Results and discussion

[Capacitor with a single $Ti_{0.87}O_2^{0.52-}$ nanosheet]

The typical size of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet was 10−30 mm in lateral size and 1.1 nm in thickness, from scanning electron microscope (SEM) and AFM measurements. Figure 3 shows an SEM image of fabricated micro-capacitors. Several single $Ti_{0.87}O_2^{0.52-}$ nanosheets were clearly observed as dark contrast. A single nanosheet successfully covered one bottom electrode, forming an insulating layer (lower micro-capacitor in Fig. 3). On the other hand, a single $Ti_{0.87}O_2^{0.52-}$ nanosheet failed to cover the other bottom electrode, leading to a short circuit between the bottom and top electrodes (upper micro-capacitor in Fig. 3). In this study, five micro-capacitors were successfully formed without any short circuit.

Figure 4 shows capacitance vs. frequency plots measured for these five micro-capacitors. Flat dispersion was observed, as was already reported in multi-layer dielectric nanosheets.[4] However, the ε_r of the single $Ti_{0.87}O_2^{0.52-}$ nanosheets calculated from the capacitance ranged from 2.1 to 2.3, which is much lower than that of the multilayer nanosheets. The formation of a so-called dead layer, the layer with lower ε_r, observed in ordinary dielectric materials might be an implausible explanation for the lower ε_r in the present micro-capacitors because the nanosheet was deposited on the bottom electrode at room temperature. One possible explanation is the presence of an ultrathin air gap between the nanosheet and the bottom electrode. The presence of even a 1 nm-thick air gap would lead to an ε_r value of 2.1, in good agreement with our observations.

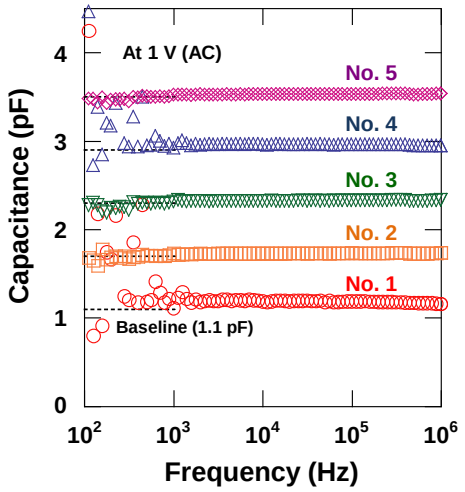

Figure 4. Capacitance vs. frequency curves for five micro-capacitors without short circuits.

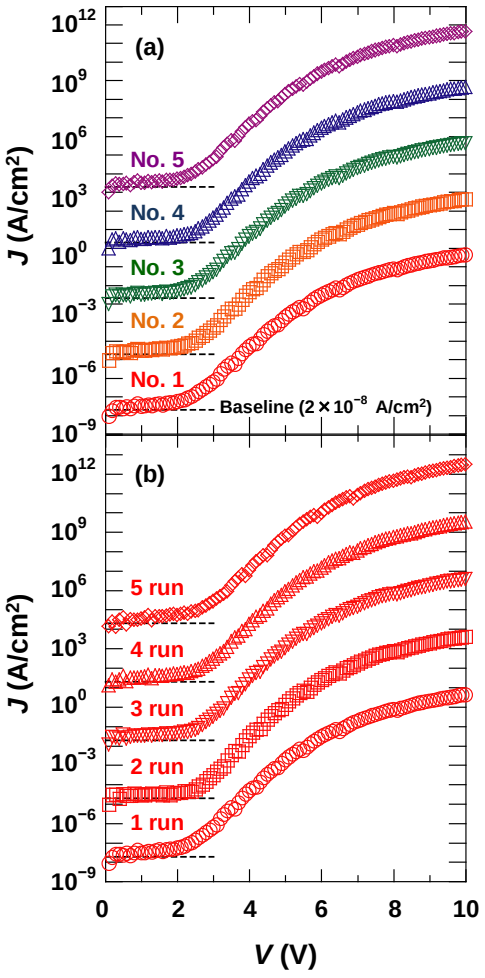

Figure 5. (a) Current density (J) vs. applied voltage (V) curves for the five micro-capacitors. (b) J vs. V curves measured in five runs for one micro-capacitor (No. 1).

Figure 5(a) shows current density (J) vs. voltage (V) curves for the five micro-capacitors. The J–V curves were nearly identical, indicating that the fabricated micro-capacitors showed good device yield once the single nanosheets were properly deposited on the bottom electrodes, as was also seen in Fig. 4. Figure 5(b) shows J–V curves for one nanosheet micro-capacitor (No. 1) measured five times. J-V curves were anearly identical, indicating that the nanosheet was not damaged by dielectric breakdown. In Fig. 5(a) and 5(b), J was almost constant at ~10^{-8} A/cm^2 at V < 2.2 V, whereas it abruptly increased above 2.2 V. At the withstand voltage of the single nanosheet, the electric field strength across the gate insulator corresponds to 20 MV/cm, even assuming that the thickness of the gate insulator was 2.1 nm (= nanosheet 1.1 nm + air gap 1.0 nm). This value is considerably superior to that of a conventional SiO_2 gate insulator, typically 10 MV/cm.[7] The possible reason why the nanosheet shows extremely high electric field endurance is that each single nanosheet is the crystallite, not amorphous like thermally oxidized surface of the silicon. The abrupt increase of J above 2.2 V is attributed to the Fowler-Nordheim tunneling based on the evaluation of the barrier height at the interface between the nanosheet and the electrode.

[FET with dielectric nanosheets as gate insulator]

In both top gate and bottom gate FETs, nanosheets did not provide enough insulation between semiconductor and gate electrode. In top gate FETs, bended nanosheets at the edge of electrode could be an origin of leakage current path. In the case of bottom gate FETs, in contrast, the nanosheets were deposited on the flat surface. However, the gated area had to be much larger than that of top gate structure because of the limitation of fabrication process. The larger area contains large amounts of inter-nanosheet grain boundaries, possibly yielding the leakage current path.

4. Summary

Micro-capacitors and FETs by using dielectric nanosheet as insulator were developed. A single $Ti_{0.87}O_2^{0.52-}$ nanosheet covering the whole of the bottom electrode pad reproducibly worked as an insulator with very high electric field endurance. From the result of AFM observation and micro-capacitors fabrication, it was revealed that a single nanosheet itself is surely insulating. However, until now, FETs with enough insulation between semiconductor channel and gate electrode have not been obtained. Therefore, as future works, proper processes to ensure high insulation should be developed. For example, burying source and drain electrodes into semiconductor, or attaching single crystal of semiconductor with atomically flat surface are a promising way to realize both short length and atomically flat surface of the channel.

References

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