学位論文（要約）

Development of high electric field effect devices by using ultrathin oxide nanosheet

（酸化物ナノシート超薄膜を用いた高電界効果素子の開発）

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申請

東京大学大学院理学系研究科

化学専攻

小川　大輔

Abstract

Carrier doping into semiconductors or insulators with the application of electric field by means of field effect transistor (FET) has been intensively studied to induce or modify various functionalities, such as superconductivity and room-temperature ferromagnetism. In principle, FET is composed of trilayer structure, gate electrode/gate insulator/semiconductor. To apply a higher electric field for modulating a larger amount of carrier, a thinner gate insulator with high voltage endurance is required. However, thin gate insulators made of typical dielectric materials such as SiO_2 often result in considerable leakage current and/or reduced dielectric constant.

Recently, several kinds of dielectric oxide nanosheets with the thicknesses of only about 1 nm and the lateral sizes of about several μm have been synthesized by exfoliating single crystals of a layered oxide. It was reported that multi-layered densely packed dielectric oxide nanosheets maintained a large relative dielectric constant ε_r higher than 100 and a leakage current density lower than 10^{-7} A/cm^2 at a gate voltage of 1 V. Thus, these dielectric oxide nanosheets are promising materials as the gate insulators of FETs. The ultimate gate insulator is a single dielectric oxide nanosheet because the application of a small gate voltage will produce high electric field, leading to a large amount of carrier modulation, in principle. Thus, the dielectric and insulating properties of a single nanosheet are of strong interest.

Conductive atomic force microscopy

The insulating property of the single nanosheet was confirmed by current image mapping of the tip of atomic force microscope (AFM) / a single nanosheet / a conductive substrate geometry. In this geometry, the quantitative evaluation of insulating and dielectric properties is quite difficult because the electric field distribution is completely different from that of a planar capacitor in a practical device. Therefore, it is strongly demanded to evaluate a single nanosheet as an insulator in a well-defined planar capacitor structure with sufficiently small electrodes.

A single $Ti_{0.87}O_2^{0.52-}$ nanosheet obtained from mm-scale single crystal of mother compound was used as the insulator, because it has the largest lateral size among various nanosheets. The typical size of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet was evaluated to be 10−30 mm in lateral size and 1.1 nm in thickness, from scanning electron microscope (SEM) and AFM measurements.

Micro-capacitors

Au / a single $Ti_{0.87}O_2^{0.52-}$ nanosheet / Au planar micro-capacitors were fabricated on an insulating $SrTiO_3$ (001) single crystal substrate with an atomically flat surface. In this study, five micro-capacitors were successfully formed without any short circuit. In capacitance - frequency measurements for these five micro-capacitors, flat dispersion was observed, as was already reported in multi-layer dielectric nanosheets. However, the ε_r of the single $Ti_{0.87}O_2^{0.52-}$ nanosheets calculated from the capacitance ranged from 2.1 to 2.3, which is much lower than that of the multilayer nanosheets. The formation of a so-called dead layer, the layer with lower ε_r, observed

in ordinary dielectric materials might be an implausible explanation for the lower ε_r in the present micro-capacitors because the nanosheet was deposited on the bottom electrode at room temperature. One possible explanation is the presence of an ultrathin air gap between the nanosheet and the bottom electrode. The presence of even a 1 nm-thick air gap would lead to an ε_r value of 2.1, in good agreement with our observations in the present study. In current density - voltage measurement for the five micro-capacitors, the results were nearly identical, indicating that the fabricated micro-capacitors showed good device yield once the single nanosheets were properly deposited on the bottom electrodes. Moreover, five times repeated measurements for one nanosheet micro-capacitor were nearly identical, indicating that the nanosheet was not damaged by dielectric breakdown. Current density was almost constant at ~10^{-8} A/cm^2 at $V < 2.2$ V, whereas it abruptly increased above 2.2 V. At the withstand voltage of the single nanosheet, the electric field strength across the gate insulator corresponds to 20 MV/cm, even assuming that the thickness of the gate insulator was 2.1 nm (= nanosheet 1.1 nm + air gap 1.0 nm). This value is considerably superior to that of a conventional SiO_2 gate insulator, typically 10 MV/cm.

Based on the results that even a single dielectric oxide nanosheet works as good insulator, both top and bottom gate FETs with dielectric oxide nanosheet as insulator were fabricated.

Top gate FETs

A $SrTiO_3$ (001) single crystal substrate with an atomically flat surface was used as a semiconductor channel. Ti/Au source and drain electrodes were fabricated by electron beam lithography, electron beam evaporation, and lift off method. The

multi-layer films of nanosheets were fabricated by layer-by-layer assembly using the Langmuir-Blodgett (LB) method. Gate electrodes were fabricated in the same manner as bottom electrodes.

Bottom gate FETs

The multi-layer films of nanosheets were fabricated by layer-by-layer assembly using the LB method on atomically flat $SrRuO_3$ or indium-tin-oxide (ITO). On the multi-layer film, ZnO thin film was sputtered, followed by the fabrication of source and drain electrodes of silver paste.

In both top gate and bottom gate FETs, nanosheets did not provide enough insulation between semiconductor and gate electrode. In top gate FETs, bended nanosheets at the edge of electrode could be an origin of leakage current path. In the case of bottom gate FETs, in contrast, the nanosheets were deposited on the flat surface. However, the gated area had to be much larger than that of top gate structure because of the limitation of fabrication process. The larger area contains large amounts of inter-nanosheet grain boundaries, possibly yielding the leakage current path.

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Chapter 1

1.1 Carrier doping by field effect transistor

Carrier density is one of the key parameters to govern the electronic and/or magnetic state in solids such as semiconductors. **Figure 1.1** shows several examples of properties of solids as a function of sheet carrier density: (1) organics, fullerenes, and novel compounds; (2) colossal magnetoresistance manganites; (3) high-T_c cuprate superconductors; (4) Nb-doped $SrTiO_3$; (4) single molecule devices; and (5) silicon. It can be clearly seen that the property of solid matters is dependent on carrier density.

To change the carrier density, substitutional or interstitial chemical and/or electrochemical doping into the solids is the most common method (**Figure 1.2**). However, the structural disorders induced by dopants, that are inherent in this method, always cause unnecessary complexity in the physical properties. Accordingly, it's quite difficult to change carrier density without changing other sample parameters by the chemical doping.

On the other hand, carrier modulation (accumulation or depletion) of surface carrier density by electric field in metal–insulator–semiconductor field effect transistor (FET) structure (**Figure 1.3**) is free from the induced structural disorders, thus is attractive method to control properties of materials such as ferromagnetic semiconductors and oxide superconductors by modulating a wide range of carrier density.[1, 2] Semiconductor field effect devices such as metal-oxide-semiconductor field effect transistor (MOSFET) are consisted of source and drain electrodes, a

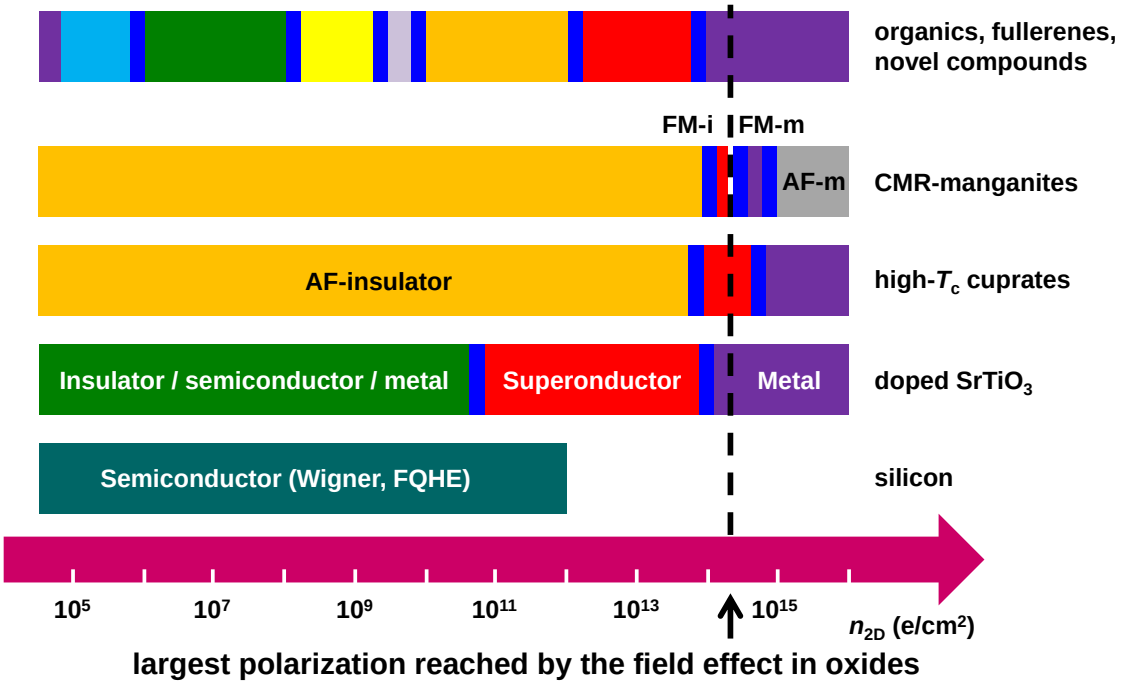

Figure 1.1 Illustration of the zero temperature behavior of various correlated materials as a function of sheet charge density. Silicon is shown as a reference. The examples for high-temperature superconductors and for colossal magnetoresistive manganites reflect $YBa_2Cu_3O_7$ and (La, Sr)MnO_3, respectively. Top bar shows schematically the richness of materials available for field-effect tuning and the spectrum of their phases. AF, FM, I, M, SC, FQHE, and Wigner stand for antiferromagnetic, ferromagnetic, insulator, metal, superconductor, fractional quantum Hall effect, and Wigner crystal, respectively. This figure was drawn according to the ref. 2. [C. H. Ahn et al., *Nature* **424**, 1015, (2003).]

semiconductor channel between them, and a gate electrode that modulates the conductance of the channel.[3] The channel denotes, for example, a thin layer at the surface of a doped semiconductor, a semiconductor thin film, or a two-dimensional

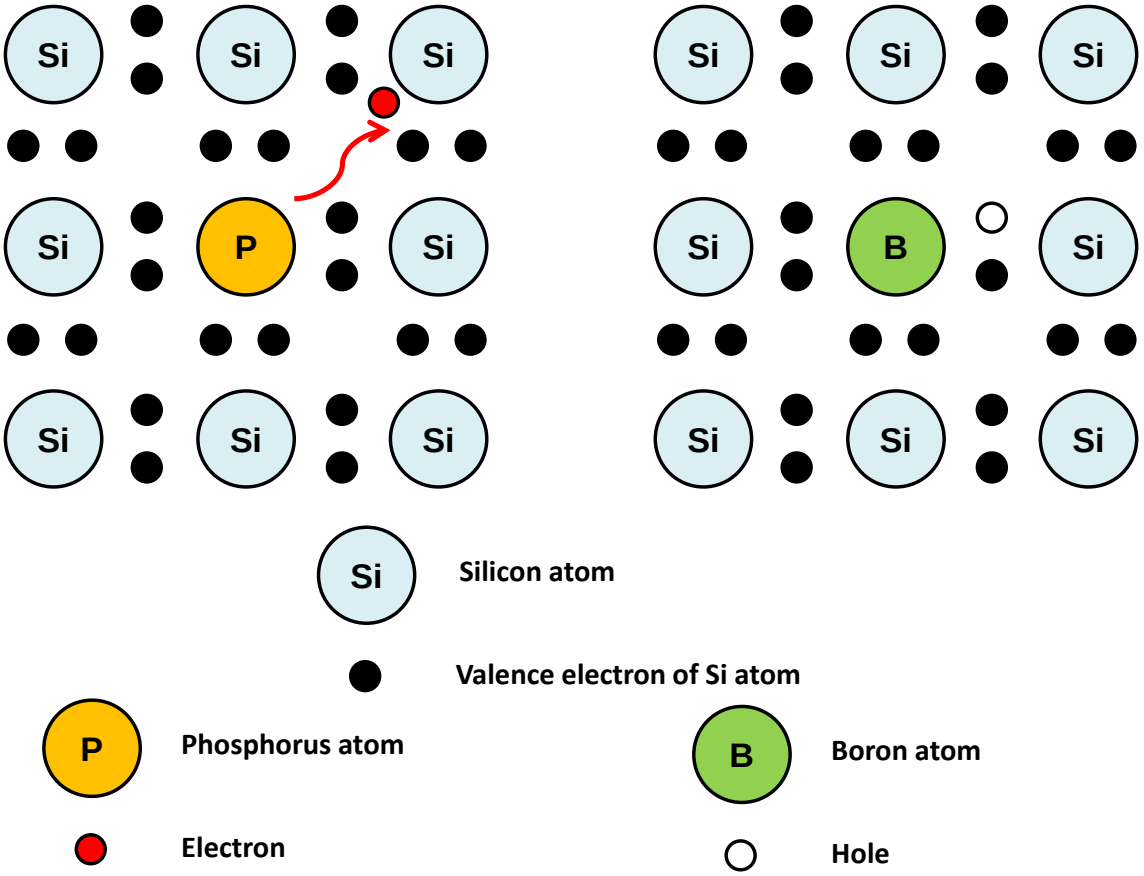

Figure 1.2 Schematic diagram of chemical doping in silicon.

electron gas in a quantum well. It is preferred that the source and drain contacts to the channel are ohmic with low resistance. The gate electrode and channel are isolated each another by an insulating dielectric corresponding to a parallel plate capacitor structure. The application of a gate voltage across this capacitor induces charges into the channel near the semiconductor-dielectric interface. The modulated carrier density in the bulk of a doped semiconductor is typically 10^{18-19} /cm^3, that is equal to a sheet carrier density of 10^{12-13} /cm^2 for a channel with the thickness of 100 Å. In many of the thin film and single crystal materials of interest, the electrostatic screening lengths are short (of the order of a lattice constant), so that the charge induced by electric field remains within

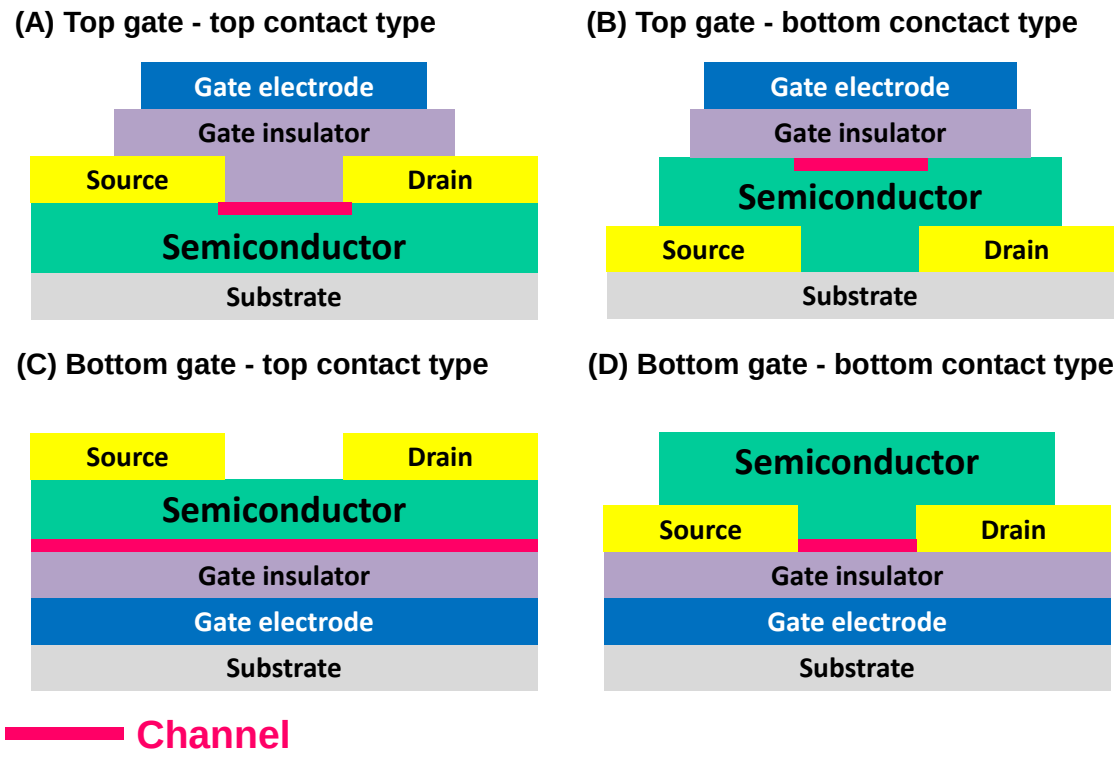

Figure 1.3 Four representative structures of FETs.

one or two unit cell(s) of the interface between the semiconductor and the gate insulator. This is a result of the relatively high carrier densities in these matters.

In the case of modulation of carrier density by electric field, carrier density is determined by the simple principle of capacitor (**Figure 1.4**), as follows.

$$Q = CV \quad (1)$$

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d} \quad (2)$$

Here Q, C, V, ε_0, ε_r, A, and d means the amount of charge, the capacitance, the voltage, the dielectric constant in vacuum, the relative dielectric constant, the area of capacitance, and the distance between two counter electrodes, respectively. ε_r is often described as k. From equation (1) and (2), we obtain sheet carrier density n_{2D} as follows.

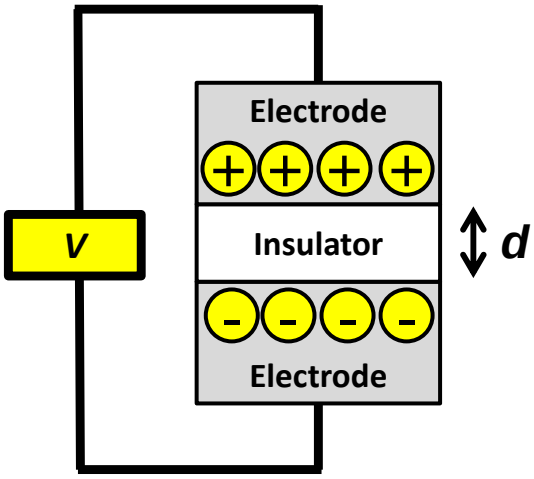

Figure 1.4 Typical structure of capacitor.

$$n_{2D} = \frac{Q}{A} = \varepsilon_r \varepsilon_0 \frac{V}{d} = \varepsilon_r \varepsilon_0 E \quad (3)$$

Here *E* denotes electric field. According to equation (3), thinner gate insulator would lead to higher carrier density, because the electric field is enhanced for a certain voltage.

1.2 FET with solid gate insulator

1.2.1 SiO_2 gate insulator

The most typical and widely used combination of the semiconductor and the gate insulator is that of Si with oxidized silicon, i.e. SiO_2, due to the fortuitous nature of silicon as a material — it can be reacted with oxygen or nitrogen in a controlled manner to form superb insulators with excellent mechanical, electrical and dielectric properties. The combination with ultra-high purity and the ultra-fine controllability of processing is quite rare. Over the past 30 years, astounding progress in the silicon technology has been made through continual scaling of semiconductor devices to further smaller dimensions, resulting in a constant increase in the number of components per chip. These developments contribute to an increase in performance and a decrease in the cost

of the devices (a decrease of ~25% per year per function), fuelling an average market growth of ~15% per annum. These phenomenal trends are well-known as 'Moore's law', which predicts that the number of components per chip is doubled every 18 months.[4, 5] The Moore's law has been continued for surprisingly long time.

However, the ε_r of SiO_2 is only 3.9. And in general, ultra-thin gate insulator usually suffers from non-negligible tunneling current, which exponentially increases as the thickness of the insulator decreases. At a gate length of 60 nm or less, the gate oxide thickness decreases below the critical value of ~1.5 nm when made from SiO_2. The thickness of SiO_2 is becoming sufficiently thin that leakage currents arising from electron tunneling through the dielectrics are posing a problem, and are viewed as a major technical barrier (**Figure 1.5**).[6] In addition, poorly crystalline gate insulator tends to be broken easily by dielectric breakdown at insufficiently high electric field strength. From these circumstances, the carrier density of the order of $10^{12–13}$ /cm^2 is average upper limit for typical dielectrics like SiO_2.

1.2.2 High-*k* materials

So as to overcome the demerit of SiO_2, the materials with a high ε_r, i.e. high-*k* materials, are being used.[7-9] With these materials, the same gate capacitance can be obtained with thicker layers because high-*k* gate insulators afford high capacitance without relying on ultra-small film thicknesses, thus allowing for efficient charge injection into transistor channels while reducing direct tunneling leakage currents.

It is now technically possible to supply a level of charge transfer of (1–3) $\times 10^{14}$ /cm^2 or about 0.3 carrier per unit cell to the surface region of several novel materials, using either the surface charge of a high-*k* material[10] or of a ferroelectric.[11] To further

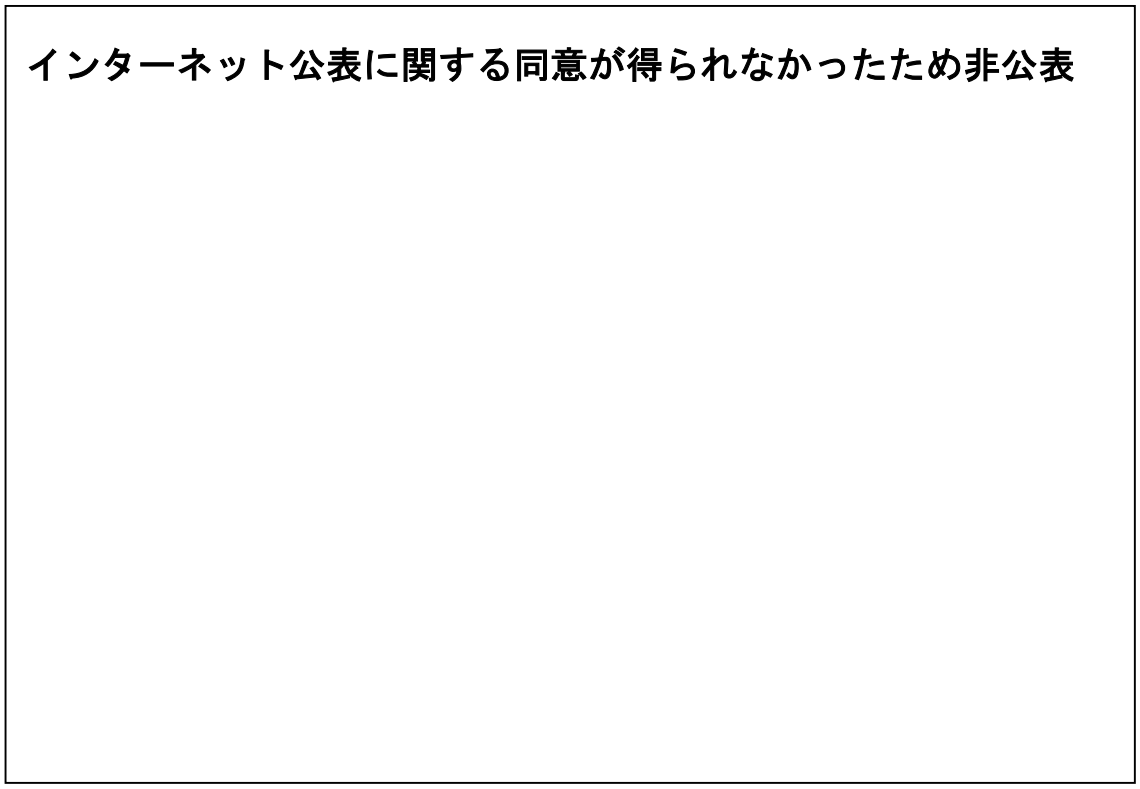

Figure 1.5 Plots of the gate current density flowing between gate contact and channel through a SiO_2 gate insulator, for various thicknesses of SiO_2, as a function of applied gate voltage. The horizontal lines indicate maximum allowable current densities for nMOSFET.

[From S. H. Lo et al., *IEEE ELECTRON DEVICE LETT.* **18**, 209, (1997).]

reduce gate length, new gate dielectrics with higher dielectric constants must be developed.This has motivated intense research on the synthesis and device integration of high-*k* films (ε_r = 20–30) – an area that is at one of the forefronts of materials science and semiconductor electronics. High-*k* dielectric materials have played a significant role in capacitor and memory devices.[7, 12-17] **Table 1.1** lists the dielectric materials currently used for high-*k* applications. These dielectrics can be divided into two groups according to their polarization nature: metal oxides with centrosymmetric (nonpolar) atomic

Table 1.1 ε_r of typical high-*k* materials. This table was made according to the ref. 72. [M. Osada and T. Sasaki, *Adv. Mater.* **24**, 210 (2012).]

Composition	Relative dielectric constant
SiO_2	3.9
Al_2O_3	9
$HfSiO_4$	11
ZrO_2	25
HfO_2	25
Ta_2O_5	27
La_2O_3	30
$LaAlO_3$	30
Nb_2O_5	35
TiO_2	30−40 (Anatase), 80−100 (Rutile)
$BaTiO_3$	1700
$SrTiO_3$	2000
$Pb(Zr, Ti)O_3$, $(Pb, La)(Zr, Ti)O_3$	2500
$CaCu_3Ti_4O_{12}$	80000

arrangements and ferroelectric materials with residual dipoles that result from static atomic displacements. The materials of the former class, including such oxides as Al_2O_3,[8, 18] TiO_2,[8, 19, 20] ZrO_2,[8] Nb_2O_5,[18, 21] HfO_2,[8] and Ta_2O_5,[8, 18] have the advantages of low tanδ and a fairly low temperature coefficient for the ε_r but suffer inherently from relatively low ε_r values (typically < 100). In contrast, the latter class of materials, mainly based on perovskites, can be tailored to yield high ε_r values (ε_r > 200). So far, two kinds of high-*k* perovskites have been developed with static dielectric constant values above 1,000.[7, 8, 17] One kind is the family of ferroelectric oxides, e.g., $(Ba_{1-x}Sr_x)TiO_3$ and $Pb(Zr,Ti)O_3$, that exhibit a dipole moment in the absence of an external electric field; the other family are relaxor oxides, e.g., $PbMg_{1/3}Nb_{2/3}O_3$, characterized by a

ferroelectric response under high electric fields at lower temperature but no macroscopic spontaneous polarization.

However, both kinds of materials show large variations in their dielectric constants with temperature, which is undesirable for many applications. For instance, capacitor applications must stably maintain static dielectric constant values to operate properly under a variety of conditions; if the static dielectric constant has strong temperature dependence, then the device will not be robust and may fail. Typically, tanδ values are also considerably larger in ferroelectric thin films. The desirable combination of high-*k* and low tanδ values is rarely found in a single-phase material, and current research studies have thus focused on mixed-phase or nanolaminate materials such as TiO_2–Ta_2O_5,[20] TiO_2–Nb_2O_5,[21] Nb_2O_5–Ta_2O_5,[18, 22] and ZrO_2–Ta_2O_5.[23] Recently, several intriguing exceptions have been reported in centrosymmetric compounds such as $CaCu_3Ti_4O_{12}$ (ε_r > 80,000) [24] and $ATaO_2N$ (A = Ca, Sr, Ba) (ε_r > 200).[25, 26] However, thin films of these compounds often yield reduced *k* values that are a few orders of magnitude smaller than bulk values, and high-*k* properties in nanofilms are hindered by tradeoffs inherent to high loss and leakage. The design of robust high-*k* properties in nanofilms remains an unresolved and challenging issue in nanoelectronics.

1.3 FET with liquid electrolyte

Recently, a new type of FETs, named electric double layer transistor (EDLT), has been employed for modulating a high carrier density by using polymer electrolytes or ionic liquids (ILs) as gate dielectrics, in which larger capacitances than solid gate insulator can be achieved in the EDLT.[27-42] **Figure 1.6** displays a cross-section of an IL-gated EDLT. When a gate voltage is applied between the gate electrode and the

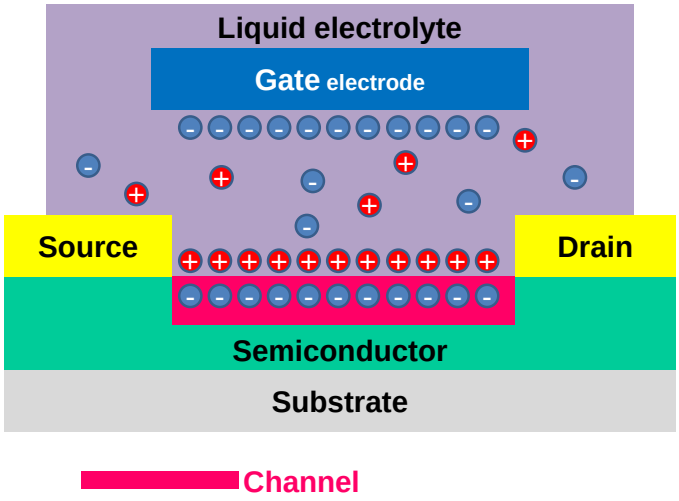

Figure 1.6 Schematic diagram of electric double layer transistor.

channel, the mobile cations and anions in the IL move towards the oppositely charged electrodes to form a set of EDLs. The EDL at the IL/semiconductor interface, regarded as a nanogap capacitor with a huge capacitance, can modulate charges in the channel, in which the accumulated amount of charges is much higher than that in all solid FETs with conventional solid gate dielectrics. For example, in the case of ZnO, a direct estimate for accumulated carrier density obtained through Hall effect measurement was 4×10^{13} /cm^2,[34] that is much higher than that for ZnO FETs with oxide dielectric (< 10^{13} /cm^2).[43-49] More importantly, two-dimensional (2D) superconductivity was electrostatically induced in the insulating $SrTiO_3$ by accumulating very high density of 1×10^{14} /cm^2 with EDLT.[39]

However, the EDLT has several demerits. Firstly, the application of electric field is impossible at low temperature owing to the freezing of ILs. Secondly, the compatibility of EDLT with other solid devices is poor. In addition, switching speed is not so fast. Such demerits are not seen in all solid state FET.

1.4 Colloidal suspension of charge-bearing nanosheets

Colloidal suspension of the charge-bearing oxide nanosheets, which possess atomic- or molecular- level thickness with approximately infinite plane, is synthesized by soft-chemical delamination of layered metal oxide (**Figure 1.7**). Successful delamination of layered titanates into single titanate nanosheets was reported by Sasaki et al. in the 1990s.[50, 51] The protonation of layered metal oxide (ion exchange from alkali cation to proton with water) followed by intercalation of bulky organic ions, typically tetra(*n*-butyl)ammonium (TBA^+) cation, usually results in electrostatic repulsions that facilitate the exfoliation. By applying this procedure, single layers of Ti oxides,[50-52] Mn oxides,[53] Nb/Ta oxides,[54-58] Mo oxides,[59] Ru oxides,[60, 61] and W oxides[62] as well as nanosheets of several perovskites[54, 63-66] have been exfoliated from bulk samples (**Figure 1.8**).

The formation of unilamellar nanosheets is confirmed by direct observation using atomic force microscopy (AFM) and transmission electron microscopy (TEM).

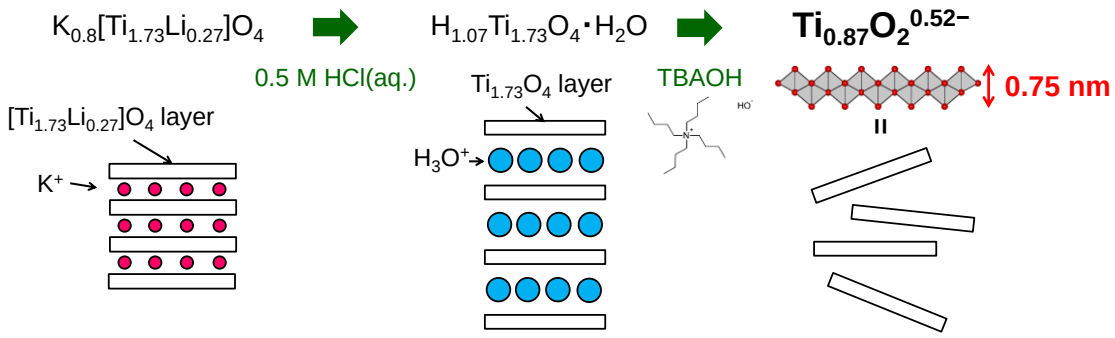

Figure 1.7 How to synthesize nanosheet colloidal suspension (Example is $Ti_{0.87}O_2^{0.52-}$ nanosheet). TBAOH means tetra(*n*-butyl)ammonium hydroxide.

The thickness of the single nanosheet ranges typically between 0.7 and 3 nm, depending on the crystallographic thickness of the host layers in the starting layer metal compounds. Their lateral size depends on the choice of starting materials. From polycrystalline starting materials, the lateral size ranges from sub-micrometer to several tens of micrometers. On the other hand, from single crystal starting materials, the lateral size is increased up to > 100 μm, which is easily handled. Most of oxide nanosheets synthesized to date are d^0 transition metal oxides (with Ti^{4+}, Nb^{5+}, Ta^{5+}, W^{6+}), that are insulator or semiconductor in contrast with graphene.

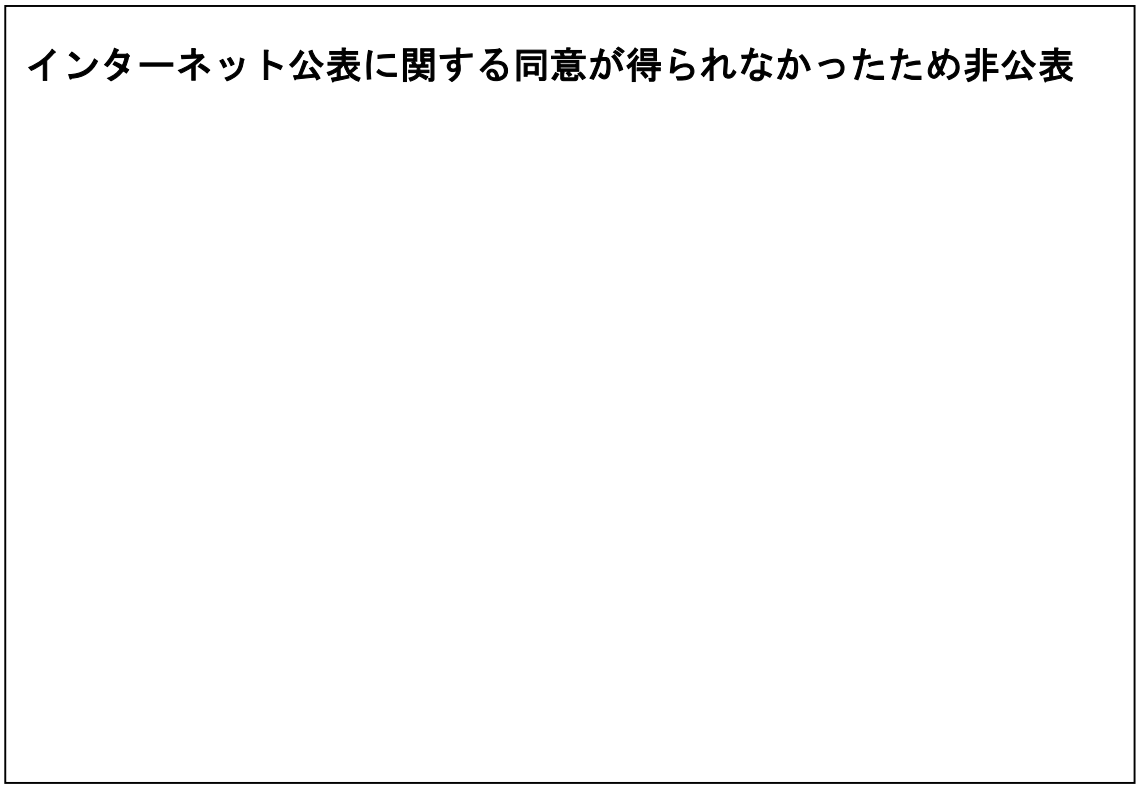

Figure 1.8 Structure of typical oxide nanosheets. A) Titanium oxide; B) calcium niobium oxide; C) manganese oxide; D) niobium oxide; E) tantalum oxide; F) titanium niobium oxide; and G) cesium tungsten oxide.

[From R. Ma and T. Sasaki, *Adv. Mater.* **22**, 5082 (2010).]

1.5 Multi-layer of oxide nanosheets with high ε_r

Various nanostructures such as aggregated flocculates, hollow nanocapsules, and multi-layer thin films, can be fabricated by using these charge-bearing nature, that is, we can use oxide nanosheets as building blocks of nanostructures.[67, 68] Some kinds of the oxide nanosheets including d^0 metal, such as $Ti_{0.87}O_2^{0.52-}$, $Ca_2Nb_3O_{10}^-$, $Ca_2NaNb_4O_{13}^-$, and so on, have a band gap of 3−5 eV[68, 69] and high chemical and thermal stability.[70, 71] The multi-layer of the densely packed film of those nanosheets can be fabricated on various kinds of substrates at room temperature, and so show the large ε_r (> 100) while keeping a leakage current density lower than 10^{-7} A/cm^2 with a gate voltage of 1 V,[72] regardless of only 10 - 20 nm thickness.[72-75] These oxide nanosheets are considered to be promising candidates for future electronic applications[68, 76] as gate insulator materials for various FETs.

However, in macroscopic scale (or typical device scale), the multilayer of dielectric oxide nanosheets inevitably contained intralayer grain boundaries due to the micrometer-sized lateral area, thus suffered from significant leakage current and dielectric breakdown $\leq$ 4 MV/cm.[73] Due to this dielectric breakdown, upper limit of induced carrier density with FET using the multi-layer of dielectric oxide nanosheets is almost the same with that of typical FET using high-*k* solid gate insulator.

1.6 A single nanosheet as a gate insulator

The ultimate gate insulator is one using a single nanosheet because the application of a small gate voltage will produce a high electric field strength, leading to high charge accumulation, in principle (**Figure 1.9**). In addition, a single nanosheet is a

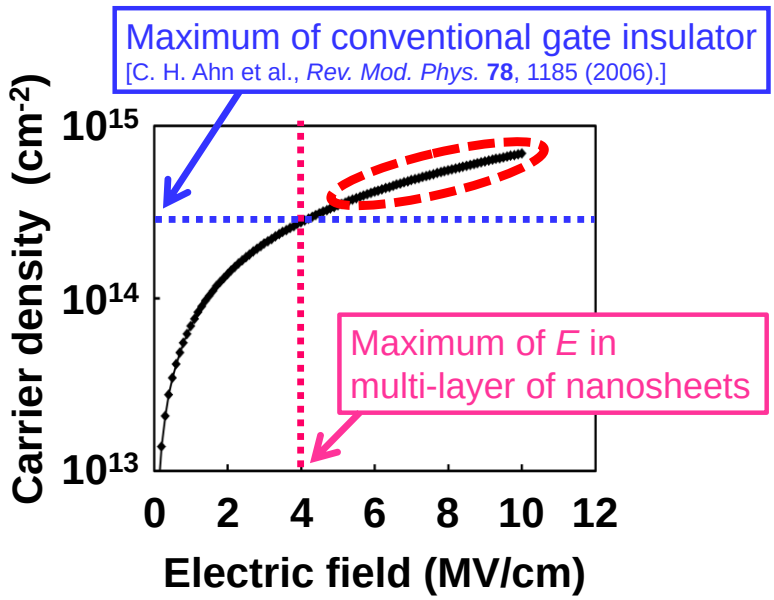

Figure 1.9 Potential of a single dielectric nanosheet as gate insulator.

crystallite without any grain boundary if appropriately small device size is prepared. Thus, the dielectric and insulating properties of a single nanosheet are of strong interest.

Recently, electric measurements of a single nanosheet have been reported by using a conductive atomic force microscope (conductive-AFM).[77] However, the electric field distribution in the geometry of the AFM tip / nanosheet / conductive substrate is completely different from that of an actual capacitor used in a practical device. Therefore, it is strongly desired to evaluate a single nanosheet as a gate insulator in a well-defined planar capacitor structure with sufficiently small electrodes.

Chapter 2 Aim of this research

Concerning the modulation of huge amount of sheet carrier density at the surface of semiconductor materials, there are various problems described in chapter 1. Solid gate insulators have the dilemma between the thickness and the tunneling current, and the size effect. On the other hand, in the case of EDL-FET, working temperature, the compatibility with other devices, and switching speed are essentially difficult to overcome.

In order to resolve these problems, firstly I tried to examine insulating property of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet obtained from the single crystal grown by the flux method, the dielectric oxide nanosheet with the thinnest thickness and the largest lateral size, as described in chapter 4. Secondly, I fabricated planar micro-capacitors, in which the single $Ti_{0.87}O_2^{0.52-}$ nanosheet was sandwiched by sufficiently small electrodes, in order to quantitatively investigate electric and dielectric properties of the single $Ti_{0.87}O_2^{0.52-}$ nanosheet. As the result, the $Ti_{0.87}O_2^{0.52-}$ nanosheet itself was found to have excellent insulating properties as described in chapter 5. Finally, I tried to fabricate both top gate and bottom gate types FETs with the nanosheet gate insulator, aiming FET operation with the modulation of huge amount of carriers in all-solid state FET. In the trial of top-gate FET fabrication, since the channel area can be smaller than the size of single nanosheets, both a single nanosheet and multi-layer of nanosheets were tested as gate insulator. On the other hand, in the trial of bottom-gate FET fabrication, since the channel area should be larger than the size of single nanosheets from the viewpoint of the device structure, only multi-layer of nanosheets were tested as gate insulator.

Chapter 3 Experimental techniques

In this chapter, I explain about several experimental techniques used in this thesis.

3.1 Cleanroom

A cleanroom is a room in which there are lower level of environmental pollutants such as dust, aerosol particles, and/or chemical vapors. The level of a cleanroom is defined by the number of particles per cubic meter at a specified particle size. The ambient air outside in a typical urban environment contains 35,000,000 particles with the diameter $\geq$ 0.5 μm per cubic meter, corresponding to an ISO 9 cleanroom, while an ISO 1 cleanroom allows no particles with such range of size and only 12 particles $\leq$ 0.3 μm per cubic meter.

3.2 Lithography

Lithography (from Greek λίθος, lithos, "stone" + γράφειν, graphein, "to write") is originally a method of printing. It was invented in 1796 as a cheap method of publishing theatrical works. Lithography can be used to print text or artwork onto paper or other suitable material. In modern lithography, the image is made by chemical reaction of polymer, called as "resist". The image can be printed directly from the plate (the orientation of the image is reversed), or it can be offset, by transferring the image onto a flexible sheet (rubber) for printing and publication.

3.2.1 Photolithography

Photolithography is a type of lithography using UV light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photoresist. For example, in complex integrated circuits, a modern comprehensive MOS (so called CMOS) substrate will go through the photolithographic cycle up to 50 times.

Some fundamental principles of photolithography are same with photography in that the pattern in the etching resist is created by exposing it to light, either directly (without using a mask) or with a projected image using an optical mask. This procedure is comparable to a high precision version of the method used to make printed circuit boards. Subsequent stages in the process have more in common with etching than with lithographic printing. It is used because it can create extremely small patterns (down to a few tens of nanometers in size), it affords exact control over the shape and size of the objects it creates, and because it can create patterns over an entire surface cost-effectively.

The resolution and the accuracy of the position of the pattern are determined essentially by the wavelength of the UV light, and practically by the quality of the system. In general, 1-2 μm is the lower limit (not so easy).

3.2.2 Electron beam lithography

Electron beam (EB) lithography is also a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. It uses beam of accelerated electrons to draw a geometric pattern onto electron-beam-sensitive resist on the substrate. A series of chemical treatments after drawing is done in the same manner with photolithography.

The difference from photolithography is the resolution. In the case of photolithography, a few μm is the limit of resolution. On the other hand, in the EB lithography, the de Broglie wavelength of accelerated EB is much shorter than wavelength of light for photolithography, and so to draw much finer pattern is possible. Limit of resolution of typical EB lithography is less than 100 nm.

3.3 Basic procedure of lithography

One lithography procedure consists of several steps in sequence (**Figure 3.1**).

3.3.1 Cleaning

If organic or inorganic contaminations are present on the substrates, they are removed simply by cleaning in ultrasonic bath or strictly by wet chemical treatment, e.g. the RCA clean procedure based on solutions containing hydrogen peroxide.

3.3.2 Preparation

The substrate is initially heated to a temperature sufficient to drive off any moisture that may be present on the substrate surface. Substrates that have been in

storage must be chemically cleaned to remove contamination by methods described in

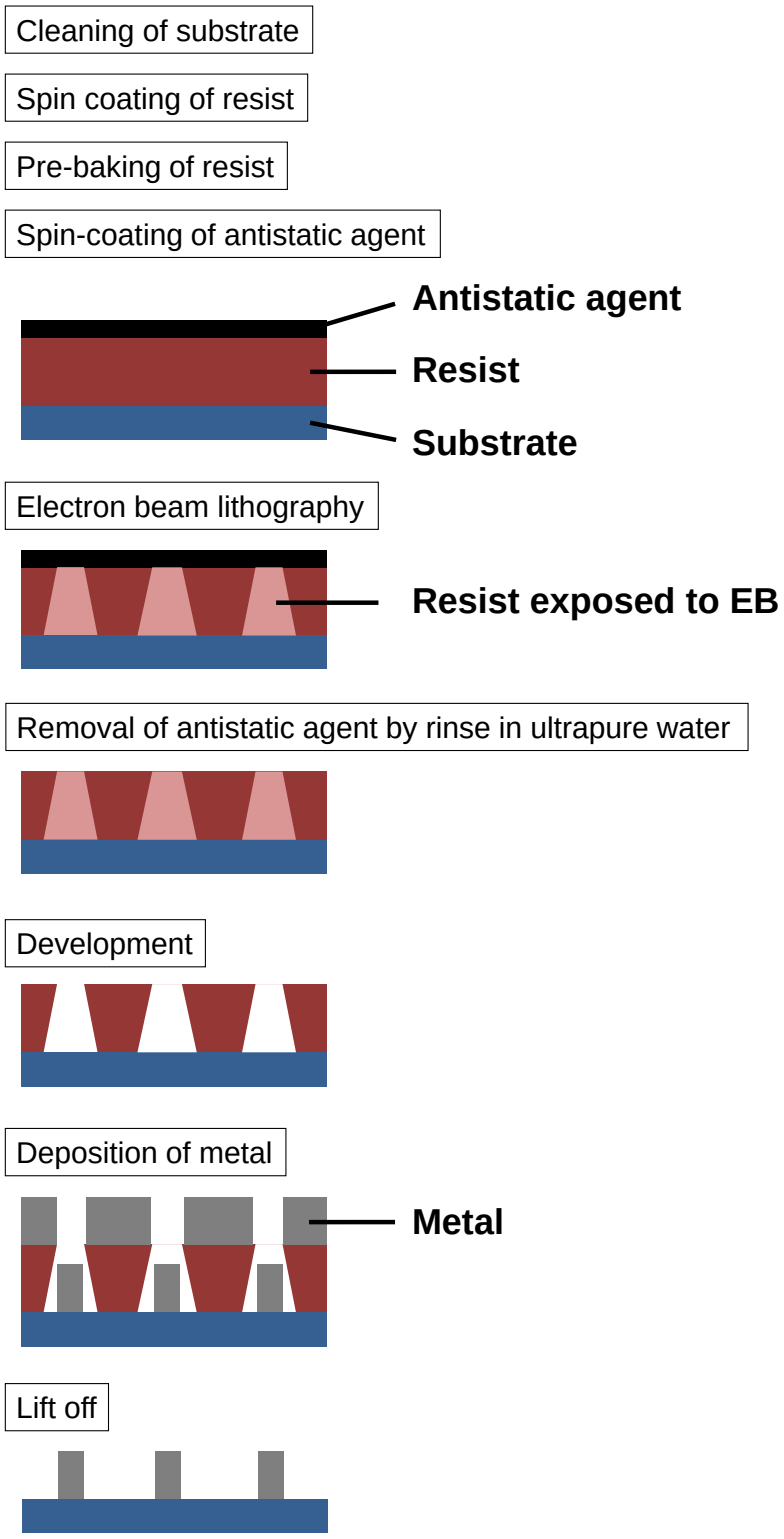

Figure 3.1 Simplified illustration of procedure (not to scale).

previous section. In the case of silicon substrate, a liquid or gaseous "adhesion promoter", such as bis(trimethylsilyl)amine ("hexamethyldisilazane", HMDS), is applied to promote adhesion of the photoresist to the substrate. The surface layer of silicon dioxide on the silicon substrate reacts with HMDS to form tri-methylated silicon-dioxide, a highly water repellent layer not unlike the layer of wax on a car's paint. This water repellent layer prevents the aqueous developer from penetrating between the photoresist layer and the substrate's surface, thus preventing so-called lifting of small photoresist structures in the (developing) pattern. However, in this thesis, the formation of SiO_2 layer must be avoided, because the layer works as low-k layer. Therefore, this step was skipped in this thesis.

3.3.3 Resist application

The substrate is covered with resist by spin coating. A viscous, liquid solution of resist is dropped onto the substrate, and then the substrate is spun rapidly to produce a uniformly thick layer. The spin coating typically runs at 1200 to 4800 rpm for 30 to 60 seconds, and produces a layer between 0.5 and 2.5 μm thick, and also results in a uniformly thin layer, usually with uniformity of within 5 to 10 nm. And especially, when charge-up is concerned in EB lithography, antistatic agent is also coated on the pre-baked EB resist.

This uniformity can be explained by fluid-mechanical modelling, which shows that the resist moves much faster at the top of the layer than at the bottom, where viscous forces bind the resist to the substrate surface. Thus, the top layer of resist is quickly ejected from the substrate's edge while the bottom layer still creeps slowly radially along the substrate. In this way, any 'bump' or 'ridge' of resist is removed,

leaving a very flat layer. Final thickness is also determined by the evaporation of liquid solvents from the resist. For very small, dense features (< 125 or so nm), lower resist thicknesses (< 0.5 micrometers) are needed to overcome collapse effects at high aspect ratios; typical aspect ratios are < 4:1.

The resist-coated substrate is then pre-baked to drive off excess photoresist solvent, typically at 90 to 100 °C for 30 to 60 seconds on a hotplate. In this thesis, two kinds of EB resists, ZEP-520A and OEBR-CAP112, were used. The detail of treatment parameters were summarized in **Table 3.1**.

Table 3.1 Summary of treatment parameters of EB resist used in this thesis.

EB resist	ZEP 520-A	OEBR-CAP 112
Type	Normal	CAR
Rotation speed of spin coating / rpm	4000	2500
Rotation time of spin coating / sec.	60	60
Pre-baking temperature / ^{o}C	180	110
Pre-baking time / min.	15	5
Antistatic agent	Espacer 300Z	Espacer AX
Rotation speed of spin coating / rpm	2000	2000
Rotation time of spin coating / sec.	60	60
Pre-baking temperature / ^{o}C	110	110
Pre-baking time / min.	10	10
Dose / μC cm^{-2}	104	6
Baking temperature before development / ^{o}C	No process	110
Baking time before development / sec.	No process	90
Developer	ZED-N50	TMAOH
Development time / sec.	90	60
Agent for rinse of pattern	ZMD-B	Ultrapure water
Rinse time / sec.	60	60
Baking temperature after development / ^{o}C	No process	110
Baking time after development / sec.	No process	90
Typical thickness / nm	400	1500

3.3.4 Exposure and developing

After pre-baking, the resist is exposed to a pattern of intense light or EB. The exposure to light or EB causes a chemical change that allows some of the resist to be removed by a special solution, called "developer (*Genzoueki* in Japanese)" by analogy with photographic developer. Positive resist, the most common type, becomes soluble in the developer when exposed; with negative resist, unexposed regions are soluble in the developer.

If "chemically amplified resist (CAR)" is used, then post-exposure bake (PEB) is performed before developing, typically to help reduce standing wave phenomena caused by the destructive and constructive interference patterns of the incident light or resist. This process is much more sensitive to PEB time, temperature, and delay, as most of the "exposure" reaction (creating acid, making the polymer soluble in the basic developer) actually occurs in the PEB. In this thesis, OEBR-CAP 112 is a CAR.

In the past, developers often contained sodium hydroxide (NaOH). However, sodium is considered an extremely undesirable contaminant, "mobile ion", in MOSFET fabrication because it degrades the insulating properties of gate oxides (specifically, sodium ions can migrate in and out of the gate, changing the threshold voltage of the transistor and making it harder or easier to turn the transistor on over time). Metal-ion-free developers such as tetramethylammonium hydroxide (TMAOH) are now used. However, TMA^+ cation can exfoliate the protonated layered metal oxide into nanosheets. Therefore, this developer (and so, related chemicals including the resist) cannot be used.

The resulting substrate is then "hard-baked" if a CAR was used, typically at 120 to 180 °C for 20 to 30 minutes. The hard bake solidifies the remaining photoresist,

to make a more durable protecting layer in future ion implantation, wet chemical etching, or plasma etching, especially ozone plasma.

3.3.5 Etching

In etching, a liquid ("wet") or plasma ("dry") chemical agent removes the uppermost layer of the substrate in the areas that are not protected by resist. In semiconductor fabrication, dry etching techniques are generally used, as they can be made anisotropic, in order to avoid significant undercutting of the photoresist pattern. This is essential when the width of the features to be defined is similar to or less than the thickness of the material being etched (i.e. when the aspect ratio approaches unity). Wet etch processes are generally isotropic in nature, which is often indispensable for microelectromechanical systems, where suspended structures must be "released" from the underlying layer. The development of low-defectivity anisotropic dry-etch process has enabled the ever-smaller features defined photolithographically in the resist to be transferred to the substrate material.

3.3.6 Removal of resist

After a resist is no longer needed, it must be removed from the substrate. This usually requires a liquid "resist stripper", which chemically alters the resist so that it no longer adheres to the substrate. When some thin films such as metals as electrodes and/or oxides as insulators were deposited into the developed cavities, films on the resist are also removed at the same time. This process is called as "lift-off".

3.4 Etching

Etching is used in microfabrication to chemically remove layers from the surface of a substrate during manufacturing. Etching is a critically important process module, and every substrate undergoes many etching steps before it is complete.

For many etch steps, part of the substrate is protected from the etchant by a "masking" material which resists etching. In some cases, the masking material is a resist which has been patterned using lithography. Other situations require a more durable mask, such as chromium deposited by thermal evaporation.

3.4.1 Figure of merit

If the etch is intended to make a cavity in a material, the depth of the cavity may be controlled approximately using the etching time and the known etch rate. More often, though, etching must entirely remove the top layer of a multilayer structure, without damaging the underlying or masking layers. The etching system's ability to do this depends on the ratio of etch rates in the two materials (selectivity, see **Figure 3.2**).

Some etches undercut the masking layer and form cavities with sloping sidewalls. The distance of undercutting is called bias. Etchants with large bias are called isotropic, because they erode the substrate equally in all directions. Modern processes greatly prefer anisotropic etches, because they produce sharp, well-controlled features (isotropy, see **Figure 3.3**).

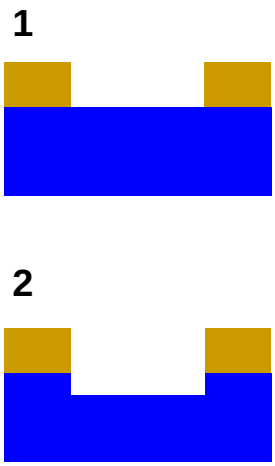

Figure 3.2 Schematic diagram to explain selectivity. Yellow is the layer to be removed. Blue is the layer to remained. ; 1. A poorly selective etch removes the top layer, but also attacks the underlying material. ; 2. A highly selective etch leaves the underlying material unharmed.

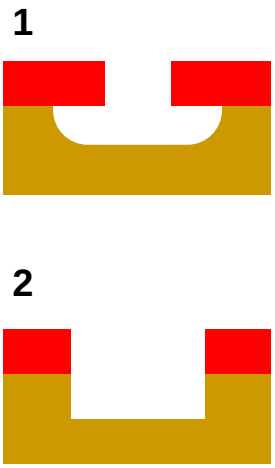

Figure 3.3 Schematic diagram to explain Isotropy. Red is the masking layer. Yellow is the layer to be removed. ; 1. A perfectly isotropic etch produces round sidewalls. ; 2. A perfectly anisotropic etch produces vertical sidewalls.

3.4.2 Etching media and technology

3.4.2.1 Wet etching

The etching processes using liquid-phase ("wet") etchants is named as "wet etching." The substrate can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffered hydrofluoric acid is used commonly to etch silicon dioxide over a silicon substrate.

Different specialized etchants can be used to characterize the surface etched. Wet etchants are usually isotropic, which leads to large bias when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes. However, the photographic developer used for photoresist resembles wet etching.

3.4.2.2 Plasma etching

Modern VLSI processes avoid wet etching, and use plasma etching instead. Plasma etchers can operate in several modes by adjusting the parameters of the plasma. Ordinary plasma etching operates between 10 and 500 Pa. The plasma produces energetic free radicals, neutrally charged, that react at the surface of the substrate. Since neutral particles attack the substrate from all angles, this process is isotropic.

Plasma etching can be isotropic, i.e., exhibiting a lateral undercut rate on a patterned surface approximately the same as its downward etch rate, or can be anisotropic, i.e., exhibiting a smaller lateral undercut rate than its downward etch rate. Such anisotropy is maximized in deep reactive ion etching. The use of the term anisotropy for plasma etching should not be conflated with the use of the same term when referring to orientation-dependent etching. A plasma containing oxygen is used to

oxidize ("ash") resist and facilitate its removal.

Especially, ion milling, or sputter etching, uses lower pressures, often as low as 10 mPa. It bombards the substrate with energetic ions of noble gases, often Ar^+, which knock atoms from the substrate by transferring momentum. Because the etching is performed by ions, which approach the substrate approximately from one direction, this process is highly anisotropic. On the other hand, it tends to display poor selectivity.

3.5 Evaporation

Evaporation is a common method of thin-film deposition. The source material is evaporated in a vacuum. The vacuum allows vapor particles to travel directly to the target object, i.e. substrate, where they condense back to a solid state. Evaporation is used in microfabrication, and to make macro-scale products such as metallized plastic film.

3.5.1 Physical principle

Evaporation involves two basic processes: a hot source material evaporates and condenses on the substrate. It resembles the familiar process by which liquid water appears on the lid of a boiling pot. However, the gaseous environment and heat source are different.

Evaporation takes place in a vacuum, i.e. vapors other than the source material are almost entirely removed before the process begins. In high vacuum (with a long mean free path), evaporated particles can travel directly to the deposition target without colliding with the background gas. By contrast, in the boiling pot example, the water

vapor pushes the air out of the pot before it can reach the lid. At a typical pressure of 10^{-4} Pa, an 0.4-nm particle has a mean free path of 60 m. Hot objects in the evaporation chamber, such as heating filaments, produce unwanted vapors that limit the quality of the vacuum.

Evaporated atoms that collide with foreign particles may react with them; for instance, if aluminum is deposited in the presence of oxygen, it will be oxidized and form aluminum oxide. They also reduce the amount of vapor that reaches the substrate, which makes the thickness difficult to control.

Evaporated materials deposit not uniformly if the substrate has a rough surface (as integrated circuits often do). Because the evaporated material attacks the substrate mostly from a single direction, protruding features block the evaporated material from some areas. This phenomenon is called "shadowing" or "step coverage."

When evaporation is performed in poor vacuum or close to atmospheric pressure, the resulting deposition is generally non-uniform and tends not to be a continuous or smooth film. Rather, the deposition will appear to be fuzzy.

3.5.2 Equipment

Any evaporation system includes a vacuum pump. It also includes an energy source that evaporates the material to be deposited. Many different energy sources exist: In the thermal method, metal wire is fed onto heated semimetal (ceramic) evaporators known as "boats" due to their shape. A pool of melted metal forms in the boat cavity and evaporates into a cloud above the source. Alternatively the source material is placed in a crucible, which is radiatively heated by an electric filament, or the source material may be hung from the filament itself (filament evaporation).

In the EB method, the source is heated by an EB with an energy over 15 keV. Therefore, evaporation of sources with higher melting (or sublimation) point is possible. As point to notice, in the EB evaporation of ferroelectric sources, the course of flight of EB can be affected by magnetic field from the ferroelectric source. This means that as the temperature of source becomes higher, the point where EB attacks the source moves.

Finally, I'd like to note molecular beam epitaxy and pulsed laser deposition are an advanced form of thermal evaporation.

3.6 Oxide nanosheets

3.6.1 Synthesis

3.6.1.1 Synthesis of colloidal suspension

Chemical exfoliation is the easiest method to exfoliate single layers (i.e. oxide nanosheets) with lateral size of up to several μm from layered mother compounds. As schematically shown in **Figure 1.8**, oxide nanosheets are routinely synthesized by chemical exfoliation of a parent layered metal oxides.

So far, various layered metal oxides, e.g., $K_{0.8}Ti_{1.73}Li_{0.27}O_4$,[78] $Cs_{0.7}Ti_{1.825}O_4$,[50, 51] $KCa_2Nb_3O_{10}$,[63, 79] $KCa_2NaNb_4O_{13}$,[80] $K_{0.45}MnO_2$,[53, 81, 82] $K_4Nb_6O_{17}$,[56] $RbTaO_3$,[55] $KTiNbO_5$ [54, 57, 83, 84] and $Cs_{6+x}W_{11}O_{36}$ [62] have been delaminated into their elemental layers, i.e., oxide nanosheets, as shown in **Figure 1.9**. The host compounds as precursors are all constituted of stacked negatively charged slabs, corner- and/or edge-shared MO_6 (M = Ti, Nb, Mn, Ta, W) octahedral units, and alkali metal cations (K^+, Rb^+, Cs^+) occupying the interlayer space. A common feature of these layered oxides is their cation-exchange property involving interlayer alkali metal ions.

Ion-exchange and intercalation properties facilitate the process for chemically modifying the composition of the interlayer space at room temperature, while retaining the host layer units.

A multistep soft-chemical exfoliation process has been well-established for the purpose of exfoliating layered metal oxides. In general, parent layered compounds are first synthesized by a conventional solid-state calcination method at high temperature (800 – 1300 °C). Then, they are treated in acidic solution to produce their hydrated protonic form, e.g., $H_{1.07}Ti_{1.73}O_4 \cdot H_2O$, $H_{0.7}Ti_{1.825}O_4 \cdot H_2O$, $HCa_2Nb_3O_{10} \cdot 1.5H_2O$, $HCa_2NaNb_4O_{13} \cdot 1.5H_2O$, $H_{0.13}MnO_2 \cdot 0.7H_2O$, $K_{0.8}H_{3.2}Nb_6O_{17} \cdot nH_2O$, $Rb_{0.1}H_{0.9}TaO_3 \cdot 1.3H_2O$, $HTiNbO_5$, and $H_{2.1}Cs_{3.9}W_{11}O_{36} \cdot 6H_2O$, by ion-exchange reaction. Furthermore, the interlayer gallery can be substantially expanded by substituting the protons with a sufficient number of bulky organic ions, e.g., TBA^+ cations, in aqueous solution, e.g. ultrapure water. The swelling decreases the electrostatic interaction between the host layers and the cationic interlayer species, resulting in final exfoliation with the aid of a weak shear force applied by mechanical shaking. In this manner, negatively charged nanosheets, $Ti_{0.87}O_2^{0.52-}$,[52] $Ti_{0.91}O_2^{0.36-}$,[50, 51] $Ca_2Nb_3O_{10}^-$,[63, 79] $Ca_2NaNb_4O_{13}^-$,[80] $MnO_2^{0.4-}$,[53, 81, 82] $Nb_6O_{17}^{4-}$,[56] TaO_3^-,[55] $TiNbO_5^-$ [54, 57, 83, 84] and $Cs_4W_{11}O_{36}^{2-}$ [62] are derived from the corresponding protonic form in *n*-tetrabutylammonium hydroxide, TBAOH solutions at suitable concentrations.

The electrostatic repulsion between negatively charged oxide nanosheets blanketed with electrical double layers generates a stable aqueous colloidal suspension. A clear Tyndall light scattering effect is always observed for these suspensions using a side-incident light beam, demonstrating that the nanosheets are in a well-dispersed state.

3.6.1.2 How to obtain large size nanosheet

Large size nanosheets are obtainable via the swelling and exfoliation of large single crystalline precursors. For example, large single crystals of $K_{0.8}Ti_{1.73}Li_{0.27}O_4$ are grown via a melting and recrystallization process in molten K_2MoO_4. Platy single crystals with a lateral dimension of 4 mm are produced.[52] By exfoliating its proton-exchanged form, $H_{1.07}Ti_{1.73}O_4 \cdot H_2O$, through gentle shaking in aqueous TBAOH solution, oversized $Ti_{0.87}O_2^{0.52-}$ nanosheets are obtained at a lateral size of several tens of micrometers, which is approximately 100 times larger than that of the nanosheets synthesized from conventional polycrystalline samples [52]. In the similar manner, the synthesis of large niobium oxide nanosheets by delaminating millimeter-sized $K_4Nb_6O_{17}$ crystals has also been achieved.[85]

3.6.2 Layer-by-layer assembly of nanosheets

Nanosheets are charge-bearing and dispersed as a colloidal suspension. Therefore, various solution-based techniques can be applied to construct a range of functional materials by employing them as building blocks. For example, freeze drying is performed as a gelation method for the titanium oxide nanosheet suspension.[86] It was also reported that the formation of novel hollow microspheres with extremely thin shells is possible by spray-drying of an aqueous colloidal suspension of the exfoliated nanosheets.[87] In particular, 2D nanosheets are capable of forming highly oriented films by aligning them parallel to the substrate surface. In this regard, traditional wet-processing film fabrication techniques such as spin-coating, dip-coating and electrophoretic deposition may be used with the advantage of relatively easy handling of nanosheets while many layers (usually > 100 nm) can be quickly applied in a single

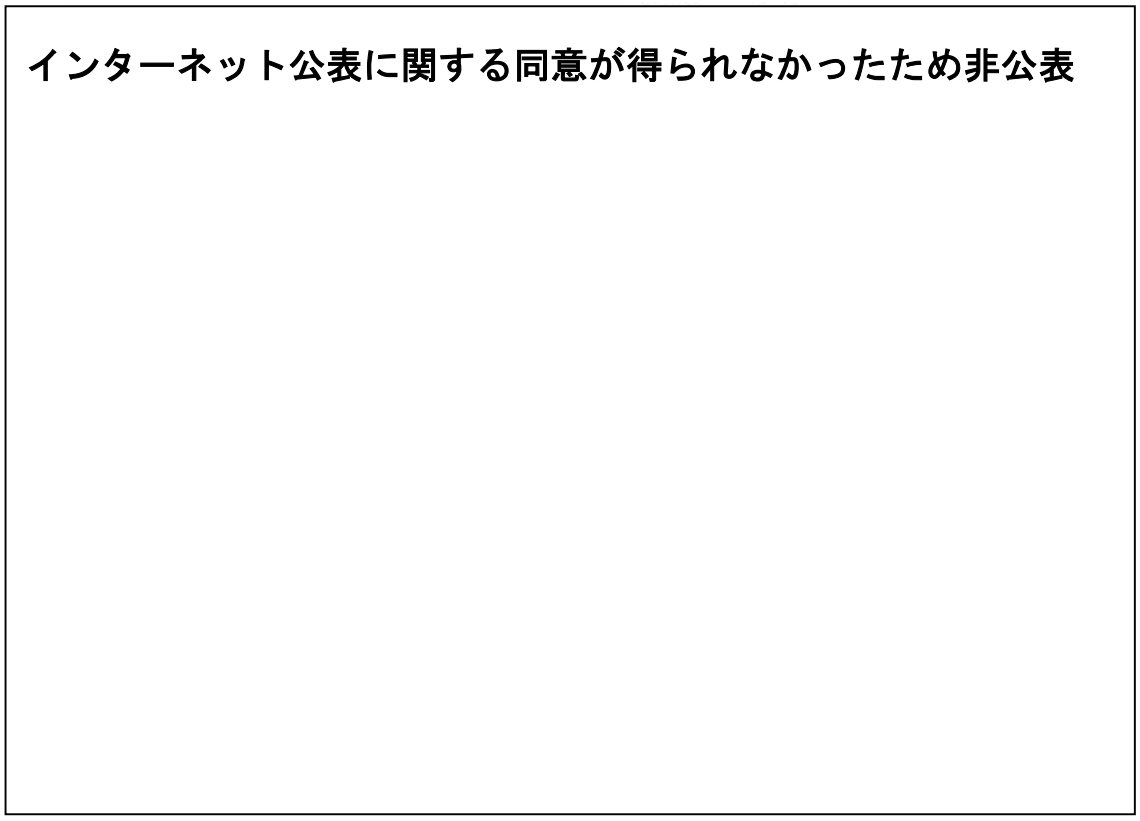

Figure 3.4 Schematic assembling processes for nanosheets. A) Flocculation; B) Electrostatic sequential adsorption; and C) Langmuir–Blodgett method.

[From R. Ma and T. Sasaki, *Adv. Mater.* **22**, 5082 (2010).]

process.[88-90] For example, thin films of titanium oxide nanosheet deposited on an indium-tin oxide (ITO) substrate by electrophoretic deposition exhibit high transmittance in visible light regions.[89]

In addition to these relatively macroscale assembling techniques, elegant methods with more precise control at the nanometer scale have also been developed. Typical assembling processes for nanosheets, flocculation and layer-by-layer (LbL) assembly, are schematically illustrated in **Figure 3.4**. Utilizing the charged feature, flocculation is a very convenient protocol for preparing micro- and mesoporous lamellar solids or nanocomposites based on nanosheets, although not suitable to fabricate thin

film. On the other hand, electrostatic sequential adsorption and Langmuir–Blodgett (LB) deposition are most frequently used to design and build up multilayer nanofilms and core–shell nano-architectures on a planar or curved (spherical) surface, respectively, in an LbL manner. In the electrostatic sequential deposition and the LB method, a multi-layered nano-architecture or nanofilm can, in principle, be controlled in 1-nm steps or the nanosheet thickness. This controllability is far superior to that of conventional solution-based techniques such as spin-coating, dip-coating, electrophoretic deposition, etc. Thus-fabricated nanoarchitectures and nanofilms are attractive for various electronic, magneto-optical, catalytic, and photosynthetic applications, taking advantage of both the unique properties of nanosheets and possible coupled interactions between nanosheets and carefully designed functional counter components.

3.6.2.1 Electrostatic sequential deposition

The electrostatic sequential deposition to fabricate polymer films was developed, and the concept has been extended to various systems with a wide range of charge-bearing materials including proteins and colloidal nanoparticles.[91] Due to their charge-bearing nature, nanosheets are perfectly suitable for electrostatic sequential deposition. In this approach, a multi-layer film can be built up by alternately dipping a substrate into the properly diluted colloidal suspension of nanosheets and an aqueous solution of suitable polyelectrolytes, i.e., LbL.[54, 92-95]

However, in this method, overlapping between nanosheets occurs, and so this method is not suitable to fabricate gate insulator with low number of leakage current paths.[74]

3.6.2.2 Langmuir–Blodgett deposition

LB film deposition, the formation of a floating monolayer on a liquid (usually water) surface in a LB trough followed by an appropriate level of compression, is preferable for achieving densely packing or neat tiling (imagine drifting-ice on the sea). Through vertical-dipping or lifting, the monolayer is deposited onto a flat, hydrophilic substrate in LbL manner. The LB technique was initially used mainly for organic materials, typically in the case of fatty acids, and then it has been extended to a variety of inorganic nanomaterials.[96] Suspensions of inorganic nano-materials capped with surfactants can be well dispersed on a water surface, and then the floating monolayers can be forced to assemble at a high density and can be transferred onto a substrate. Pioneering work has demonstrated that exfoliated nanosheets of aluminosilicate, molybdenum disulfide, and layered titanium oxide could float by adhering to amphiphilic ammonium cations at the air/water interface through electrostatic interaction, and thus the ordinary LB procedure is applicable for fabricating nanosheet films.[97-100]

Muramatsu et al. reported an LB deposition method for nanosheets without the use of amphiphiles.[101] TBA^+ contained in an oxide colloidal nanosheet suspension acts as a supporting electrolyte to float nanosheets spontaneously at the air/water interface and nanosheets are successfully transferred onto the substrate after suitable compression. In the resulting LB film, the nanosheets are densely packed. The film thus obtained is exposed to UV light to make the substrate surface hydrophilic, which is helpful for stable repetition of monolayer deposition. This direct nanosheet transfer method has been widely applied for many types of nanosheets such as $Ti_{0.91}O_2^{0.36-}$, $Ca_2Nb_3O_{10}^-$, $La_{0.95}Nb_2O_7^-$, etc.[74, 75, 102]

Chapter 4 Conductive atomic force microscopy of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet as insulator

本章については、５年以内に雑誌等で刊行予定のため、非公開。

Chapter 5 Fabrication of planar micro-capacitors by using a single $Ti_{0.87}O_2^{0.52-}$ nanosheet as insulator

In this chapter, insulating and dielectric properties of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet was evaluated by fabrication of micro-capacitor in order to confirm the properties qualitatively.

5.1 Experimental

In order to evaluate the dielectric and insulating properties of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet, we fabricated an Au / a single $Ti_{0.87}O_2^{0.52-}$ nanosheet / Au planar micro-capacitor structure (**Figure 5.1**). As a substrate for the micro-capacitor structure, we used a $SrTiO_3$ single crystal with a step and terrace (100) surface (5 × 5 × 0.5 mm^3) made by SHINKOSHA, in which the step height is one unit cell of $SrTiO_3$ (3.905 Å). The substrate was highly insulating, with a resistivity of > 10^7 Ω cm. 600 capacitors were fabricated on the substrate by using electron beam lithography as described below (**Figure 5.2**).

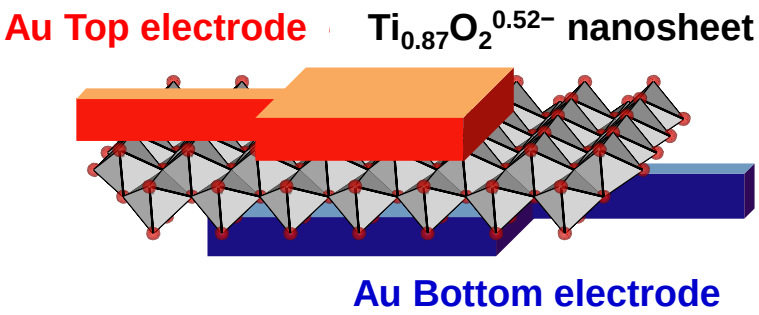

Figure 5.1 Schematic diagram of fabricated capacitor.

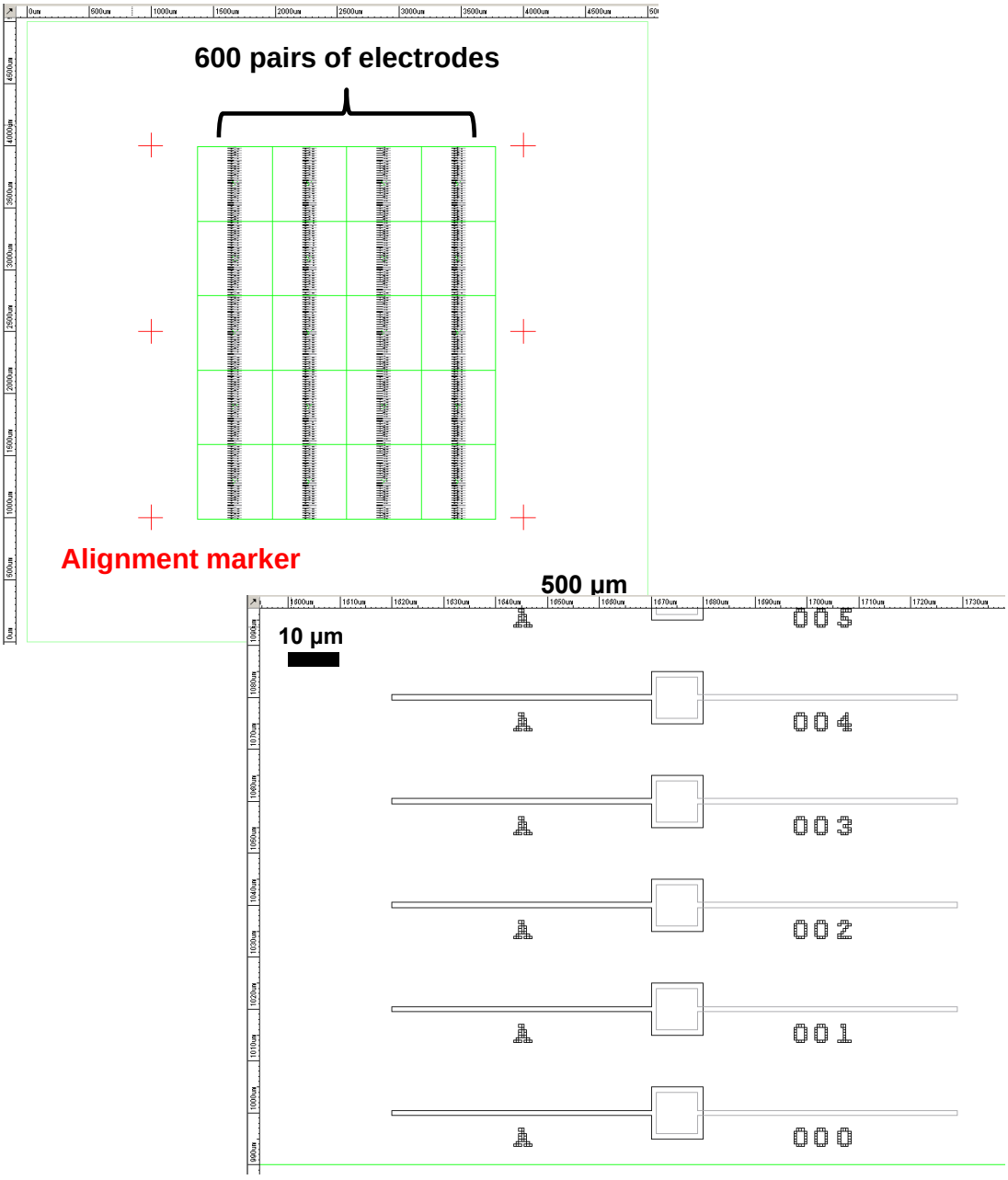

Figure 5.2 CAD patterns of bottom and top electrodes.

5.1.1 Fabrication of alignment markers and bottom electrodes

On the substrate, an array of Au (50 nm)/Cr (5 nm) alignment markers and bottom electrodes with 10 μm-square pads were formed by EB lithography, ashing, EB evaporation, lift off (**Figure 5.3**). The following is the detail procedure.

1) Wash $SrTiO_3$ substrate by ultrasonication in EL acetone for 5 minutes and in EL

ethanol for 5 minutes, then dry it by N_2 gas blow with air gun.

2) Spin-coat the substrate with EB resist (ZEP-520A, ZEON) (4000 rpm, 60 seconds), bake it on a hot plate (180 ^{o}C, 15 minutes), and cool it down on another hot plate (room temperature, 1 minute).

3) Spin-coat the substrate with antistatic agent (Espacer 300Z, SHOWA DENKO) (2000 rpm, 60 seconds), bake it on a hot plate (110 ^{o}C, 10 minutes), and cool it down on another hot plate (room temperature, 1 minute).

4) Draw the pattern of a set of 600 bottom electrodes (dose 26 μC/mm^2 × 4) with electron beam. The four repeated dose is to prevent EB resist from the evaporation and the damage by electron beam due to low thermal conductivity of $SrTiO_3$.

5) Remove Espacer 300Z by rinsing the substrate in ultrapure water.

6) Develop the substrate in ZED-N50 (ZEON) for 90 seconds, rinse it in ZMD-B

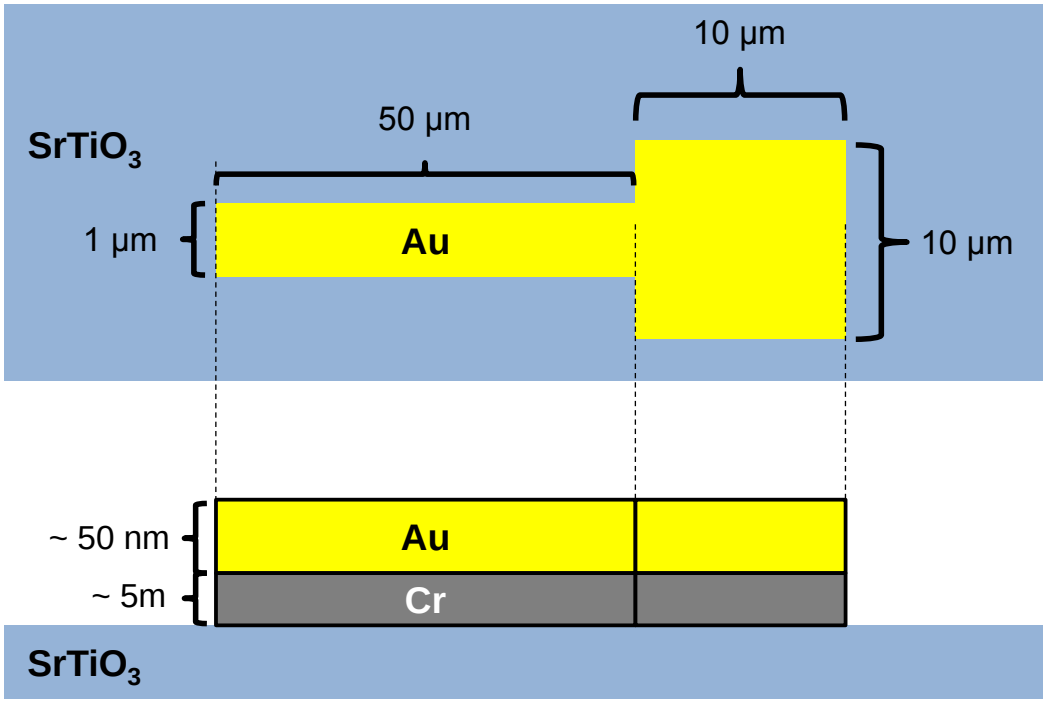

Figure 5.3 Schematic diagram of the fabricated bottom electrode.

(ZEON) for 30 seconds twice at room temperature, dry it by N_2 gas blow with air gun, and remove residual organics on the substrate by ashing (O_2 gas, 100 W, 8 seconds, at room temperature).

7) Perform successive deposition of Cr and Au electrodes by EB evaporation (< 10^{-5} Pa, at room temperature).
8) Lift it off in remover (ZDMAC, ZEON) at room temperature, wash by ultrasonication in EL acetone and in EL ethanol, and dry it by N_2 gas blow with air gun.

5.1.2 Deposition of $Ti_{0.87}O_2^{0.52-}$ nanosheets on bottom electrodes

$Ti_{0.87}O_2^{0.52-}$ nanosheets were deposited on the substrate in order to cover the bottom electrodes, in the same manner with previous chapter. The size of $Ti_{0.87}O_2^{0.52-}$ nanosheets are from 10 to 30 μm (**Figure 5.4**). So some nanosheets covered the whole area of the bottom electrode at randomly.

5.1.3 Fabrication of top electrodes

Finally, an array of Au (100 nm)/Cr (5 nm) top electrodes with 8 μm-square pads was formed (**Figure 5.5**). The following is the detail procedure.

1) Spin-coat the substrate (deposited with the nanosheet) with EB resist (ZEP-520A, ZEON) by a spin coater (4000 rpm, 60 seconds), bake it on a hot plate (180 ^oC, 15 minutes), and cool it down on another hot plate (room temperature, 1 minute). It is noted that the ultrasonication was skipped because the nanosheets were easily

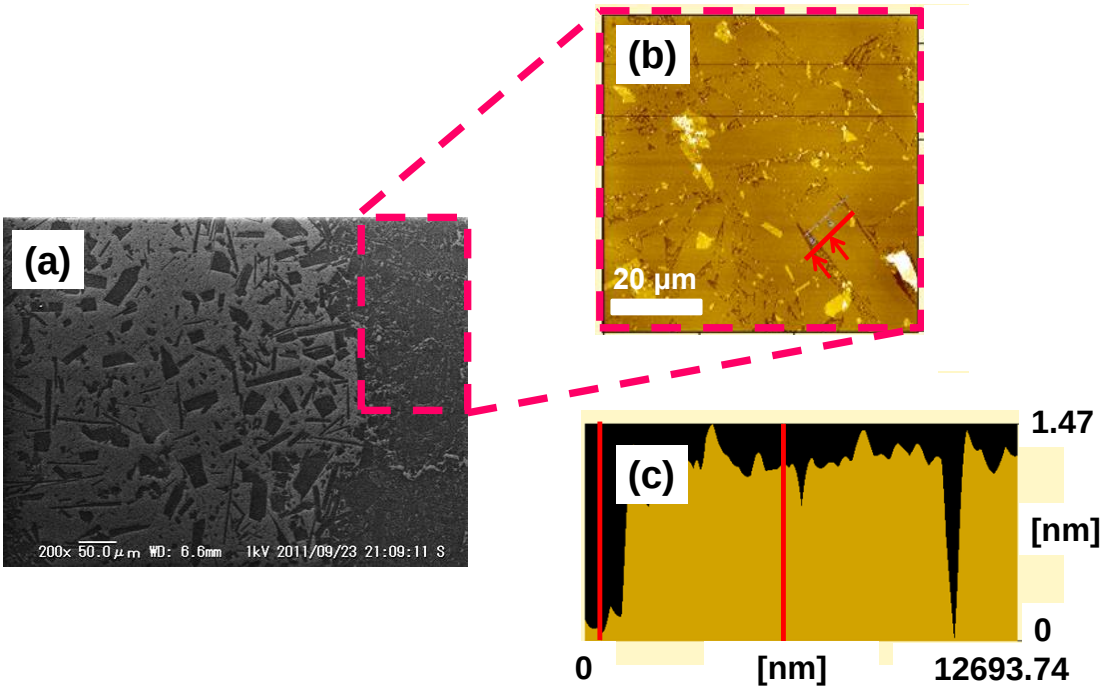

Figure 5.4 (a) SEM and (b) AFM images of $Ti_{0.87}O_2^{0.52-}$ nanosheets to observe the size and the thickness of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet for capacitor. (c) Height profile of single $Ti_{0.87}O_2^{0.52-}$ nanosheet.

peeled off from the substrate.

2) Spin-coated the substrate with antistatic agent (Espacer 300Z, SHOWA DENKO) by a spin coater (2000 rpm, 60 seconds), bake it on a hot plate (110 ^oC, 10 minutes), and cool it down on another hot plate (room temperature, 1 minute).

3) Draw the pattern of a set of 600 top electrodes (dose 26 $\mu C/mm^2 \times 4$) with electron beam.

4) Remove ESpacer 300Z by rinsing in ultrapure water, develop in ZED-N50 (ZEON) for 90 seconds, rinse in ZMD-B (ZEON) for 30 seconds twice at room temperature, and dry the substrate by N_2 gas blow with air gun.

5) Remove residual organics on the substrate by ashing (O_2 gas, 100 W, 8 seconds, at

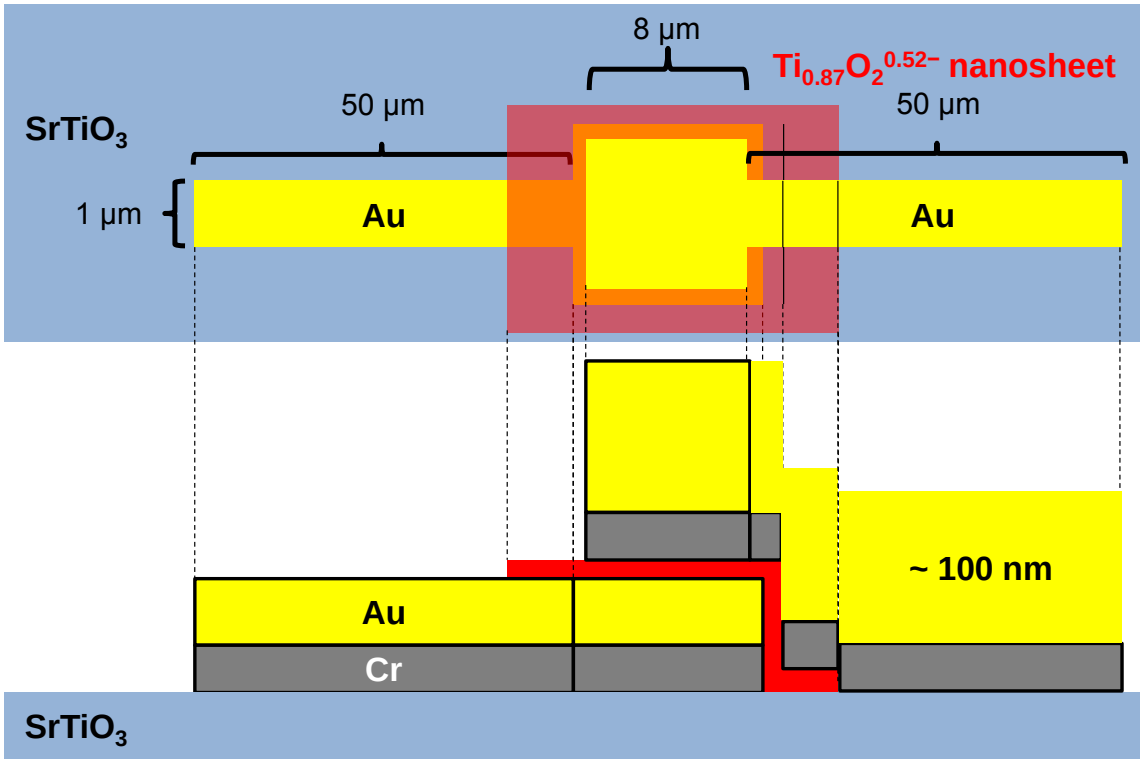

Figure 5.5 Schematic diagram of the fabricated capacitors.

room temperature).

6) Perform successive deposition of Cr and Au by EB evaporation (< 10^{-5} Pa, at room temperature).

7) Lift it off in remover (ZDMAC, ZEON), rinse in EL acetone for 30 seconds, rinse in EL ethanol for 30 seconds at room temperature, and dry it by N_2 gas blow with air gun

5.1.4 Characterization of electric and dielectric properties

Each micro-capacitor structure was observed by a scanning electron microscope (SEM) to inspect if a single nanosheet cover the whole area of the bottom electrode pad (10 μm square) without a short circuit between top and bottom electrodes.

Large 200 μm-square Au/Cr contact pads were deposited beside the micro-capacitors for electric contacts via a prober system (**Figure 5.6**).

The dielectric properties were evaluated from the capacitance in a frequency range of 10^2–10^6 Hz with a precision impedance analyzer (Agilent Technologies 4294A), and the insulating properties were evaluated from the current–voltage curves measured with a semiconductor parameter analyzer (Keithley 4200-SCS). Both measurements were performed in an electrically shielded prober system in vacuum (below 10^{-4} Pa) at room temperature.

5.2 Results and discussion

The surface roughness of the Au electrodes measured by AFM was typically 10 nm over the area of a 2 μm square (**Figure 5.7**). The typical size of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet was evaluated to be 10−30 μm in lateral size and 1.1 nm in thickness, from

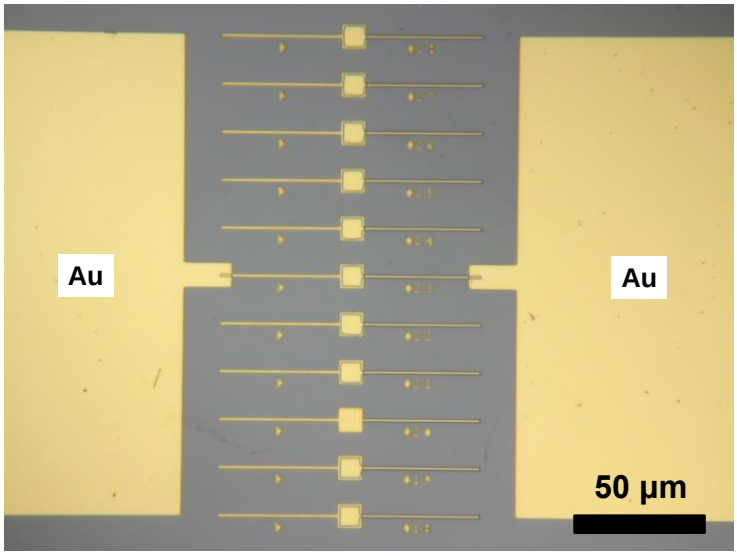

Figure 5.6 Optical microscope image of a fabricated capacitor with contact pads.

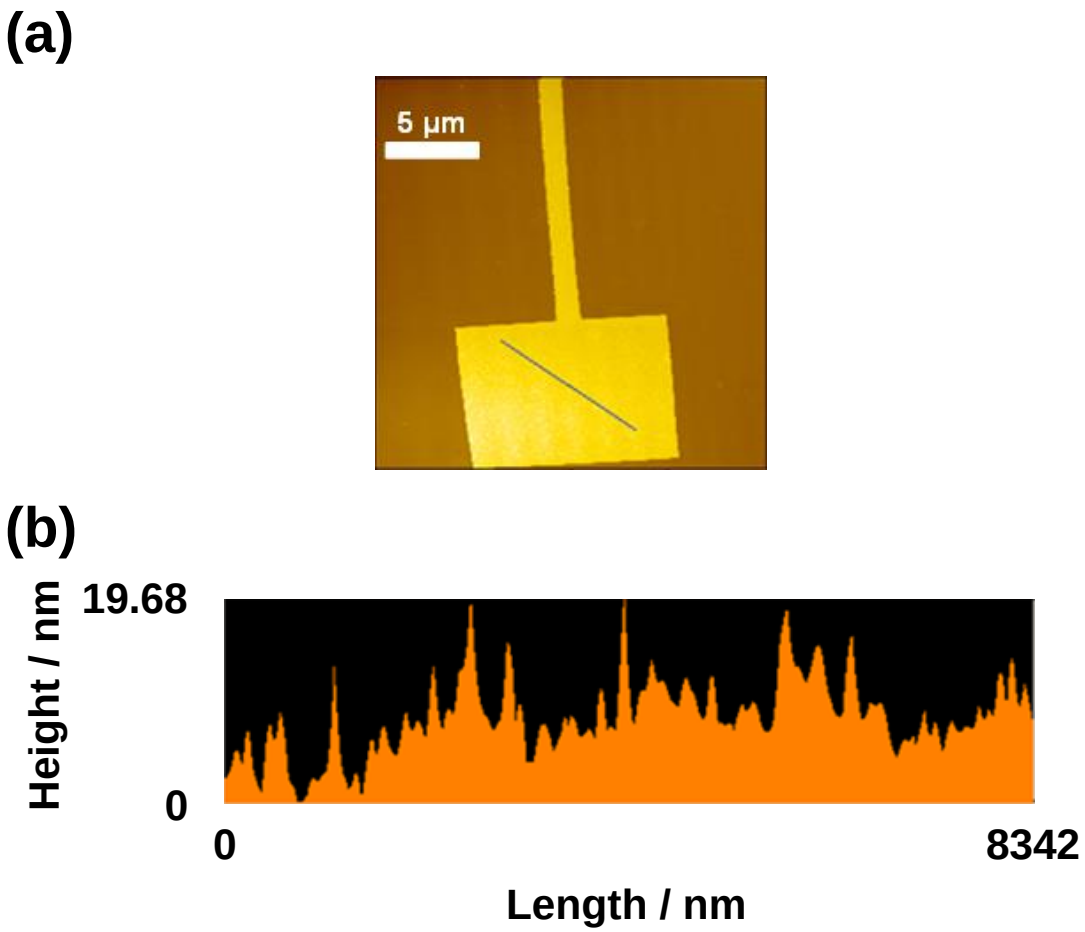

Figure 5.7 (a) Topographic image and (b) height profile of a bottom electrode.

SEM and AFM measurements (**Figure 5.4**). The observed thickness larger than 0.75 nm is due to the adsorption of H_2O, H^+, and/or NH_4^+.

Figure 5.8 shows an SEM image of Au / single nanosheet / Au micro-capacitors. Several single $Ti_{0.87}O_2^{0.52-}$ nanosheets are clearly observed with dark contrast. One bottom electrode pad was successfully covered by a single $Ti_{0.87}O_2^{0.52-}$ nanosheet, forming a gate insulator (lower micro-capacitor in **Figure 5.8**), whereas a single $Ti_{0.87}O_2^{0.52-}$ nanosheet failed to cover the other bottom electrode, leading to a short circuit between the bottom and top electrodes (upper micro-capacitor in Figure 5.8). In this study, five micro-capacitors were successfully formed without short circuits.

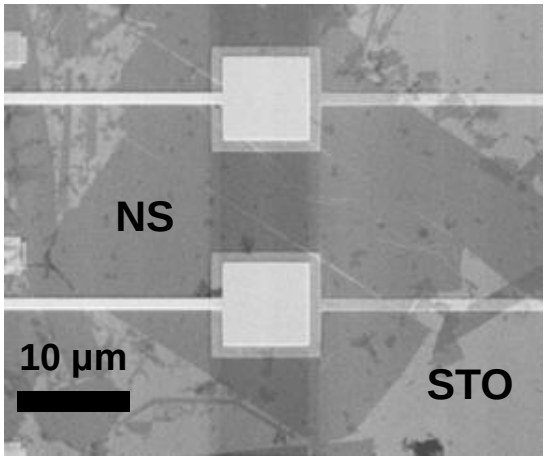

Figure 5.8 Magnified view of the micro-capacitors observed with a scanning electron microscope. Dark and light gray areas, except the electrodes, correspond to $Ti_{0.87}O_2^{0.52-}$ nanosheets (NS) and the $SrTiO_3$ (STO) surface, respectively.

Capacitance vs. frequency curves measured for these five nanosheet micro-capacitors are shown in **Figure 5.9**. Flat dispersion was observed, as already reported in multilayer of $Ti_{0.87}O_2^{0.52-}$ nanosheets.[104] However, the relative dielectric constant (ε_r) of the single $Ti_{0.87}O_2^{0.52-}$ nanosheets calculated from the capacitance ranged from 2.1 to 2.3, which is much lower than that of the multilayer of $Ti_{0.87}O_2^{0.52-}$ nanosheets. The formation of a dead layer observed in ordinary dielectric materials might be an implausible explanation for the lower ε_r in the present micro-capacitors because the nanosheet was deposited on the bottom electrode at room temperature. One possible explanation is the presence of an ultrathin air gap between the single $Ti_{0.87}O_2^{0.52-}$ nanosheet and the bottom electrode. The presence of even a 1 nm-thick air gap would lead to an ε_r value of 2.1, in good agreement with our observations in the present study.

Current density (J) vs. voltage (V) curves for the five nanosheet micro-capacitors are shown in **Figure 5.10(a)**.[104] The J–V curves were nearly identical,

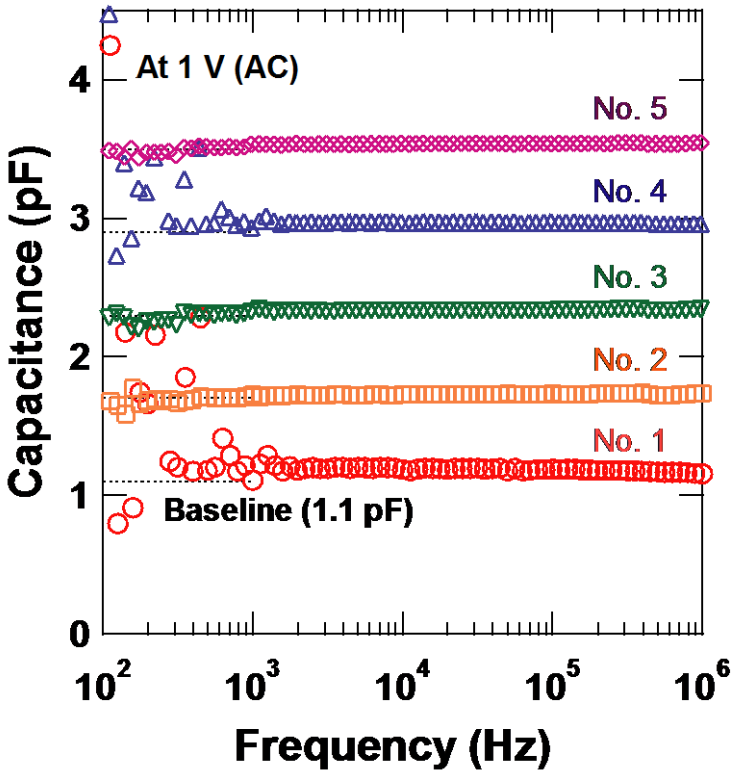

Figure 5.9 Capacitance vs. frequency curves for five micro-capacitors without short circuits. Curve Nos. 2–5 are shifted vertically for convenience. Horizontal lines denote baselines corresponding to 1.1 pF.

indicating that the fabricated nanosheet micro-capacitors showed good device yield once the single $Ti_{0.87}O_2^{0.52-}$ nanosheets were properly deposited on the bottom electrodes, as was also seen in **Figure 5.9**. **Figure 5.10(b)** shows *J*–*V* curves for a single $Ti_{0.87}O_2^{0.52-}$ nanosheet micro-capacitor (No. 1) measured five times. Again, the *J*–*V* curves were nearly identical, indicating that the nanosheet was not damaged by dielectric breakdown.[104] In **Figure 5.10**, *J* was almost constant at ~10^{-8} A/cm2 at $V <$ 2.2 V, whereas it abruptly increased above 2.2 V. At the withstand voltage of the single nanosheet, the electric field strength across the gate insulator corresponds to 20 MV/cm, even assuming that the thickness of the gate insulator was 2.1 nm (= nanosheet 1.1 nm +

air gap 1.0 nm). This value is considerably superior to that of a conventional SiO_2 gate insulator, typically 10 MV/cm. The possible reason why a single $Ti_{0.87}O_2^{0.52-}$ nanosheet repeatedly endures extremely high electric field is that a single nanosheet is crystallite, not amorphous like thermally oxidized silicon.

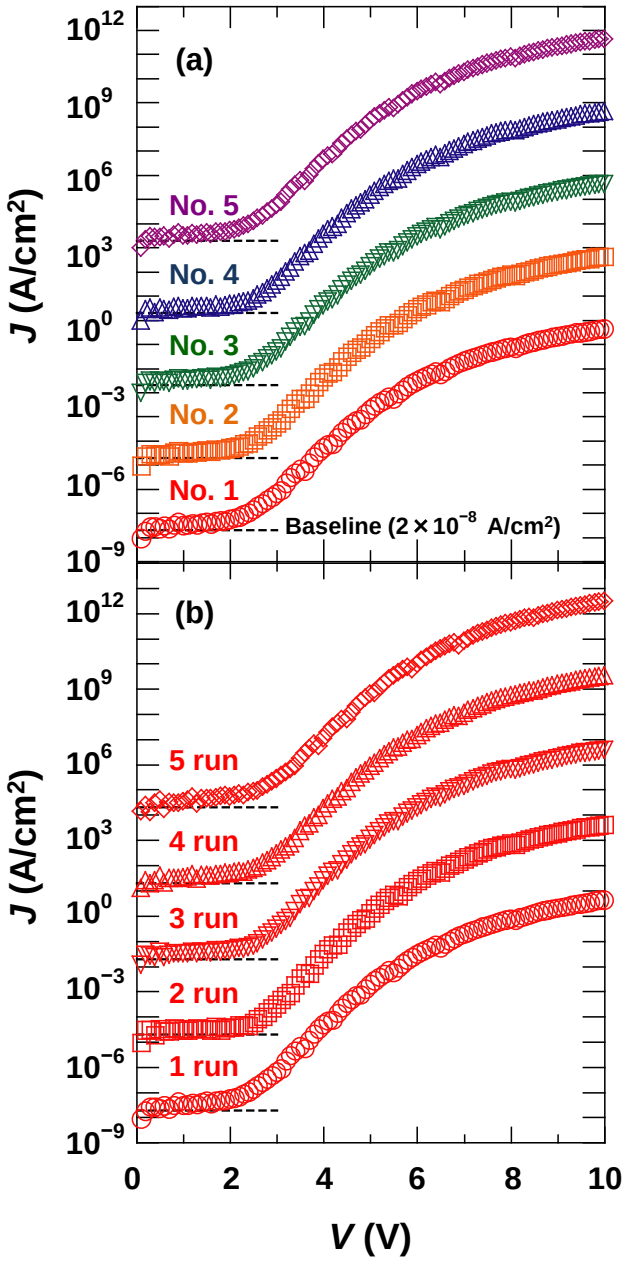

Figure 5.10 (a) Current density (*J*) vs. applied voltage (*V*) curves for the five micro-capacitors. (b) *J* vs. *V* curves measured in five runs for one micro-capacitor (No. 1). Curves for device Nos. 2–5 in (a) and runs 2–5 in (b) are shifted vertically for convenience. Horizontal lines denote baselines corresponding to 2×10^{-8} A/cm^2.

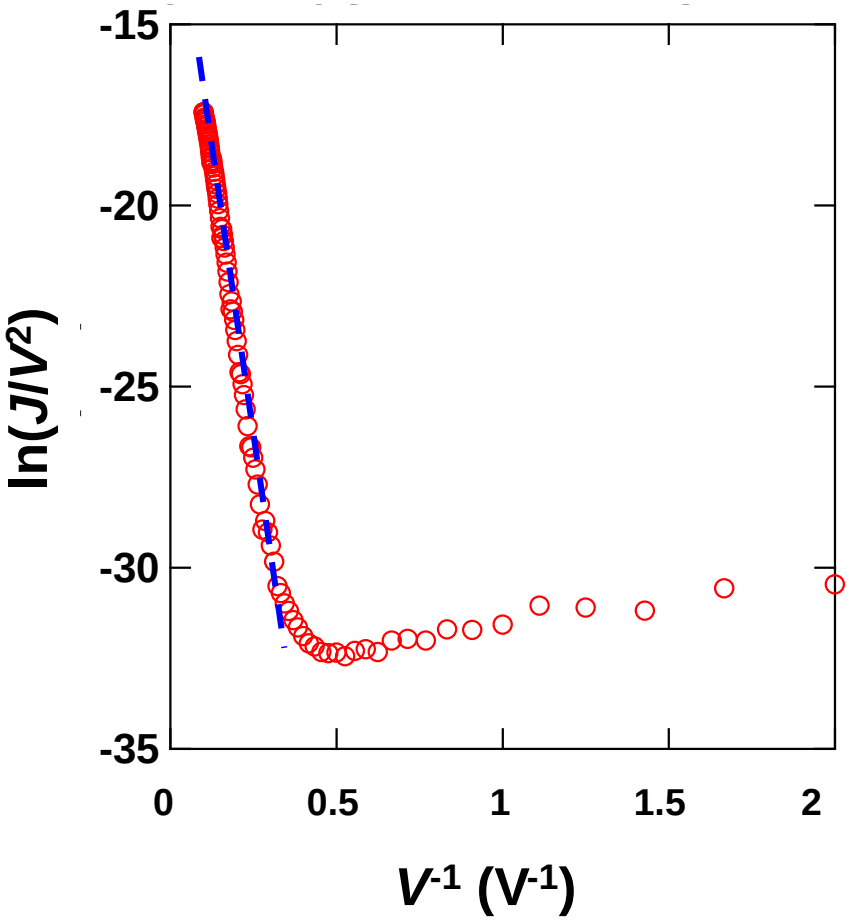

Figure 5.11 ln(*J*/*V*) vs. V^{-1} plot of the data for device No. 1 in (a).

Figure 5.11 is a plot of ln(I/V^2) against V^{-1}. In the higher voltage region of V^{-1} < 0.3 (V > 3.5 V), the points lie on a straight line with a slope of -50, indicating that the electric conduction is described by Fowler-Nordheim Tunneling mechanism.[105]

$$J = \frac{e^3E^2}{4h\Phi}\exp\left(\frac{-16\pi^2\sqrt{2m\Phi^3}}{3heE}\right) \quad (1)$$

J is the current density, *E* is the electric field (*E = V/d*, *V* is the applied voltage and *d* is the thickness of tunnel barrier), ϕ is the barrier height. *h* is the Planck's constant, *e* is the charge of electron, and *m* is the mass of free electron. By substituting *d* = 2.1 nm (nanosheet 1.1 nm + air gap 1.0 nm) into Eq.(1), the barrier height is calculated as 2.3 eV, and indeed the current density began to increase abruptly over 2.3 V (see **Figure 5.10**). Because the work function of gold, electron affinity of the $Ti_{0.87}O_2^{0.52-}$ nanosheet, and band gap of a single $Ti_{0.87}O_2^{0.52-}$ nanosheet are 5.1 eV,[106] 4.1 eV,[77] and 3.8 eV,[70] respectively, the barrier height should be less than 1.3 eV assuming no air gap and/or organic impurity at nanosheet / electrode interface. The possible reason why a single $Ti_{0.87}O_2^{0.52-}$ nanosheet repeatedly endures extremely high electric field is that a single nanosheet is crystallite, not amorphous like thermally oxidized silicon. **Table 5.1** is the comparison between a single $Ti_{0.87}O_2^{0.52-}$ and ultra-thin SiO_2 as insulator. Clearly seen in Table 5.1, a single nanosheet is quite promising as ultra-thin gate insulator.

Table 5.1 the comparison between a single $Ti_{0.87}O_2^{0.52-}$ and ultra-thin SiO_2 as insulator.

	$Ti_{0.87}O_2^{0.52-}$ Nanosheet	**SiO_2 (thermally oxidized)**
Achievable *E*	> 20 MV/cm	10 MV/cm
***J* at 1 V**	< 10^{-7} A/cm^2	3 nm : ~ 10^{-7} A/cm^2 2 nm : ~ 10^{-1} A/cm^2
ε_r	Multi-layer : 125 Single-layer : 2.4	3.9

5.3 Summary of this chapter

I investigated the dielectric and insulating properties of single $Ti_{0.87}O_2$ nanosheet micro-capacitors fabricated by electron beam lithography. A single nanosheet covering the whole of the bottom electrode pad reproducibly worked as a gate insulator with a very high electric field endurance of $\geq$ 20 MV/cm. A single $Ti_{0.87}O_2$ nanosheet is a promising gate insulator because of its extremely small thickness, high electric field endurance, and easy deposition on various substrates such as single crystals and epitaxial thin films at room temperature, i.e. without high temperature process.

Chapter 6 Fabrication of top gate FET

In this chapter, I describe the fabrication of the top gate FETs. The reason why I started from the top gate FETs is because the channel area can be smaller than the size of a single nanosheet in the structure, ultimately.

First of all, I tried to fabricate the top gate FET with conventional SiO_2 gate insulator in order to check whether the other components of the FET work or not (**Figure 6.1(a)**). Secondly, I moved to trial to fabricate the top gate FET with nanosheet gate insulator (**Figure 6.1(b)**). However, the fabricated FETs didn't work due to the shortcut between source/drain and gate electrode. Since the cause of the shortcut was considered as the bending of nanosheets, I tried to bury the source and drain electrodes in the substrate (**Figure 6.1(c)**).

6.1 With conventional SiO_2 gate insulator

First of all, I tried to fabricate the top gate FET with conventional SiO_2 gate insulator in order to check whether the other components of the FET work or not (**Figure 6.2**).

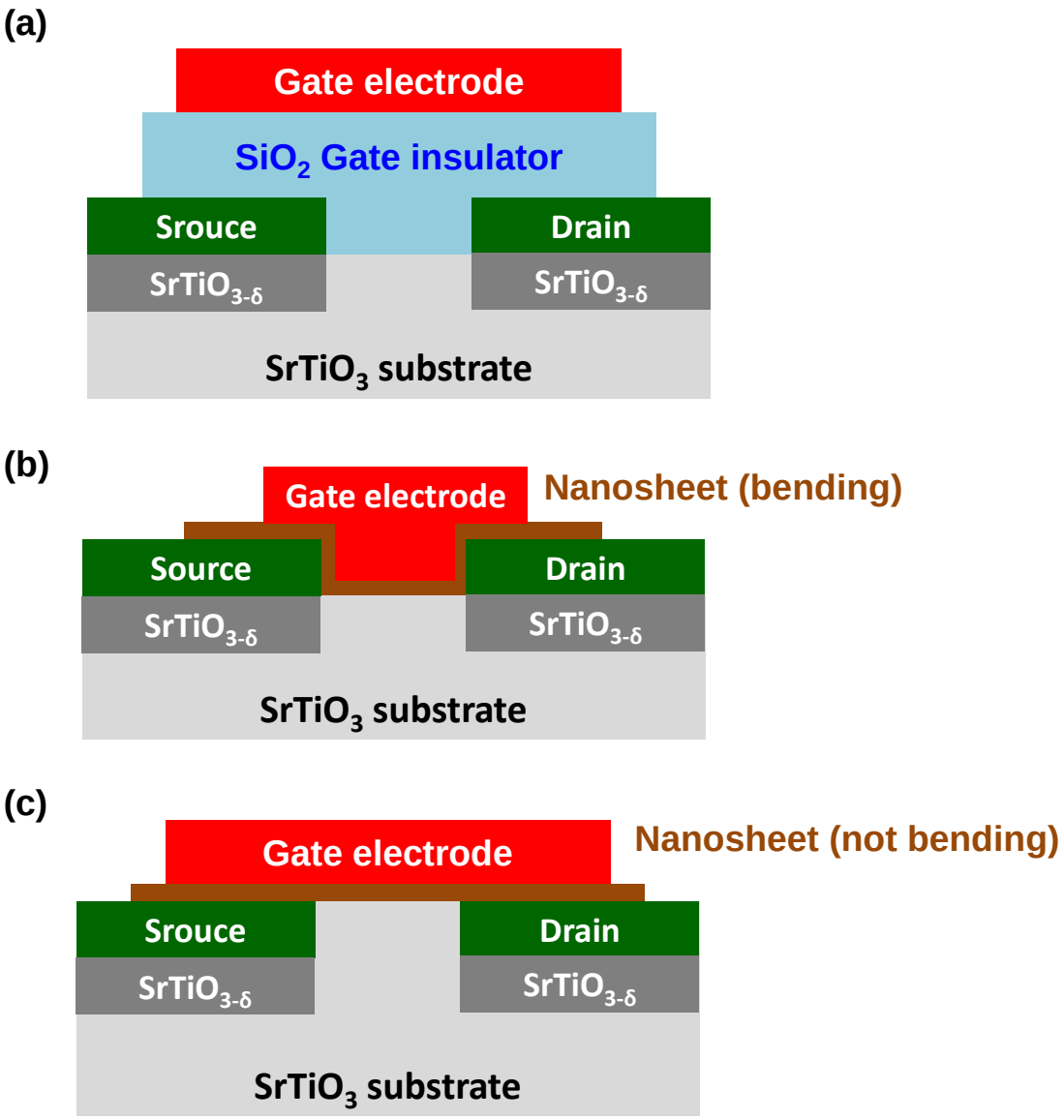

Figure 6.1 Three kinds of the structures of fabricated top gate FETs. **(a)** with conventional SiO_2 gate insulator. **(b)** with bending nanosheet gate insulator. **(c)** with buried source and drain electrodes and not bending nanosheet gate insulator.

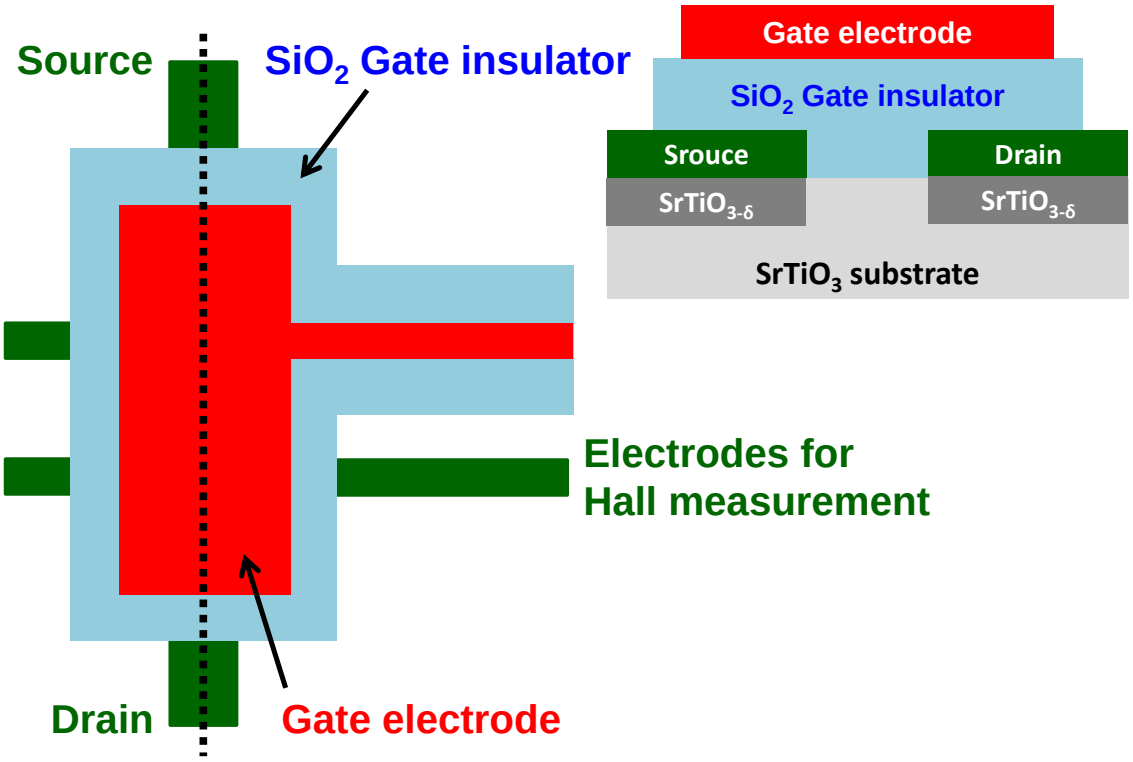

Figure 6.2 Schematic diagram of top gate FET.

6.1.1 Experimental

As a substrate for the top gate FET, I used a $SrTiO_3$ single crystal with a step and terrace (100) surface (15 × 15 × 0.5 mm^3) made by SHINKOSHA. As shown in Figure 6.1, FET structure is gate electrode / single $Ti_{0.87}O_2$ nanosheet gate insulator / $SrTiO_3$. The $SrTiO_3$ as the semiconductor channel was highly insulating, with a resistivity of > 10^7 Ω cm. With the application of positive (negative) gate voltage, electron carriers at $SrTiO_3$ surface was expected to be accumulated (depleted). We fabricated 54 FETs. The detail arrangement of FETs on $SrTiO_3$ is shown in **Figure 6.3**. One FET contains six electrodes: green square pads correspond to source, drain, and Hall effect electrodes, and red square pads correspond to gate electrode. In between the six electrodes, gate electrode / single $Ti_{0.87}O_2$ nanosheet gate insulator / $SrTiO_3$ trilayer

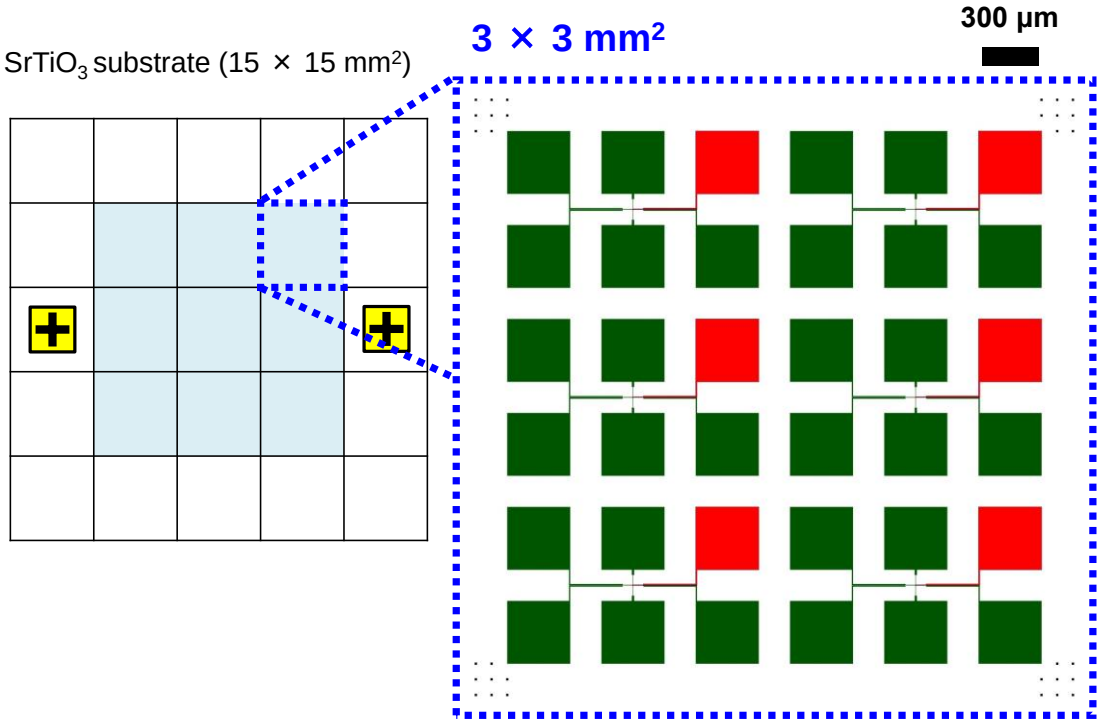

Figure 6.3 Patterns of fabricated devices and markaers.

was located. We describe below the detail fabrication procedures for each FET component.

6.1.1.1 Creation of alignment and chip markers

On the substrate, a set of alignment markers (two substrate markers and an array of the chip markers) were fabricated. The markers, Au (100 nm)/Cr (20 nm), were formed by EB lithography, ashing, EB evaporation, and lift off (**Figure 6.4**). The processes are the same with 5.1.1.

6.1.1.2 Fabrication of source and drain electrodes

On the substrate, an array of Au (50 nm)/Ti (20 nm)/$SrTiO_{3-\delta}$ source and drain

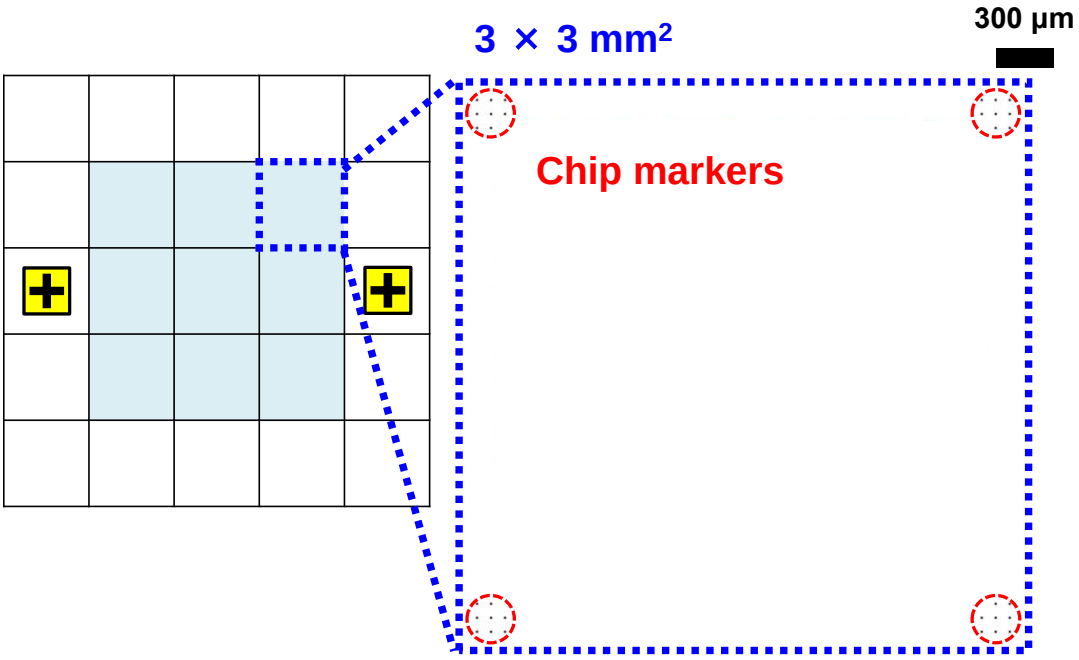

Figure 6.4 Patterns of alignment markers and chip marks.

electrodes was formed by EB lithography, ashing, dry etching by Ar^+, EB evaporation, and lift off (**Figure 6.5**). The following is the detail procedure. From Process No. 1 to No. 5 were the same with 5.1.1.Remove residual organics on the substrate by ashing (O_2 gas, 100 W, 8 seconds, room temperature) and etch the surface by Ar^+ induced coupled plasma (300 W, 300 seconds), according to the etching rate of $SrTiO_3$ by Ar^+ irradiation as shown in **Figure 6.6**.

7) Perform successive deposition of Ti and Au by EB evaporation (< 10^{-5} Pa, at room temperature).

8) Lift off in remover (ZDMAC, ZEON), rinse in EL acetone for 30 seconds twice, and dry the substrate by N_2 gas blow with air gun.

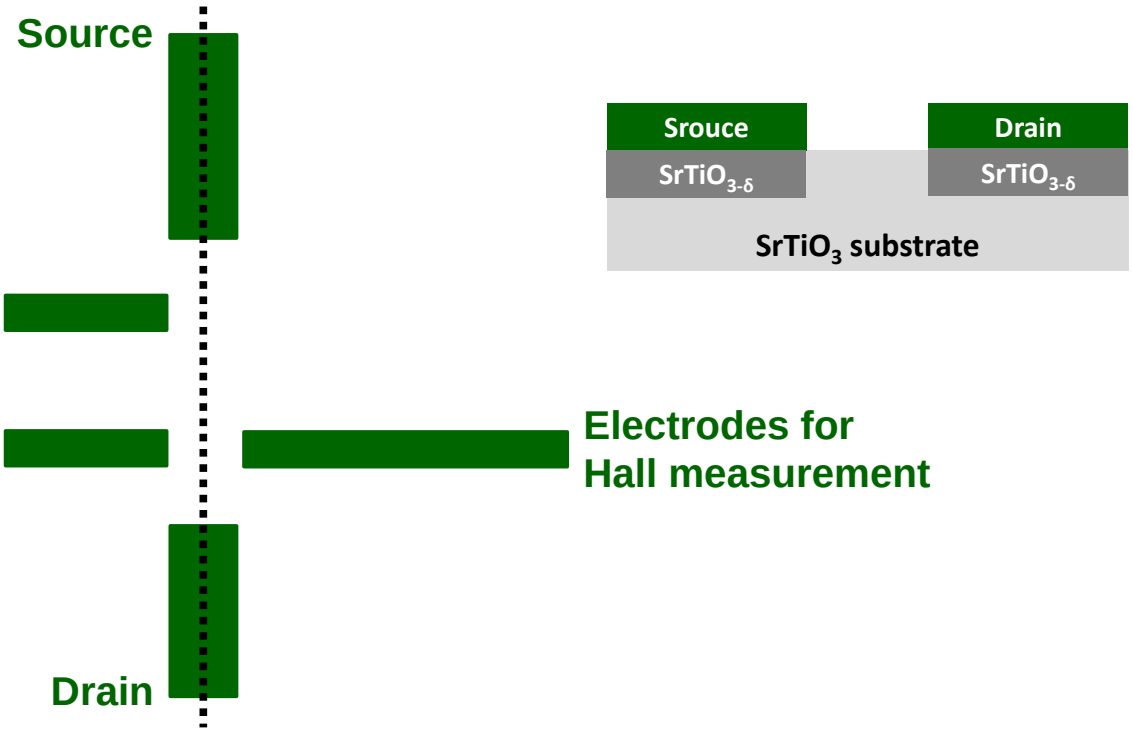

Figure 6.5 Schematic diagram of source and drain electrodes.

6.1.1.3 Deposition of SiO_2 gate insulator on the $SrTiO_3$ substrate

On the substrate, an array of SiO_2 (150 nm) gate insulator was formed by EB lithography, ashing, EB evaporation, and lift off (**Figure 6.7**). The following is the

detail procedure. From process No.1 to No. 6 were the same with 5.1.1.

7) Perform EB evaporation of SiO_2 (< 10^{-5} Pa, at room temperature).

8) Lift off in remover (ZDMAC, ZEON), rinse in EL acetone for 30 seconds twice, and dry the substrate by N_2 gas blow with air gun.

6.1.1.4 Fabrication of gate electrodes

Finally, an array of Au (100 nm)/Cr (15 nm) gate electrodes was formed (**Figure 6.1**). The following is the detail procedure. From process No.1 to No. 6 were the same with 5.1.1.

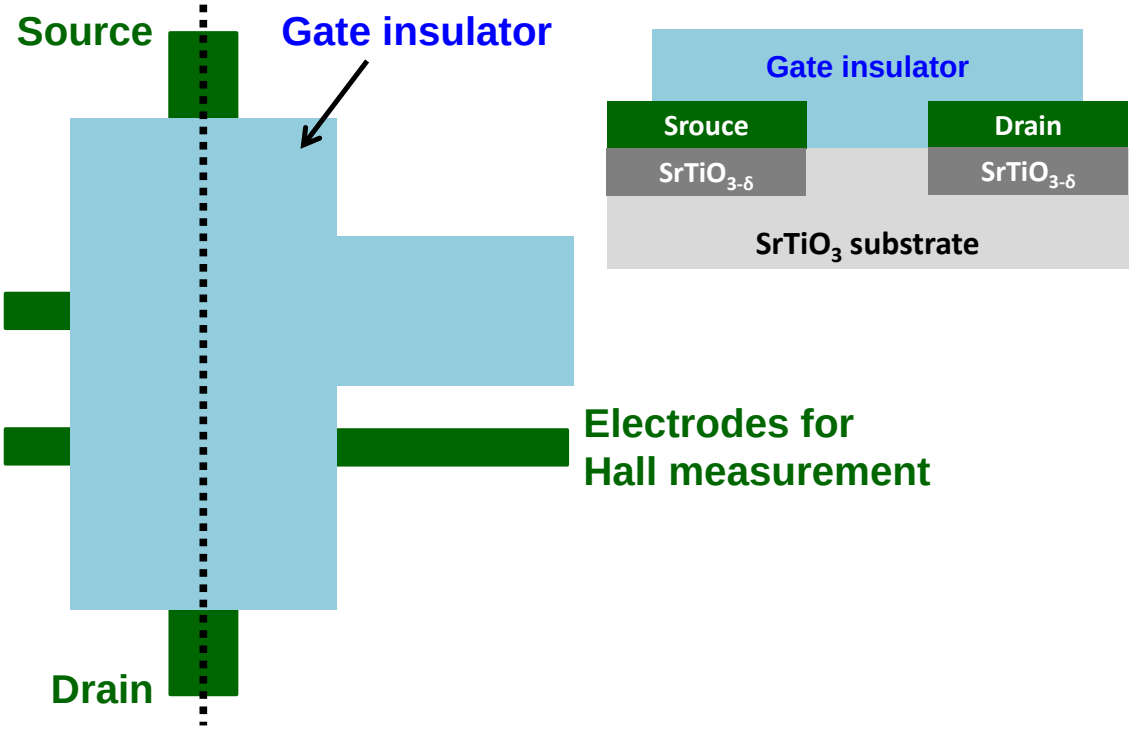

Figure 6.7 Schematic diagram of SiO_2 gate insulator and source/drain electrodes.

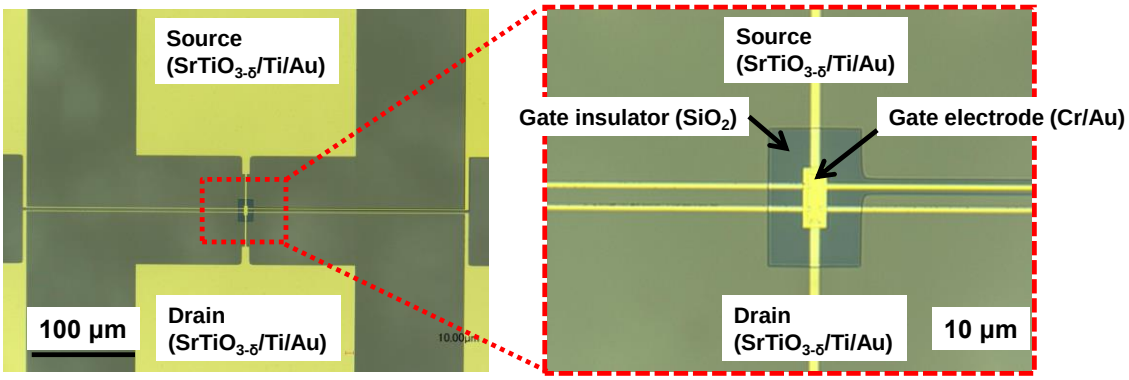

Figure 6.8 Optical microscope image of the fabricated top gate FET with SiO_2 gate insulator.

7) Perform EB evaporation of SiO_2 (< 10^{-5} Pa, at room temperature).
8) Lift off in remover (ZDMAC, ZEON), rinse in EL acetone for 30 seconds twice, and dry the substrate by N_2 gas blow with air gun.
9) Observe by an optical microscope to confirm the process (**Figure 6.8**). The SiO_2 layer perfectly covered the channel and separated the gate electrode from the substrate.

6.1.2 Results and discussion

The fabricated devices worked as the FETs (**Figure 6.9**). As the gate voltage increased, the current through the channel increased since the electrons were accumulated at the surface of the $SrTiO_3$ substrate.

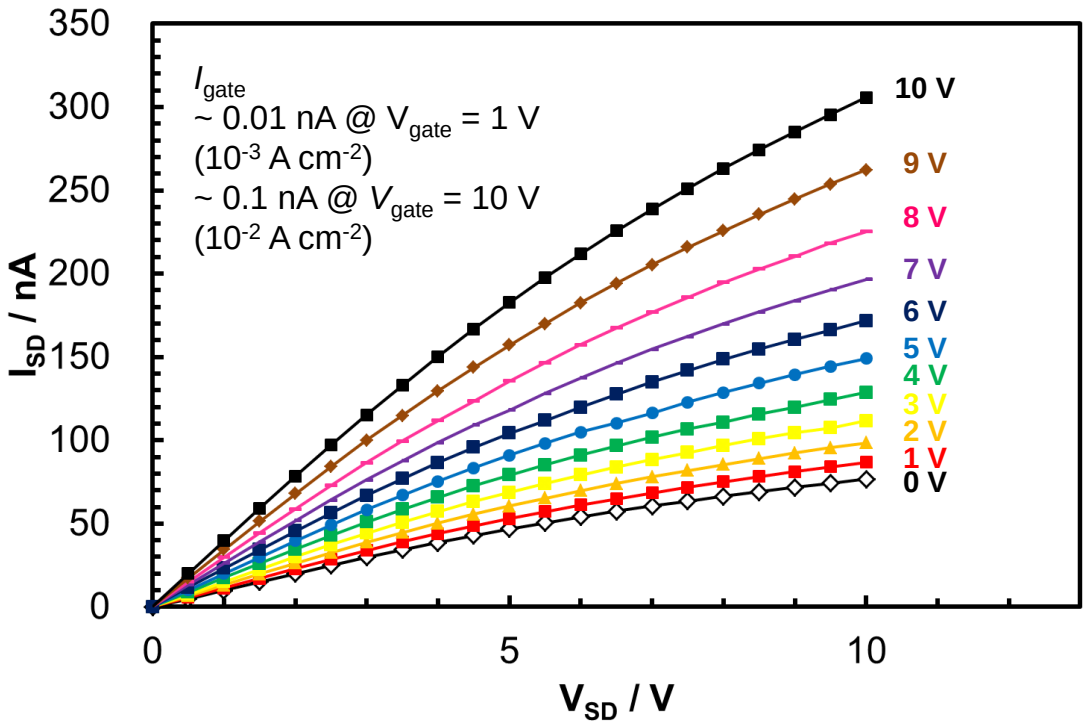

Figure 6.9 Current between source and drain (I_{SD}) vs. Voltage between source and drain (V_{SD}) plot of the fabricated top gate FET with SiO_2 gate insulator.

6.2 With nanosheet gate insulator

本節については、５年以内に雑誌等で刊行予定のため、非公開。

6.3 With buried source and drain

Thirdly, I tried to fabricate the top gate FET with buried sources and drains, in order to deposit nanosheets on the flatter surface (**Figure 6.15**). As a substrate for the top gate FET, I used a $SrTiO_3$ single crystal with a step and terrace (100) surface (15 × 15 × 0.5 mm^3) made by SHINKOSHA, intending that the surface of the substrate works

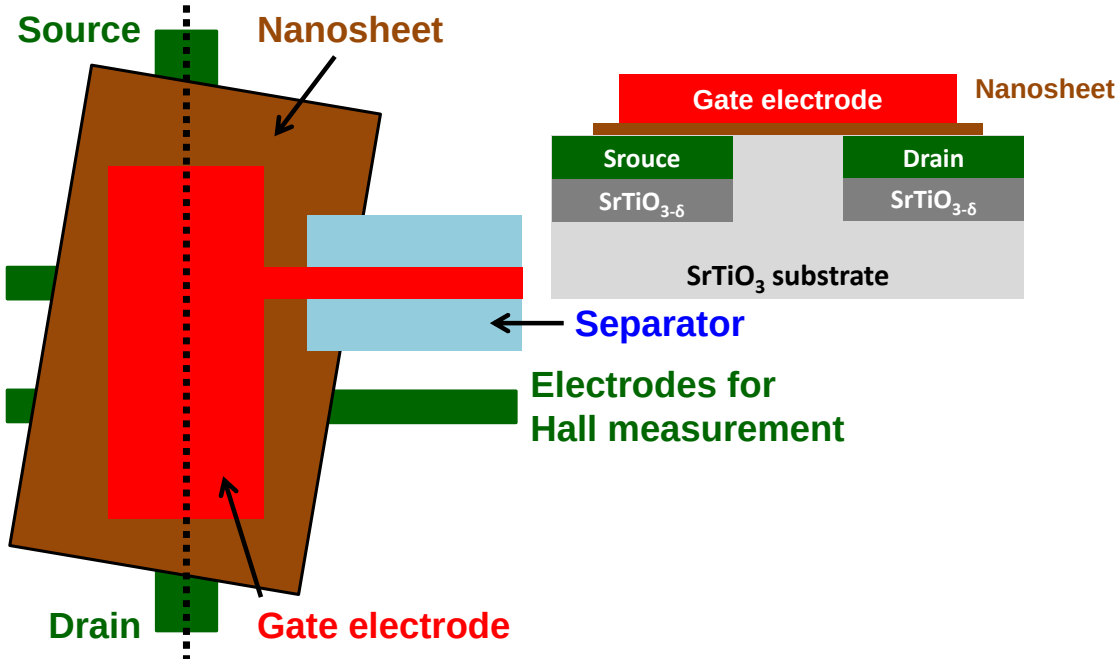

Figure 6.15 Schematic diagram of fabricated top gate FET with buried source and drain.

as the channel. The substrate was highly insulating, with a resistivity of > 10^7 Ω cm.

6.3.1 Experimental

6.3.1.1 Creation of alignment markers

On the substrate, a set of alignment markers (two substrate markers and an array of chip markers) were fabricated in the same manner described in previous session.

6.3.1.2 Fabrication of source and drain electrodes

In the substrate, an array of Au (50 nm)/Ti (20 nm)/$SrTiO_{3-\delta}$ source and drain electrodes was formed by EB lithography, ashing, dry etching by Ar^+, EB evaporation,

and lift off, by using thick EB resists. To be more precise,

1) Wash the substrate by ultrasonication in EL acetone for 5 minutes, in EL ethanol for 5 minutes, and then dry the substrate by N_2 gas blow with air gun
2) Spin-coat EB resist (OEBR-CAP112, TOKYO-OUKA) (2000 rpm, 60 seconds), bake the substrate on a hot plate (110 ^oC, 5 minutes), and then cool down the substrate on another hot plate (room temperature, 1 minute)
3) Spin-coat antistatic agent (Espacer AX, SHOWA DENKO) (2000 rpm, 60 seconds), bake the substrate on a hot plate (110 ^oC, 10 minutes), and then cool down the substrate on another hot plate (room temperature, 1 minute)
4) Draw the pattern of a set of 54 source and drain electrodes (Dose 6 $\mu C/mm^2$)
5) Bake the substrate on a hot plate (110 ^oC, 90 seconds)
6) Develop in 2.38 wt.% tetramethylammonium hydroxide for 60 seconds at room temperature. At the same time, Espacer AX was removed. And then rinse in ultrapure water for 30 seconds at room temperature two times. Finally dry the substrate by N_2 gas blow with air gun.
7) Bake the substrate on a hot plate (110 ^oC, 60 seconds), and confirm the pattern by an optical microscope.
8) Remove residual organics on the substrate by ashing (O_2 gas, 100 W, 8 seconds, room temperature) and etch the surface by Ar^+ induced coupled plasma (300 W, 300 seconds), according to the etching rate of $SrTiO_3$ by Ar^+ irradiation as shown in **Figure 6.6**.
9) Perform successive EB evaporation of Ti and Au (< 10^{-5} Pa, at room temperature).
10) Lift off in remover (HAKURI-EKI, ZEON), rinse in EL acetone for 30 seconds twice, and dry the substrate by N_2 gas blow with air gun.

11) Observe by an optical microscope to confirm the process succeeded.

6.3.2 Results and discussion

By AFM observation, the formation of burr was observed. (**Figure 6.16**) This formation is from the side etch of EB resist and following EB deposition. I tried to remove this burr by Ar^+ dry etching, but not only burr but also electrodes were etched. (**Figure 6.17**). Although I tried to fabricate top gate FET with burr (**Figure 6.18**), the device didn't work due to the shortcut between source/drain and gate electrodes. (**Figure 6.19**)

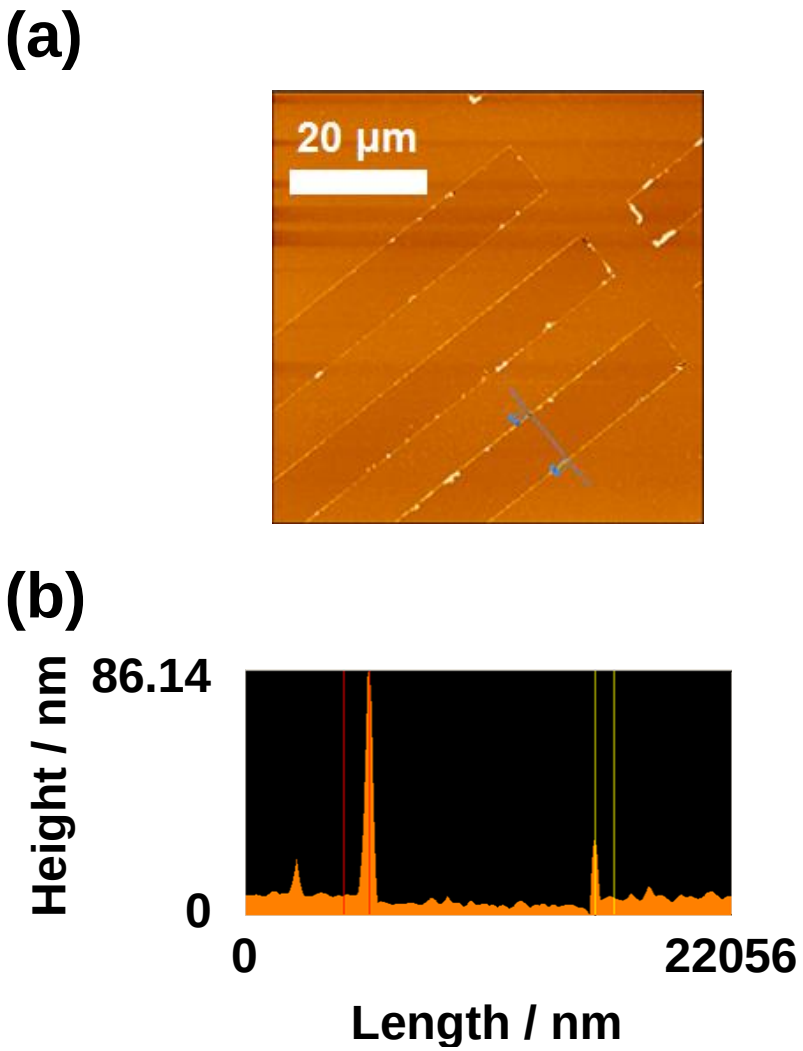

Figure 6.16 (a) Topographic image and (b) height profile of the burr between the substrate and the electrodes before Ar^+ dry etching.

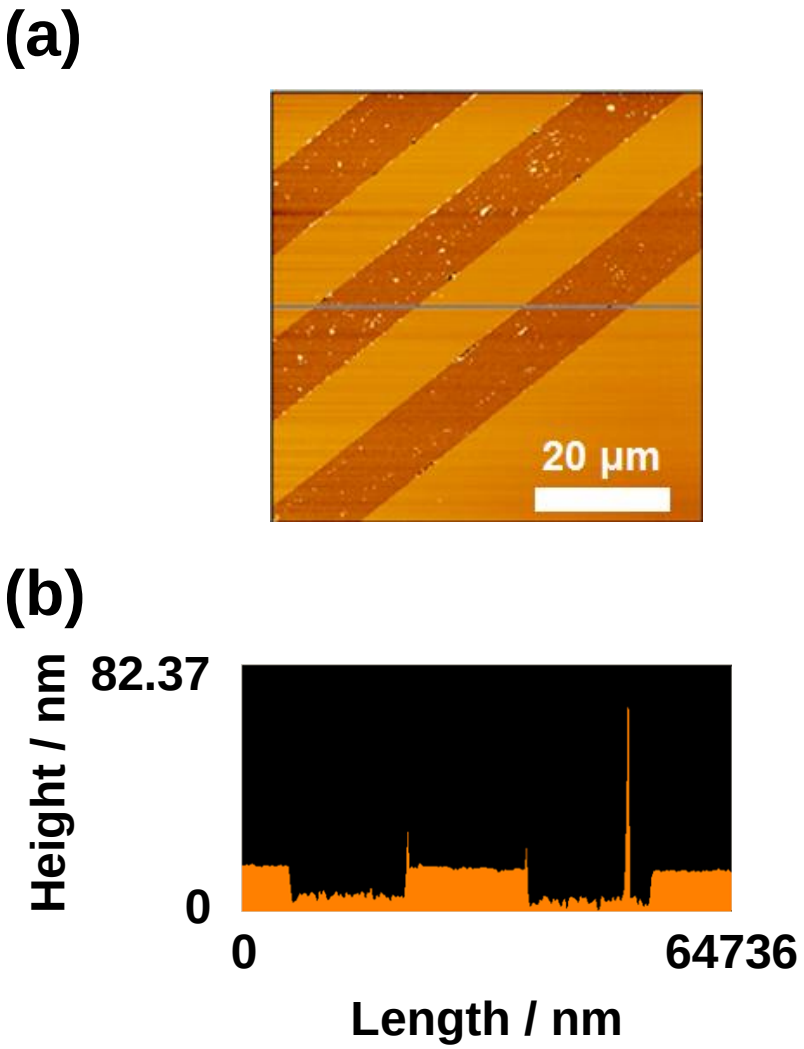

Figure 6.17 (a) Topographic image and (b) height profile of the burr between the substrate and the electrodes after Ar^+ etching.

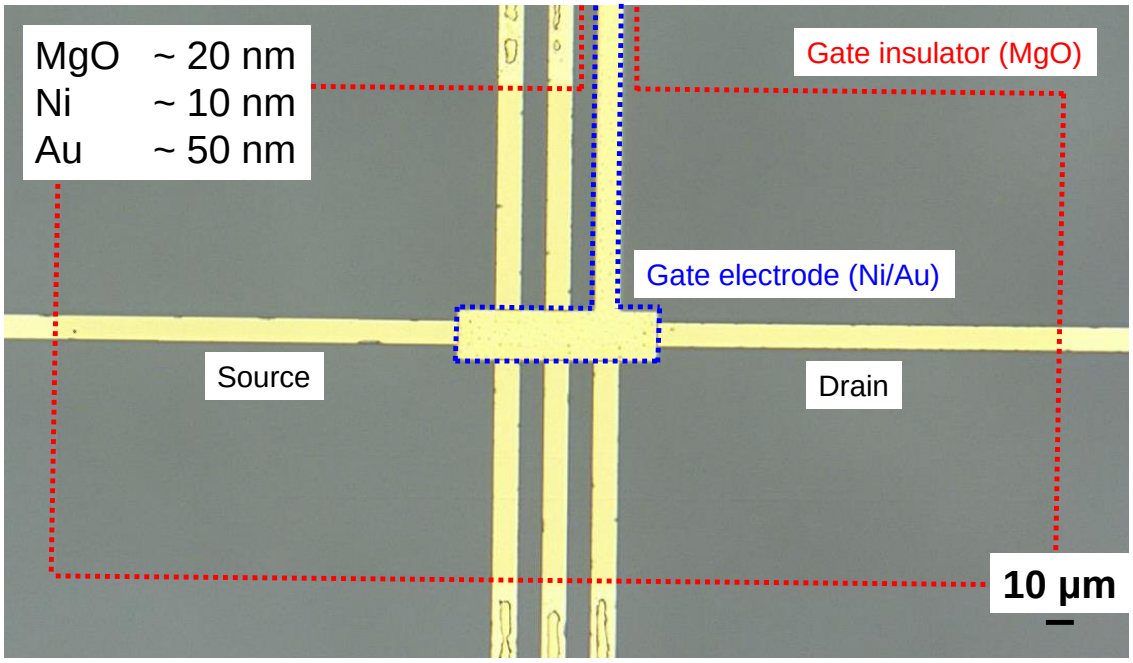

Figure 6.18 Optical microscope image of the fabricated top gate FET with buried source and drain.

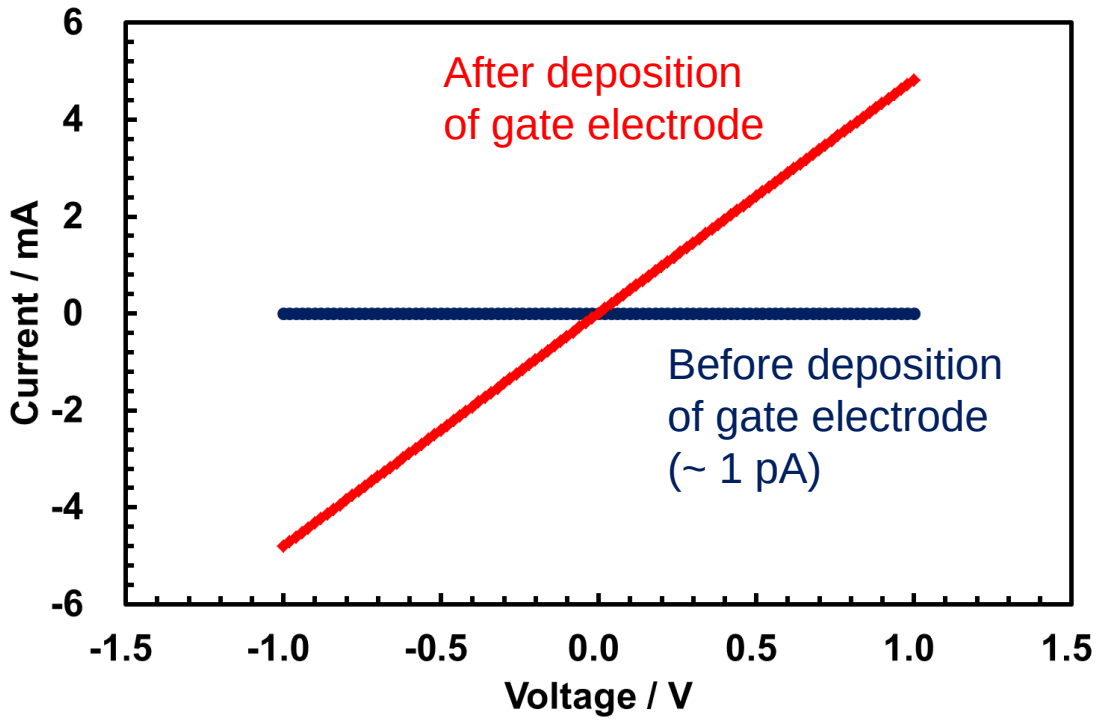

Figure 6. 19 I-V plot showing the shortcut between source/drain and gate electrodes.

6.4 Summary of this chapter

In top gate FETs, nanosheets did not provide enough insulation between semiconductor and gate electrode. In top gate FETs, bended nanosheets at the edge of electrode could be an origin of leakage current path.

Chapter 7 Fabrication of bottom gate FETs

In previous chapter, I figured out making flat surface suitable for deposition of nanosheets in the processes for top gate FET. Therefore, in this chapter, I tried to fabricate bottom gate FETs. (**Figure 7.1**) Firstly I tried to fabricate the bottom gate FET with conventional SiO_2 gate insulator in order to check whether the other components of the FET work or not. As the next step, I moved to trial to fabricate the bottom gate FET with nanosheet gate insulator.

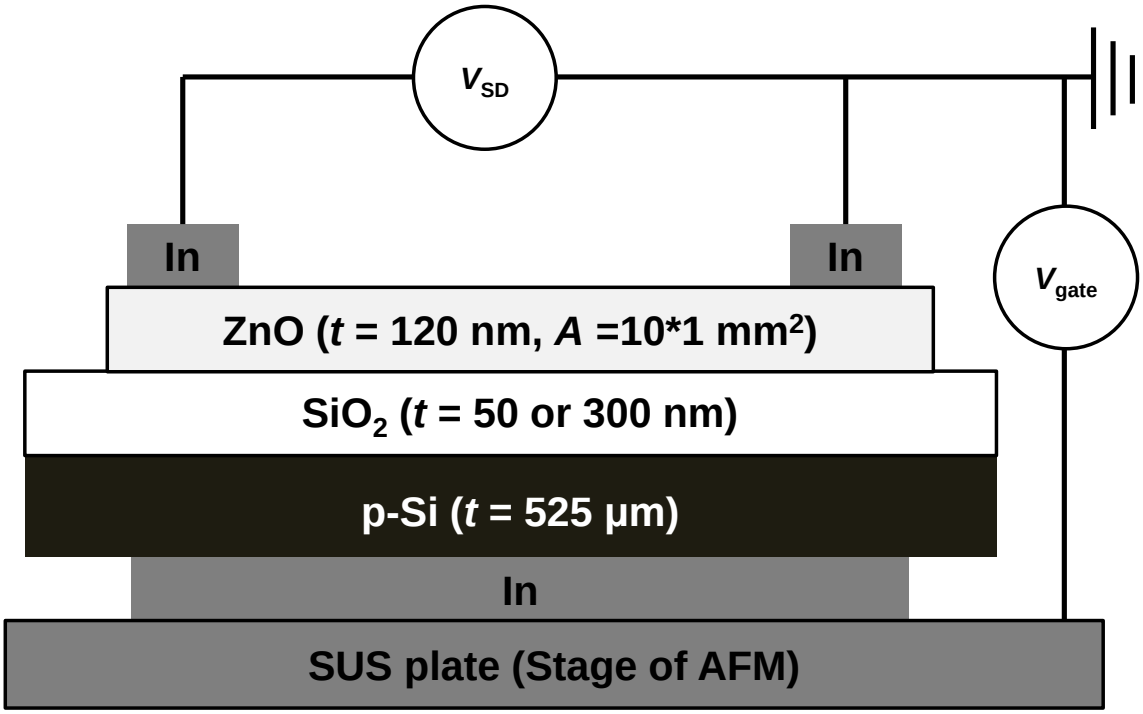

Figure 7.1 Schematic diagram of fabricated bottom gate FET with SiO_2 gate insulator.

7.1 With SiO_2 gate insulator

7.1.1 Experimental

Heavily doped silicon substrate (525 μm thick, p^{++}), whose surface is thermally oxidized (50 nm thick of SiO_2) was used for gate electrode and gate insulator, respectively. To be more precise,

1) Cut the substrate ($20 \times 30 \times 0.525$ mm^2)
2) Wash the substrate by ultrasonication in EL acetone for 5 minutes, ultrasonication in EL ethanol for 5 minutes, and then dry the substrate by N_2 gas blow with air gun
3) Deposition of sputtered ZnO thin film (Total pressure of argon and oxygen was 20 mTorr, partial oxygen pressure was 3×10^{-5} Torr, at room temperature, 380 seconds) through IC gage board (500 × 1000 μm^2)
4) Put indium chip as source and drain electrodes on ZnO thin film

7.1.2 Results and discussion

The fabricated devices worked as the FETs up to 7 MV/cm of electric field applied to SiO_2 gate insulator. (**Figure 7.2**) I also tested ultra-flat indium-tin-oxide substrate (**Figure 7.3**) with 150 nm thick of SiO_2 (deposited by EB evaporation) as gate electrode and gate insulator, and the devices also worked as the FETs.

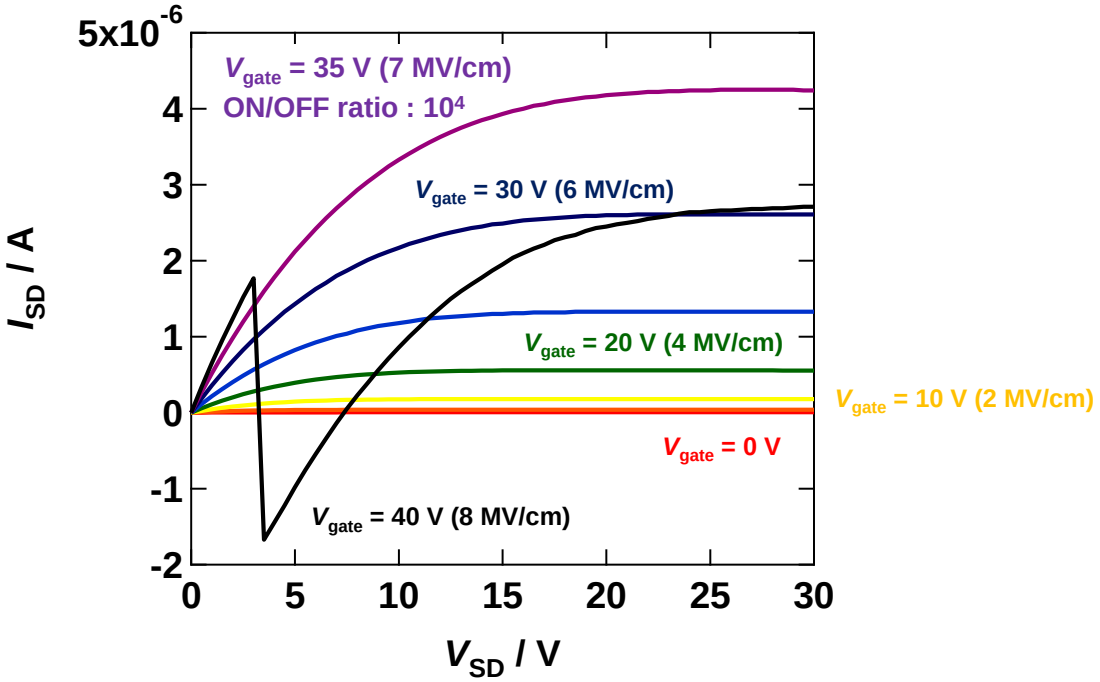

Figure 7.2 Current between source and drain (I_{SD}) vs. Voltage between source and drain (V_{SD}) plot of the fabricated bottom gate FET with SiO_2 gate insulator.

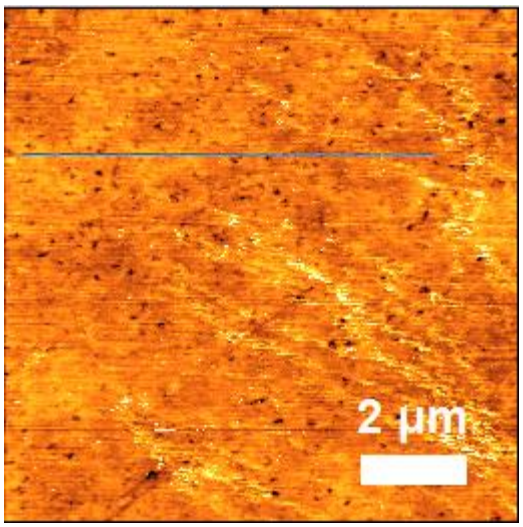

Figure 7.3 AFM image of ITO substrate used in this research. The roughness was about 0.5 nm.

7.2 With nanosheet gate insulator

本節については、５年以内に雑誌等で刊行予定のため、非公開。

Chapter 8 Summary of this thesis

In this thesis, aiming to the application of oxide nanosheets with high ε_r as a gate insulator, insulating and dielectric properties of $Ti_{0.87}O_2^{0.52-}$ nanosheet were investigated by observation with C-AFM and by fabrication of micro-capacitors. From the results of the C-AFM, it was qualitatively revealed that even a single $Ti_{0.87}O_2^{0.52-}$ nanosheet behaves as an insulator. Moreover, from the results of electrical and dielectric measurements of the micro-capacitor, it was quantitatively revealed that even a single $Ti_{0.87}O_2^{0.52-}$ nanosheet behaves as an insulator, although the evaluated ε_r was lower than that of multi-layer due to the air gap between a single nanosheet and electrodes. A single $Ti_{0.87}O_2^{0.52-}$ nanosheet covering the whole of the bottom electrode pad reproducibly worked as an insulator with very high electric field endurance.

Based on the results that even a single nanosheet is insulating, both top and bottom gate FETs by using dielectric nanosheet as insulator were developed. However, until now, FETs with enough insulation between semiconductor channel and gate electrode have not been obtained. Therefore, as future works, proper processes to ensure high insulation should be developed. For example, burying source and drain electrodes into semiconductor, or attaching single crystal of semiconductor with atomically flat surface are a promising way to realize both short length and atomically flat surface of the channel.

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