Study on Threshold Voltage Shifts and Reliability in PFETs by High-Voltage ON-State and OFF-State Stress

（オンおよびオフ状態高電圧ストレスによるPFETのしきい値電圧シフトと信頼性に関する研究）

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In recent decades, electronics have made much progress thanks to the scaling of silicon CMOS LSIs. Now dimensions of state-of-the-art MOSFETs are already as small as tens of nanometers. The size of metal-oxide-semiconductor field effect transistors (MOSFETs) in large scale integrated circuits (VLSI) has been rapidly scaled down for more than forty years for higher performance, lower power consumption, and higher integration. In such aggressively scaled MOSFETs, the short-channel effects and variability have large impact on the behavior of devices, and other problems are arising.

It is well known that the random variability is caused by the statistical nature of dopant atoms in the transistor channel which is called as random dopant fluctuation (RDF). The number and position of impurity atoms in the channel depletion layer in determining the Vth of the transistor is randomly distributed. It is well known that the variability of transistor characteristics is one of the most critical challenges in VLSI. In particular, the instability in static random-access memory (SRAM) cells due to the variability of individual transistors in the cells is known as a serious problem that will prevent further device integration and supply voltage lowering. Therefore, the analysis of cell unbalances at the transistor level is needed for better understanding of SRAM stability at low supply voltage (V_{DD}) operation, which leads to a severe yield loss of SRAM. The large variation leads to the instability in SRAM cells. Hence, the suppression of this large variation is strongly required in order to reduce the instability in SRAM cell. In particular, some of SRAM cells fail due to cell unbalance caused by individual transistor variability.

Recently, a new concept of post-fabrication self-improvement technique of SRAM cell stability has been demonstrated. The self-improvement scheme in SRAM is

used to improve cell stability after chip fabrication. This technique simply applying stress voltage to the V_{DD} node, when V_{DD} is raised to high voltage, stronger pFETs is stressed by ON-state stress, |Vth| is increased and selectively weakened by self-improvement scheme indicating self-improvement mechanism works. On the other hand, the weaker pFETs is stressed by OFF-state stress, |Vth| is decreased and selectively strengthened by self-improvement scheme which is favorable for self-improvement technique. As a result SRAM cell stability is self-improved.

In this work, experimental study on |Vth| shift and reliability in pFETs by high voltage ON-State and OFF-State Stress are intensively investigated. Variability of |Vth| shift by ON-state and OFF-state stress for post-fabrication SRAM cell stability self-improvement technique is experimentally investigated. The variability of |Vth| shift is controllable, with proper choice of stress voltage and stress time, larger shift can be obtained with less variability. Sigma variability does not depend on the stress voltage nor stress time, but it depends on the average of |Vth| shift. The magnitude of |Vth| shift in pFETs by high voltage ON-state and OFF-state stress are also very important because the magnitude of |Vth| shift is varies for different transistor. Some transistor has large |Vth| shift and some transistor has small |Vth| shift. The maginitude of |Vth| shift by high voltage ON-state and OFF-state stress itself has variability. From the experimental result, it shows that |Vth| shifts are process and transistor size dependence.

In terms of reliability, recover behavior of |Vth| shift by high-voltage ON-state and OFF-state stress under SRAM self-improvement technique also an important issue. This is because after stress application, |Vth| shifted, but after some relaxation period, |Vth| shift tend to move back to its initial state, but how much the |Vth| shift is recover and become permanent part has been throughly discussed in this dissertation. Even though there is a sudden recovery just after the stress is removed, from long-time recovery measurements, it is found that the permanent part (|Vth| shift) are certainly exist even after 2 to 3 months relaxation period. From the experimental results, it is also newly found that |Vth| shift in pFETs by high voltage ON-state and OFF-state stress for SRAM cell stability self-improvement technique has no critical recovery issue.

One of the major concerns in SRAM self-improvement technique is the reliability issue. The transistors particularly pFETs are stressed by high voltage, and, therefore, the reliability may be degraded. Hence, the realiability measurements of pFETs under the post-fabrication SRAM self-improvement technique has been performed. NBTI degradation and NBTI lifetime estimation of pFETs under this technique are compared with fresh pFETs. It is found that although the NBTI lifetime of pFETs is slightly shorthened by the application of self-improvement technique, the lifetime difference is

just a little, indicating the self-improvement cheme has no critical issues in reliability.

In conclusion, the experimental study on |Vth| shift in pFETs by ON-state and OFF-state stress for SRAM cell stability self-improvement scheme have been investigated through this study. The experimental results that have been obtained in this dissertation show important information on the |Vth| shifts and their variability behaviors in pFETs by high voltage ON-state and OFF-state stress for post-fabrication SRAM cell stability self-improvement scheme. It is found that the reliability of pFETs under this technique has no critical reliability issue. This is an important step for the realization of this self-improvement technique. These measurement data provide clear device design guidelines for the post-fabrication self-improvement scheme of static random access memory (SRAM) cell stability.