博士論文（要約）

Study on InGaAs-On-Insulator MOSFETs for III-V logic LSI on Si platform

（Si プラットフォーム上 III-V ロジック LSI のための InGaAs-On-Insulator MOSFET に関する研究）

A DISSERTATION
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Conventional device scaling strategy to enhance device performance become confronting the fundamental physical limit. Therefore, the introduction of new principle and new material become more important for the further improvement of the metal-oxide-semiconductor field-effect transistor (MOSFET) performance. InGaAs, one of III-V compound semiconductors is being considered as the promising channel materials for the next generation MOSFETs thanks to their small effective mass and high electron mobility. Moreover, extremely-thin body (ETB) InGaAs-on-insulator (InGaAs-OI) structure is strongly needed to achieve both of good short channel effect (SCE) control and high on-performance. However, there are three main technological issues to realize high performance InGaAs-OI MOSFETs, which are source/drain (S/D) formation for a low resistance, channel engineering to enhance electron transport, and channel formation on Si wafer. Therefore, in this thesis, we suggest the possible solutions for each issue and have realized the high performance InGaAs-OI MOSFETs.

For the S/D formation, we have suggested the metal S/D structure using Ni-InGaAs alloy formed by the direct alloy reaction between Ni and InGaAs. We have found that Ni-InGaAs has a low sheet resistance and Schottky barrier height for electron and Ni can be selectively etched by HCl solutions without etching of Ni-InGaAs. Utilizing these favorable characteristics, we have fabricated self-aligned metal S/D InGaAs-OI MOSFETs, for the first time. Also, we have systematically investigated all the components of the S/D parasitic resistance (R_{SD}) in InGaAs MOSFETs with Ni-InGaAs metal S/D and have developed a technology to reduce all components of R_{SD}. The increase of Indium content in the channel was found to decrease the interface resistance between Ni-InGaAs and InGaAs channel. Therefore, by increasing Indium content up to 100 %, the interface resistance was significantly decreased to the theoretical limit of the interface resistance. Moreover, contact resistance between metal pad and Ni-InGaAs was reduced by developing surface cleaning technology. Finally, we have demonstrated high performance InAs-OI MOSFETs with Ni-InGaAs metal S/D structure by employing these technologies.

Channel engineering includes two parts, which are quantum well (QW) channel engineering by introducing MOS interface buffer layer and strain engineering. Firstly, we have introduced InGaAs layer with a lower Indium content than that of channel InGaAs as the MOS interface buffer layer at the both interface with top gate dielectric and buried oxide and increased the Indium content in the channel layer. This makes the change of the electron distribution in the channel layer, resulting the enhancement of electron mobility. Finally, therefore, we have demonstrated a high peak mobility of 3180 $cm^2/V{\bullet}s$ in our InAs-OI MOSFETs, which were fabricated on Si substrates with

MOS interface buffer layers. The scattering mechanisms for the electron mobility in InGaAs-OI MOSFETs are systematically analyzed and identified. We conclude that the increase of the Indium content enhances phonon-limited mobility, whereas the use of the MOS interface buffer enhances thickness-fluctuation-limited mobility through the suppression of thickness fluctuation at the MOS interface.

Also, we have strained $In_{0.53}Ga_{0.47}As$ MOSFETs on both of bulk III-V substrate and $In_{0.53}Ga_{0.47}As$-OI substrate. 1.7% highly strained $In_{0.53}Ga_{0.47}As$-OI structures are fabricated on Si substrate. Fabricated devices are systematically analyzed with different channel strain values. Strained $In_{0.53}Ga_{0.47}As$-OI MOSFETs with Ni-InGaAs S/D have been operated with high on-current (I_{on})/off-current (I_{off}) ratio of 10^5 and good current saturation in output characteristics. MOSFETs with 1.7% tensile strain exhibits 1.65 times effective mobility (μ_{eff}) enhancement against $In_{0.53}Ga_{0.47}As$ MOSFET without strain. We found that this μ_{eff} enhancement is attributed to the increase in mobile free electron concentration under tensile strain, which leads to the lowering in the conduction band minimum (CBM) and the increase in the energy difference between CBM and the Fermi level pinning position due to a large amount of interface states by Hall measurements.

Moreover, using QW-OI channel structure, we have fabricated deeply scaled InGaAs MOSFETs. QW-OI structure provided us large on-performance enhancement and better electrostatic control than InGaAs-OI without QW structure. In addition, from the simulation study, we have found that further vertical scaling and back biasing techniques can improve the control of short channel effect in InGaAs-OI MOSFETs. By hinted from these simulation results, we have investigated the effects of vertical scaling and the tri-gate structure on electrical properties of ETB InAs-OI MOSFETs. It was found that body thickness (T_{body}) scaling provides better SCEs control, whereas T_{body} scaling causes the reduction of the mobility limited by channel thickness fluctuation (δT_{body}) scattering ($\mu_{fluctuation}$). To achieve better SCEs control, the thickness of channel layer ($T_{channel}$) scaling is more favorable than the thickness of MOS interface buffer layer (T_{buffer}) scaling, indicating necessity of QW channel structure. Also, the Tri-gate ETB InAs-OI MOSFETs shows significant improvement of SCEs control with small μ_{eff} reduction. As a result, we have successfully fabricated sub-20-nm-channel length InAs-OI MOSFETs with good electrostatic. Furthermore, we have demonstrated wide-range threshold voltage (V_{th}) tunability in Tri-gate InAs-OI MOSFETs through back bias voltage control.

Finally, we have proposed the new concept of III-V integration on Si wafer using improved direct wafer bonding (DWB) techniques using Si donor wafer. By changing

donor wafer from III-V to Si, this technique can offer 300 mm and/or larger wafer scalability.