Master's thesis

Fabrication and Characterization of Polarization-Converter-Integrated InGaAsP/InP Multiple Quantum Well Photodetector

偏波変換器を集積化した InGaAsP/InP 多重量子井戸光検出器の試作と評価

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Chapter 1

Introduction

Optical integration is needed in the form of Photonic integrated circuits to achieve low power, small form factor and a minimal footprint for the optical transceivers required currently in the long haul fiber communication networks. Also advanced modulation formats are in need for increasing the data carrying capacity of optical communication networks. In this chapter we review the approaches in implementing photonic integrated circuits. We will then look at current integration and issues with respect to the two major competing technologies namely Silicon PICs and Indium Phosphide PICs. Lastly we will try to build an opinion on the possible future trends in optical communication photonic integrated circuits.

1.1 Trends in Data Communication Traffic

There is a global demand for information communication via optical transmission systems to obtain high spectral efficiency, channel data rate and low cost. Moreover current Network traffic is increasing at a rate that will overpower the growth of optical communication system (OCS) capacity. Hence while looking into the next decade with regards to the current trend, a system capacity of 100Tb/s and a spectral efficiency of 20b/s/Hz is a requirement[1][2][3]. The advances in the fields of Photonic Integrated Circuits (PICs) working on polarization division multiplexing (PDM), wavelength division multiplexing (WDM) along with optical modulation formats are a few factors that have played and will enable us in achieving this target.

These along with coherent optical transmission are responsible for present day and future push in long haul communication with channel data rates at and above 100 GB/s [3][4][5]. In the early 1980s efforts were made to evaluate and control the state of polarization and prevent the instability caused due to polarization state and polarization mode dispersion in single mode fibers. To overcome this issue many techniques including but not limited to polarization maintaining optical fibers, single polarization fibers and polarization diversity heterodyne receivers were implemented. These schemes along with phase diversity, polarization diversity and an advance in Digital signal processing (DSP) capabilities have made PDM-PICs a reality today. A quick look at the current state of the art OCS in context of PDM involving modulation

formats of Quadrature Amplitude modulation (QAM) and Quadrature Phase Shift Keying(Q-PSK) displays the possibility of bringing the 40 and 100Gb/s optical signal at around 10 and 25GBaud, enabling DSP to counter chromatic and polarization mode dispersion and enabling frequency, phase- locking and polarization de-multiplexing [4], [6], [7].Moreover as shown in fig. 1-1 it's the higher order optical modulation format along with PDM which have pushed the growth in OCS bit rate in optical communication fiber(OCF).

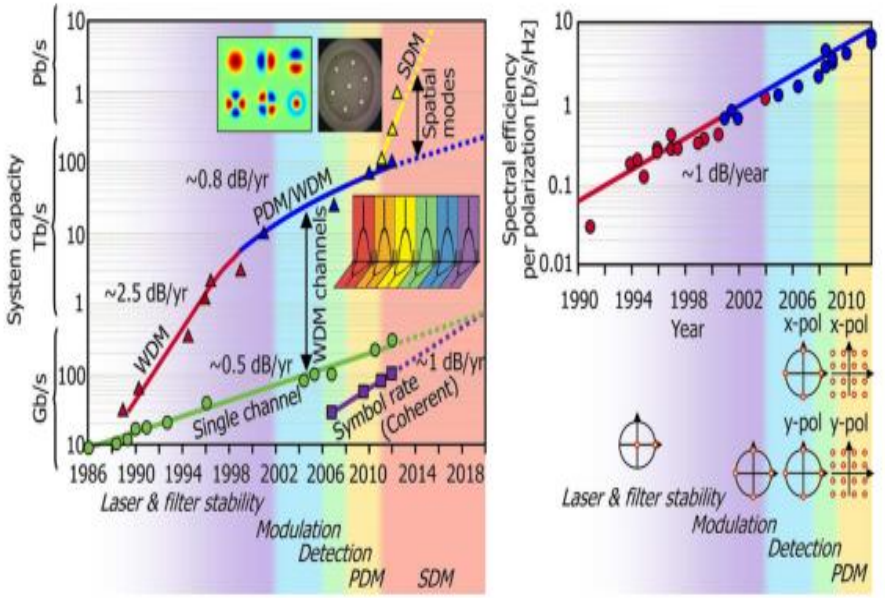

Figure 1-1: (a) Evolution of bit rate, symbol rate aggregate per fiber capacity (b) experimentally achieved per-polarization spectral efficiency (red-single polarization, blue-dual polarization) [4]

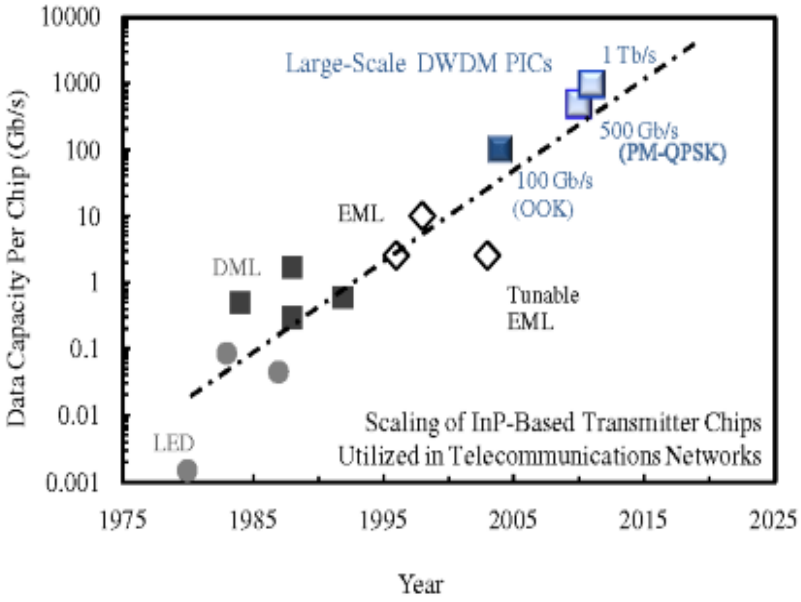

Figure 1-2: Data capacity vs. Time (InP -Platform) [8]

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1.2 Photonic Integrated Circuits

Photonic integration has a very rich and active research history dating back to the late 1960s [9]. This Integration has to be understood with respect to the invention of the transistor in 1947 which affected the technological developments not only in electronics but also in many other domains of science. The transistor had further enabled the invention of Integrated Circuits(IC) which has changed the way we communicate and process information. The IC has become ubiquitous as a result of the ability of these devices to continually increase the functionality, performance and reliability while simultaneously reducing power dissipation, size and cost. The invention of laser in 1960[10] and the realization of a semiconductor version laid the ground work for the possibility of extending the electronic IC concept to photonics [11]. Monolithic integration is a key technology that will facilitate this shift with PICs.

Today photonic integration is being pushed by a demand for higher data bandwidth and minimization of cost. The situation is further exasperated by the fact that PICs are getting more complex and costlier. On the other hand network carriers are trying to reduce the price per bit per second with the equipment price increasing. An answer to this is optical integration which provides an opportunity for simultaneous bandwidth scaling & cost reduction. Monolithic optical integration reduces the footprint of the device. Improved reliability is also one of advantages of PICs. In order to understand the trends in OCS PICs, progress in two important PIC groups comprising of Group III-V (mostly Indium-Phosphide) and Group IV (mostly Silicon) needs to be understood.

1.2.1 Indium Phosphide PICs

InP is considered as a good integration platform for optical generation, switching and detection components. Moreover the operating range is 1.3-1.6 μm, these wavelengths fall in the telecom window of optical communication. Fig.1-3 shows the development of the complexity of reported photonic ICs for WDM application measured as the number of components per chip. This pattern shows a remarkable similarity with the electronic ICs in its early days except that the market development doesn't follow suit. WDM transmitter chips with record complexity were reported by Tolstikhin in 2003(n=45). Infinera demonstrated a 40 channel WDM transmitter with 241 components. The current state of the art as of 2013 is an 8x8 wavelength switch with 256 components [12].

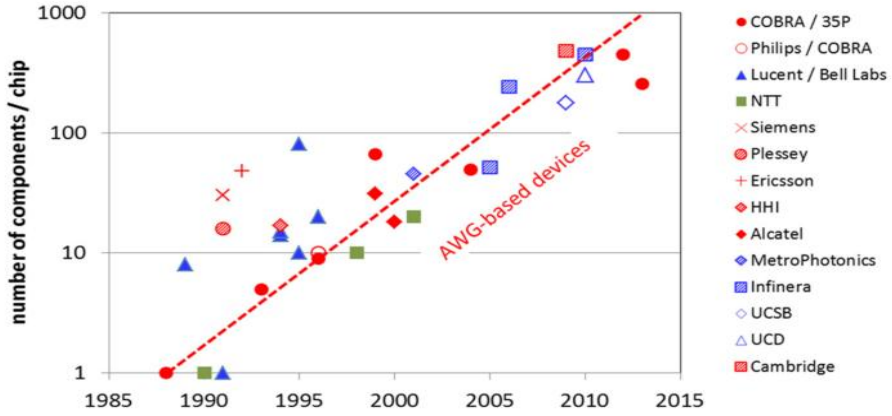

Figure 1-3: Development of chip complexity measured as the number of components per chip [12]

1.2.2 Silicon PICs

Silicon is one of the most attractive materials for the photonics industry due to the possibility of integrating the photonic and the electronic circuits on the same platform[13]. A highly established Silicon microelectronic industry, economics and the abundant availability in the earth's crust add to it being the element of choice.

Silicon photonics is also very promising platform as we can utilize the high refractive index contrast between silicon and Silicon on insulator(SOI) thus tremendously scaling down the size and ultimately reducing the footprint of the integrated optical function. Moreover much effort has been taken to overcome the absence of active source of light in silicon PICs due to the indirect bandgap in group IV elements. Some of these efforts have led to the development of very fast modulators, optical buffers and Photodetectors [14][15][16].

Another possible challenge of silicon photonics is its application to System on Chip (SoC) to develop complex systems integrating wide range of functionalities. Si PICs have also been found to be suitable for meeting the requirements of mobile computing and data centers.

1.3 Polarization manipulating devices

In PICs the handling of polarization state of light has been dealt with in various ways. Some of the issues are due to the geometry of waveguides fabricated which are inherently birefringent in nature. The optical polarization variation can be a serious issue when not required in design and

systems like polarization diversity have been designed to eliminate them to large extent.

Polarization control provides us with the avenues to reduce or enhance the use of polarization property in our designed circuit. In these paragraphs we will discuss the components required for the same. The control of the state of polarization is achieved using either the phase difference between TE and TM mode or the relative strength between these modes.

1.3.1 Polarization Converter

We will briefly discuss the types of polarization converters on both the platforms. An effort will also be made to understand our choice of using an InP converter for our design. The details of the PC design and operating principle will be discussed in chapter 2.

1.3.1.1 Polarization Converter in Si PICs

In Silicon various techniques have been employed to obtain polarization rotation (PR). Adiabatic mode resolution is one of the promising methods to obtain PR[17]. In this a Si_3N_4 structure is placed above a Silicon waveguide. This Si_3N_4 structure causes modulation in the refractive index in the mode of light in Si waveguide. Thus at the end of the rotator the TE fundamental mode has a higher RI compared to TM fundamental mode.

Recently a SOI Polarization Rotator was demonstrated with CMOS compatible fabrication process[18]. One of the major advantages of Si platform is its small footprint which can help to realize an ultra-compact Polarization converter[19].

There are a few drawbacks which are associated with a silicon waveguide as it has polarization dependent loss, polarization mode dispersion and polarization dependent wavelength characteristics which limit its application as Polarization converters in an integrated circuit[20]. These are being minimized with ongoing research.

1.3.1.2 Polarization Converter in InP PICs

The Indium Phosphide platform is a very promising and dynamic platform due the presence of an active light source with a very high commercial success for the InP PICs. The integration of PC with Receivers or Transmitter can give birth to many innovative applications

Many Passive Polarization Converters have been designed and fabricated by various research groups with different structures and properties. The polarization conversion has been obtained by methods not limited to Periodically loaded waveguide sections [21], [22] , by using a single bend waveguide, integrated waveguide[23] , with vertical and slanted sidewalls using a

single waveguide[24] and with slope with etched trenches [25].

A narrow waveguide having a sidewall slope was observed to rotate the mode by 45°[21]. So when we couple a mode of light into the asymmetric waveguide two rotated orthogonal modes will be excited simultaneously which will propagate with different propagation constants (β_1 &β_2). This wave after having travelled a half beat length would recombine as the opposite mode (TE/TM). More details on the conversion will be discussed in chapter 2.

1.3.2 Polarization Splitter/Combiner

This is one of the important components used in PICs for manipulating the polarization of light. The polarization splitter is based on the concept of modal birefringence. In this there is a small difference in the propagation constants of TE- and TM modes of light. Also we know that the coupling length of TM mode is considerably shorter than TE. This difference allows us to couple light to a different waveguide in proximity.

The Polarization splitter rotators are key for obtaining a polarization diversity circuit. One can use the large birefringence of SOI platform to easily fabricate a polarization beam splitter (PBS) or a Polarization beam splitter-rotator (PBS-R). An integrated mode evolution based polarization splitter has been also proposed by Watts et al. In this a high index contrast waveguide is used to confine optical modes[26]. The two waveguides are tightly coupled together and the index contrast is varied as the modes propagate along the two waveguides. The change in index contrast induces differences between the lateral boundary conditions of TE and TM modes. This achieves device parameters like propagation rate and coupling strength to become polarization dependent[26]. Passive polarization splitters are preferred over the active type as we don’t need to continuously tune them and also to minimize power consumption. These are divided into two main types as mode coupling and Mode-evolution based splitters. Also various types of Polarization splitters and combiners have been demonstrated based on the Mach-Zehnder interferometer [27], [28].

1.4 Polarization Division Multiplexed PICs

Polarization division multiplexed PICS is one of exciting and key technologies for improving OCS data capacities. Even though till date most of the research in all optical signal processing

in PDM OCS is focused on only a single polarization state foucs has recently shifted to using the two orthogonal polarization in the systems with capacity of 100Gb/s and above. This provides us with an opportunity to double the system capacity and spectral efficiency by working with two independent orthogonally polarized light modes[29], [30].

There are two popular approaches at the transmitter side:

Hybrid approach – using $LiNbO_3$ based modulator with PIC chip and micro optic polarization elements.

Indium-Phosphide PIC- having an integrated tunable laser with I/Q modulator.

Similar to transmitter side, for receiver there are two conventional approaches which are:

Hybrid approach- with silicon PIC with PD

Indium Phosphide PIC- with a integrated tunable laser on a coherent receiver.

A few years back a researcher at Bell labs had reported a dual polarization Silicon coherent receiver PIC which used 2D grating but had high coupling loss for polarization splitting, rotation and fiber coupling[31]

1.4.1 Transmitter and Receiver PDM PIC: Current State of the Art

1.4.1.1 Silicon PDM-PICs

The primary advantage of Group –IV /Si platform is its abundance on earth in addition to its high mechanical strength. Also another positive is the mature and huge infrastructure already existing for electronics industry. Its current major focus is on developing high-volume and low-cost applications. The current successful demonstration in Si for transceivers is at 224-Gb/s PDM-16-QAM and 112-Gb/s PDM-QPSK

I. 224-Gb/s PDM-16-QAM PIC

The Si PIC consists of four single drive push pull, Mach-Zehnder modulator (MZMs), multiple phase shifter with integrated silicon heaters, polarization rotator (PR) and polarization beam combiner (PBC). The silicon MZM employ a reverse biased PN junction embedded in the waveguide. High speed modulation is achieved by modulating the junction depletion width such that the effective index of the silicon waveguide is changed. Two arms of MZMs which

are identically configured to facilitate single drive push-push operation. The operation of PR is based on adiabatic mode. This is achieved by a tapered SiN waveguide on top of the silicon waveguide. Also PBC is implemented by a simple directional coupler. The receiver consists of two inverse tapers (ITs), two polarization beam splitters (PBSs), two PRs, two Multi Mode Interference couplers (MMI) 90-degree hybrids and eight Germanium photo detectors (PDs). The optical signal enters the PIC with two polarizations. The LO and the signal are divided into TE and TM polarizations by two PBSs. The TE light passes through the 4x4 MMI based 90 degree hybrids, with the four outputs detected by the PDs. The balance detection between first and fourth PDs produces the in phase TE-Polarization components and the second and third PDs produce quadrature TE-polarization components. In a similar way we get the I/Q TM-polarization components at the receiver.

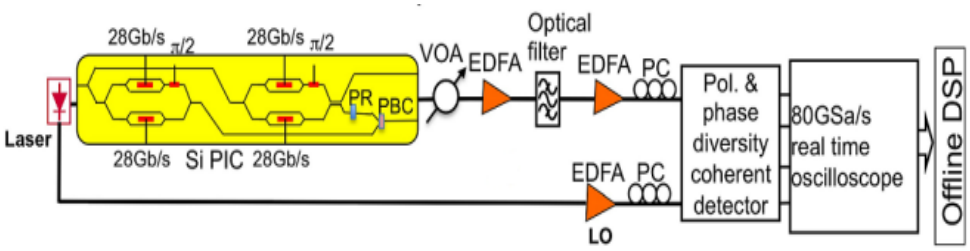

Figure 1-4: Optical setup for Silicon PIC[32]

II. 112-Gb/s PDM-QPSK PIC

In figure 4 shows the experimental setup for PDM-QPSK generation. The in-phase/quadrature (I/Q) drive signal uses a 28-Gb/s pseudorandom bit sequence (PRBS) of length $2^{15} - 1$from a pattern generator with a 64-bit delay. The signal is amplified individually by two amplifiers. A TE mode is launched into the modulator and a polarization diversity detector used at the receiver. The polarization diversity 90 degree hybrids with LO with the same frequency at the transmitter (homodyne detection). The required OSNR values at a BER of $2.4x10^{-2}$, which is a typical threshold for soft-decision forward error coding (FEC), also it is ~26dB for PDM-16-QAM and ~12dB for PDM-QPSK. For a comparison with single channel 112Gb/s PDM-QPSK we observe an extra 0.9dB penalty due to the presence of PR and PBC.

1.4.1.2 Indium Phosphide PDM-PICs

Group III-V/ InP based PICs have achieved the highest level of integration and

commercial success. These are now widely used as transceivers in optical communication industry as they have improved component and network scaling. The current state of the art in this domain is reviewed as follows. The current successful demonstration in InP-PICs for transmitters (Tx) is at

1) 1.12-Tb/s super channel coherent PM-QPSK InP
2) 854 Gb/s Super channel PM-8QAM

I. 1.12Tb/s super channel PM-QPSK

This PIC design consists of 10 DFB Lasers supplying light to two channels, each for TE/TM polarization. This PIC operates at 200GHz channel spacing and covers half of the C-band

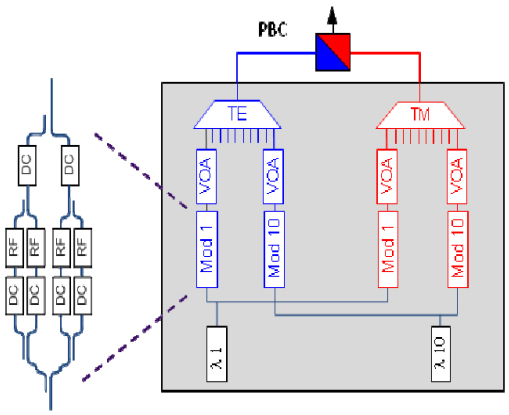

Figure 1-5: Schematic of PIC with functional blocks of modulator section consisting of a nested MZM for each polarization[33]

In total there are 20 MZMs. A DC signal is used to balance the modulators,variable optical attenuators are required to equalize the power for each wavelength and polarization covering the entire spectrum. Lastly the arrayed waveguide grating (AWG) is integrated on the chip as seen in figure 1-6.

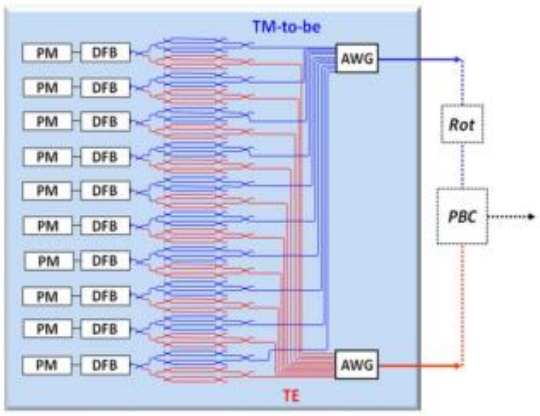

Figure 1-6: Schematic of 10-channel PDM transmitter PIC [34]

The output of AWGs are combined and coupled to a fiber off chip. The performance of the DFB array is evaluated by noise spectra of the DFB array of the transmitter PIC.This transmitter has more than doubled the capacity of a 10-λ transmitter PIC which had been reported earlier.

II. 854 Gb/s Super channel PM-8QAM

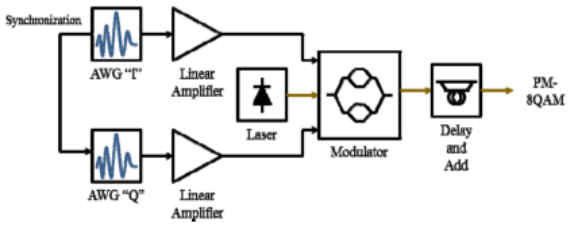

Figure 1-7: PM-8AM transmitter block diagram[35]

It uses two arbitrary waveform generators (AWG) for I and Q signal modulation. Both are synchronized in time using a common high speed RF clock. Multi-level signals are generated by the AWG for 8QAM signals obtained in Fig.1-7. This 8QAM constellation has a phase margin of 45 degrees and is more robust against phase noise.

The RF waveforms are amplified and fed to a Lithium Niobate QPSK modulator. The output of this is then passed to a delay and add block which generates the dual-polarization optical signal.

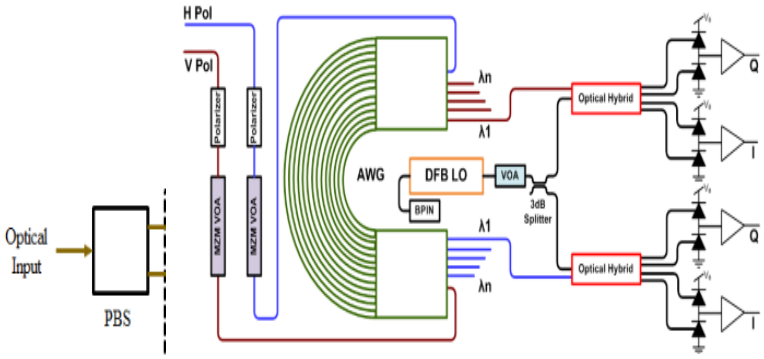

Figure 1-8: Schematic of coherent Receiver with an embedded PIC layout [34]

The Receiver in Fig.1-8 consists of a 10 channel PIC layout in case of a 10 channel, Polarization multiplexed QPSK PIC. The TE and TM signal components are split off- chip using a PBS. The signals are then launched into the TE waveguide mode of the PIC. The 10 wavelength are separated using a spectral de-multiplexer. Each channel signal then mixed with LO in 90-degree optical hybrids. The Los are tunable DFB lasers on the same InP substrate and are tuned to the incoming signal frequencies.

A single LO is split to mix with both the V and H polarization. The 90 degree hybrids outputs are terminated in high speed, balanced photo-detector (HSPD) pairs. The HSPD are wire bonded to a high speed TIA (trans-impedance amplifier) array off-PIC inside the package. The TIA outputs are then sampled using a real time, high speed analog to digital converter and electronically processed offline. The channel separation is 25GHZ making the entire 10 channel block only occupy 250GHz bandwidth.

Thus this receiver with all 10 channels operating at 28Gbaud in the polarization multiplexed QPSK mode is capable of a 1.12Tb/s super channel.

1.5 Photo-Detector

The Photodetector we have fabricated works on the photoelectric effect. In this effect absorption of photons causes the electrons to gain energy and jump to higher energy levels. Under an applied electric field these carries produce a current which can be measure using an ammeter. The photo effect takes two forms namely external photo effect and internal photo effect [36] . We consider the internal photo effect as it gives to the excited carriers in our material and takes into consideration the photoconductivity of the device.

A photoelectric detector has gain and is a result of the following three physical phenomenon:

i. Generation: This is responsible for the generation of free carriers from absorbed photons.
ii. Transport: A current flows through the external circuit with the application of a voltage bias.
iii. Gain: Internal amplification of generated carriers due to various factors (impact ionization being one of them), thus improving the responsivity of the Photodetector.

The Quantum efficiency of the Photodetector is the probability of a single incident photon on the detector to contribute towards the photocurrent by generating a electron-hole pair. This efficiency can be explained by a mathematical eq. (1.1)

$$\eta = (1 - R)\zeta[1 - e^{(-\alpha d)}] \qquad (1.1)$$

Here, $R\ is\ the\ optical\ reflectance\ and\ (1 - R)$ represents the effect on the surface of the device. The factor ζ is the fraction of electron-hole pairs that successfully avoid recombination and contribute towards photocurrent. The Third factor displays the fraction of the photon flux absorbed by the bulk of the material.

1.5.1 Photo-Conductor

A material where its electrical conductivity σ increases with proportion to the incident photon flux Φ can be used as a photoconductor. When a external voltage difference is applied to photoconductor on being irradiated a current flows through the circuit due to the generated charge carriers. This photocurrent i_p is proportional to the photon flux Φ or the voltage drop across the Resistor placed in series with the circuit.

The Photo-Conductor can be classified as being formed Intrinsic Material or Extrinsic material. We will discuss the Extrinsic Material photoconductor in detail as it can be doped for use a longer wavelengths.

An important point to note is that photo-conductors provide gain whereas the p-n and p-i-n photodiodes do not. Moreover the photoconductors are generally slower in operating speeds compared to the photodiodes.

1.5.2 p-n Junction Photodiode

This photodiode works under reverse bias for operating as a Photodetector. In this as the photon flux incident on the junction increases the current generated in it also increases.

An ideal reverse bias junction is shown in the fig.3.1. An applied electric field is

mostly concentrated on the depletion region and thus it is where we need to focus our attention for carrier collection. Most of the places where we can collect the electron-hole pairs can be roughly grouped into three categories:

The depletion region is the major contributor the reverse photocurrent as it is the place where all the applied voltage is concentrated. Moreover this current is mostly drift in nature.

Some of the carriers are generated far from the depletion region and are lost due to recombination within the material. This energy is lost partly as heat.

Lastly some of the electron-hole pairs found close to the depletion region and which are not lost due to recombination contribute to the photocurrent due to diffusion.

Thus the photocurrent in a p-n junction photodiode consists of a combination of drift and diffusion currents generated in the Photodetector on irradiation.

This current is given by the equation1.2

$$i = i_s \left[e^{\left(\frac{eV}{KT}\right)-1} \right] - i_p \qquad (1.2)$$

Where, i_p is proportional to the incident photon flux and i_s represents the dark current (current in absence of the photon flux).

1.5.3 p-i-n Junction Photodiode

The structure we have employed for our PD is a p-i-n photodiode. This structure makes our PD a dynamic structure as many parameters can be varied for obtaining a sensitive receiver which is suitable for working with advanced modulation formats (State Of Polarization in our case) . Some of the advantages are as follows:

i. The intrinsic layer provides us the opportunity to increase the effective area of the depletion region. Thus the effective area to obtain photon irradiation increases.
ii. The response RC-time of the device decreases due to the decrease in junction capacitance.
iii. The contribution to the photocurrent by the drift process increases thereby improving the responsivity of the device structure.

We have chosen a Quaternary structure as it provides us the freedom to adjust the lattice constant and band energy of the PD simultaneously during the epitaxial crystal growth using MOCVD. Moreover the InGaAsP/InP structure provides us a with a useful range that covers the C-band especially the telecommunication window used in Optical Fiber Communication (0.92 to 1.7μm).

1.6 Summary

The scaling of PICs would continue to be pushed by demand in network capacity. To further increase scaling PICs, one would have to use a Combination of higher order modulation formats, baud rates and more Transmission channels (larger number of sub-carriers or super-channel). Both of these provide complex challenges for improving receiver sensitivity and the error free message reception in an already crowded constellation diagram and to improve the selectivity of the front end optical receivers PICS for the super channel.

The successful realization of Si-PDM PICs confirms the readiness of Si-Platform for applications in 100Gb/s coherent OCS. As of now successful commercialization is absent in Si, but a possibility of hybrid III-V/Si laser being integrated on a silicon platform for future coherent transceiver systems is imminent.

The 1st and 2nd generation of 100 GB/s InP-large scale PICs have demonstrated their capability, performance & economic feasibility for commercial deployment. Further these PICs have current capabilities exceeding 500 GB/s with more than 400 functions and would be commercially deployed in the next few years.

Lastly for research towards the future of PM-PICs, one will have to learn from the semiconductor industry, which provides us a learning curve towards enhancing the boundaries of PIC technology.

Characteristic	Group III-V	Group IV
Combining Electronic and Optical Function Monolithically	low integration density	high integration density
Commercial Wafer Diameter	50-100mm	200-300mm
Laser/Optical Amplifier	Possible	Currently not possible(or very inefficient)
Optical connection/Fiber	Possible	Possible but needs

coupling		integrated gain elements
Testing	Possible as integration with active devices is easy	No integrated source but optical access possible with grating couplers
Modulator Performance	Good	~10 x higher V_π for low loss modulation
Integrating different passive optical Components	Good	Better than III-V as extremely compact components can be fabricated with CMOS process technology
Reliability vs. Discrete components	Excellent for both active and passive components for commercially deployed PICs	Excellent for passive but currently emerging for modulators and other active components
Power Consumption vs. Discrete components	Excellent as low modulator voltage and ease of integration of active components	Relatively good due to excellent thermo-optics

Table 1.1: Comparison of group IV & group III-V PICs

1.7 Research Objective and Thesis Outline

Usage of the state of polarization (SOP) of a fully polarized light as an additional degree of freedom in optical communication systems employing advanced modulation formats is becoming increasingly important for enhancing data capacity [37]. Moreover there is an absence of a monolithic Polarization Analyzer in the form of PIC. In literature the only standalone polarization analyzer in an integrated form we could find was on a glass substrate[38]. By combining a polarization converter (PC) it is possible to manipulate the parameters of the Stokes vector at the receiver end for a possible polarization analysis and for enabling detection of the polarization state, without the requirement of coherent system. Receivers will become compact and simple if a PC is integrated with a polarization-dependent Photodetector (PD) which can if required employ Stokes Vector Modulation format[37].

For this purpose, we aim to monolithically integrate the half-ridge waveguide PCs, which we have developed previously [39], [40], with multiple-quantum-well (MQW) PDs. We employ the active/passive integration platform known as offset quantum well (OQW) on

InP, which requires only a single re-growth step for the integration of MQW PDs with PCs.

This thesis focuses on the science of Design, Fabrication and Characterization of Integrating a Polarization Converter with a MQW Photo detector.

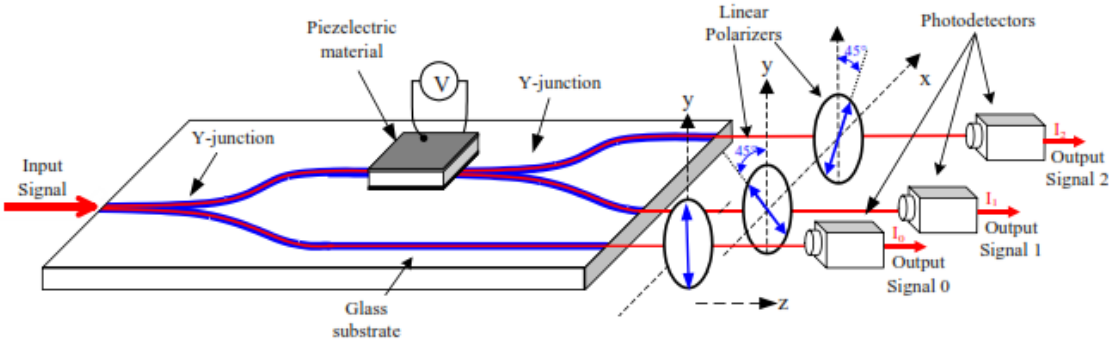

Figure 1-9: Schematic of an Integrated Polarization Analyzer[38]

Chapter 2

Fundamentals of Theory and Device Design

In this chapter we will look into the theory of polarization of light and semiconductor photonic devices. First we will look into the basic theory of light wave polarization then we will discuss the Johnes Matrix Formalism and Poincare sphere. Next we will look into the theory of light propagation in a Birefringent medium. Lastly we will look into the working of the Polarization Converter and Summarize by discussing the need for required fabrication techniques to be discussed in Chapter 4**.**

2.1 Electrodynamics in Continuous Media

The light waves propagate in vacuum or in a medium with the interaction between their Energy fields defined by the Maxwell's equations. This light radiation can be defined by the Electric E(r, t) and the magnetic B(r, t) fields. The Maxwell's equations governing these fields are given as below:

$$\left.\begin{aligned} \nabla \,.\, \vec{E} &= \rho_a \, 1/\varepsilon_\circ \\ \nabla \,.\, \vec{B} &= 0 \\ \nabla \times \vec{E} &= -\frac{\partial \vec{B}}{\partial t} \\ \nabla \times \vec{B} &= \mu_\circ \vec{J}_a + \varepsilon_\circ \mu_\circ \frac{\partial \vec{B}}{\partial t} \end{aligned}\right\} \quad (2.1)$$

These equations are coupled partial differential equations with ρ_a and J_a being the source terms. Here,

ρ_a is the charge density due to both separate and polarization charges.

J_a is the current density due to free , polarization and magnetization.

The source terms vanish in vacuum and the Electric **E** and Magnetic induction **B** are continuous.

2.2 Polarization of Light

The Electric field vector E(r, t) and its evolution over a course of time defines the polarization of light at a particular location. The orthogonal components of this vector while propagating vary in their parameters like amplitude and phase as a sinusoid with time. The end point of this vector traces an ellipse which determines the state of polarization depending on the orientation and ellipticity of the polarization ellipse. The plane wave which is defined by this ellipse can be said to be elliptically polarized for the state of light. Moreover when this same ellipse degenerates to straight line or a circle, the light wave is known to be linearly and circularly polarized respectively.

Polarization state is an important property of light while defining its interaction with matter which can be understood by observing some of the phenomenon in nature like the reflection at boundaries of different materials, amount of light absorbed by materials, light scattering for media and the mode of light being rotated while propagating through some media[36].

2.2.1 Jones Vector and Matrix Formalism

The polarization state of a light wave can be comprehensively defined by a two dimensional vector known as the Jones vector. In the following description we will try to understand and derive the Jones matrix formalism.

Consider a light propagating in the z-direction and being a polarized plane wave. The components of this vector are given by the equation 2.2 and the corresponding figure is illustrated in fig.2.1

$$\left.\begin{aligned} E_x &= A_x e^{i(wt-kz+\Phi_x)} \\ E_y &= A_y e^{i(wt-kz+\Phi_y)} \end{aligned}\right\} \quad (2.2)$$

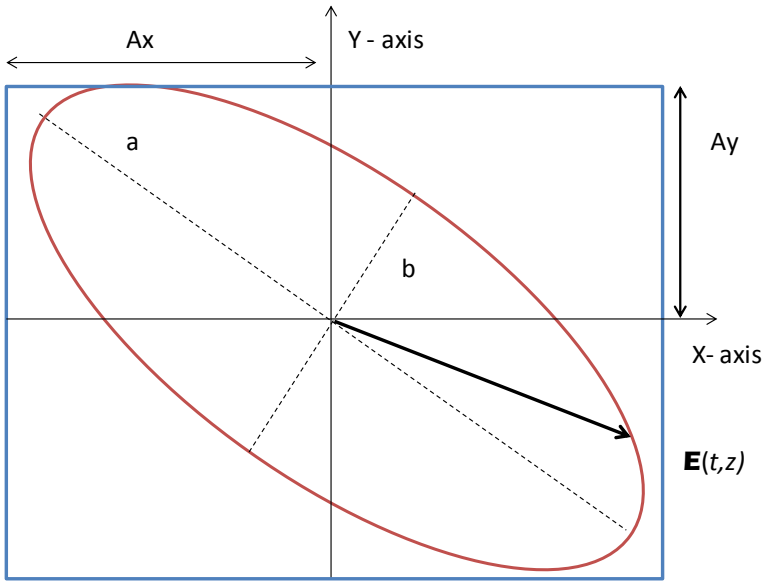

Figure 2-1: Polarization ellipse in xy-plane propagating in z-direction

The light can be classified into either elliptically, linearly or circularly polarized light depending on the phase and amplitude of light. Light is said to be

I- Linearly polarized if $\Phi_y - \Phi_x = n\pi$, where $'n'$ is $0,\pm1,\pm2$ ... .

II- Elliptically polarized if $\Phi_y - \Phi_x = n\pi + \pi/2$,where $'n'$ is $0,\pm1,\pm2$ ... .

III- And it is circularly polarized for $\Phi_y - \Phi_x = n\pi + \pi/2$ and $A_x = A_y$. This light can be further classified as Right handed polarized (RCP) or left handed polarized (LCP) depending one direction of rotation.

The Jones vector is a 2Dimensional Matrix and describes the SOP of light using a simple notation convention.

$$\begin{bmatrix} E_{x0} \\ E_{y0} \end{bmatrix} = \begin{bmatrix} A_x e^{i\Phi_x} \\ A_y e^{i\Phi_y} \end{bmatrix} \qquad (2.3)$$

The Jones Vectors for various polarizations are shown in Table 2.1

Polarization of Light	**Jones Vector**
Linear Horizontally Polarized	$\begin{bmatrix}1\\0\end{bmatrix}$
Linear Vertically Polarized	$\begin{bmatrix}0\\1\end{bmatrix}$
Right Circularly Polarized	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\j\end{bmatrix}$
Left Circularly Polarized	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\-j\end{bmatrix}$

Table 2.1: Jones vectors for polarized light

The Jones vector J_a and J_b represent two orthogonal states of polarization if their inner product is zero.

2.2.2 Poincare Sphere and Stokes Parameter

Stokes vector consists of Stokes parameters (S_0, S_1, S_2 and S_3) and defines the SOP of light along with its intensity. The Stokes parameter S_0 gives the intensity of light by the relation $S_0 = a_x^2 + a_y^2$, where as the rest of the parameters of stokes can be defined in terms of field parameters (as $a_x, a_y \; and \; \Phi$) and the envelope function (A_x and A_y) from figure 2-1 . It should also be noted that only three of the four components of Stokes vector are independent as $S_0^2 = S_1^2 + S_2^2 + S_3^2$

$$\left.\begin{aligned} S_0 = a_x^2 + a_y^2 &= |A_x|^2 + |A_y|^2 \\ S_1 = a_x^2 - a_y^2 &= |A_x|^2 - |A_y|^2 \\ S_2 = 2a_x a_y \cos\Phi &= 2Re\{A_x^* A_y\} \\ S_3 = 2a_x a_y \sin\Phi &= 2\mathrm{Im}\{A_x^* A_y\} \end{aligned}\right\} \quad (2.4)$$

The Poincare Sphere provides an expressive and intuitive visual representation for the state of polarization of light. It is basically a sphere of unit radius in a normalized stokes parameter space. Phase difference and ratio of amplitudes (A_x/A_y) are enough to define the polarization of light. These along with two angles of orientation χ and ψ are used to plot the polarization state on the sphere**.**

The point on the surface of this sphere defined in the spherical coordinate system defines the SOP of light wave. The points on the equator of the sphere represent the linearly

polarized light. The north and south poles are used to represent the RCP and LCP respectively. The center of sphere represents completely un-polarized light. Thus one can find all possible polarization states on or within the Poincare sphere.

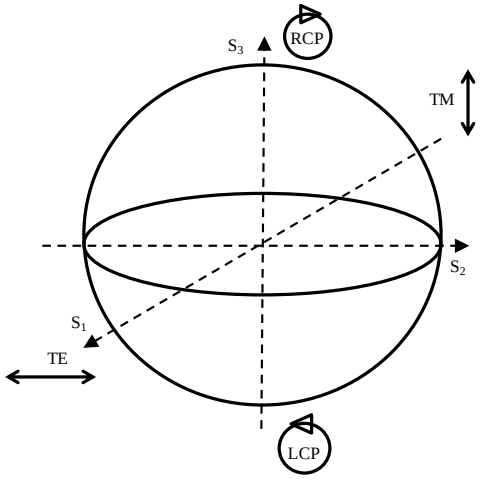

Figure 2-2: Poincare Sphere

2.3 Theory of Light Propagation in Birefringent Medium

A propagating light wave maintains its polarization state while travelling through an isotropic medium. Moreover for the isotropic layered media the EM- radiation can be decomposed into independent TE and TM Modes[41]. These modes can be manipulated by a different birefringent medium with along the propagating direction.

In the following paragraphs we will look into the propagation of EM-radiation through a birefringent medium. Let us consider a plane wave expressed by the Jones Vector $\vec{E}_1$ incident on the birefringent Medium 'R' and emerging out as $\vec{E}$. These vector $\vec{E}_1$ & $\vec{E}_2$ are related with the equation:

$$\left.\begin{aligned} E_x &= J_{11}E_{x1} + J_{12}E_{y1} \\ E_y &= J_{21}E_{x1} + J_{12}E_{y1} \end{aligned}\right\} \quad (2.5)$$

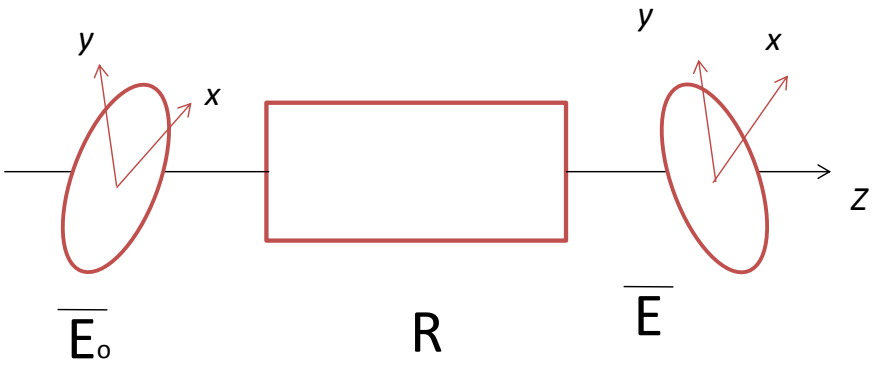

Figure 2-3: Optical system R with E-0 incident as the Tx Jones vector

These equations can also be represented as matrix form as,

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix} . \begin{bmatrix} E_{x1} \\ E_{y1} \end{bmatrix} = J. \begin{bmatrix} E_{x1} \\ E_{y1} \end{bmatrix} \quad (2.6)$$

Here, J is the Jones matrix of the optical conducting medium. Using the above equation 2.6 and generalizing it for propagation through an isotropic medium with thickness 'd' and refractive index 'n' we obtain phase retardation of $\frac{2\pi nd}{\lambda}$. Thus the Jones matrix formulation for a retarder plate is given by

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = \begin{bmatrix} e^{-i\frac{2\pi nd}{\lambda}} & 0 \\ 0 & e^{-i\frac{2\pi nd}{\lambda}} \end{bmatrix} . \begin{bmatrix} E_{x1} \\ E_{y1} \end{bmatrix} \quad (2.7)$$

The retardation plates are generally made in such way that the c-axis lies in the plane of the plate surface and thus in a direction where normally incident light is perpendicular to the c-axis. The different polarization mode of light will experience a different retardation while travelling through a uniaxial crystal as they will experience different refractive index in the ordinary or extraordinary axes. This difference in phase between the two modes is known as Phase retardation. The Jones matrix representation will be given as below:

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = \begin{bmatrix} e^{-i\frac{2\pi dn_e}{\lambda}} & 0 \\ 0 & e^{-i\frac{2\pi dn_o}{\lambda}} \end{bmatrix} . \begin{bmatrix} E_{x1} \\ E_{y1} \end{bmatrix} \quad (2.8)$$

This phase retardation is simple expressed as $\Gamma = \frac{2\pi}{\lambda}(n_e - n_o)d$;

The most common wave plates are Quarter wave plate with $\Gamma = \pi/2$.

For the case that the principal axis of medium is tilted by an angle θ with respect to the horizontal axis , the incident radiation is decomposed into two perpendicular modes the Jones vector of which are $(cos\theta, \sin\theta)$ and $(-\sin\theta, cos\theta)$ with the propagation constants β_1 and β_2 respectively. Deducing by Jones vector calculation we obtain the output light in this case for half –beat wavelength $L_\pi = \frac{\pi}{\beta_1 - \beta_2}$

$$\mathrm{E}(L_\pi) = \left[\frac{cos2\theta}{sin2\theta}\right].\mathrm{j}e^{j\frac{\beta_1+\beta_2}{2}L_\pi} \quad (2.9)$$

In this case the wave plate is known as the half wave plate as the retardation due to plate is $\Gamma = \pi$ and the length $L_\pi$is known as the half beat length. Using the eq.3.4 the stokes parameters at the output would be

$$\left.\begin{aligned} S_0 &= cos^2 2\theta + sin^2 2\theta \\ S_1 &= cos^2 2\theta - sin^2 2\theta \\ \mathrm{S}_2 &= 2\sin 2\theta \cos 2\theta \\ \mathrm{S}_3 &= 0 \end{aligned}\right\} \quad (2.10)$$

In these equations S_3 is zero as the polarization state is changed in the bound of $S_1 - S_2$ plane.

2.4 InP Half Ridge Polarization Converter

Various InP PCs have been demonstrated till date based on either periodically loaded waveguide or slanted sidewall or asymmetric trenches and so on. These designs have a disadvantage that they require a thin upper cladding and hence are difficult to integrate with other active InP components having a thick cladding of 1μm [42]. Recently Augustin et al. have demonstrated a monolithically integrated InP PC with highly efficient coupling from/to a standard ridge waveguide[43]. Overall one problem with these designs is the difficulty to integrate them with passive and specifically with active components. This leads to a relatively complicated fabrication process with critical lithographical alignment, which might become the drawback in practical implementation. Hence we would be integrating our OQW-PD with a novel type of InP waveguide PC which is fully compatible with other InP components and can

be fabricated by a simple self aligned process. This PC has been fabricated and experimentally demonstrated at our lab, and is optimally suited for monolithically integrating with our OQW-PD.

In short the disadvantages of these PCs as compared to the one which we have employed are large modal mismatch with other ridge components, strict lithographic alignment and Special etching techniques for fabrication.

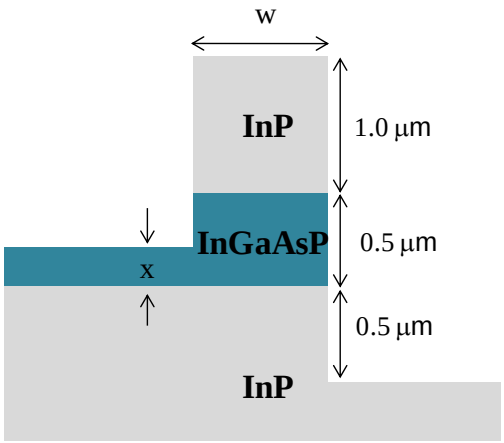

Figure 2-4: Polarization Converter [39]

It was observed during previous work on the PC shown in Fig.2.4 that 96% polarization conversion was achieved over a length of 150μm. The refractive indices of InP, InGaAsP and SiO_2 are taken as 3.17, 3.40 and 1.45 respectively. Silicon di-oxide was used to cover the PC and the PD for passivation. The best conversion result obtained by simulation where for a width 'w' of 1μm and ridge side quaternary layer thickness 'x' of 0.3μm. Also the thickness of the residual core for InGaAsP layer has to be lower than 300nm for efficient polarization conversion. Moreover It was also understood that the thickness 'x' of the Quaternary layer at the ridge side had a crucial role in extending the tolerance of the error in width 'w' introduced in fabrication.

As the PC shown in Fig. 2-4 has a cross section compatible with our OQW-PD using a simple self-aligned process we employ it for integrating into our device.

2.5 Summary

In this chapter we studied the basics of light propagation in continuous media with an emphasis on birefringent medium. Later we tried to make a case for the use InP half ridge polarization converter for integrating into our device.

Chapter 3

PC-Integrated InGaAsP/InP MQW Photodetector

3.1 Introduction

We propose a novel monolithically integrated InGaAsP/InP multiple-quantum-well photodetector integrated with a half-ridge polarization converter. A proof-of-concept device is fabricated using the offset quantum-well active/passive integration and self-aligned half-ridge polarization converter processes.

3.2 Concept of Design

A MQW structure inserted above an InGaAsP core layer in the active part of the device is employed for carrier generation and this photocurrent is subsequently collected by reverse-biasing the detector. The PC is an asymmetric waveguide acting as a birefringent medium with principal axis rotated by +/-45°. Thus a TM–mode light can be converted to a TE-mode by travelling a half beat length L_π in the PC section which has been optimised for its width and Length [3]. The photocurrent depends dominantly on the S1 parameter of the SOP, i.e. when S1 is maximum then the absorption for TE mode will also be maximum. The combination of the PC and a symmetric waveguide (WG) with the OQW-photodiodes (Fig.3-1) allow us to electrically detect the polarization state as the current value and to restore the data stream.

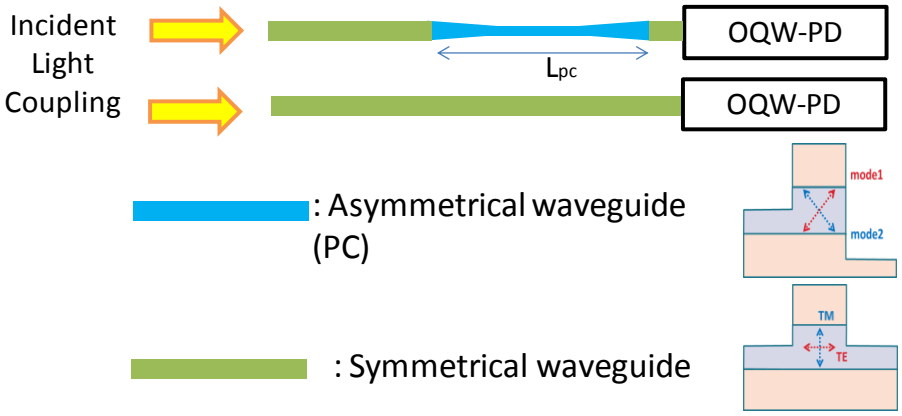

Figure 3-1: Schematic of proposed monolithic PC integrated MQW PD

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3.3 Active Symmetric waveguide

Photodiodes with waveguide structure is an efficient way to obtain high bandwidth and responsivity and are thus a potential choice for the Photodetector fabrication process. The active symmetric waveguide used in our device is as shown in Fig.3-2. It is basically a p-i-n diode with the substrate and the lower cladding n-doped whereas the upper cladding InP and contact layer InGaAs are p-doped. The core of the device is undoped with Quaternary InGaAsP layer. A stack of 6 Quantum wells is placed above the core and hence the name offset-Quantum well. The light launched into the core from the passive and asymmetric PC is absorbed by the MQW layer. The MQW layer is 0.4% compressively strained and hence has a preference for absorption of TE –mode over the TM-mode[44].

Moreover at higher wavelengths TE mode is absorbed as the heavy hole is at a lower energy level. The use of this effect was first proposed in the work of Yablonowitch[45] and Adams[46] for reducing the lasing threshold of semiconductor lasers. The absorption is stronger for the heavy hole exciton that is parallel to the plane and it is also possible to absorb only the TE mode by having a suitable design for the device. The strain in the QW increases the band gap by pushing the conducting and valance band simultaneously to a higher and lower level respectively. We have designed the active waveguide such that the photocurrent is maximum for TE mode polarization. The width of this waveguide is 2.5μm in this region and thus supports single mode operation in both the polarization modes. The waveguide is fabricated with a layer stack of semiconductors to confine light in the vertical and horizontal directions to the core which has a higher refractive index compared with the cladding layers.

The waveguide at the active/passive interface are tilted by few degrees for reducing

undesirable reflections and a good interface regrowth. The upper cladding is p-doped along with the InGaAs contact layer whereas the lower cladding is n-doped with the core Q1.25 InGaAsP layer remaining undoped. The side walls of the cladding were etched using the dry etching technique till just above MQW layers. Later the sidewalls were covered by silicon di-oxide for passivation. A polyimide layer was coated and later etched out till the surface of InGaAs was visible through the optical microscope. Later metal electrodes were deposited forming ohmic contacts for connections to the external world. An SEM image of the fabricated OQW-PD active waveguide is shown in Fig.3-2.

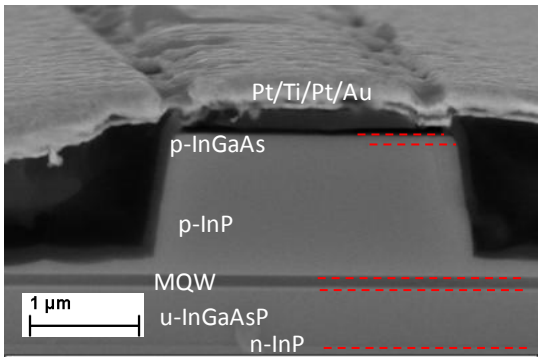

Figure 3-2: SEM image of Active Symmetric ridge Waveguide

3.4 Passive Symmetric waveguide

This waveguide connects the output of Taper from PC to the active OQW-PD. It is a simple ridge waveguide as shown in Fig.3-3 with InP claddings and a Q1.25 InGaAsP core layer. These passive symmetric waveguides were fabricated with dry etching process with a width of 2.5µm and they were later covered with silicon di-oxide and polyimide. It must be noted here that the quality of waveguide achieved was good and the losses were low and within permissible limits.

It should be noted that the absorption losses in the a direct bandgap dielectric waveguide like our case are due to inherent material nature , fabrication inconsistencies , scattering losses at the walls due to surface roughness and radiation losses to the surrounding cladding layers. It must also the remembered that the semiconductor material used for fabricating the devices have prominent absorption values for light with wavelength shorter than the corresponding bandedge. Thus we chose the layer stack of semiconductor compound

composition to avoid these losses near the c-band wavelengths. Also the confinement factor Γ of the mode of light is designed in such a way with the help of Separate Confinement Hetero-structure (SCH) that there is a minimum overlap with the clad layer and thus avoid free carrier absorption loss. The fabricated device is shown in Fig.3.3

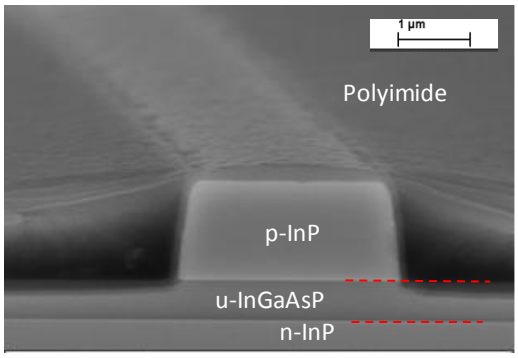

Figure 3-3: SEM image of Passive Symmetric Waveguide

3.5 Passive Asymmetric waveguide

3.5.1 Operation Principle of Polarization Converter

At the PC region, the waveguide has an asymmetric cross section, the half ridge structure; on one side of this structure we have a ridge while on the other side we have a high mesa structure. The modes in a half-ridge PC are hybridized and their electric fields are tilted from the horizontal axis. Symmetric ridge waveguides have horizontal and vertical eigen modes because of its optical confinement structure (e.g. refractive index) exists along horizontal and vertical axis. The asymmetric waveguides have eigen modes whose principal axis are rotated by a certain angle where the cross sectional structures are regarded as symmetric ones. This rotation angle is determined by the cross section of the waveguide width 'w' and the InGaAsP core thickness at the ridge side 'x' as shown in Fig.2-4 are dominant. The operating principle of this PC is similar to that of a bulk birefringent medium with the principal axes rotated by θ which by design is made to be equal to 45°. As shown in Fig.3-5 a TE mode input is divided into two eigen modes as An efficient mode conversion between the transverse-electric (TE) and transverse-magnetic states has been demonstrated in previous work for a 180μm long PC section with insertion loss of 0.4dB dB extinction ratio of 16.6dB [42]

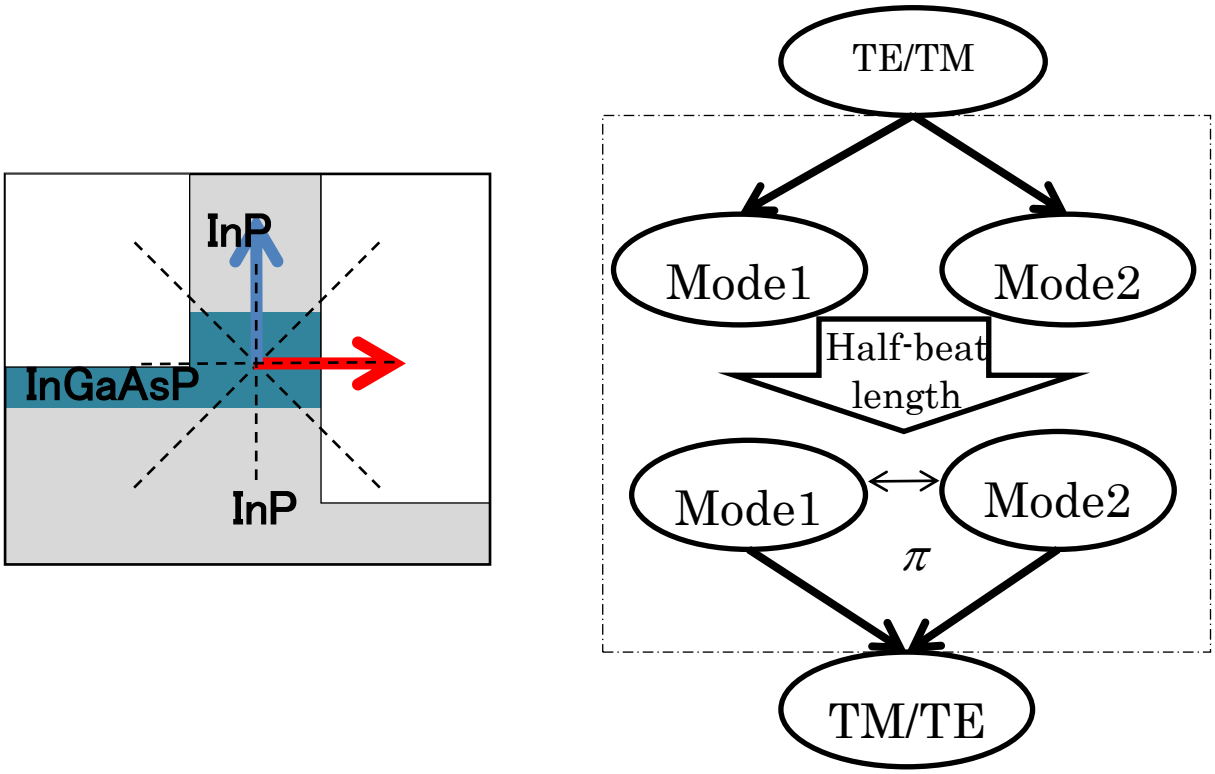

Figure 3-4: Operating principle of InP half ridge polarization converter

The input TE/TM mode excites two eigen modes labeled mode1 and mode2 in Fig.3-5 travel in the PC over a half-beat length L_π with propagation constants β_1 and β_2. After travelling through the PC over a length 'L' known as the half-beat length L_π these two modes recombined into the other orthogonal TM/TE- state.

$$\left(\frac{E_x}{E_y}\right) = \frac{1}{2}\left(\frac{\cos\left(\frac{\Delta\beta}{2}L\right)}{\sin\left(\frac{\Delta\beta}{2}L\right)}\right) \qquad (3.1)$$

Where, Δβ= β1-β2, being the expression same as the Half wave plate. In this case the birefringent plate properties are obtained in an asymmetric waveguide on an InP monolithic PIC. In this design the rotation parameter 'R' is defined by the equation 3.2 .The modes conversion is assumed to be between linear modes TE/TM whose principal axes are rotated by θ and θ+π/2. Thus the optical axis rotation is measure by the eq.3.2

$$R \equiv \frac{\iint |H_x|^2 dxdy}{\iint |H_y|^2 dxdy} \qquad (3.2)$$

Where, H_x and H_y are the magnitude of magnetic field along x- and y directions respectively.

Also the maximum conversion efficiency between the modes is calculated by eq. 3.3 as

$$C_{max} = \frac{4R}{(1+R)^2} \qquad (3.3)$$

One of the advantages of our thick cladding and the half-ridge structure, these modes have large overlap with the TE and TM modes of the symmetric ridge waveguide , which allows low-loss integration with the standard ridge components. An SEM image of the fabricated PC is shown in fig. 3-5

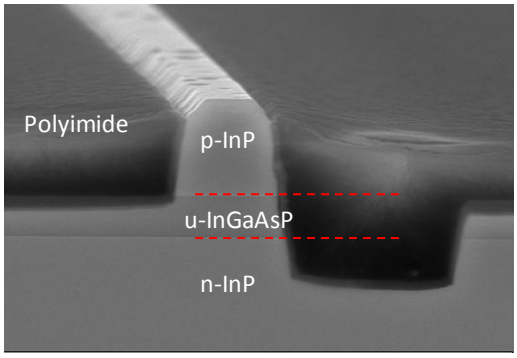

Figure 3-5: SEM image of a Passive Asymmetric Waveguide

3.6 Summary

In this chapter we looked into the concept of design of our integrated device. Later we discussed the various individual components and looked into details the working principle of Photodetector and the InP half-ridge PC.

Chapter 4

Device Fabrication

4.1 Introduction

In this chapter we will discuss about the various device fabrication techniques, conditions and equipment employed. This device fabrication involves the use of equipment widely used in semiconductor micro-technology. Moreover an emphasis will be given to understand the fundamentals of fabrication methods related to InP related optical devices. The device fabrication will mainly involve Etching, Deposition, Patterning and crystal growth. A step wise discussion will be made on the device fabrication process flow towards the end.

A simple self-aligned process is used for the monolithic integration of the PC with the OQW-PD. We employ an OQW epitaxially grown layer stack. The chip has identical epitaxial layers of p-i-n in both the active and passive parts of the InGaAsP/InP double heterojunction. In addition the active part contains the 0.4% compressively strained InGaAsP/InGaAsP MQW layers for the PD section. Fig. 3.1 shows a schematic of the integrated device consisting of a half-ridge PC, a middle-mesa ridge waveguide and an MQW PD. The device consists of PDs with PCs of different lengths and position, corresponding to each parameter of SOP. The bottom OQW-PD has no PC section and is used as a reference WG. The PC section is designed with width ranging from 0.8 to 1.3 μm and lengths from 95 to 215 μm. By using the self-aligned process with angled deposition technique, the PC structure can be fabricated without any critical lithographic alignment of sub-micron scale [40].

4.2 Active-Passive Integration

Many of the photonic devices require the integration of various active and passive devices on a single monolithic chip. Hence for having high functionality PICs an integration platform should be available which provides the possibility of simple fabrication, minimizing cost and provides a higher production yield. In order to integrate an active device like laser, semiconductor optical amplifier (SOA) or Photodetector with a passive device such as a waveguide the use of active-passive integration platforms is essential. One also has to make an

effort to integrate passive part having larger bandgap energy with active part with larger bandgap for reducing the absorption loss. In our case the Photodetector or light emitting regions, usually have a lower band gap which matches with the desired wavelength absorption or emitting range respectively. The important requirement of guiding light in a PIC is to ensure bandgap compatibility between various monolithically integrated devices on chip.

In order to achieve successful monolithic active-passive integration a few practical requirements that have to be met are listed as follows[47] :

i. There should be large dynamic range to control the bandgap energies between various devices on the chip.
ii. The losses in the grown (re-growth) structure should be in comparable or lower than the previously existing structure.
iii. The processing for active-passive integration should not affect the operating lifetime of various PIC devices.
iv. The process should not change the electrical and optical properties of the devices and should be neutral or better for the monolithic PIC chip.

We will look into the possible platforms available for integration of the InGaAsP-InP material system[48][49] and make a comment on the choice of offset quantum well employed for the integration of PC with a PD in this work. The various choices included

I. Selective Area Growth
II. Butt-Joint Re-Growth
III. Quantum Well Intermixing
IV. Dual Core Waveguide and
V. Offset-Quantum Well

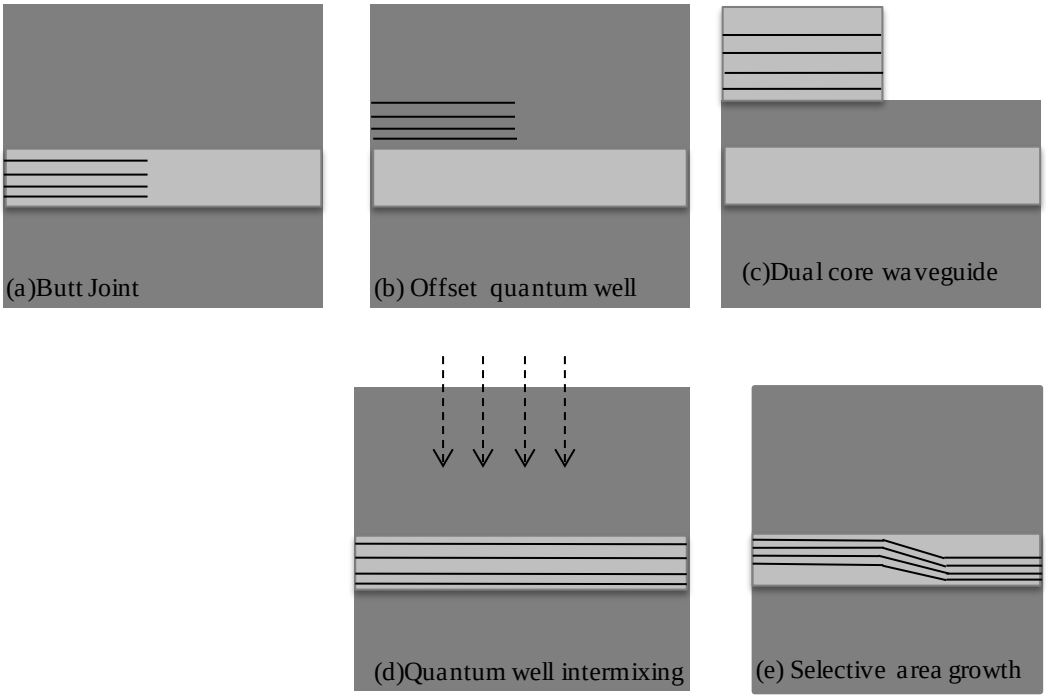

Figure 4-1: Different Integration Platform in InP

4.2.1 Selective Area Growth

This platform uses dielectric masking method to vary the growth rate so as to obtain quantum wells (QWs) and barriers of different thickness on the fabricated chip. The selective area growth (SAG) technique can integrate the active-passive parts of the device with only one metal oxide chemical vapor deposition (MOCVD) re-growth step[50]. It has also been learned from experience that this technique requires careful growth calibration to obtain required band edges; moreover it is also very challenging to change the confinement factors from one section to the other for the integration. Both Quantum Well Inter-mixing (QWI) and SAG can realize the active-passive integration in a single re-growth step. The advantage of SAG over QWI is that it is possible to maintain the crystal quality and exciton peak decay while continuously adjusting the gain peak. Thus the selectively grown region can be used as a light source. A application of this technique can be found in the literature for coarse wavelength division multiplexing of light sources[51].

Even though SAG has several advantages but it lacks the design flexibility of PICs[52].

4.2.2 Butt-Joint Re-Growth

The Butt-Joint Re-Growth (BJT) provides a lot of flexibility with integrating active-passive devices monolithically on the III-V semiconductor photonics platform. BJT first defines the waveguide for the active part while the waveguide is etched away elsewhere on the chip. Monolithic Integration of different material systems have also been achieved using BJT platform, also recently for InGaAlAs/InGaAsP integration was done for Multiple BJT lasers[53]. A regrowth step is required for the upper cladding once all the growths are completed. Even though platform is quite versatile it has some drawbacks such as

Requires good growth calibration to match adjacent sections waveguide characteristics as mismatches can cause optical reflection and insertion losses at the interface [54], [55]

Needs three step MOCVD growths (2 Re-Growths).

There can be growth abnormality at active-passive interface due to large growth rate enhancements[56]

BJT platform is quite complex for fabrication with low yield and difficult reputability of previous obtained conditions.

4.2.3 Quantum Well Intermixing

Active-Passive integration using intermixing of wells and barriers can be achieved by the Quantum Well Intermixing (QWI) Platform. The QWI is used to engineer the refractive index and band gap energy for QW laser hetero-structures [47]. The QWI technique is relatively simple and powerful for fabricating photonic integrated circuits. The intermixing process is improved due to the presence of impurities and defects at the interface between active and passive parts, this allows for intermixing at quite lower temperatures. Different methods have been proposed to achieve QWI namely photo-absorption induced heating, ion implantation and surface dopant diffusion.

This Platform is a very dynamic and versatile platform as we can make transmitter with only a single regrowth. Also the QWs are localized in the waveguide providing a possibility of high confinement factors which is ideal for lasers and modulators. An important advantage of the QWI platform is that we can have multiple bandgaps on the chip with a single MOCVD process without the need of Re-growth.

At the same time semiconductor optical amplifiers and detectors require additional regrowth steps of the p-cladding to form the ridge structure. Also it has been observed that low saturation power is obtained in case of SOAs and photodetectors.

The processing procedure is as follows in [57]. The QWI platform allows for good spatial resolution for bandgap engineering with real time control of temperature and implant dose. The used implant dose can be used to control the extent of intermixing using a single anneal step providing a possibility for obtaining several bandedges on the same chip, thus improving the integration of photonic components[58]

4.2.4 Dual Core Waveguide

This is a regrowth free technique for active-passive integration. This method was proposed in [59]. This platform has two or more waveguide cores and is suitable for multiguide vertical integration (MGVI). The MGVI is a platform aimed at multi-functional PICs. The Dual Core Waveguide (DCW) has been employed successfully for active passive integration for spot size converter(SSC) [60] and Optical amplifier and Electro-absorption modulator with SSC [61]. The DCW technique was used in the later to increase the mode spot size for coupling to a single mode fiber. In this DCW structure the active waveguide was laterally tapered and combined with the underlying passive waveguide.

The DCW technology is low-loss and compatible with current structures which are grown epitaxially on the InP platform[61]. One of the most important advantages of the DCW technology is that it does not require re-growth step, Electron beam lithography even for alignment of waveguide tapers. On the downside a high degree of control is required for dry etching of the waveguides[62].

4.2.5 Offset-Quantum well

We employ a simple active/passive integration using the offset Quantum Well (OQW) method. This OQW structure is obtained with two Metal Oxide Vapor Phase Epitaxial (MOVPE) growths. In this platform, growth with dielectric mask is not required which is an advantage as it is essential in butt-joint technology. In this we get a uniform crystal growth along the entire sample with a higher process yield. The important feature of OQW is that the MQW is not placed at the center of the core but is at the top of the core hence its name, as shown in Fig. The brief procedure for OQW is as follows:

- First MOVPE growth of a waveguide core, a thin InP etch-stop, a gain layer and a cap InP layer.
- Gain layer removal at the passive regions.

- Second MOVPE growth (first re-growth) of a waveguide cladding. (i.e. selective removal of quantum well in passive region followed by a blanket regrowth)

The OQW process has been considered as a dominant technology to realize active/passive integration [63], [64].We use OQW for our photodiode as this technique has been optimized and demonstrated as early as 1988[64]. One of the main advantages of the OQW is that this etch-and-regrowth procedure can obtain a high band gap contrast between the active region and passive waveguide as we can get 1550nm in the active region and 1300nm is passive waveguide. This contrast cannot be realized in the re-growth free process (i.e. Quantum Well Intermixing and Selective Area Growth). Now within the etch-and-re-growth technique (i.e. Butt Joint Technique (BJT) and OQW), the OQW has an important advantage over the BJT being that it is simple in processing. An additional potential disadvantage of BJT is not only the extra growth step required but also it is difficult to reproduce the joint geometry in each run process [65]. Also the BJT requires a 3-step MOVPE (2 re-growths) whereas the OQW can be fabricated with a 2-step MOVPE (1 re-growth). The disadvantage of the OQW process as compared to the other active/passive integration is that only two band gaps can be obtained and hence the passive waveguide core should be of the same material as the SCH. Moreover as the MQW is not in the center of the core so the optical confinement is relatively weak in this region. Even though this can be considered a drawback; an advantage of it is that it enables fine tuning of the confinement factor [43].

4.3 Etching

This one of the most important procedures employed in Photonic/Electronic semiconductor integrated circuit manufacturing. I have employed both the wet and dry etching technique for fabricating the PC integrated MQW PD.

4.3.1 Wet Etching

This Process involves the use of liquid chemical etchants. It is simple as one needs to dip the PIC chip in a chemical solution to allow the semiconductor to react with the chemical ions of the etchant. The etching profile strongly depends on the orientation of crystal plane being etched for a crystalline chip and its chemical properties. In addition to this the wet etching is isotropic. We have used the selectivity property of the chemical and substrates to our advantage. The wet etchant solutions used in our process are listed in the following table.

Material	Solution (Ratio)	Etching Rate
InP	HCl + H_3PO_4(1:3)	500nm/minute (RT)
InGaAs	H_2SO_4+H_2O_2+H_2O(1:1:10)	0.10μm/minute (RT) 140nm/minute ($8^\circ C$)
InGaAsP (MQW 0.4% CS^*)	H_2SO_4+H_2O_2+10H_2O(1:1:10)	50nm/minute ($5^\circ C$)
InGaAsP Q1.25	SBW^*+10HBr+40H_2O(1:10:40)	5nm/minute ($5^\circ C$)
SiO_2	Buffered HF	500nm/minute (RT)

Table 4.1: Wet Etching Process condition

CS : $Compressively\ strained$

SBW : $Saturated\ Bromine\ Water$

The Indium Phosphide 200nm Passive cap was etched after standard photo-lithography (PL) for defining the active and passive part of the chip. I did a 20second etch at room temperature, while vigorously shaking the sample during acid rinse. This is needed to avoid adhesion of the bubbles to the chip surface as Phosphoric acid is a sticky liquid. We also have to make sure that we do not do InP wet etching for a long time as there will be an undercut and the PL pattern can disappear.

For the InGaAsP MQW (104nm) + Separate confinement hetero-structure (SCH) (40nm) wet etching a mixture of Sulphuric acid and hydrogen per oxide acid along with water was used. These layers are present in the passive part of the chip and are etched at the same time. The temperature was maintained at $5^\circ C$ by using a portable water chiller. Moreover the acid solution was used within an hour because the acid solution may stop etching due to instability.

The InGaAsP Q1.25 Core thickness was adjusted using a mixture of Saturated Bromine water (SBW), HBr and water. The temperature was maintained at $5^\circ C$ for the etching solution. The etch solution was not stirred as the etching rate changes and we have to limit the etching rate to liquid phase diffusion.

4.3.2 Dry Etching

This type of etching is anisotropic and is also known as directional etch. It uses free radicals in plasma to remove material in gas phase from that part of the chip which is patterned by a photo resist. This is a technique which precisely controls etching depth a sidewall quality of the structure. We use an Inductively Coupled Plasma (ICP)- Reactive Ion Etcher (RIE) for dry etching the desired symmetric and Asymmetric Waveguide ridge structure. It should be noted that we did used the ICP-RIE etching instead of only ICP for smooth waveguide side walls. In ICP-RIE the plasma is generated and controlled by Radio Frequency (RF) powered magnetic field. The condition of etching depends on various process parameters some of them are gas flow rate, gas pressure, RF power etc.

For InP related material there are two type of chemistry used for generated plasma I. Ar/Cl_2 mixture and II. CH_4/H_2 + O_2 . Moreover O_2 is used to clean the chip and for Ashing process by which various resists and polyimide films are removed. The conditions I have used for dry etching with 'OXFORD PlasmaPro100 Cobra' ICP Etch System for InP and InGaAsP are listed in the table as follows:

	InP etching	InGaAsP etching	O_2 plasma cleaning
Gas Pressure	15.0mTorr	15.0mTorr	75.0mTorr
Source power	80w	80w	40w
Step Time	5 minute	5 minute	1 minute
O_2flow rate	0 sccm	0 sccm	50 sccm
H_2flow rate	48 sccm	48 sccm	0 sccm
CH_4flow rate	7 sccm	7 sccm	0 sccm
Etch rate	75nm/1$cycle^*$	38nm/1$cycle^*$	-

Table 4.2: Dry Etching Process condition

$1\ cycle^* = 5minutes$

The dry etching of SiO_2 was done for contact opening using the SAMCO dry etcher. The gases used and their flow rates are Argon=10sccm, CHF3 =10sccm; Chamber Pressure = 1 Pascal ; Forward Power(W_F)=100Watt and Reflected Power(W_r)=9Watt . The plasma observed was pinkish in color and stable. The schematic of the etcher is shown in Fig 4.3.

Before the deposition of silicon-dioxide using the sputtering process, I did the SiO_2 dry etching for the silicon-dioxide deposited by the Electron beam evaporation process. The condition of this 'ANELVA L-201D' ICP-RIE etching process are listed in the table below. The condition of this process is listed in the following table:

	Chamber Pressure	Source Power	Bias Power	O_2 flow rate	Ar flow rate	CHF_3 flow rate	Etching rate
Si O_2 etching	1 Pa	60w	25w	0 sccm	5.0 sccm	5.0 sccm	25nm/minute (approx.)

Table 4.3: Dry Etching Process condition for ANELVA ICP-RIE

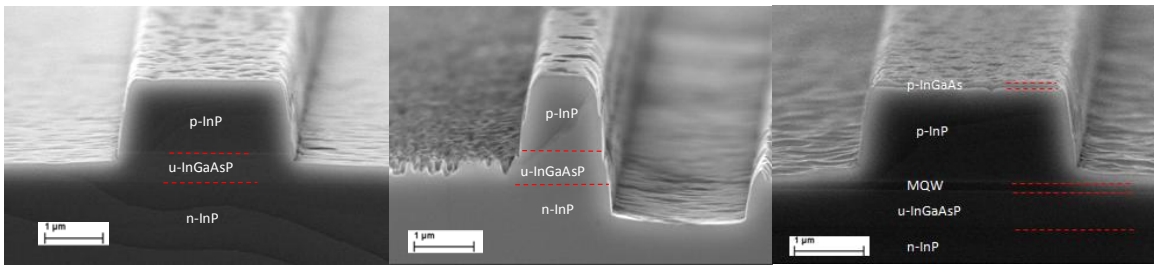

Figure 4-2: SEM images of cross sections of (a) passive (b) PC and (c) active parts of the fabricated monolithic device after SiO_2 wet etch (before passivation).

4.3.3 Ashing

This is the process of photo/electron beam –lithography resist removal using a plasma source. Oxygen and fluorine are the most common gases used for producing ions species for interacting with the resist.

For our process we use oxygen to remove the deposited polyimide for electrode contact opening for our Photodetector diode. The machine used for this process is the table top Samco dry etcher as shown in the Fig 3.2. The condition for removing polyimide are as follows; gas flow rate for O_2=10sccm; Chamber Pressure =45Pascal; Forward Power (W_F) =100Watt

and Reflected Power (W_r) =0Watt. The observed plasma during the process was white in color and stable.

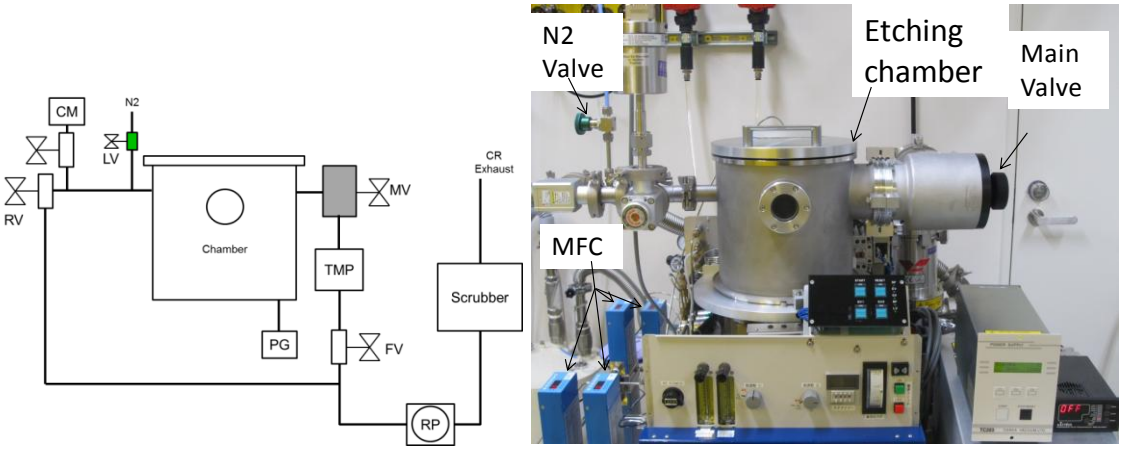

Figure 4-3: a) Schema tic of SAMCO dry etcher b) SAMCO Dry etcher Photograph

4.4 Deposition

This technique is used to deposit amorphous or poly-crystalline thin films. This technology differs from epitaxial crystal growth as there is no need of lattice matching with the underlying material. There are various deposition technologies depending on the requirement of the process. I have used first two technologies of the following namely

I. Sputtering deposition
II. Electron Beam evaporation
III. Atomic Layer deposition

This technique has provided me with etching masks, Passivation layer and electrode contact for the Photo-diode. The Atomic layer deposition was not used as the deposition rate is low and also the deposition takes place at a high temperature ($350^{\circ}C$). The high temperature causes the structure to be deformed and is a possible reason for the failure of re-growth for our fabricated device.

4.4.1 Sputtering

This process is also known as Physical Vapor deposition (PVD) and is used to deposit thin layers of semiconductor metals or dielectric. The basic idea is to deposit sputtered source material from the target on to the substrate sample. The source material is sputtered by ions or atoms of high kinetic energy. These high kinetic energy ions or atoms are generated using a radio frequency or DC power source. In our case we evacuate the chamber to a very low pressure (5×10^{-4}Pa) to reduce the possibility of contaminants in the sputter chamber. Later Argon gas is introduced in the chamber at 12sccm while the chamber pressure is maintained at

0.5Pa. one of the advantage of ANELVA sputter machine we use compared to older machines is that the sample is continuously rotating and thus we can obtain a uniform deposited thickness on the sample.

We have deposited a 150nm thick SiO_2 film on the sample. The quality of thin film in the sputter process is better than the Electron beam deposition as the material is deposited at high kinetic energy. Moreover mean free path of the deposited atom is shorter and hence the material is deposited from all directions. We can also use Plasma Enhanced Chemical Vapor Deposition (PECVD) in case one wants a higher quality film compared to sputter deposition.

<table>
<tr><td colspan="2">Pressure before use</td><td>Sample</td><td>Target</td><td colspan="2">RF/DC</td></tr>
<tr><td colspan="2">~5.7x10^{-5} Pa</td><td>InP</td><td>SiO_2
(150 nm)</td><td colspan="2">RF</td></tr>
<tr><td>Temperature at deposition</td><td>Height during deposition</td><td>RF Power Forward Power(W_F) & (W_r)</td><td rowspan="2">Ar : 12 sccm
O_2: 0 sccm
N_2: 0 sccm</td><td>Chamber Pressure at deposition</td><td>Time</td></tr>
<tr><td>Room Temperature</td><td>80 cm</td><td>W_F=100W
W_r=0W</td><td>0.5 Pa</td><td>40 minute for 150nm</td></tr>
</table>

Table 4.4: Sputtering Process Condition

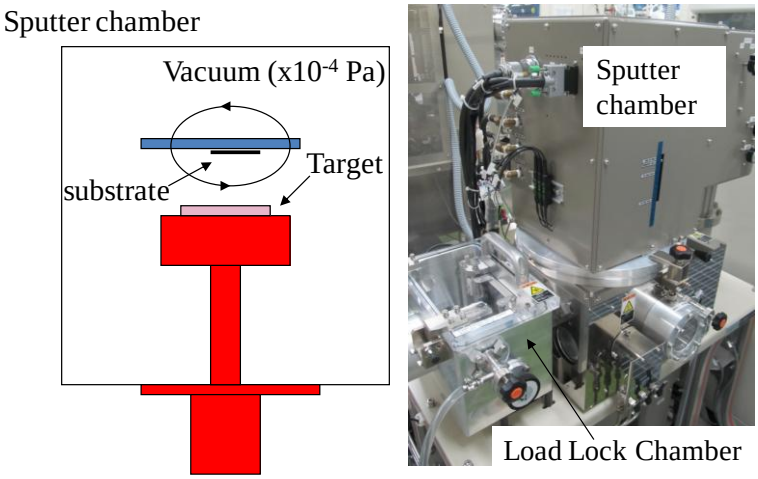

Figure 4-4: a) Simplified Schematic of sputter machine b) photograph of sputter machine

4.4.2 Electron Beam Evaporation

This is also a Physical vapor deposition process like sputtering but the quality of the thin film deposited is of a considerably low quality. In this a electron beam under high vacuum(less than $10^{-4}Pa$) is incident on the target material. This condition causes the atoms of the target material to travel in the gaseous phase toward the sample placed face down in the chamber.

This technique has been used quite often by me when depositing on electron-/photo-lithography resist mask. The reason for using this technique is that the quality of the film is low and hence allows for easy liftoff by Acetone or ZDMAC for photo- or electron beam-lithography masks respectively. Another reason for employing the EB evaporation method is that as the power of deposition is lower the surface of the device is not adversely affected, this because the kinetic energy of the atoms being low the amorphous film being formed has many atomic vacancies.

I have done SiO_2 angled deposition at 60° while defining the Polarization converter and have also done flat SiO_2 0° deposition for defining the waveguide for active-passive regions. Moreover I have also done electrode deposition for Platinum (20nm)/Titanium (10nm)/Platinum (20nm)/Gold (400nm) for the top electrode contact. The Au top contact was deposited at 0° for 200nm and at $+60^\circ$ for the rest of 200nm. The back contact of the device was also made using Electron Beam evaporator at 0° for 400nm. The process for both flat and angled deposition is as shown below:

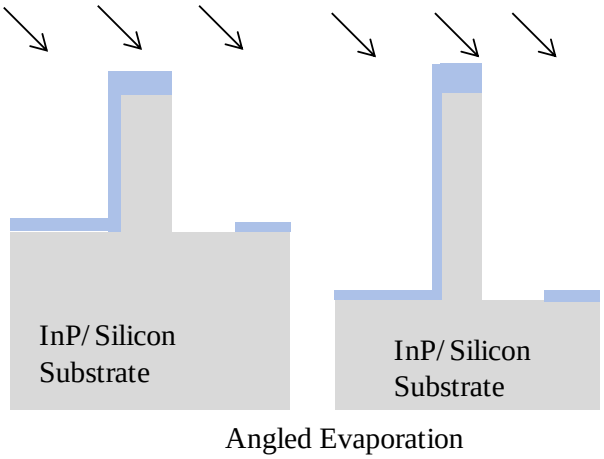

Figure 4-5: Self-aligned Angled deposition using Electron Beam Evaporator

4.5 Crystal Growth/Re-Growth

4.5.1 Metal Oxide Vapor Phase Epitaxy

All crystal growths are done by using Metal Oxide Vapor Phase Epitaxy (MOVPE) on an Aixtron200/4 system. In this the sources used for Group-III elements were trimethylgallium (TMGa), trimethlyindium (TMIn) and for group-V elements were tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP). Dimethyl-zinc (DMZn) and Hydrogen sulphide (H2S) are used for p-type and n-type doping respectively. It is essential to keep the reactor used for crystal growth turbulence free to avoid imperfect interfaces. This is achieved by keeping the gas flow rates always constant so as to maintain the appropriate partial pressure. In our case the flow rate was kept constant on the run hydride, run Fe and run MO lines with 5500sccm, 1500sccm and 6000sccm respectively. Also the reactor pressure is maintained constant at 100mbar. The wafer is rotated at 50rpm on the suseptor during growth to obtain a uniform growth over all the sample area.

Moreover we can change the partial pressure of the materials being deposited to control the growth rate, composition and doping level. We grow InP/InGaAs on a Quaternary Q1.25 InGaAsP layer. This Quaternary structure is the undoped passive core of our PC-Integrated PD structure. The advantage of having a quaternary core is that we can adjust the bandgap and lattice constant simultaneously for this layer. The band gap of this layer is engineered to support modes in the wavelength range of the C-band (1.3μm to 1.6μm)

The pressure we use for our MOVPE process is 100mbar which is advantageous as compared to Molecular Beam Epitaxy (MBE) as this can be used for mass production. We grow both undoped (u-) and p-doped Indium Phosphide at $610^{\circ}C$ to obtain a high quality crystal structure. The p-InGaAs contact layer is grown at $550^{\circ}C$. I have also made sure that the V/III ratio is high for my re-growth so as to attain a higher quality of crystal growth. An important dynamic that was understood while doing the crystal growth was to flow both Arsenic and phosphorous in a pre-determined ration so as to avoid desorption of arsenic from the chip and hence preventing the semiconductor chip becoming metallic (as Indium content would be higher).

The Gas flow rate Table for the recipe I used is shown in the Table 4.5, also the gas line schematic is presented in figure 4-6.

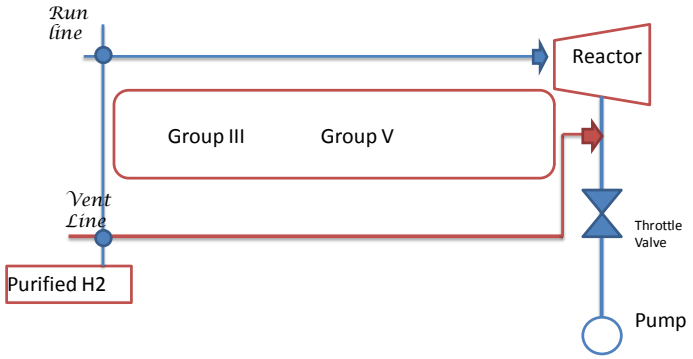

Figure 4-6: Simplified Schematic of MOVPE Process equipment

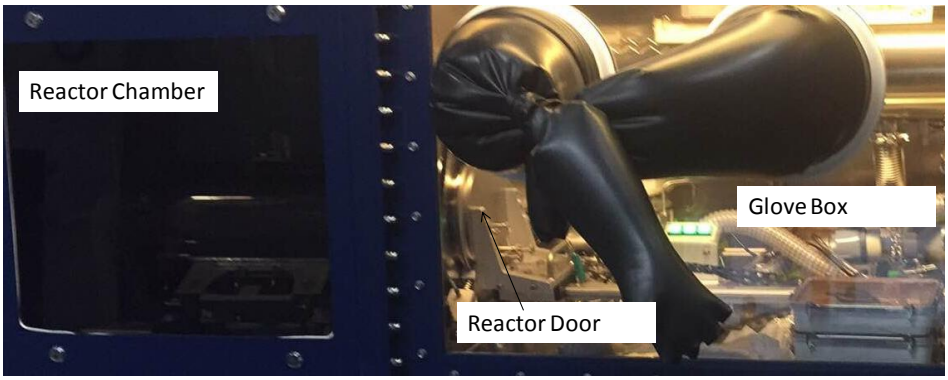

Figure 4-7: MOVPE Process equipment photograph

		Base flow			**Vent**								**Total flow**			
Process	Temperature	Run_ MO feed	Run_ Fe feed	Run_ Hydrid feed	Run_ MO vent	Run_ Fe vent	Run_ Hyd vent	TMGa _1 .inject1	TMIn _1 .inject 1	TBAs_ 1 .inject1	TBP_ 1 .inject 1	TBP_1 .inject1	III 属流量 [sccm]	V 属流量 [sccm]	総流量 [sccm]	V/ III
Initialization		5096	1500	4519	600	150	550	190	230	25	280	12	7500	5500	13000	**40**
Ramp up	RT to 200	5096	1500	4519	600	150	550	190	230	25	280	12	7500	5500	13000	**40**
V pre-flow	200 to 610	5338	1500	4824	600	150	550	190	0	0	280	0	7500	5500	13000	**-**
Change reactor pressure & source set	610	5528	1500	4824	600	150	550	0	0	0	280	0	7500	5500	13000	**-**
Hydride switching	610	5528	1500	4824	600	150	550	0	0	0	280	0	7500	5500	13000	**-**
u-InP	610	5528	1500	4824	600	150	550	0	230	0	280	0	7500	5500	13000	**30**
p-InP	610	5298	1500	4824	600	150	550	0	230	0	280	0	7500	5500	13000	**30**
Ramp down	610 to 550	5103	1500	4324	600	150	550	0	230	250	280	120	7500	5500	13000	**49**
p-InGaAs	550	5460	1500	4970	600	150	550	190	230	250	0	120	7500	5500	13000	**12**
cool down		6000	1500	5500	600	150	550	0	0	0	0	0	7500	5500	13000	

Table 4.5: MOVPE Re-Growth Condition

4.6 Lithography

This involved making patterns or design on a semiconductor wafer. This process is widely used in the electronic and photonic semiconductor manufacturing. It involves the use of a light or energy sensitive resist made of polymer or organic resin. I have used both the Photo- and Electron Beam lithography for my device fabrication. Electron beam lithography is only required when the pattern to be transferred on the semiconductor chip is in sub-micron scale. I have used the EB-Lithography process only during waveguide patterning for PC and active regions. The lithography process can be simplified to three major steps which are Coating, Exposure and Development.

I have defined both lithographic techniques in detail as follows:

4.6.1 Photo- Lithography

This consists of various optical Photographic techniques used to transfer patterns from masks to the semiconductor wafer. The various windows obtained in this process are used to define spaces for semiconductor processing (mostly etching). I have used contact photolithography for defining the active-passive region, polarization converter and Electrode definition. During this process the resist is exposed to light coming through a glass/Quartz substrate with etched chrome. Part of the light which goes through the mask changes the properties of the resist. Further chemical process removes or retains the resist depending on its type. The Photo-lithographic imaging system used by us are two fundamental governing equations given in eq.4.1 and 4.2 which limit its applicability in the sub-micron scale due to the light source used. The PL does provide us a possibility to shift to Extreme Ultraviolet Light source which can give us feature size as small as 30nm [66].

$$\text{RES} = \frac{k_1 \lambda}{NA} \qquad (4.1)$$

$$\text{DOF} = (k_2 \lambda)/(NA)^2 \qquad (4.2)$$

Where, λ is the wavelength of light source used in the photo-lithography equipment

Except for the PC mask which used a negative tone resist (AZ5214E), the other two lithography steps used a positive resist(S-1805 & AZ5200NJ). AZ5214E negative tone resist was used for defining the PC region on the wafer. Also I have made sure to use soft contact during the transfer of pattern, as InP is quite brittle and may fracture due

to applied high pressure. Also specific care should be taken to make sure the photoresist is properly exposed else there can be some or total loss of the pattern. While the rest of the details are listed in the appendix we explain the first photolithography process in the table below:

Photo-Lithography: Active/Passive Area Definition
i. **Organic cleaning :** Cleaning with Acetone for 3 minutes & with IPA for 2 minutes twice. The N2 gun cleaning will remove any organic waster or moisture. ii. **Spin Coat Resist :** a. Use Primer & S-1805 resist to spin individually with conditions :- i. 500 rpm for 5 seconds ii. slope for 5 seconds iii. 6000 rpm for 40 seconds iii. **Pre-Bake** : $110^{\circ}C$ for 90 seconds iv. **Photo-lithography:** a. Measure the power of Hg-Bulb by using power meter(generally power is 24mw/cm^3) b. Exposure for the sample for 2.5 seconds v. **Developing resist** : a. NMD3 rinse for least 8 minutes while vigorously shaking ,then rinse in two water beakers for 2minutes each

Table 4.6: Photo-Lithography Process Condition

4.6.2 Electron Beam- Lithography

As the name suggests we use a beam of electrons to draw custom shapes or patterns on the surface of the semiconductor material covered with an EB sensitive resist. This involves the use of sophisticated equipment housing an electron gun in an almost vacuum chamber. A solution of resist is coated onto the semiconductor for a focused electron beam to be selectively exposed on it. The desired pattern is drawn on to resist coated chip by exposing it to the electron beam. This electron beam is focused and can be deflected in different directions. This chip is then developed using chemical solution for obtaining the desired pattern. Even though the volume of devices which can be fabricated with this method is low, feature sizes as low as 2nm has been achieved [67].

The EB-lithography is also used to fabricate the masks used in

photolithography or in fundamental Nano-science Research & Development. The waveguide mask pattern and the procedure to transfer it to the chip for our device fabrication are as follows:

Electron-Beam Lithography: Waveguide Patterning
i. **Organic cleaning:** Cleaning with Acetone for 3 minutes & with IPA for 2 minutes twice. The N2 gun cleaning will remove any organic waste or moisture. ii. **Spin Coat Resist :** a. Use Primer & ZEPP520A resist to spin individually with conditions :- i. 500rpm for 5 seconds ii. slope 5 seconds iii. 4000rpm for 60 seconds iii. **Pre-Bake** : $180^{\circ}c$ for 3 minutes iv. **Electron Beam-Lithography:** a. Adjust the proper dosage information before exposure 30μC/cm^2 v. **Developing resist** : a. ZED-N50 rinse for least 6 minutes or till the pattern is clearly visible while vigorously shaking, then rinse in two IPA beakers for 2minutes each.

Table 4.7: Electron Beam-Lithography Process Condition

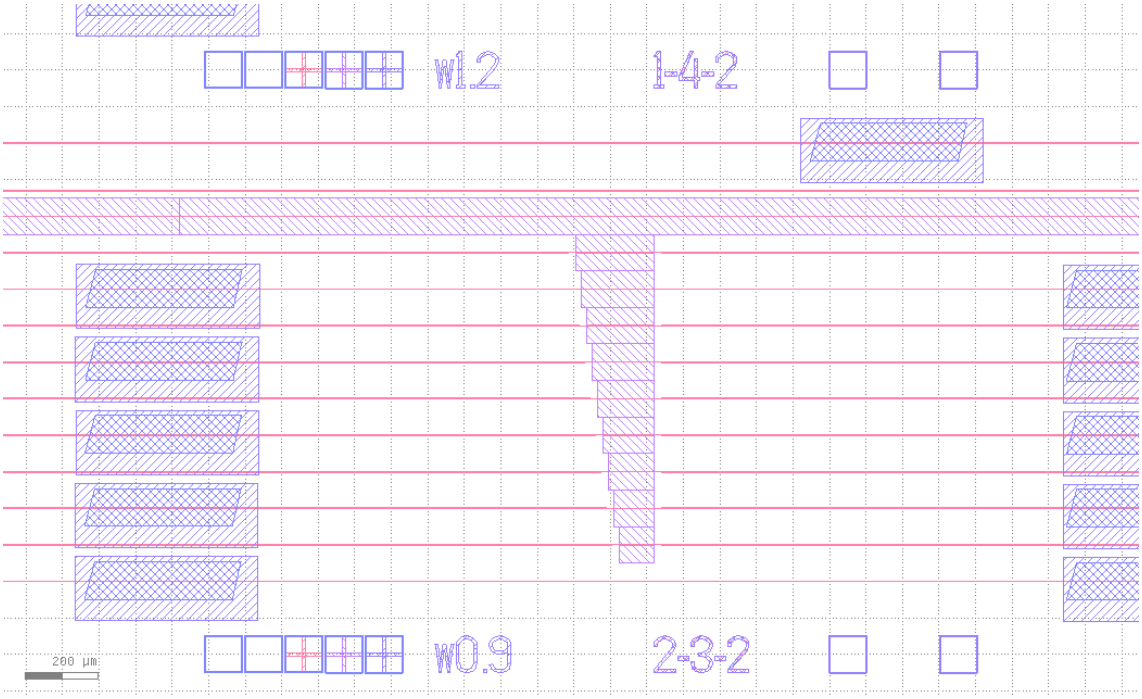

Figure 4-8: Waveguide Mask in K-Layout software used for Electron Beam Lithography for fabricated device.

4.7 Lift-off

This Process is used for creating structures by using a sacrificial layer on the semiconductor surface. It works in an opposite way to etching and is generally used for structures which are difficult to etch away properly. In this the material is blanket deposited over all the area of the resist (including the etched/developed part of resist). Then the chip is immersed in a solvent which 'lifts-off' the resist along with the deposited material, leaving the material in the trench (etched/developed part of resist) as it is. Thus providing us with the film deposited directly on the semiconductor surface.
We use AZ5214E which is apt for lift-off process as a negative resist. The optical microscope pictures of before and after liftoff process are as shown in Fig. 4-9.

Moreover we have employed this technique for waveguide and electrode formation. For the waveguide formation I deposited SiO_2 on the developed EB-resist and used ZDMAC for liftoff of the ZEP520 (EB-resist). The amount of SiO_2 was approximately 375nm which was easily lifted off along with ZEP520. For the Electrode Formation we have deposited Platinum 20nm/Titanium 10nm/Platinum 20nm and Gold 400nm on the top of the chip coated with AZ5200NJ**.** For lift-off we heated the acetone

at $70^{\circ}C$ for about 20 minutes then immersed the chip in same acetone beaker for an overnight liftoff. A little air bubbling was required after the overnight (7 hours) liftoff to help the metal and the photo resist come off easily.

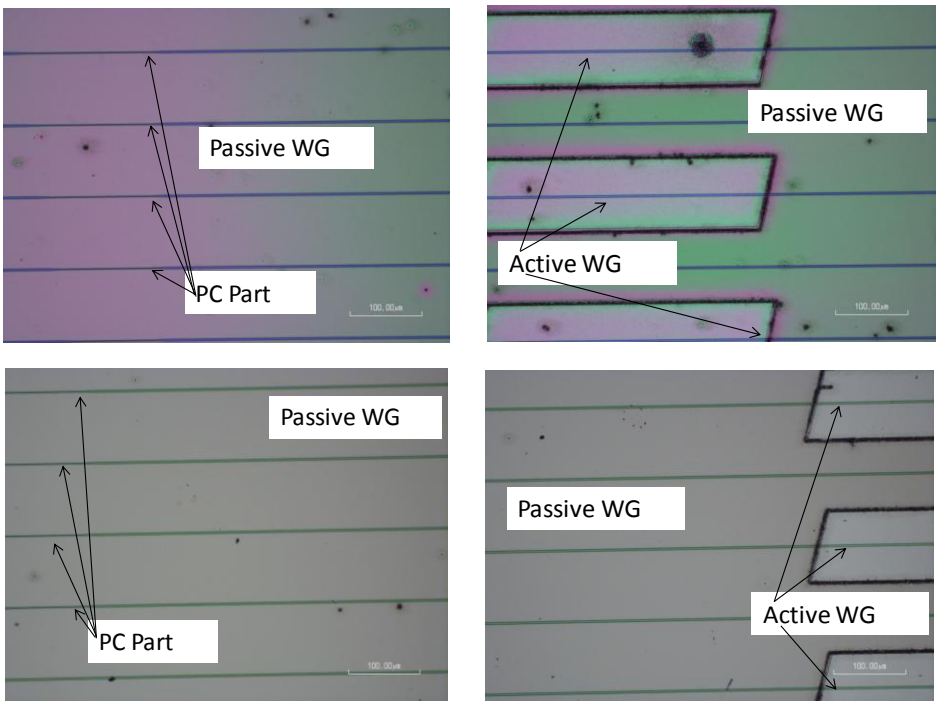

Figure 4-9: Optical Microscope images of a) Before SiO_2 Liftoff b) after SiO2 Liftoff during WG fabrication.

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4.8 Process Flow

The step wise fabrication process is displayed in this process flow and a brief explanation has also been provided for the same. Detailed explanation with the corresponding process condition has already been given previous in this chapter.

The Semiconductor layer stack used in this fabrication was produced by Land Mark Optoelectronic Corporation and its details are displayed in Table 4.8.

Sr. no	Layer name (doping concentration)	Thickness
1	InP Substrate S-doped (2-8 x 10^{18} cm^{-3})	$2^{"}wafer$ 350+/- 25µm
2	n-InP (5x$10^{17}cm^{-3}$)	300nm
3	u-InP	200nm
4	u-1.25µm InGaAsP	540nm
5	u-InP	10nm
6	u-InGaAsP	20nm
72	6x u-InGaAsP(QW + 0.4% CS) / 7x u-InGaAsP Barrier ($\lambda_{PL} = 1540$nm)	8nm /8nm (total : 6*8 + 7*8 = 104nm)
8	u-1.25µm InGaAsP	20nm
9	u-InP	200nm

Table 4.8: Epitaxial wafer Layer Stack.

The fabrication process flow is explained as follows:

1. The wafer layer stack is as given in Table 4.8 and it consists of an n-doped InP layer followed with an un-doped InP layer 300nm thick. On top of these layers we have a 540nm un-doped InGaAsP core layer. A stack of 0.4% compressively strained MQWs is above the core and has a $\lambda_{PL} = 1540nm$. An 10nm etch stop layer is present between the Q1.25 Core and MQW layer which does not affect the optical confinement.
2. Active-passive region is defined using photolithography by S-1805 resist. Next the InP from the passive part is Etched using a solution of HCl + 3H_3PO_4. It should be noted that vigorous shaking of the etch solution is important so as to avoid adhesion of bubbles to the sample being etched.
3. After Confirming the etched layer thickness by a surface stylus profilometer, we proceed for MQW/InGaAsP etching of passive part using an acid etch solution with composition of H_2SO_4+H_2O_2+10H_2O. We observe the change in color of the surface of sample being etched along with time to stop etching. Also we etch out the etch stop layer using same acid solution described earlier. The etch stop

layer etching is done for 5 seconds or till the bubbles stop. This etching should not be done long as there will be a large undercut and can damage the sample.

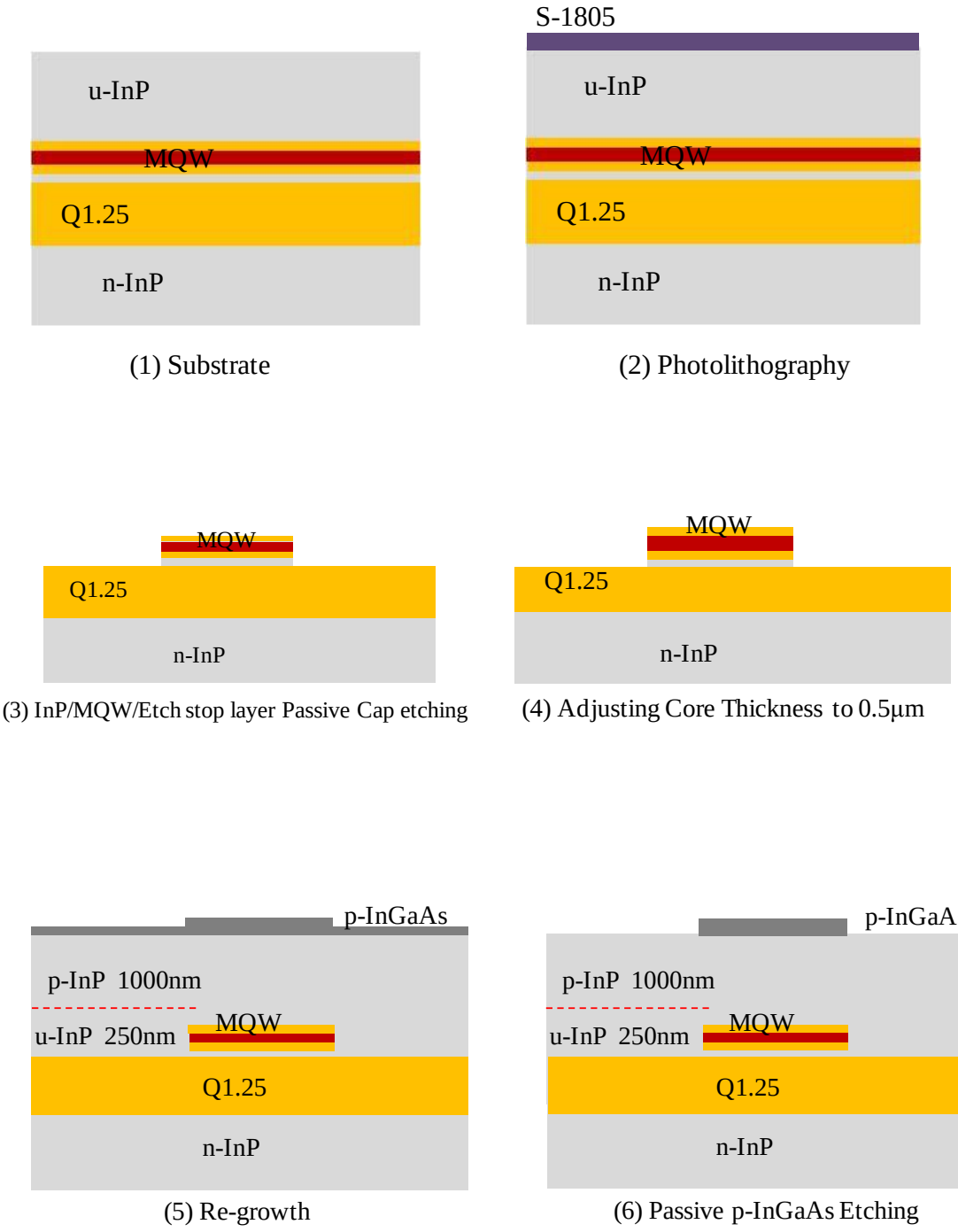
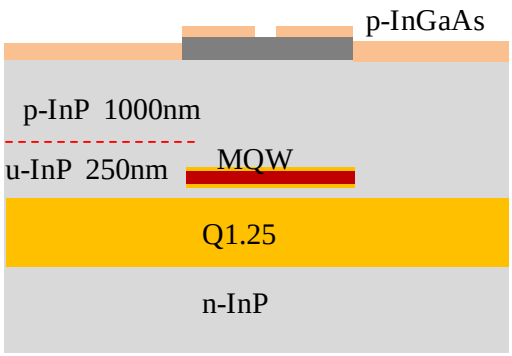
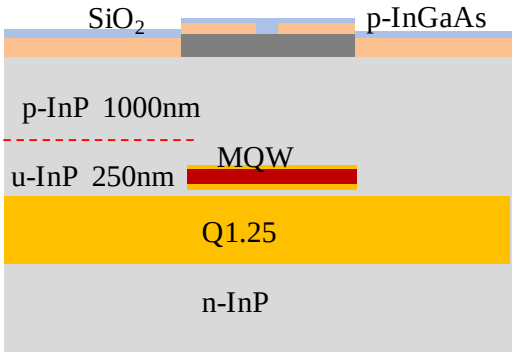


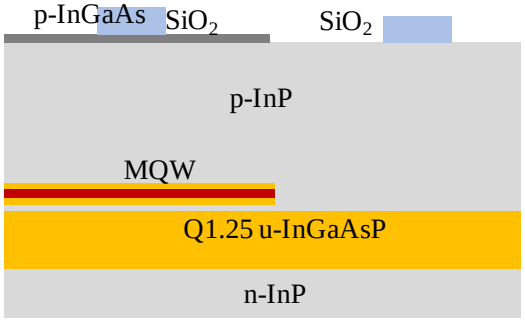
Figure 4-10: Device Fabrication Process Flow



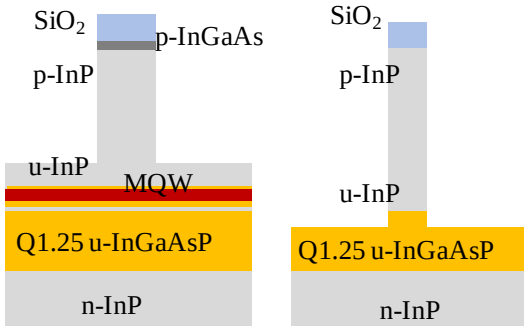
(7) Waveguide Patterning



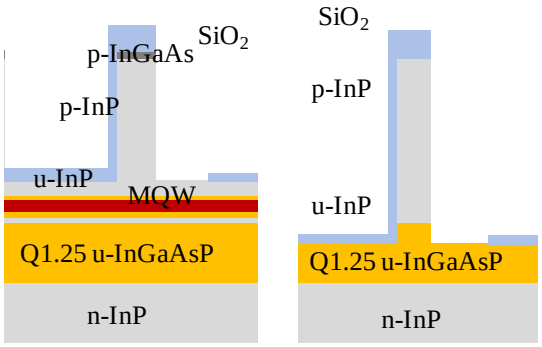
(8) SiO_2 Evaporation



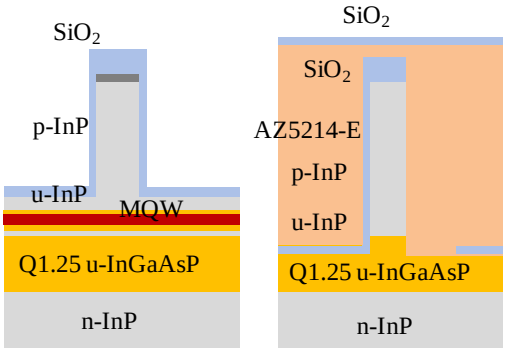
(9) SiO_2 Lift-off



(10) InP /InGaAs/InGaAsP Dry Etching

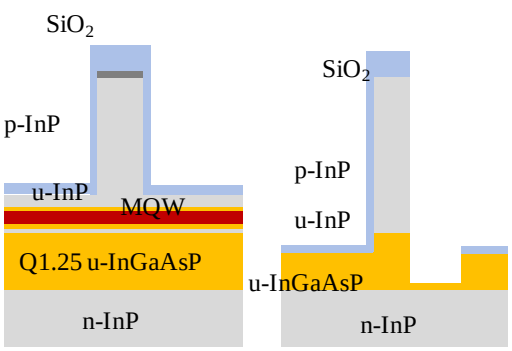


(11) SiO_2 Angled Evaporation

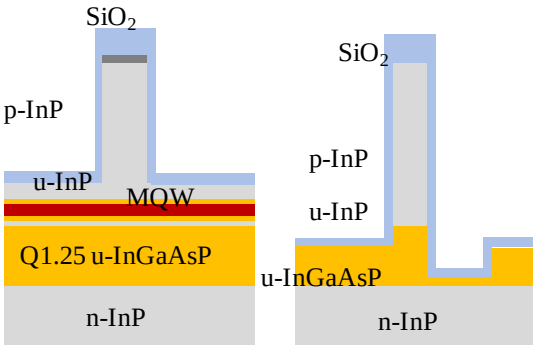


(12) Photo-lithography & SiO2 Angled Evaporation

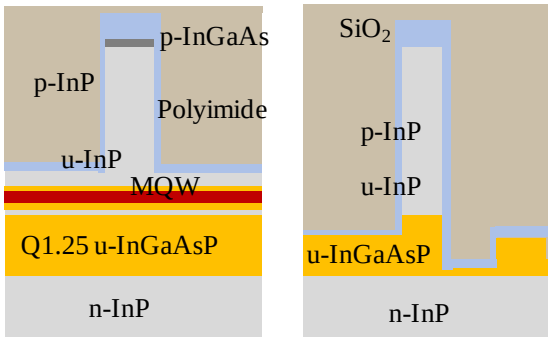
Figure 4-10: Device Fabrication Process Flow



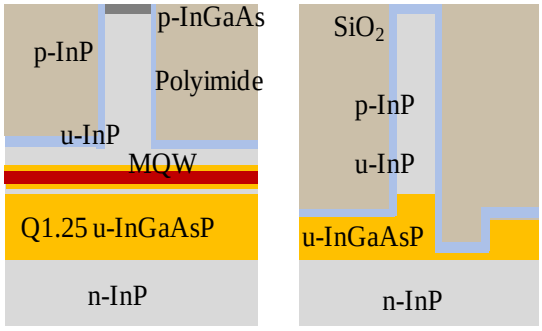
(13) Polarization Convertor Definition



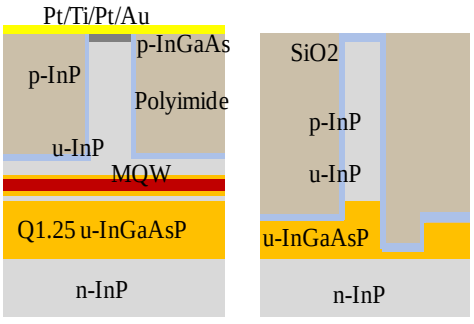
(14) Sputter SiO_2



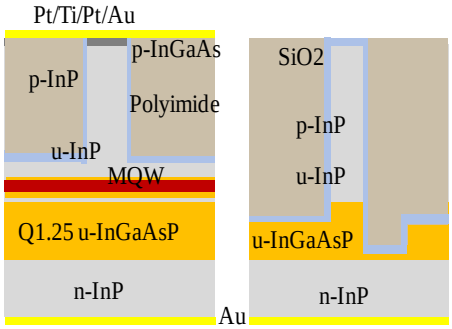
(15) Polyimide Coating & Curing



(16) Electrode Contact Open



(17) Electrode Metal Deposition & Lift-off: Front Contact



(18) Electrode Metal Deposition : Back Contact

Figure 4-10: Device Fabrication Process Flow

4. Next we will try to do the u-InGaAsP core etch to adjust its thickness to 500μm. For this we employ a Br-based etchant at $8^{\circ}C$ for 2 minutes with a composition of acid being SBW+10HBr+40 H_2O. Moreover one should not stir the sample/solution while etching to make the etching rate limited to liquid phase diffusion.
5. In this step we first remove the S-1805 photo-resist using acetone at $50^{\circ}C$ for about 10 minutes to ensure a proper removal. Next we remove the InP from the active region using the procedure mentioned earlier. After a proper cleaning with Sulphuric acid and Buffered HydroFluoric (BHF) Acid cleaning the sample was put on the MOVPE suseptor for a blanket re-growth of u- and p-InP along with p^+-InGaAs cladding and contact layers respectively. Moreover it should be noted that the transfer of the sample to the glove box should be as soon as possible. The re-grown epitaxial layer stack thickness of u-InP , p-InP and p^+-InGaAs is 250nm , 1000nm and 200nm respectively.
6. Using S-1805 and the active-passive photo-lithography definition again we remove the p^+-InGaAs cap layer from the passive region using the acid etchant with composition H_2SO_4+H_2O_2+10H_2O. Next the photo-resist was removed by acetone and the surface was cleaned with isopropyl alcohol.
7. Next waveguide patterning was carried out using Electron-beam lithography. For this first ZEP520A was spin coated onto the sample and exposed to the electron beam to write the waveguide pattern for both the active and passive part. The waveguides for OQW-PD and passive part except for the PC could have been made using photolithography as the resolution required was not in sub-micron scale. After this the EB-resist was developed using ZED-N50 (n-Amyl acetate) to obtain the required WG pattern.
8. After obtaining the waveguide pattern we deposited 375nm silicon di-oxide using an electron beam evaporator over the entire sample. Precaution must be taken while depositing SiO_2 as the oxide deposition is not stable and a very thick deposition can be the cause for lift-off process to be unsuccessful.
9. After the deposition has been completed we immediately put the sample into ZDMAC (Dimethylacetamide) at $80^{\circ}C$ for 25 minutes and then at room temperature for an hour. After removing the sample we got a complete sample lift-off process success.
10. After obtaining the waveguide pattern with the lift-off process, we continued with the Ridge area patterning using ICP dry etching for forming the waveguide structure. We etched 1450nm and 1200nm from the passive and active regions

respectively using the difference in etching rates of InP, InGaAs and InGaAsP respectively.

11. Next SiO_2 was deposited with a thickness of 100nm on one side of the device at an angle of 60° using an EB-evaporation technique explained earlier in this chapter.
12. Having covered the device on one side by SiO_2 a standard photolithography process was done using AZ5214E as a negative photo resist. This was done for defining the PC. After this a blanket deposition of SiO_2 was carried out with a thickness 100nm. Lift-off was done using acetone for 20 minutes at $55^{\circ}C$ and later at room temperature overnight. We did an overnight liftoff to avoid the use of an ultrasonic agitator which may damage the device.
13. The polarization converter was defined by dry etching the InGaAsP core and n-InP to fabricate the high-mesa structure on one side of the waveguide. After completion of dry etch, we used BHF to wet etching to remove the SiO_2 hard mask completely. I also did a few minutes dry etch to remove SiO_2 perfectly.
14. Next Passivation of our device was carried out by deposition SiO_2 using sputter at room temperature. The SiO_2 layer thickness was 150nm.
15. Later polyimide UR-3100E was coated and cured for an hour at $350^{\circ}C$ using a Rapid Thermal Annealer (RTA).
16. Electrode contact open process was done by a combination of ashing and silicon di-oxide etching. O_2 ashing by RIE was carried to remove the polyimide on top of the PD waveguide. SiO_2 dry etching was also carried out in the same samco etcher used for ashing in the contact open process.
17. Photolithography was done with AZ5200NJ for defining the electrode location for metal deposition. Later the metal Pt/Ti/Pt/Au was blanket deposited using electron beam evaporation process. The Pt/Ti/Pt/Au was deposited with a thickness of 20nm , 10nm , 20nm and 400nm respectively. In order to have a proper electrode contact with the external world, 200nm gold was deposited over the complete sample and the remaining 200nm was angle deposited at 60°. In the end acetone was used for liftoff for a period over six hours.
18. The back contact was formed by electron beam evaporation of 400nm of Gold on the back substrate surface of the sample. After this the sample was annealed using a RTA at $350^{\circ}C$ for 2 minutes to obtain sufficient ohmic contacts.
19. In the end the chip was cleaved into unit devices for optical characterization and mounted on the Copper plate using Ag-paste as conductive glue. The silver paste was heated for 20 minutes at $150^{\circ}C$ to solidify and dry out the glue.

4.9 X-Ray Diffraction Analysis

X-ray diffraction (XRD) is a tool which is very useful for identifying the atomic and molecular structure of a crystal. In this and incident X-ray beam on a crystal is diffracted into many specific directions depending on the crystal structure. One can obtain information like the structure of crystal lattice, electron density, the mean position of the atoms in the crystal as well as their chemical bonds and disorder information.

In this process a single crystal is mounted on a goniometer. The goniometer is used to position the crystal at the selected orientation. The crystal is bombarded with finely focused monochromatic beam of x-rays which produces a diffraction pattern of regularly spaced spots known as reflections. These reflections may add constructively in a few specific directions determined by the Bragg's Law. The two- dimensional images taken at different rotations are converted into a three dimensional model of the density of electrons within the crystal using the mathematical method of Fourier transforms combined with chemical data known for the sample. This process makes use of the Bragg's law of diffraction

$$2d\sin\theta = n\lambda \qquad (4.3)$$

Here'd' is specific to the target (crystal or sample).

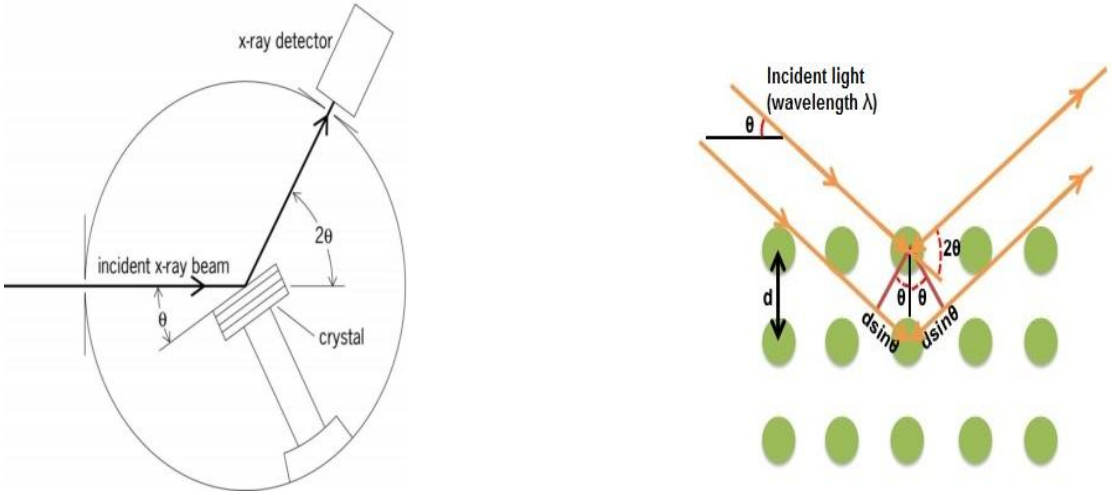


Figure 4-11: (a) An XRD setup (b) X-ray diffraction on the crystal surface (the crystal is periodic in both vertical and lateral directions in our case).

4.9.1 Condition for InGaAs Contact layer

The recipe designed for obtaining the growth for InGaAs and InP observed a good growth on visual inspection, but a closer observation using XRD showed a lattice mismatch with a strain higher than 1000ppm. The XRD plot for this measurement is displayed in Fig. 4-12.

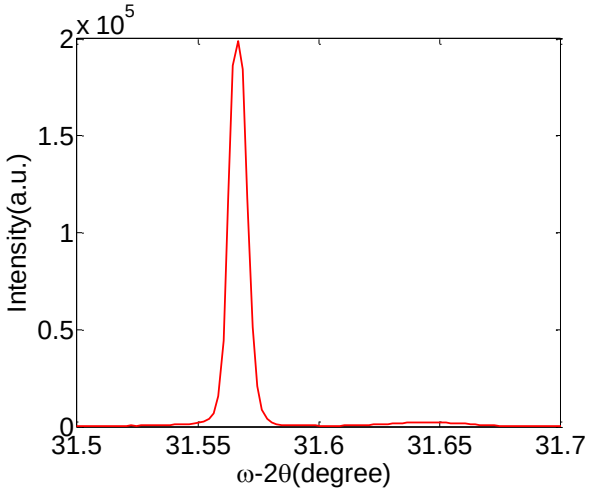


Figure 4-12: XRD plot for InGaAs condition

We used a rocking curve to plot the XRD graph. In this the sensitivity of the reciever is low but it takes the measurement doesn't take a long time to complete. In Fig. 4-12. We observe that there is absence of lattice matching between the InP and InGaAs layers. The stronger peak on the left corresponds to the InP and one on the right corresponds to InGaAs. It can be infered from the fitting that Gallium is too much. Moreover we need more Indium now from $In_{0.512}$,we need $In_{0.53}$ for obtianing a lattice matched condition.

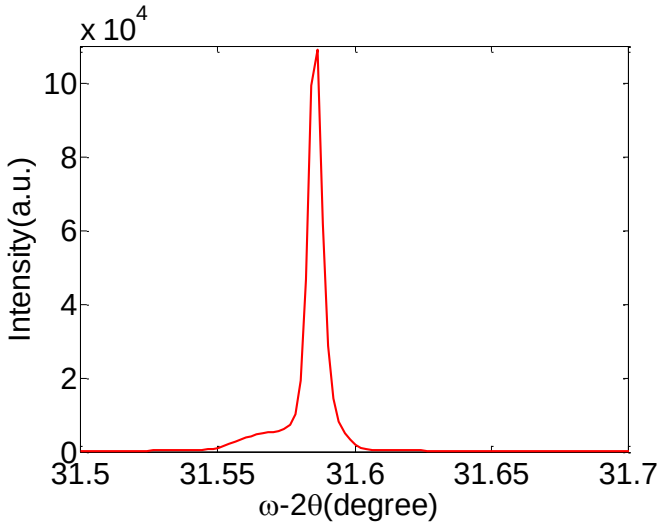


Figure 4-13: XRD plot for InGaAs condition with In0.53

As can be observed in Fig.4-13, we obtain a lattice matched condition with a reduced gallium content for the InGaAs layer. The strain obtained in this condition is 248ppm which is suitable for fabricating our InP PC integrated OQW-PD.

4.10 Summary

The scanning electron microscope (SEM) images of the fabricated PC-integrated MQW PD along with its cross sectional schematics are shown in Figs. 4-14.

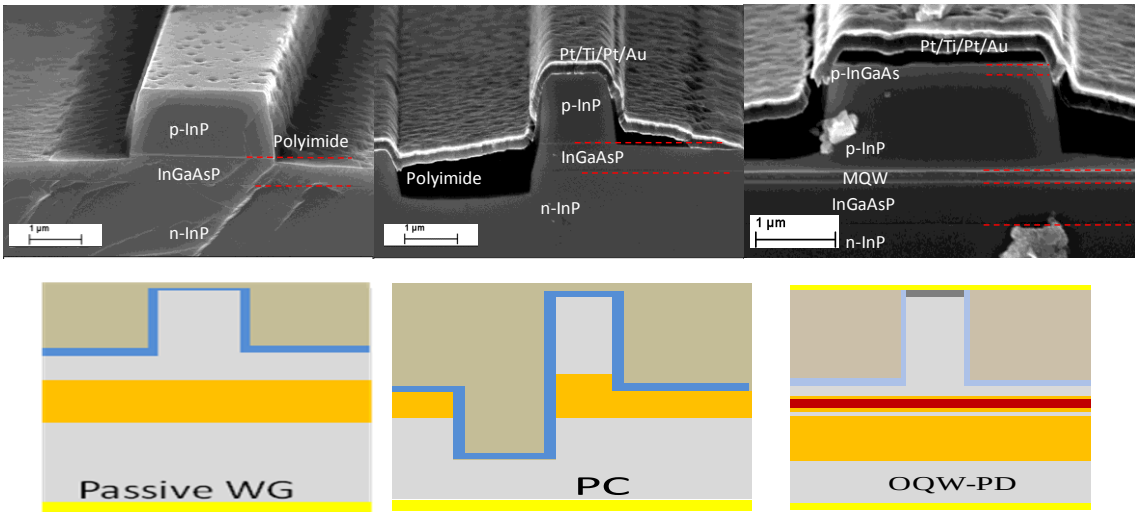


Figure 4-14: SEM images of cross sections of (a) passive (b) PC and (c) active parts of the fabricated monolithic device. The schematic views are also shown

.

We have successfully fabricated a monolithically integrated half-ridge PC and an MQW PD on an InP substrate. With this relatively simple fabrication process and its compatibility with standard ridge waveguide components, future integration with other components can be expected to obtain large-scale photonic integrated circuits (PICs) with on-chip polarization manipulation.

Chapter 5

Device Characterization

The range of wavelengths used in Telecommunication including optical fiber communication network is of interest to us. This is the target range for the device we have fabricated. Evaluating our device for both the active and passive parts is essential to prove its working and understanding its characteristics.

This chapter starts with first characterizing the Photodiode for evaluating its electrical properties. Having confirmed its working we moved on for optical characterization of the integrated device. For the optical characterization it is important to evaluate the fabricated waveguide quality. This quality can be experimentally studied by using the Fabry-Perot Resonance Technique[68]. Once it was established that the waveguides were good enough for optical characterization with losses in the permissible range, we proceed towards characterizing the monolithic integrated device consisting of a polarization converter integrated with a Photodetector.

For starting with the characterization, we cleaved the chips carefully so as not to degrade the quality of chip physically. Next the cleaved samples were mounted on a Copper (Cu) plate. The Cu plate and InP sample were glued using Silver paste heated for 15 minutes at$150^{\circ}c$. Next an aluminum metal adhesive tape was put below the Cu plate to attach the electric common or ground cable to the copper plate with the back contact electrode of the InP chip in contact. This measurement setup is as shown in the Fig.5-1.

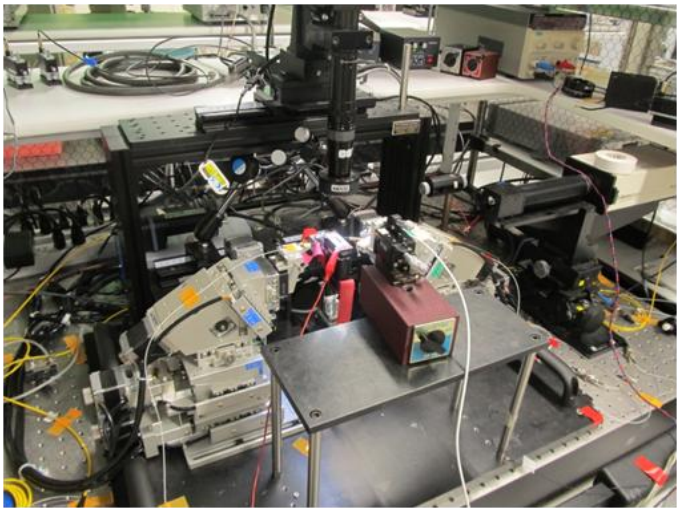


Figure 5-1: Photograph of Measurement Setup

5.1 Electrical Characterization

To verify the functioning of the p-i-n-junction formed with the OQW re-growth process the Current-Voltage (I-V) characteristics are measured in dark condition (No photon flux present). The IV-Curve is as shown in figure 5-2. This PD was characterized by applying a voltage over a range of -2 volts to +2 volts. It is essential to evaluate the magnitude of reverse current flowing through the semiconductor diode to understand its applicability for use as Photodetector in reverse bias. We have found as illustrated in figure 5-2 that the reverse bias current is in nA range which is small enough to use the device successfully as a Photodetector.

At this point I must mention that the electrode contact open step was critical and was found to be the main culprit for fabricated leaky diodes found on an earlier device made by us during an identical earlier process.

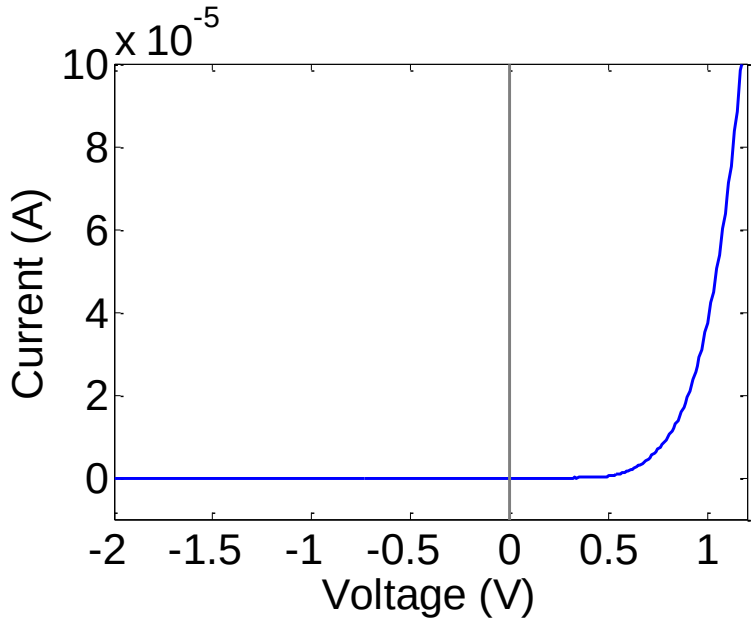


Figure 5-2: Photograph of Measurement Setup

5.2 Optical Characterization Setup

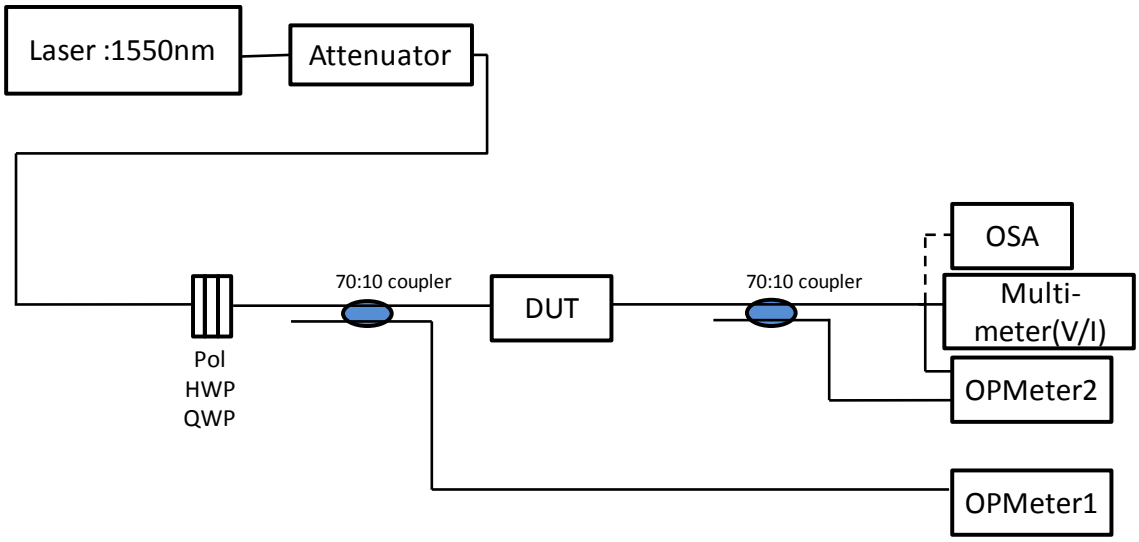


Figure.5-3: Optical Measurement for WG loss measurement using Fabry-Perot Technique

In Fig.5-3 shows the setup for measuring the attenuation loss in the waveguide by using Fabry-Perot Resonance Technique. In this we use a tunable laser source with emission wavelength at 1550nm. This light is then sent through an attenuator to obtain a pre-determined input; this is then sent through a polarizer

consisting a polarizing plate. Half wave plate and a Quarter wave plate. At the output of the this optical setup we obtain either a TE- or TM- mode of light depending on the adjustment of the wave plates. This input light mode is then sent to a 70:10 light coupler. Thus 70% input light is coupled to the core layer of device under test (DUT) whereas the rest of the light is sent to the Photodetector measuring equipment. The light is coupled with some losses (insertion/facet loss) into the DUT.

At the output facet of the DUT we collect the light by aligning the output optical fiber to the Core layer of the DUT passive waveguide. This light mode is then sent to the output 70:10 coupler where 70 % of the light is sent to the power meter and the rest is used for fiber alignment. As can be seen from the Fig.5-5 that the Total Attenuation loss (waveguide propagation + Insertion + Excess) is higher for the TM-mode as compared to the TE-Mode; this is in agreement to the theory as TE mode is more confined to the core than TM-mode due to the Maxwell's equation and the boundary conditions applicable to this structure. It can be said that the total losses are loss and hence the waveguide fabrication was successful and the fabrication quality was high. From the setup in Fig.5-3 the Total Loss for TE mode was found to be α_{TE}=13dB and for TM-Mode it was α_{TM}=15.7dB at 1550nm.

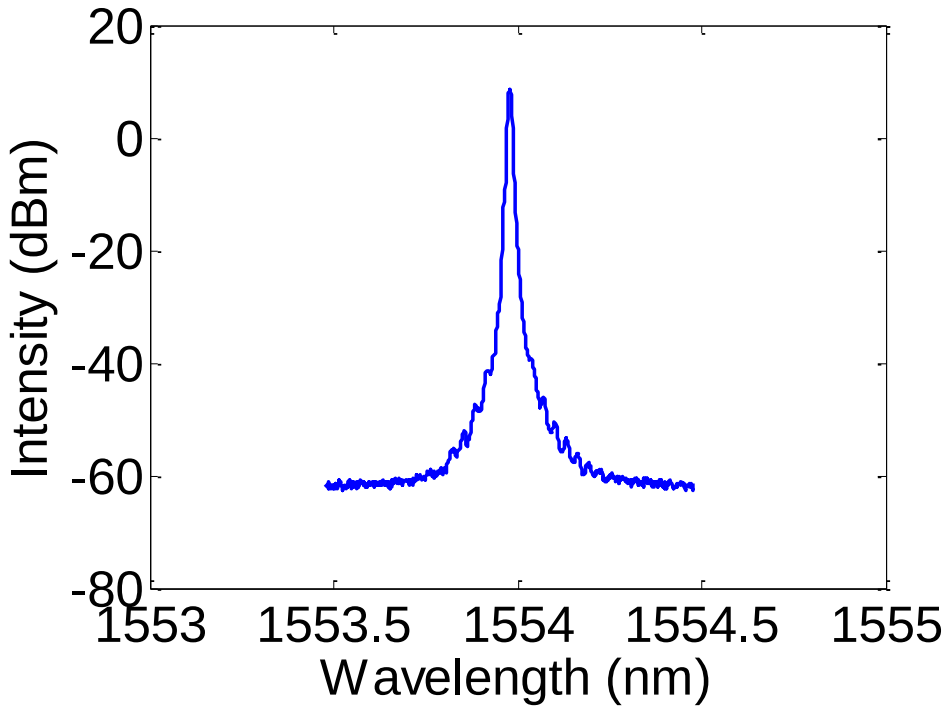


Figure 5-4: Input Signal Spectrum for Fabry-Perot Technique

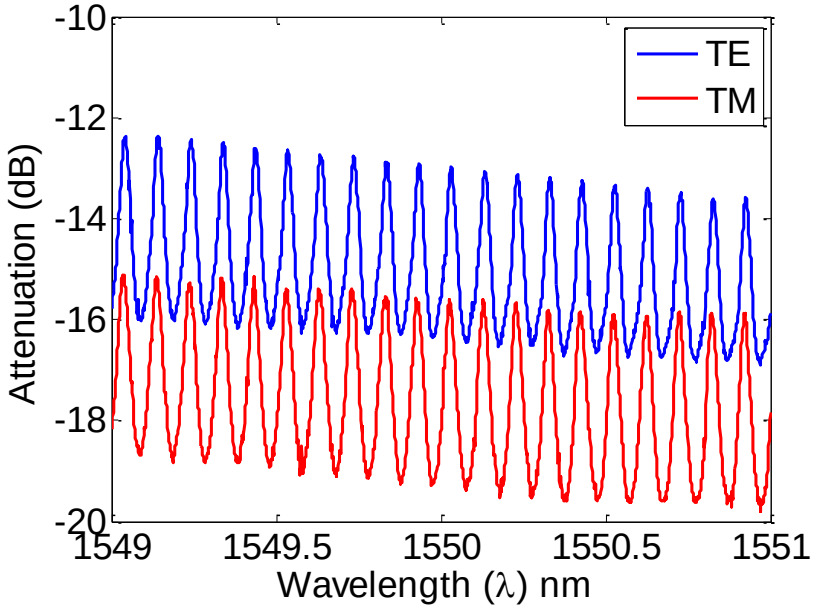


Figure 5-5: Total Attenuation of passive waveguide for TE- and TM- mode

Next we proceeded to evaluate the waveguide quality by calculating the waveguide loss for both TE and TM modes. For this we assumed the reflection at the facets to be 30%, this can be verified by using the formula given in equation 5.1. During coupling the end faces of the fiber were considered to be perpendicular with the waveguide. Moreover by visual observation using an optical microscope we deduced that the end faces of the waveguide were good and sharp, thus we consider scattering losses to be negligible. The reflectance is thus measured by eq. 5.1 given below:

$$R = \left(\frac{n_0 - n_{eff}}{n_0 + n_{eff}}\right)^2 \quad (5.1)$$

Here, $'n_0'$ and n_{eff} are the refractive indices of adjacent medium and the waveguide mode.

Using the value of 'R' in the equation 5.2 we can calculate the total waveguide loss for both the modes. We have in Fig.5-5 plotted the difference of output power and input power over a wavelength range from 1549nm to 1551nm. This sweep helps us evaluating the P_{max} and P_{min} values for both TE & TM modes. Substituting these values in eq.5.2 gives us the required parameters.

$$\alpha L = ln\left(R\frac{1+\sqrt{\frac{P_{min}}{P_{max}}}}{1-\sqrt{\frac{P_{min}}{P_{max}}}}\right) \qquad (5.2)$$

Here, 'α' is the attenuation, 'L' is the length of the device, 'R' is the reflection, P_{min} & P_{max} is the minimum and maximum ratio of the transmitted power.

The length of the passive waveguide was measured to be 3308μm .Thus calculating using eq.5.2 we obtain $\alpha_{TE} = 3.8965 dB/cm$ and the Total waveguide loss for TE mode $(\alpha_{TE}L) = 1.288\ dB$. Similarly for the TM mode the attenuation was calculated to be $\alpha_{TM} = 4.4767\ dB/cm$ and the total waveguide loss for TM mode to be $(\alpha_{TM}L) = 1.4809 dB$

5.3 Measurement Results and Discussion

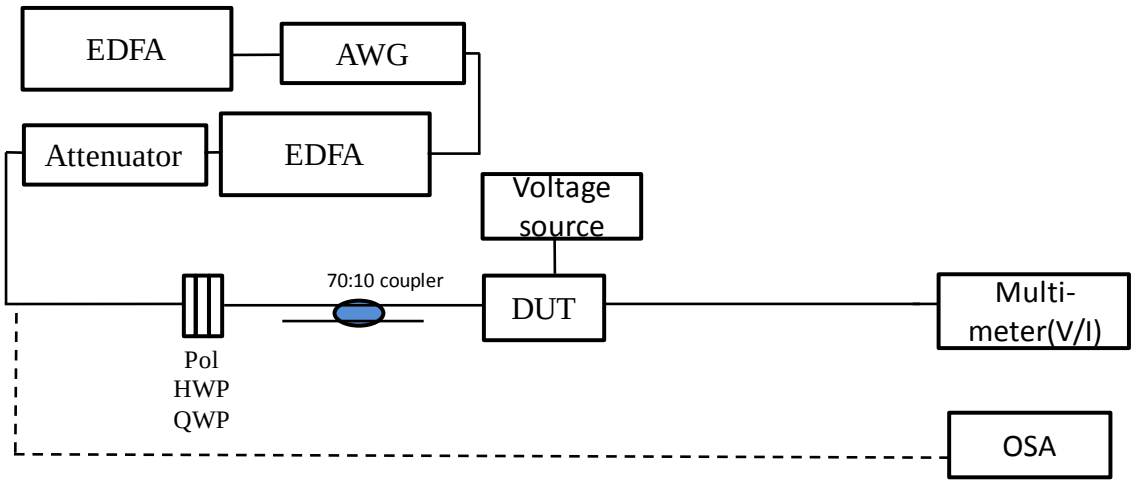


Figure 5-6: Optical Measurement Setup for Device Characterization

In Fig.5-6 shows the setup for measuring the PC-Integrated OQW PD characteristics. In this we use a use a Light source with two Arrayed Wave Guides (AWG) in series with emission wavelength at 1557nm. The wavelength was chosen to be longer than the wave guide attenuation measurement as longer wavelengths showed better extinction ratio. This light is then sent through an attenuator to obtain a pre-determined input; this is then sent through a polarizer consisting a polarizing plate. Half wave plate and a Quarter wave plate. At the output of the this optical setup we obtain either a TE- or TM-mode of light depending on the adjustment of the wave plates. This input light mode is then sent to a 70:10 light coupler. Thus 70% input light is coupled to the core layer of

device under test (DUT) whereas the rest of the light is sent to the Photodetector measuring equipment. The light is coupled with some losses (insertion/facet loss) into the DUT.

At the Electrodes of the DUT we collect the current generated in the OQW by aligning the output optical fiber to the Core layer of the DUT passive waveguide. As can be seen from the magnitude of current is higher for the TE- mode as compared to the TM-Mode; this is in agreement to the theory as TE mode is more confined to the core than TM-mode due to the Maxwell's equation and the boundary conditions applicable to this structure.

The input signal spectrum applied to the device is shown in Fig.5-7. We Measured the Measured Output Current for different length PCs at 300μW input optical power as shown in Fig.5-8.

In this we measured the current in OQW-PD while varying the angle of half-wave plate and keeping the quarter wave plate angle constant. Thus we were varying the input mode of light from TE mode to TM mode. We varied the HWP angle from 0° through 360° for the different combination of PC lengths. Thus we coupled light individually to all the PCs and tried to make the condition for measurement as similar over all the different PC-PD combinations.

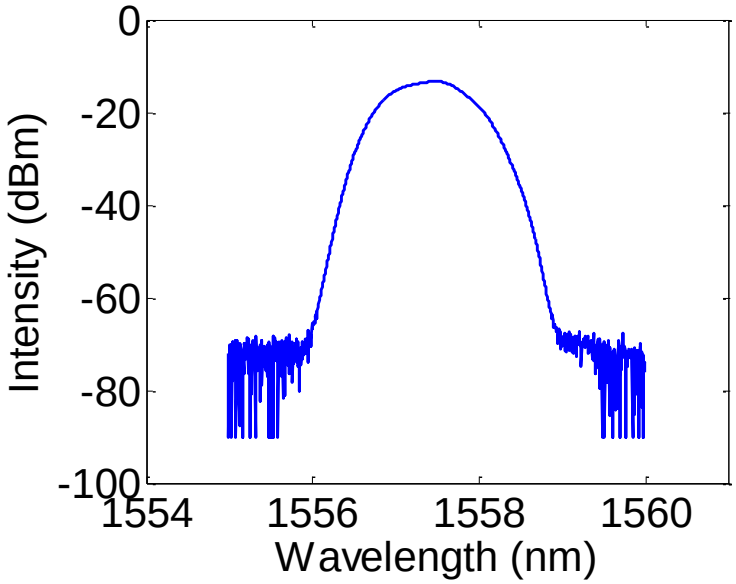


Figure 5-7: Input Signal Spectrum for optical characterization of PC and PD for polarization dependence measurements

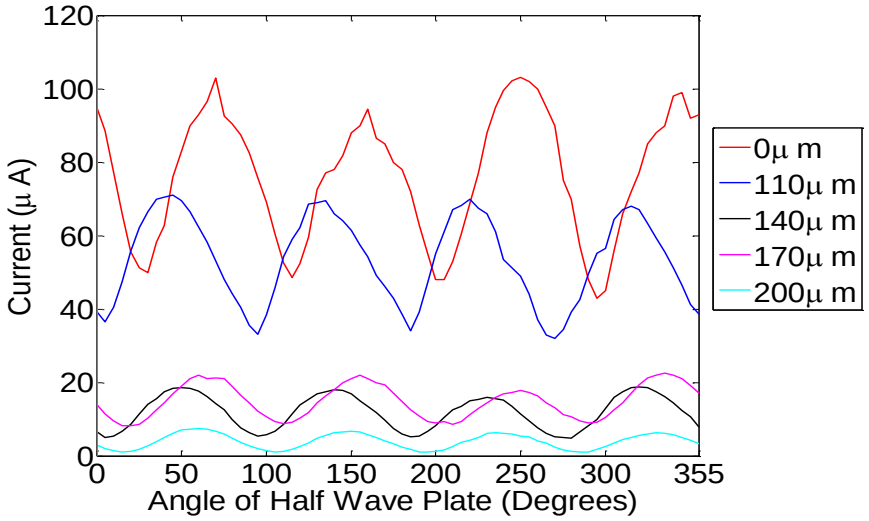


Figure 5-8: Measured Output Current for different length PCs at 300μW input optical power.

It can be observed from Fig.5-8 that there is a gradual phase shift between the condition for no polarization converter and a PD with converter length of 110μm. A gradual phase shift can also be observed for PC length 140/170/200μm. It can be observed that the current magnitude suddenly drops for longer PC lengths; this is expected as a longer PC length will induce higher losses in the mode of propagating light. Hence longer the PC length more the losses and lower the amount of current obtained at the PD. It can be safely said that the polarization rotation is not efficient in the integrated device.

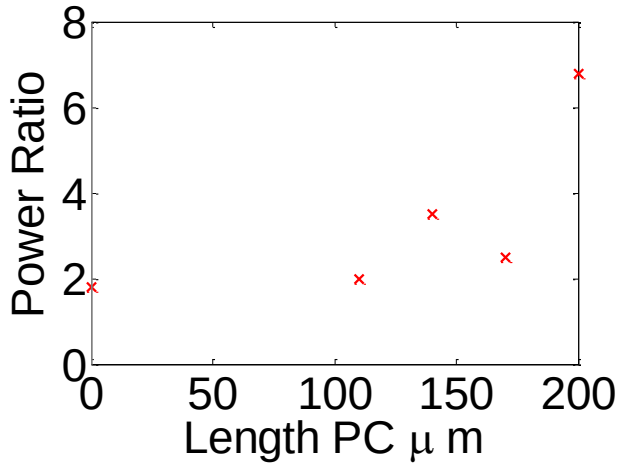


Figure 5-9: Power Ratio (I_{TE}/I_{TM}) measured for different PC lengths

Next we tried to deduce the power ratio for different length PCs. In this we took the ratio of current at PD from TE and TM modes at a similar power input for different length PCs. We can observe using this plot that the PC with length 170μm is not working satisfactorily. This can be due to fabrication processing issues and not due to design. For the rest of PCs the trend is visible.

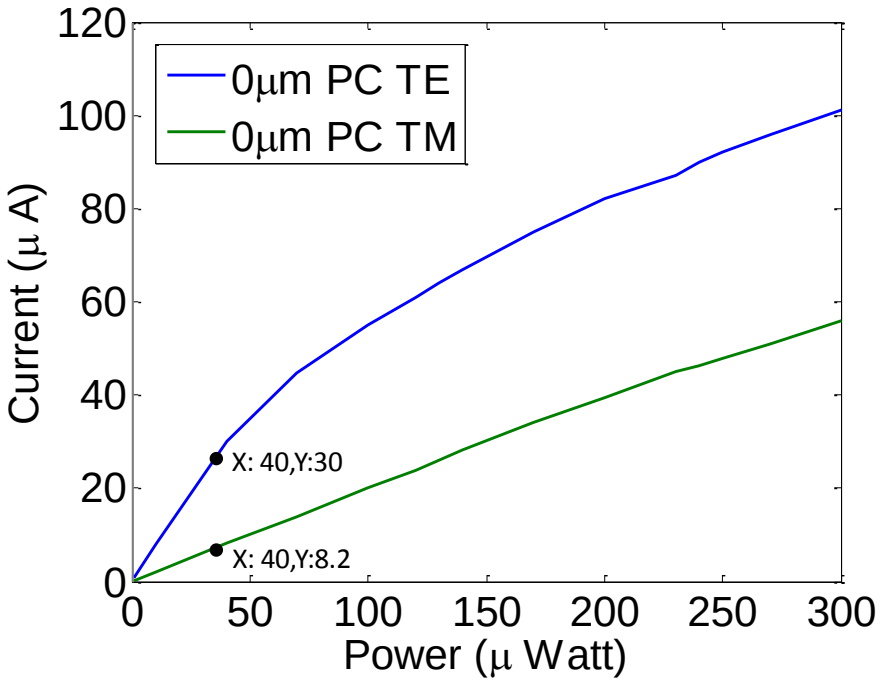


Figure 5-10: EQE measured for PD at varying Input Powers

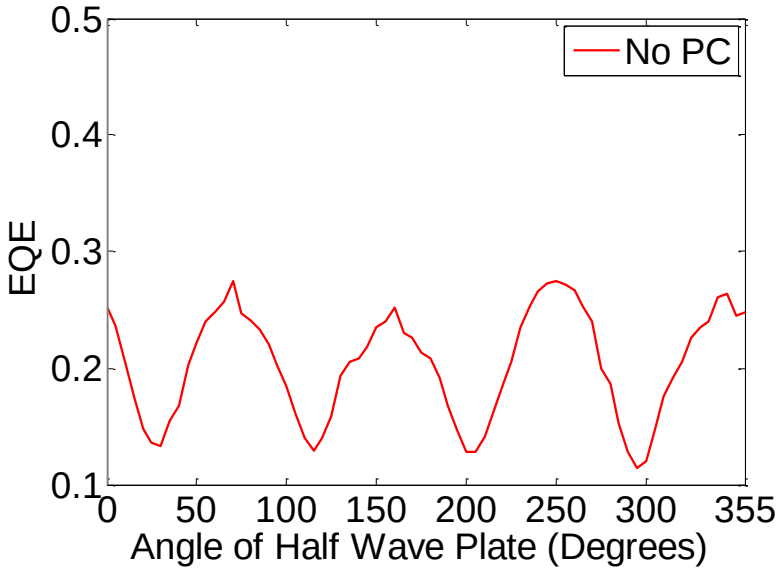


Figure 5-11: EQE measured for varying polarization at 300μW input optical power

To evaluate the performance of the Photodetector we evaluated the external quantum efficiency (EQE) at the location where the PC was absent. The EQE is the ratio of charge carriers successfully collected by the PD to the number of photons incident on the PD. It must also be noted that the wavelength of incident light was 1557nm and thus the energy of one photon was 0.7963eV. We were able to observe the polarization dependence of EQE as shown in Fig.5-11. It should be noted that the EQE is lower for a higher optical input power of 300μW due to saturation and losses in the PD. The EQE is given by the equation 5.3 as follows:

$$EQE = \frac{\text{number of charge carriers generate per second}}{\text{number of photons incident per second}} \qquad (5.3)$$

Form Fig.5-10 the EQE for TE mode was calculated to be 0.60 and for TM mode it was 0.164. Whereas at a higher power input the EQE values for TE- and TM mode where considerably lower due to saturation. Hence we can consider the EQE_{TE}=0.60 and EQE_{TM}=0.164. It was also observed that the effect of input power was prominent on the EQE measured for the TE-mode as compared to TM-mode. A higher EQE is possible to achieved using heterostructure photodiodes as we can make use of transparency of junction to minimize absorption outside the depletion region.

Next we calculated the responsivity of the detector as the photocurrent generated I_o is directly proportional to the incident optical power P_{in} . This proportionality constant is known as responsivity of the Photodetector. The Responsivity is given by the eq.5.4 as follows:

$$R = \frac{\eta\lambda}{h\nu} = \frac{\eta\lambda}{1.24} \qquad (5.4)$$

We consider the quantum efficiency of our device to be its EQE, also the wavelength of incident light is 1.557μm. Using the eq.5.4 we calculated the Responsivity of our Photodetector to be R=0.7533 Ampere/Watt.

Next we tried to measure the current for different power inputs for both the TE and TM mode of light input. The measured data can be observed in Fig. 5-12 and Fig.5-13. The later includes data from 110μm PC integrated with PD. It is expected that the magnitude of TE would decrease and TM would increase for an equal amount of input optical power for a longer PC. This theoretical deduction could be observed in our experimental characterization as shown in Fig.5-12. The distance between TE and TM mode currents decreased progressively with longer PC lengths in Fig.5-12. Even though the condition for measurement was same a similar trend could not be observed with the PC with length 110μm as seen in Fig.5-13.

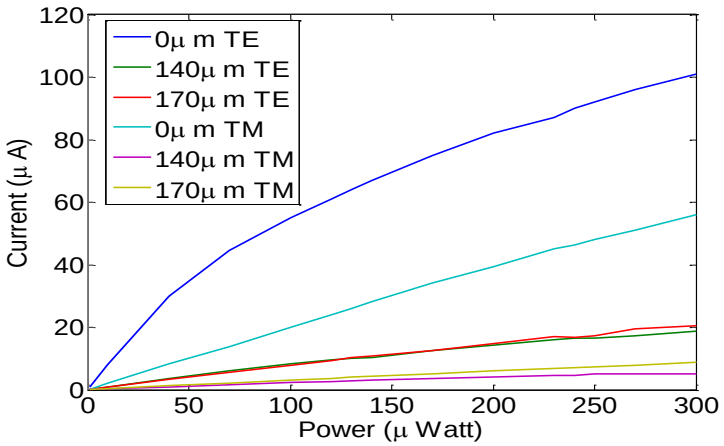


Figure 5-12: Measured output current for different length PCs at a given power for both the optical modes.

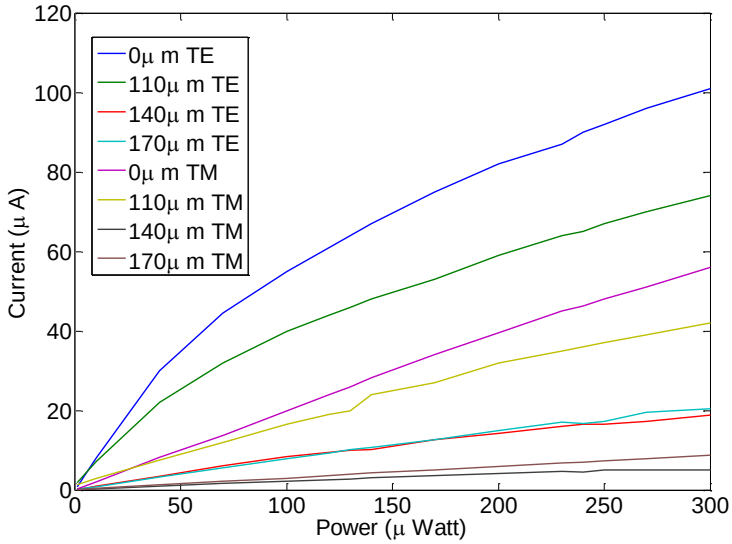


Figure 5-13: Measured output current for different length PCs at a given power for both the optical modes.

5.5 Summary

We have successfully characterized the PC-integrated OQW-PD. The quality of fabrication and operation for passive waveguide and also the active waveguide Photodetector was observed to be good. Some of the PCs were found to be inefficient and not working properly and would require improvement for future fabrication process. Finally an optical microscope image and a SEM image of a similar device used for characterization is shown in Fig.5-14 and Fig.5-15 respectively.

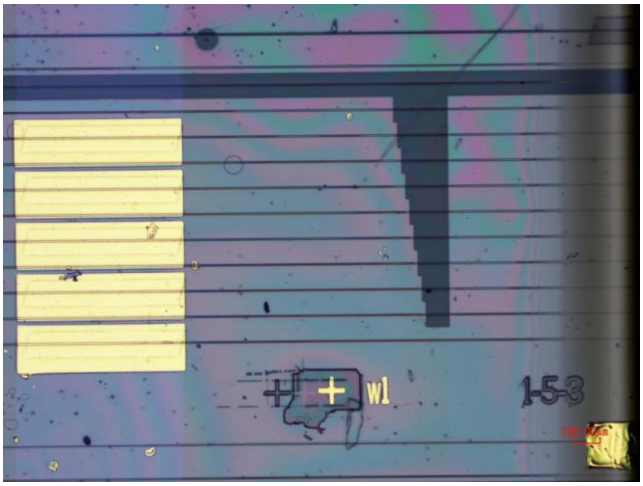


Figure 5-14: Optical Microscope image of the final device.

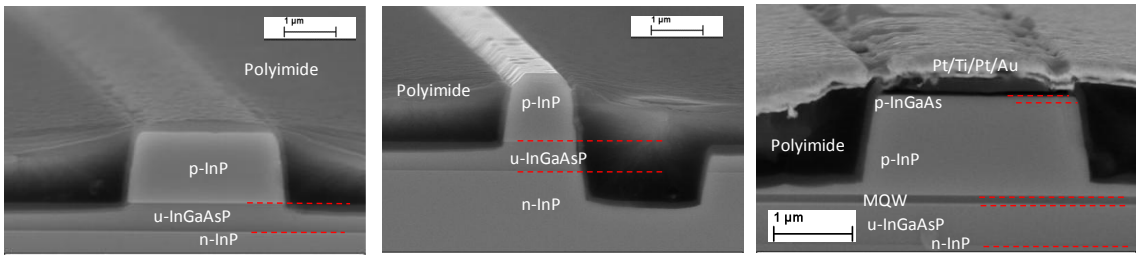


Figure 5-15: SEM images of cross sections of (a) passive (b) PC and (c) active parts of the final monolithic device

Chapter 6

Conclusion

In this thesis we presented the work of fabricating and characterizing a Polarization Converter integrated with a MQW Photodetector which is one of the advanced photonic integrated circuit. This added functionality of polarization manipulation and detection will hopefully provide a platform for reducing the footprint and increasing the functionality of a PIC. There is still a lot of scope for improving the work which can be carried out in the future.

In chapter 1 we discussed the background of this work along with the motivation for this research. Next in Chapter 2 we looked into the basic theory of light propagation in continuous and birefringent media. In chapter 3 we discussed the operating principle of the integrated device and looked into each individual component. Further more in chapter 4 we discussed in detail the fabrication procedure. An effort was made to describe in details each process involved and its dynamics.

In addition, the characterization of the device in chapter 5 displayed potential for extending the work for utilizing it as a receiver for utilizing SOP as a modulation format. This is an encouraging development as we could eliminate the need for coherent reception and employ the direct detection method in optical communication. These advanced modulation formats are the future of optical fiber communication.

In conclusion, we employed a promising simple and self-aligned fabrication process to integrated half-ridge PC and an MQW PD on an InP substrate and were successful in characterizing the device. For future work we would try to extend the work to design and fabricate a polarization analyzer monolithically integrated on a PIC. Further study on the possible compatibility with standard ridge waveguide components for future integration with other active and passive components to obtain large-scale Photonic integrated circuits with on-chip polarization manipulation is needed.

List of publication

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Appendix

Equipment used in the experiment

Electron Beam Lithography: Raith eLINE Plus
Spin coater: 1. MIKASA 1H-D7
2. MIKASA Opticoat MS-A100

Dry etcher: 1. PlasmaPro100 Cobra
2. ANELVA L-201D

Photolithography: Karl SussMicroTec MJB3

Electon Beam Evaporator: ULVAC UEP-2000
Sputter（SiO2）: ULVAC MNS-2000RF

Reference

[1] A. Chralyvy, “Plenary paper: The coming capacity crunch,” *2009 35th Eur. Conf. Opt. Commun.*, p. 8007, 2009.

[2] R. W. Tkach, “Scaling Optical Communications for the next decade and beyond,” *Bell Labs Tech. J.*, vol. 18, no. 4, pp. 3–17, 2010.

[3] a. D. Ellis, F. C. G. Gunning, B. Cuenot, T. C. Healy, and E. Pincemin, “Towards 1TbE using Coherent WDM,” *2008 Jt. Conf. Opto-Electronics Commun. Conf. Aust. Conf. Opt. Fibre Technol. OECC/ACOFT 2008*, 2008.

[4] P. J. Winzer, “High-Spectral-Ef fi ciency Optical Modulation Formats,” vol. 30, no. 24, pp. 3824–3835, 2012.

[5] K. Kikuchi, “Digital coherent optical communication systems: Fundamentals and future prospects,” *IEICE Electron. Express*, vol. 8, no. 20, pp. 1642–1662, 2011.

[6] P. Winzer, “Beyond 100G ethernet,” *IEEE Commun. Mag.*, vol. 48, no. 7, pp. 26–30, 2010.

[7] H. Sun, K.-T. Wu, and K. Roberts, “Real-time measurements of a 40 Gb/s coherent system.,” *Opt. Express*, vol. 16, no. 2, pp. 873–879, 2008.

[8] P. Evans, M. Fisher, R. Malendevich, a. James, G. Goldfarb, T. Vallaitis, M. Kato, P. Samra, S. Corzine, E. Strzelecka, P. Studenkov, R. Salvatore, F. Sedgwick, M. Kuntz, V. Lal, D. Lambert, a. Dentai, D. Pavinski, J. Zhang, J. Cornelius, T. Tsai, B. Behnia, J. Bostak, V. Dominic, a. Nilsson, B. Taylor, J. Rahn, S. Sanders, H. Sun, K.-T. Wu, J. Pleumeekers, R. Muthiah, M. Missey, R. Schneider, J. Stewart, M. Reffle, T. Butrie, R. Nagarajan, M. Ziari, F. Kish, and D. Welch, “112 Tb/s superchannel coherent PM-QPSK InP transmitter photonic integrated circuit (PIC),” *Opt. Express*, vol. 19, no. 26, p. B154, 2011.

[9] R. Nagarajan and M. Smit, “Photonic Integration,” *IEEE LEOS Newsl.*, no. June 2007, pp. 4–10, 2007.

[10] T. H. Maiman, “Stimulated Optical Radiation in Ruby,” *Nature*, vol. 187, no. 4736, pp. 493–494, 1960.

[11] S. E. Miller, “Integrated optics: An Introduction,” *bell Syst. Tech. J.*, vol. 48, pp. 2059–2069, 1969.

[12] M. Smit, X. Leijtens, H. Ambrosius, E. Bente, J. van der Tol, B. Smalbrugge, T. de Vries, E.-J. Geluk, J. Bolk, R. van Veldhoven, L. Augustin, P. Thijs, D. D’Agostino, H. Rabbani, K. Lawniczuk, S. Stopinski, S. Tahvili, A. Corradi, E. Kleijn, D. Dzibrou, M. Felicetti, E. Bitincka, V. Moskalenko, J. Zhao, R. Santos, G. Gilardi, W. Yao, K. Williams, P. Stabile, P. Kuindersma, J. Pello, S. Bhat, Y. Jiao, D. Heiss, G. Roelkens, M. Wale, P. Firth, F. Soares, N. Grote, M. Schell, H. Debregeas, M. Achouche, J.-L. Gentner, A. Bakker, T. Korthorst, D. Gallagher, A. Dabbs, A. Melloni, F. Morichetti, D. Melati, A. Wonfor, R. Penty, R. Broeke, B. Musk, and D. Robbins, “An introduction to InP-based generic integration technology,” *Semicond. Sci. Technol.*, vol. 29, no. 8, p. 083001, 2014.

[13] R. a. Soref, “Silicon-based optoelectronics,” *Proc. IEEE*, vol. 81, no. 12, pp. 1687–1706, 1993.

[14] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, “Micrometre-scale silicon electro-optic modulator.,” *Nature*, vol. 435, no. 7040, pp. 325–327, 2005.

[15] F. Xia, L. Sekaric, and Y. Vlasov, “Ultracompact optical buffers on a silicon chip,” *Nat. Photonics*, vol. 1, no. 1, pp. 65–71, 2007.

[16] D. Ahn, C.-Y. Hong, J. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kärtner, “High performance, waveguide integrated Ge photodetectors.,” *Opt. Express*, vol. 15, no. 7, pp. 3916–3921, 2007.

[17] L. Chen, C. R. Doerr, and Y.-K. Chen, “Compact polarization rotator on silicon for polarization-diversified circuits.,” *Opt. Lett.*, vol. 36, no. 4, pp. 469–471, 2011.

[18] D. Vermeulen, S. Selvaraja, P. Verheyen, P. Absil, W. Bogaerts, D. Van Thourhout, and G. Roelkens, “Silicon-on-insulator polarization rotator based on a symmetry breaking silicon overlay,” *IEEE Photonics Technol. Lett.*, vol. 24, no. 6, pp. 482–484, 2012.

[19] A. V. Velasco, M. L. Calvo, P. Cheben, A. Ortega-Moñux, J. H. Schmid, C. A. Ramos, Í. M. Fernandez, J. Lapointe, M. Vachon, S. Janz, and D.-X. Xu, “Ultracompact polarization converter with a dual subwavelength trench built in a silicon-on-insulator waveguide,” *Opt. Lett.*, vol. 37, no. 3, p. 365, 2012.

[20] J. Zhang, M. Yu, G. Lo, and D.-L. Kwong, “Silicon waveguide-based mode-evolution polarization rotator,” *Proc. SPIE*, vol. 7719, no. 65, p. 77190C–77190C–8, 2010.

[21] J. J. G. M. van der Tol, J. W. Pedersen, E. G. Metaal, F. Hakimzadeh, Y. S. Oei, F. H. Groen, and I. Moerman, “Realization of a short integrated optic passive polarization converter,” *IEEE Photonics Technol. Lett.*, vol. 7, no. 8, pp. 893–895, 1995.

[22] Y. Shani, R. Alferness, T. Koch, U. Koren, M. Oron, B. I. Miller, and M. G. Young, “Polarization rotation in asymmetric periodic loaded rib waveguides,” *Appl. Phys. Lett.*, vol. 59, no. 11, pp. 1278–1280, 1991.

[23] L. H. Spiekman and M. K. Smit, “Dam, L. H. Spiekman, F. P. G. M.,” vol. 8, no. 10, pp. 8–10, 1996.

[24] U. Khalique, Y. C. Zhu, J. J. G. M. van der Tol, L. M. Augustin, R. Hanfoug, F. H. Groen, P. J. van Veldhoven, M. K. Smit, M. van de Moosdijk, W. de Laat, and K. Simon, “Ultrashort Polarization Converter on InP/InGaAsP Fabricated by Optical Lithography,” *Integr. Photonics Res. Appl. Top. Meet.*, no. APRIL, pp. 1–3, 2005.

[25] M. Kotlyar, L. Bolla, M. Midrio, L. O’Faolain, and T. Krauss, “Compact polarization converter in InP-based material.,” *Opt. Express*, vol. 13, no. 13, pp. 5040–5045, 2005.

[26] M. R. Watts, H. A. Haus, and E. P. Ippen, “Integrated mode-evolution-based polarization splitter,” vol. 30, no. 9, pp. 967–969, 2005.

[27] L. B. Soldano, a. H. de Vreede, M. K. Smit, B. H. Verbeek, E. G. Metaal, and F. H. Groen, “Mach-Zehnder interferometer polarization splitter in InGaAsP/InP,” *IEEE Photonics Technol. Lett.*, vol. 6, no. 3, pp. 402–405, 1994.

[28] L. M. Augustin, J. J. G. M. van der Tol, R. Hanfoug, W. J. M. de Laat, M. J. E. van de Moosdijk, P. W. L. van Dijk, Y. S. Oei, and M. K. Smit, “A single etch-step fabrication-tolerant polarization splitter,” *J. Light. Technol.*, vol. 25, no. 3, pp. 740–746, 2007.

[29] M. I. Hayee, M. C. Cardakli, a. B. Sahin, and a. E. Willner, “Doubling of bandwidth utilization using two orthogonal polarizations and power unbalancing in a polarization-division-multiplexing scheme,” *IEEE Photonics Technol. Lett.*, vol. 13, no. 8, pp. 881–883, 2001.

[30] A. H. Gnauck, P. J. Winzer, S. Chandrasekhar, X. Liu, B. Zhu, and D. W. Peckham, "10 x 224-Gb/s WDM transmission of 28-Gbaud PDM 16-QAM on a 50-GHz grid over 1,200 km of fiber," *Opt. Fiber Commun. (OFC), collocated Natl. Fiber Opt. Eng. Conf. 2010 Conf.*, pp. 26–28, 2010.

[31] C. R. Doerr, P. J. Winzer, S. Chandrasekhar, M. Rasras, M. Earnshaw, J. Weiner, D. M. Gill, and Y. K. Chen, "Monolithic silicon coherent receiver," *2009 Conf. Opt. Fiber Commun. - incudes post deadline Pap.*, pp. 14–16, 2009.

[32] P. Dong, C. Xie, L. Chen, L. L. Buhl, and Y.-K. Chen, "112-Gb/s monolithic PDM-QPSK modulator in silicon.," *Opt. Express*, vol. 20, no. 26, pp. B624–9, 2012.

[33] P. Evans, M. Fisher, R. Malendevich, a. James, P. Studenkov, G. Goldfarb, T. Vallaitis, M. Kato, P. Samra, S. Corzine, E. Strzelecka, R. Salvatore, F. Sedgwick, M. Kuntz, V. Lal, D. Lambert, a. Dentai, D. Pavinski, J. Zhang, B. Behnia, J. Bostak, V. Dominic, a. Nilsson, B. Taylor, J. Rahn, S. Sanders, H. Sun, K.-T. Wu, J. Pleumeekers, R. Muthiah, M. Missey, R. Schneider, J. Stewart, M. Reffle, T. Butrie, R. Nagarajan, C. Joyner, M. Ziari, F. Kish, and D. Welch, "Multi-channel coherent PM-QPSK InP transmitter photonic integrated circuit (PIC) operating at 112 Gb/s per wavelength," *2011 Opt. Fiber Commun. Conf. Expo. Natl. Fiber Opt. Eng. Conf.*, pp. 1–3, 2011.

[34] R. Nagarajan, M. Kato, D. Lambert, P. Evans, S. Corzine, V. Lal, J. Rahn, A. Nilsson, M. Fisher, M. Kuntz, J. Pleumeekers, A. Dentai, H.-S. Tsai, D. Krause, H. Sun, K.-T. Wu, M. Ziari, T. Butrie, M. Reffle, M. Mitchell, F. Kish, and D. Welch, "Terabit/s class InP photonic integrated circuits," *Semicond. Sci. Technol.*, vol. 27, no. 9, p. 094003, 2012.

[35] D. Krause, H. Sun, S. Thomson, Y. Wu, K.-T. Wu, R. Malendevich, J. T. Rahn, M. Fisher, M. Kato, D. Lambert, V. Lal, R. Nagarajan, P. Evans, A. James, S. Corzine, M. Ziari, S. Yu, P. Freeman, A. Nilsson, M. Mitchell, F. Kish, and D. Welch, "854 Gb/s Superchannel InP Transmitter and Receiver Photonic Integrated Circuits utilizing Real-Time Detection of PM-8QAM - OSA Technical Digest," *Opt. Fiber Commun. Conf.*, p. OTu1G.1, 2012.

[36] B. E. A. S. Malvin Carl Teich, *Fundamentals of Photonics*, Second Edi. Wiley Series in Pure and Applied Optics, 2007.

[37] K. Kikuchi and S. Kawakami, "Multi-level signaling in the Stokes space and its application to large-capacity optical communications," *Opt. Express*, vol. 22, no. 7, pp. 7374–7387, 2014.

[38] P. Lemaître-Auger, K. Djerroud, P. Benech, and P. Benech, “Novel integrated polarization analyzer sensor made by ion-exchange in glass,” vol. 6123, p. 61230E–61230E–9, 2006.

[39] Y. Kawabata, M. Zaitsu, T. Tanemura, and Y. Nakano, “Proposal and Experimental Demonstration of Monolithic InP / InGaAsP Polarization Modulator,” vol. 2, pp. 4–6, 2014.

[40] M. Zaitsu, T. Tanemura, A. Higo, and Y. Nakano, “Self-Aligned InP/InGaAsP Polarization Converter for Polarization-Multiplexed Photonic Integrated Circuits,” *Opt. Fiber Commun. Conf. Fiber Opt. Eng. Conf. 2013*, p. OTh4I.3, 2013.

[41] P. Yeh, “Electromagnetic propagation in birefringent layered media,” *J. Opt. Soc. Am.*, vol. 69, no. 5, p. 742, 1979.

[42] T. Tanemura, T. Amemiya, K. Takeda, a. Higo, and Y. Nakano, “Simple and compact InP polarization converter for polarization-multiplexed photonic integrated circuits,” *Conf. Proc. - Lasers Electro-Optics Soc. Annu. Meet.*, vol. 2, pp. 436–437, 2009.

[43] L. M. Augustin, S. Member, J. J. G. M. Van Der Tol, E. J. Geluk, and M. K. Smit, “Short Polarization Converter Optimized for Active – Passive Integration in InGaAsP – InP,” *Ieee Photonics Technol. Lett.*, vol. 19, no. 20, pp. 1673–1675, 2007.

[44] J. S. W. and D. S. C. David A.B, Miller, “electric-field dependence of Linear optical properties in quantum well structures,” *IEEE J. Quantum Electron.*, vol. 9, p. 1816, 1986.

[45] E. Yablonovitch and E. Kane, “Reduction of lasing threshold current density by the lowering of valence band effective mass,” *J. Light. Technol.*, vol. 4, no. 5, pp. 504–506, 1986.

[46] A. R. Adams, “Band-structure engineering for low-threshold high-efficiency semiconductor lasers,” *Electron. Lett.*, vol. 22, no. 5, p. 249, 1986.

[47] S. Charbonneau, E. S. Koteles, P. J. Poole, J. J. He, G. C. Aers, J. Haysom, M. Buchanan, Y. Feng, a. Delage, F. Yang, M. Davies, R. D. Goldberg, P. G. Piva, and I. V. Mitchell, “Photonic integrated circuits fabricated using ion implantation,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 4, no. 4, pp. 772–793, 1998.

[48] J. W. Raring, M. N. Sysak, A. Tauke-Pedretti, M. Dummer, E. J. Skogen, J. S. Barton, S. P. DenBaars, and L. a. Coldren, “Advanced Integration Schemes for

High-Functionality/High-Performance Photonic Integrated Circuits," *Proc. SPIE 6126, Photonics Packag. Integr. VI*, vol. 6126, p. 61260H–61260H–20, 2006.

[49] D. J. B. Larry A.Coldren, Matthew N.Sysak, James W.Raring, "a single regrowth integration platform for photonic circuits incorporating tunable sgdbr lasers and quantum well eams," 2006.

[50] J. E. Greenspan, C. Blaauw, B. Emmerstorfer, R. W. Glew, and I. Shih, "Analysis of a time-dependent supply mechanism in selective area growth by MOCVD," *J. Cryst. Growth*, vol. 248, no. SUPPL., pp. 405–410, 2003.

[51] J. Darja, M. J. Chan, M. Sugiyama, and Y. Nakano, "Four channel DFB laser array with integrated combiner for 1.55 μm CWDM systems by MOVPE selective area growth," *IEICE Electron. Express*, vol. 3, no. 24, pp. 522–528, 2006.

[52] I. Moerman, P. P. Van Daele, and P. M. Demeester, "A review on fabrication technologies for the monolithic integration of tapers with III-V semiconductor devices," *IEEE J. Sel. Top. Quantum Electron.*, vol. 3, no. 6, pp. 1308–1320, 1997.

[53] T. Kitatani, K. Shinoda, T. Tsuchiya, H. Sato, K. Ouchi, H. Uchiyama, S. Tsuji, and M. Aoki, "Evaluation of the optical-coupling efficiency of InGaAlAs-InGaAsP butt joint using a novel multiple butt-jointed laser," *IEEE Photonics Technol. Lett.*, vol. 17, no. 6, pp. 1148–1150, 2005.

[54] Y. Barbarin, E. a J. M. Bente, C. Marquet, E. J. S. Leclère, J. J. M. Binsma, and M. K. Smit, "Measurement of reflectivity of butt-joint active-passive interfaces in integrated extended cavity lasers," *IEEE Photonics Technol. Lett.*, vol. 17, no. 11, pp. 2265–2267, 2005.

[55] J. H. Song, J. W. Park, E. D. Sim, and Y. Baek, "Measurements of coupling and reflection characteristics of butt-joints in passive waveguide integrated laser diodes," *IEEE Photonics Technol. Lett.*, vol. 17, no. 9, pp. 1791–1793, 2005.

[56] P. J. Harmsma, H. Vonk, M. R. Leys, and Y. S. Oei, "Effect pf butt joint reflections on the performance of Extended Cavity Lasers and Phassed Array Multi-Wavelength Lasers," *Proc. IEEE/LEOS Benelux Chapter*, pp. 5–8, 2000.

[57] E. J. Skogen, J. W. Raring, G. B. Morrison, C. S. Wang, V. Lai, M. L. Mašanović, and L. a. Coldren, "Monolithically integrated active components: A quantum-well intermixing approach," *IEEE J. Sel. Top. Quantum Electron.*, vol. 11, no. 2, pp. 343–355, 2005.

[58] E. J. Skogen, J. S. BARTON, S. P. DENBAARS, and L. A. COLDREN, “A quantum-well-intermixing process for wavelength-agile photonic integrated circuits,” *IEEE J. Sel. Top. quantum Electron.*, vol. 8, no. 4, pp. 863–869.

[59] V. I. Tolstikhin, C. D. Watson, K. Pimenov, R. Moore, Y. Logvin, and F. Wu, “Laterally coupled DFB lasers for one-step growth photonic integrated circuits in InP,” *IEEE Photonics Technol. Lett.*, vol. 21, no. 10, pp. 621–623, 2009.

[60] H. Lianping, Z. Hongliang, K. Qiang, D. Ying, W. Baojun, Z. Fan, and W. Wei, “1.55μm ridge DFB laser and electroabsorption modulator integrated with buried-ridge-stripe dual-waveguide spot-size converter output,” *IEEE Photonics Technol. Lett.*, vol. 18, no. 1, pp. 235–237, 2006.

[61] J. E. Johnson, L. J. P. Ketelsen, S. K. Sputz, J. Vandenberg, M. W. Focht, D. V. Stampone, L. J. Peticolas, L. E. Smith, K. G. Glogovsky, G. J. Przybylek, S. N. G. Chu, L. C. Luther, T. L. Pernell, F. S. Walters, D. M. Romero, J. M. Freund, C. L. Reynolds, R. People, M. a. Alam, J. a. Grenko, J. L. Lentz, N. N. Tzafaras, and L. a. Gruezke, “Monolithically integrated semiconductor optical amplifier and electroabsorption modulator with dual-waveguide spot-size converter input,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 6, no. 1, pp. 19–25, 2000.

[62] V. I. Tolstikhin, R. Moore, K. Pimenov, Y. Logvin, F. Wu, and C. D. Watson, “One-step growth optical transceiver PIC in InP,” *2009 35th Eur. Conf. Opt. Commun.*, pp. 5–6, 2009.

[63] B. I. M. T.L.Koch, U.Koren, “High performance tunable 1.5um InGaAs/InGaAsP multiple qunatum well distributed bragg reflector lasers,” *IEEE*, 1988.

[64] K. O. Hiroaki Takeuchi, Kazuo Kasaya, “Experimental Evaluation of the Coupling Efficiency between Monolithically Integrated DFB Lasers and Waveguides,” in *IEICE*, 1990, p. 53.

[65] M. L. Mašanović, V. Lal, E. J. Skogen, J. S. Barton, J. a. Summers, J. a. Raring, L. a. Coldren, and D. J. Blumenthal, “Cross-phase modulation efficiency in offset quantum-well and centered quantum-well semiconductor optical amplifiers,” *IEEE Photonics Technol. Lett.*, vol. 17, no. 11, pp. 2364–2366, 2005.

[66] C. W. Gwyn, “Extreme ultraviolet lithography,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 16, no. 6, p. 3142, 1998.

[67] V. R. Manfrinato, L. Zhang, D. Su, H. Duan, R. G. Hobbs, E. a. Stach, and K. K. Berggren, "Resolution limits of electron-beam lithography toward the atomic scale," *Nano Lett.*, vol. 13, no. 4, pp. 1555–1558, 2013.

[68] G. Tittelbach, B. Richter, and W. Karthe, "Comparison of three transmission methods for integrated optical waveguide propagation loss measurement," *Pure Appl. Opt. J. Eur. Opt. Soc. Part A*, vol. 2, no. 6, pp. 683–700, 1999.

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