論文の内容の要旨

Study on Tunneling Field-Effect Transistors with Ge/Si Heterojunctions

(Ge／Si ヘテロ接合を用いた トンネルFETに関する研究)

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In this thesis, tunnel field-effect transistors using band-to-band tunneling are investigated as a prospective solution of low power applications. Device structures and fabrications processes are suggested to achieve the steep SS lower than 60 mV/dec which allow a supply voltage reducing.

Band-to-band tunneling probability and current are derived from quantum mechanical Zener tunneling model. From the derived tunneling current density equation, small effective mass and energy bandgap, high electric field are needed in order to obtain high tunneling probability.

Type-II staggered heterojunctions of Ge/Si can allow such conditions for high tunneling probability. Therefore, Ge and Si heterojunction TFETs with simple structure are proposed and demonstrated. To enhance the device performance, pure Ge-source and thin body SOI substrate are used. Low power phosphorus ion implantation is investigated for drain formation for thin body devices fabrication.

Optimized 3 keV acceleration energy with phosphorus ion dose of 5×10^{14} cm^{-2} is used.

Pure-Ge layer is successfully grown on drain-formed SOI substrate by extremely low temperature MBE.

To guarantee the interface between Ge and Al_2O_3 gate oxide, ECR oxygen plasma post oxidation is carried out. The uniform interface of Ge/Al_2O_3 is confirmed by TEM images.

The effect of doping concentration of Ge-source on device performances is investigated. Highly boron doped Ge/Si heterojunction device shows improved device performance than that without boron doping. Although S factor as high as 161 mV/dec, high on/off current ratio of 6-orders of magnitude with the low leakage current and good on current saturation are obtained.

The impact of the interface state density, which exist in both of Ge/Al_2O_3 and Si/Al_2O_3 interfaces, on device performances Ge/Si heterojunction TFETs are investigated.

The low D_{it} values in the Ge/Al_2O_3 interfaces are revealed by conductance method using nGe MIS capacitors. The D_{it} values in the Si/Al_2O_3 interfaces decrease as the PMA temperature increases, resulting in the improvement of on/off current ratio and SS of Ge/Si TFETs.

Fabricated TFET devices show high on/off current ratio over 6 orders of magnitude and steep SS below 60 mV/dec are obtained after PMA at 400 ^{o}C. Through the temperature dependence of I-V characteristics, it is confirmed that the tunneling current is the dominant currents in present devices.

Finally, it is revealed that D_{it} between Al_2O_3 and Si in the channel region of the

present Ge/Si TFETs is a critical factor to realize low SS and high on/off current ratio of the proposed TFET structure and, thus, the proper thermal treatment is important for the enhancement of electrical properties.

Channel strain engineering effects on TFET's performances are investigated using different strain values in Si channel.

Three kind of different biaxial tensile strain with 0, 0.8, 1.1 % are used and the strain values are confirmed by Raman spectra.

Thanks to advantages of $E_{g.eff}$ by strain engineered Ge/Si heterojunction, high on/off current raio with low leakage current and steep SS of 51 mV/dec are obtained.