博士論文（要約）

極低電圧 CMOS デジタル回路における遅延ばらつきの特性とモデリングに関する研究

A Study on Characterization and Modeling of Delay Variations in Extremely Low Voltage CMOS Digital Circuits

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Abstract

The market demand for ultra-low-power LSIs is likely to continue to expand at an increasing rate in the foreseeable future. In order to meet the demand, the establishment of a design methodology of extremely-low-voltage CMOS digital circuits, which operate at sub-threshold region, has been expected. Extremely low voltage operation has the advantage that 10-times energy efficiency improvement compared to standard voltage can be achieved. However, it has also some disadvantages that it is more vulnerable to the performance variation of transistors, and that power efficiency and operation speed are substantially spoiled due to an excessively large design overhead to compensate it.

In practice, the biggest problem which may hinder the stable operation of extremely low voltage CMOS digital circuits is the timing violations caused by the variations in the propagation delay time of the logic gates. The delay variation of logic gates is defined as the ratio of the standard deviation of delay to the mean value of that. When the supply voltage drops, the delay variation increases, then correspondingly more and more design effort to achieve timing closure is required.

Therefore, first of all, it is necessary to understand and model the essential character of the delay variation using several basic parameters of transistors. Next, by applying the derived simple delay variation model to further miniaturized CMOS technologies, it is very important to consider the difficulty level of lowering supply voltage.

Relaxing timing constraints is the most straightforward solution to extremely low voltage digital circuit design and it is important to reduce the clock skew. Since at low voltages wire resistance is relatively small in contrast to on resistance of buffer, it is effective to implement the clock tree with less or even none of buffer/repeater.

This thesis consists of 4 chapters in total. Chapter 1 describes the energy minimum operation voltage of sub-threshold logic circuit and parameters that determine its value.

Chapter 2 introduces simple yet approximate model for delay variation. The within-die delay variations of NAND/NOR logic gates in a 40nm CMOS process are measured in the test chip by changing supply voltage and temperature, and then it is confirmed that the proposed model approximately matches the measurement and SPICE simulation results. It has been known that the main cause of speed performance variations in sub-100nm devices is the variations in their threshold voltages, which have normal distributions. The standard deviation of threshold voltages is used as a parameter in the proposed delay variation model. Delay variations have almost no temperature characteristics at standard voltages, whereas they are almost inversely

proportional to absolute temperature at low voltages. This is the reason why extra care is necessary for design under low voltage and low temperature conditions. When delay variation at standard voltage is estimated quantitatively, an analysis of current sensitivity to threshold voltage shift on the trajectory of transistor operating point during switching reveals that I_{EFF} is more suitable for transistor current model rather than conventional I_{ON}. Delay variation at standard and low voltage can be also estimated simply and roughly by substituting several basic transistor parameters into the proposed model formulas. The ratio of delay variations at low voltage to that at standard voltage means how difficult the sub-threshold logic circuit design is, and it saturates at between 5 and 10. This fact shows that there is a positive perspective when considering further reduction of supply voltage.

Chapter 3 proposes a switching system of a duplex clock tree so that optimum performance of power and speed can be obtained with a very wide range of dynamic voltage scaling. The clock tree consists of the buffered and bufferless tree for standard and low voltage operation respectively, and the tri-state buffers arranged at each leaf node of the clock tree enable switching of them. The buffered and bufferless clock skews both at standard and low voltages are measured in the test chip, which incorporates a novel method for the measurement of clock skew and is fabricated in a 65nm CMOS process. Measurement results show that switching to the bufferless clock tree can eliminate clock skew by 18% at 0.3V. As a result, the merits are as follows: (1) efficiency of power and area is improved because hold time constraint is relaxed and hold buffers are reduced, and (2) the clock frequency is enhanced because setup time constraint is also relieved. An estimates of benefits of power, area, and delay at 0.3V, which is based on the general assumption shows that a significant performance improvement can be expected if the chip size is less than 2mm square. The area overhead of this architecture is about 2% of the chip area, which is negligibly small.

Finally, this thesis concludes in Chapter 4.