論文の内容の要旨

Thesis Summary

論文題目　A Template Reduction Algorithm Using Critical Boundary Vector and an Implementation to an On-Chip Learning VLSI
（主要境界ベクトルを用いたテンプレート削減アルゴリズムとオンチップ学習 VLSI への実装）

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（本文　Body）

1. Introduction

The nearest neighbor (NN) classifier is one of the most well known nonparametric classification algorithms for its simplicity of implementation. However, there exist problems of memory requirement, classification efficiency and low tolerance to noise for NN classifier. To solve these three problems simultaneously, this paper presents a hardware-friendly template reduction (TR) method for nearest neighbor (NN) classifiers by introducing critical boundary vectors as well as its hardware implementation for acceleration.

2. Overview of Learning Algorithms for Nearest Neighbor and Template Reduction

To solve the problems of nearest neighbor classifiers, a lot of learning algorithms have been proposed, such as distance metric learning and sample weighting to improve the classification accuracy of NN, and approximate nearest neighbor searching methods to improve the classification efficiency. However, in order to solve these three problems simultaneously, a template reduction (TR) learning method is greatly desired.

A lot of work has been done to address the issue of template reduction in nearest neighbor (NN) classifiers. Among existing TR methods, Random Mutation Hill Climbing (RMHC) method, and Hit Miss Network Edition Iterative (HMNEI), show superior classification

accuracy and also good reduction rate. However, the computation needs a time-consuming iterative process, and the time complexity is high (quadratic time for HMNEI, cubic time for RMHC). As a result, the learning speed of these methods can be problematic for applications having a strict constraint on power or latency.

3. Critical Boundary Vector Concept in Nearest Neighbor Classifiers using K-means Centers for Efficient Template Reduction

This chapter presents an efficient template reduction method for the nearest neighbor classifier using K-means centers, by introducing the concept of critical boundary vectors. Different from the complex SVM training, the pro-posed method is based on simple distance calculation that is more VLSI-hardware-implementation friendly. In addition, it is easily extendible to multi-class large-scale classification. To initially condense the sample set, only K-means centers are utilized as rough templates for classification, instead of using the entire sample set. Then, in order to enhance the classification performance, boundary vectors that are critical for better accuracy are selected according to a newly proposed training algorithm. In contrast to the complex SVM training or other condensing methods, only single iteration step is sufficient for selection. Experimental results show that the proposed algorithm has a comparable performance to regular NNs.

4. A Nearest Neighbor Classifier Introducing the Concept of Critical Boundary Vectors With an Enhanced Boundary by Global Character

A new template reduction method for NN classifiers that is applicable to a variety of classification problems, by introducing the concept of critical boundary vectors. The method takes the impact of each noisy boundary vector into account during template reduction, and after that automatically decides whether the vector should be removed from the template set or not according to the nature of the problem. A novel boundary vector selection algorithm with a global characterization scheme has been proposed to solve the issue of noisy boundary vectors, in order to improve the accuracy. Initially, K-means centers are utilized as the representation of the entire template set. Then, in order to enhance the classification performance, boundary vectors are selected by the newly proposed selection algorithm, which completes within only a single iteration. However, among the selected boundary vectors, there exist noisy boundary vectors that can mislead the classification in some problems. In order to identify these noisy boundary vectors automatically, the global characterization scheme is used to categorize the classification problems into two types. For different types, different optimal selections of boundary vectors are given. Thus, the group of noisy boundary vectors can be identified and

removed, leaving only critical boundary vectors that are essential for correct classification. Finally, both critical boundary vectors and K-means centers are utilized to form the reduced template set for classification. In this way, enough information for identifying correct class boundaries is guaranteed. Experimental results show that the proposed algorithm outperforms NN classifier, and seven state-of-the-art template reduction methods in terms of classification accuracy. Moreover, the performance variation of parameters in this algorithm is also analyzed and discussed.

5. A FPGA-based Multi-Class Classifier Having an Low-Power On-Chip Learning Capability

An FPGA classification system having low-power on-chip learning capability is introduced in this chapter. Thanks to the learning algorithm critical boundary vector based nearest neighbor classifier (CBVNN) proposed in the last chapter, a classification system with a practical scale could be implemented on FPGA with a small amount of hardware resource. The system that is capable for the learning of 256 64-dimension vectors, is consists of an on-chip memory, processors for the learning algorithms, parameter registers and a winner-take-all unit for decision-making. In this implementation, the most resource-consuming part, the Manhattan distance array (MDA) are shared by different learning steps to construct relative processors for k-means, boundary selection, and global characterization in CBVNN. As a result, the implementation cost is reduced and all of these steps are accelerated by the high parallelization achieved by MDA, so that the power consumption of learning is further reduced. The measurement was carried out to verify the performance of the proposed system.

6. Conclusions

In this paper, a hardware-friendly template reduction algorithm introducing critical boundary vector is presented, and was implemented to a FPGA system. Experimental results show that the classifier can show superior performance to seven state-of-the-art template reduction classifiers. Moreover, the FPGA implementation of this algorithm further improves the learning speed, and the power consumption for learning is greatly reduced as a result.