博士論文（要約）

A Template Reduction Algorithm Using Critical Boundary Vector and an Implementation to an On-Chip Learning VLSI

(主要境界ベクトルを用いたテンプレート削減アルゴリズムとオンチップ学習 VLSI への実装)

夏　文軍

Wenjun XIA

指導教員

三田　吉郎　准教授

Supervisor

Associate Professor Yoshio MITA

Department of Electrical Engineering and Information Systems

The University of Tokyo

In this paper, the concept of critical boundary vector is proposed and introduced to build classifiers having a low-power-consumption performance. Two classifiers are proposed and implemented to improve the learning speed and reduce the power consumption by analog circuits and digital circuits respectively.

For the analog classifier, a self-adaptive Gaussian function is applied, which is very suitable for hardware implementation with a small amount of resource. The misclassification problem due to the zero tail regions has been eliminated by introducing the self-adaptive scheme in the quasi-Gaussian circuitry. By applying a floating threshold scheme, the quasi-Gaussian kernel adaptively extends its tail region according to the characteristics of input data. As a result, the problem of locating input data in zero tail regions has been completely avoided. In this way, the classification accuracy has been significantly improved. Moreover, separate bus lines are provided to individual classes for flexible resource utilization, thus resolved the problem of fixed architecture in previous work. The proposed classifier architecture has been verified by software simulation and Nanosim simulation of the designed chip. Experimental results show that the classifier can show comparable performance to other common classifiers, and the operation of the designed chip in a 180nm CMOS technology is also verified by the measurement results. However, the poor accuracy using analog circuitries for distance calculation limits its application.

For the digital classifier, the concept of critical boundary vector is introduced into the nearest neighbor classifier in combination of a global characterization for further enhancement. In this work, a hardware-friendly template reduction method for NN classifiers that is applicable to a variety of classification problems is proposed. By introducing the concept of critical boundary vectors, a novel boundary vector selection algorithm with a global characterization scheme has been proposed to solve the issue of noisy boundary vectors. Based on simple distance calculation, the method automatically decides whether the vector should be removed from the template set or not according to the nature of the problem. In this manner, the accuracy is improved. In order to achieve a fast learning process and low power consumption, hardware system is also implemented. Experimental results show that the classifier can show superior performance to other common classifiers. Moreover, the FPGA implementation of this algorithm further improves the learning speed, and the power consumption for learning is greatly reduced as a result.