博士論文(要約)

Electrical characterization of strained and unstrained Si MOS interfaces and impact of interface defects on the device properties

（ひずみ Si およびひずみのない Si MOS 界面の電気的評価と界面欠陥が素子特性に与える影響）

蔡　偉立

東京大学

工学系研究科　電気系工学専攻

2014 年 12 月

指導教師：高木　信一

With the continuing scaling down of dimension of metal-oxide-semiconductor (MOS) devices, the conventional Si technique inevitably suffers the difficulty to further improve the performance of MOS devices. Consequently, the strained-Si (sSi) MOS devices have attracted considerable research interests due to the high electron and hole mobility. On the other hand, the wide application of sSi MOS devices requires the systematical understanding of properties of SiO_2/sSi and SiO2/Si interface in order to obtain high operating performance of sSi MOS devices. In order to characterize interface properties, diverse evaluation techniques have been proposed, such as conductance method and S-factor. In this study, SiO_2/sSi and SiO_2/Si interfaces properties are demonstrated in term of the density of interface states (D_{it}) by conductance method and S factor method. And also, the validity of threshold voltage shift (ΔV_{th}) in monitoring the mobility degradation is also examined. On the other hand, a more reliable parameter, surface potential fluctuation extracted from conductance curves, in demonstration of carrier mobility degradation.

Firstly, the properties of bi-axially-strained-Si (sSi) MOS interface states has been examined by the conductance method. It has been found that the conventional conductance method cannot directly apply on the characterization of SiO_2/sSi MOS interfaces, because of additional parasitic admittance coming from sSi/SiGe hetero-interface. This additional parasitic admittance cannot be corrected by the series conventional resistance correction (SRC) model. Taking the sSi/SiGe hetero-interface effect into account, a new equivalent circuit model for the SiO_2/sSi interfaces, utilized in the conductance analysis, has been proposed. And this new model has been found can effectively eliminate the influence of the additional parasitic admittance. Additionally, in order to get the energy distribution of any parameters of interface states, the position of surface potential has been determined in this study by using the device simulator, Sentaurus. By combination of the novel model and Sentaturus, the energy distribution of interface states properties can be successfully determined. And also in order to confirm the accuracy of the modified conductance method, the properties of the SiO_2/sSi MOS interface states have been evaluated at elevated temperatures ranging from 300K to 328K. According to the result, it has been found that the properties of SiO_2/Si interface states are not strongly changed by introduced biaxial tensile strain.

Secondly, the conductance method has been taken as one of the most informative

techniques in interface properties evaluation. However, the measurable and reliable energy distribution of conductance method mainly locates on the depletion region. Therefore, in order to get the full energy distribution of $D_{it,}$ another evaluation technique is needed. However, for the conventional S-factor method only D_{it} average between mid-gap and strong inversion is extracted, rather than the energy distribution of D_{it}. In this section, firstly, the accuracy of the S-factor method for evaluating the energy distribution of density of interface states (D_{it}) at MOS interfaces has been examined by device simulation. And in order to get the D_{it} energy distribution, V_g-dependent C_d has been successfully extracted by the combination of gate-substrate capacitance (C_{gb}) and gate-channel capacitance (C_{gc}). Based on the analysis, we propose an improved S-factor method including a new term, proportion to S/φ_s , in the analytical formulation of the relationship between D_{it} and the S factor. The modified S-factor method allows us to accurately provide the energy distribution of D_{it} with the accuracy of the lower half of 10^{10} $cm^{-2}eV^{-1}$ order.

With the developed conductance method and S-factor method, the full energy distribution of D_{it}, generated by FN stress, of sSi nMOSFETs have been obtained. At the same time, the ΔV_{th} of *C-V* curves under FN stress are also extracted. It is found that there is smaller ΔV_{th} in sSi nMOSFETs judging from *C-V* curves. D_{it} generation (ΔD_{it}), however, does not show clear strain-dependency. This inconsistent strain-dependency between ΔV_{th} and ΔD_{it} can be reconciled by shrinkage of band gap due to the introduced biaxially-tensile strain, especially for the relative weak FN stress condition.

Finally, the validity of ΔV_{th} and surface potential fluctuation (σ_s) in demonstration of device mobility degradation under FN stress has been examined in detail by using Si nMOSFETs. In this work, two different FN stress conditions have been used, only positive FN stress and positive + negative FN stress. It has been found that generation of interface states is suppressed in both of the FN stress, resulting in V_g-independent $\sigma_{s.}$ In the mobility extraction, the $N_s^{0.5}$ relationship between coulomb mobility ($\mu_{coulomb}$) and surface carrier density (N_s) has been successfully obtained. According to this work, it has been found that the $\mu_{coulomb}$ is inversely proportional to ΔV_{th}, in only positive FN stress. However, this inverse relationship would lose the validity in the positive + negative FN stress, due to the compensation between negative and positive interface

charges. On the other hand, for the surface potential fluctuation (σ_s), the relationship that $\mu_{coulomb} \sim \delta_s^{-2}$ keeps the validity in both of the two different FN stress.