博士論本 (要約)

Research on High Performance Program Methods of Resistive Random Access Memories

(抵抗変化型メモリの高性能書き込み手法に関する研究**)**

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Demand for non-volatile memory (NVM) is increasing due to the growth of data centers, personal computers and mobile devices. This motivation accelerates the development of storage class memory (SCM), which requires fast write and read speeds, large endurance and low operation power compared with NAND Flash memory and conventional hard disk drive (HDD). The Resistive Random Access Memory (ReRAM) is a developing technology which is considered a promising candidate of SCM.

In chapter 1, the performance of SCM is compared with NAND flash and HDD. The SCM is expected to have faster Read/Write/Erase time, higher endurance, smaller power and lower cost. The required specification of SCM is clarified to compare with ReRAM program characteristics.

In chapter 2, first, the physical models of ReRAM are introduced. The resistance switching of transition metal oxide (TMO) based ReRAM, including TaO_x, HfO_x and Al_xO_y ReRAMs, can be attributed to the formation and rupture of filament during set and reset programs. In addition, the carbon nanotube (CNT) based RAM (NRAM) can be considered as a special type of ReRAM which changes cell resistance and tunneling current by controlling the distance between CNTs. A conjectured model is proposed to explain the physical mechanism of NRAM set and reset programs. In specific, the NRAM cell resistance is controlled by the distance between CNTs. This distance can be decreased by using an attraction force and increased by using a repulsion force. The attraction and repulsion forces are generated by electrical induction and phonon excitation, respectively. Both of these two forces exist simultaneously during set and reset. However, the dominance of these forces is reversed on set and reset programs. This is possibly because there is a large amount of CNTs are close to the top electrode of NRAM cell, whereas a small amount of CNTs are close to the bottom electrode. The large amount of CNTs close to top electrode reduces the repulsion force during set program.

After the ReRAM is manufactured, forming is needed to initialize the device for the first program. Higher program stress is needed on the forming. The Al_xO_y ReRAM and NRAM forming operations are introduced by using different forming strengths. After forming, set and reset are applied on ReRAM to decrease and increase cell resistance,

respectively. Verify-program schemes are used during set and reset which repeats program pulse and resistance read until cell resistance reaches the target value. The advantages and disadvantages of program characteristics are introduced on ReRAMs with different materials. In specific, a tradeoff of program current and verify pulses can be found. TaO_x ReRAM has large program current, which makes the set and reset programs easier to succeed by using less verify pulse tries. In contrast, the Al_xO_y ReRAM and NRAM have smaller program current, however, more pulses is needed during verify-program. In array program, large program current limits the number of cells that can be programmed in parallel, because of the maximum program current from the power supply. On the other hand, the larger number of verify pulses increases verify-program time.

From chapter 3 to 6, six proposals are introduced to improve program characteristics on Al_xO_y ReRAM and NRAM. First, Al_xO_y ReRAM program schemes investigated in chapter 3. In one program, the voltage increase and pulse width increase schemes are found suitable for verify-set and verify-reset respectively. In addition, the reset program stress needs to be increased along with write cycles to compensate device wear-out. An improved verify-reset scheme, program stress reduction, is proposed which uses optimized moderate reset pulse width increment along with write cycles. By using the proposed scheme, 17% program energy reduction, 1.2 times program speed and 1.4 times endurance are achieved on single Al_xO_y ReRAM cell measurement compared with using fast reset pulse width increase. By using this proposed scheme on Al_xO_y ReRAM array, program BER reduces 8.5% after 10^4 verify-program cycles. Moreover, 2000 write cycles are measured on Al_xO_y ReRAM array during 25°C to 125°C to 25°C temperature variation. The high temperature is found to accelerate ReRAM wear-out and increase array BER.

In chapter 4, two proposals are introduced to improve Al_xO_y ReRAM verify-reset. These proposals use flexible program pulses to adapt the variation of cell condition during verify-reset. In specific, the first proposal, controlled reset voltage (V_{reset}) increment, increases reset pulse voltage during verify-reset only when the reset pulses fail continuously (hard-to-reset). It demonstrates 32% average program energy

reduction and 6.7× program speed. However, the median cell endurance decreases 33% because more wear-out is caused by using higher reset voltage. This scheme is suitable for the application which needs fast program speed. The second proposal, set-before-reset, applies set pulse during verify-reset when the cell is hard-to-reset, which converts the filament to an easy-to-reset state. This proposal achieves 31% program energy reduction, 1.6× median cell endurance enhancement and 3.6× program speed improvement simultaneously.

In chapter 5, two verify-reset schemes are proposed to improve the NRAM program performance. The first proposal Multiple-Pulse Reset uses two continuous reset pulses between cell resistance reads. The program time reduces 23% by using this proposal. The second proposal Gate Pulse Reset limits the number of bit line charge/discharge to only once during verify-reset. 40% program energy reduction is achieved by using this proposal.

In chapter 6, a novel error correction scheme Reset Check Reverse Flag (RCRF) is proposed. By applying RCRF on NRAM array, 80% program BER reduction is achieved after 10^8 write cycles by using only 0.4% of parity overhead. After RCRF, additional error correction code (ECC) is needed to correct the remaining program error. By using RCRF and Bose-Chaudhuri-Hocquenghem (BCH) ECC, maximum parity overhead reduces 38% over 10^8 write cycles, compared with conventional error correction using only BCH ECC.

In chapter 7 the previous proposed schemes are applied on other types of ReRAM to investigate the universality of these proposals. The first five proposals in chapters 3, 4 and 5 are not found suitable to be applied to the other types of ReRAM because of the difference in their physical mechanisms of resistance switching. On the other hand, RCRF is applicable to both NRAM and Al_xO_y ReRAM, because it is not related to device physics.

Finally in chapter 8, the summary, conclusion and future perspective of this thesis are discussed. Further improvements of ReRAM program characteristics are needed.