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Dissertation

Mechanism of Stress-Induced Migration in Metal Interconnections on Semiconductor Devices

（半導体デバイスに使用される金属配線における
ストレスマイグレーションのメカニズム
に関する研究）

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Contents

CHAPTER 1

INTRODUCTION

1-1 A brief history of stress-induced migration

In 1984, a new type of failure in aluminum interconnections on very large-scale integrated circuits (VLSI) was first reported [1,2], and it has become one of the most important problems related to the reliability of aluminum and aluminum-alloy interconnections. This type of failure generates voids and fractures in interconnections during high-temperature storage without electric current.

Many studies have been performed to analyze the mechanism of this failure, because voids and fractures in interconnections were about to become recognized as being future serious problems for submicron-size semiconductor devices in the '80s. The failure mechanism has been discussed in terms of the relation between the lifetime of interconnections and the following:

(1) sample storage tests [3-11],

(2) thermal cycle tests [12],

(3) stress in interconnections [3,5,7,8,13-27],

(4) interconnection geometries such as width and thickness [3,4,11,13,28],

(5) kinds of passivation layers [4,8,10,14,29,30],

(6) kinds of interconnection and under layer materials [8,9,13,21,23,29,30],

(7) fabrication processes [18,31,32].

From the results of those studies, it was clarified that voids and fractures are generated by vacancy migration caused by the thermal stress in interconnections attributed to the difference in the thermal expansion between interconnections and passivation layers. For this reason, this type of failure is known as stress-induced migration in interconnections on

semiconductor devices. Moreover, the following guidelines were proposed to suppress the stress-induced migration;

(1) adoption of Al-alloy interconnections such as Al-Si-Cu, Al-Si-Pb and Al-Cu material [8-11,15,21,29], instead of Al and Al-Si material most commonly used in the '80s,

(2) adoption of the stack structure composed of Al or Al-alloy material interconnections and Ti or W material interconnections [16].

These guidelines succeeded in suppressing the interconnection failures caused by stress-induced migration. Due to these successes, studies on stress-induced migration have decreased, in spite of the fact that the following problems remain.

(1) The mechanism of stress-induced migration has not been clarified.

(2) The effect of guidelines taken to yield finer interconnections is not clear.

(3) Discrepancies are found among results reported by researchers on the storage temperature dependence of the interconnection lifetime. Mcpherson and Dunn [5], Tezaki et al. [8] and Kato et al. [11] reported that the peak failure rate appears in the temperature range from 150 to 200 ℃. Hinode et al. [6] reported that the failure rate increases as the temperature rises to 300 ℃. Mayumi et al. [4] reported that the failure rate is independent of temperature in the temperature range from 125 to 250 ℃.

(4) The influences of voids caused by stress-induced migration on electromigration are not clear. Electromigration is also one of the most important problems related to the reliability of interconnections on semiconductor devices, and generates voids and fractures in interconnections during high-temperature storage with high-density electric current.

Therefore studies on stress-induced migration must be continued, because the fundamental points, as mentioned above, are not clear, as yet.

1-2 Outline of this thesis

The purpose of this thesis is to clarify the mechanism of stress-induced migration in interconnections on semiconductor devices based on thermodynamics theory and experiments. This work involved the following procedures.

In chapter 2, an initial stage of stress-induced migration is experimentally studied during short-term high-temperature storage tests. Stress-induced migration usually occurs during long-term high-temperature storage, but the initial stage during high-temperature storage may influence the mechanism of stress-induced migration. Moreover, a study of the initial stage of stress-induced migration is useful for understanding the fundamental characteristics of interconnections.

In chapter 3, single-vacancy formation energy in interconnections is measured by means of experiments using a quenching technique, and a theoretical model is proposed. The results of the theoretical model are compared with the experimental results.

In chapter 4, the vacancy concentration distribution in interconnections was calculated using the stress-induced vacancy model which shows the relation between the stress and vacancy concentration. For calculating the vacancy concentration distribution in interconnections, the stress distribution in interconnections is required, which is calculated using three-dimensional thermal stress simulations.

In chapter 5, a theoretical stress-induced migration model is proposed, which consists of a vacancy continuity equation, a stress-induced vacancy equation and a thermal stress model. The vacancy continuity equation consists of a vacancy diffusion model and a vacancy drift model. The driving force of the vacancy diffusion is the gradient of vacancy concentration and that of the vacancy drift is the gradient of the free energy of the vacancy.

In chapter 6, the stress-induced migration model is applied to void formation, and the results are compared with the experimental results.

In chapter 7, the stress-induced migration model is applied to the interconnection fracture, and the results of application are compared with the experimental results.

CHAPTER 2
INITIAL STAGE OF STRESS-INDUCED MIGRATION

2-1 Introduction

Stress-induced migration, which forms voids and fractures in interconnections on semiconductor devices during high-temperature long-term storage without electric current, is caused by the thermal stress attributed to the difference in the thermal expansion between interconnections and passivation layers [3,5,7,8,13-27]. The stress-induced migration is an extremely slow phenomenon [3-11], therefore high-temperature long-term storage tests are suitable experimental methods for analyzing the mechanism of stress-induced migration. However, the initial stage of stress-induced migration may influence the stress-induced migration mechanism, and it is useful to understand the characteristics of thin film interconnections.

In this chapter, the initial stage of the stress-induced migration in interconnections on semiconductor devices was studied through measurements of the electric resistivity and the thermal stress, as well as observations of the interconnection surfaces.

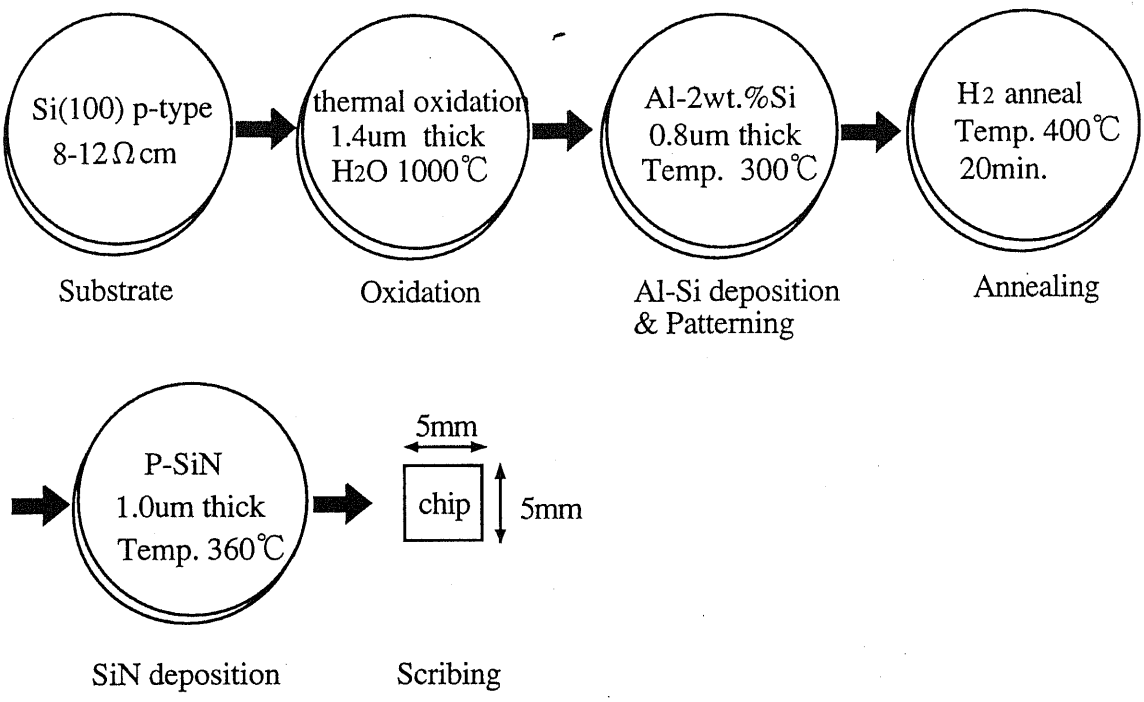


Fig. 2-1. Summary of the sample fabrication process.

2-2 Sample preparation and experimental method

2-2-1 Sample preparation

Samples were prepared by the conventional VLSI fabrication process. Aluminum alloy (Al-2wt.%Si) was sputter-deposited on thermally oxidized silicon wafers at a stage temperature of 300 ℃. Si wafers were p-type, 8～12 Ω-cm, <100>-oriented and 500 um thick, and the thermal oxidization layer of 1.4 um thickness was grown on the Si wafers at 1000 ℃ in H_2O ambient. Patterns of interconnections were formed by means of the plasma etching method. After interconnection patterning, the wafers were annealed at 400 ℃ for 20 minutes in H_2 ambient, and subsequently covered with a plasma-chemical-vapor-deposited SiN layer, 1.0 um thick, at a stage temperature of 360 ℃. Finally, the wafers were scribed into chips of 5 mm×5 mm size. These processes are summarized in Fig. 2-1 and are the

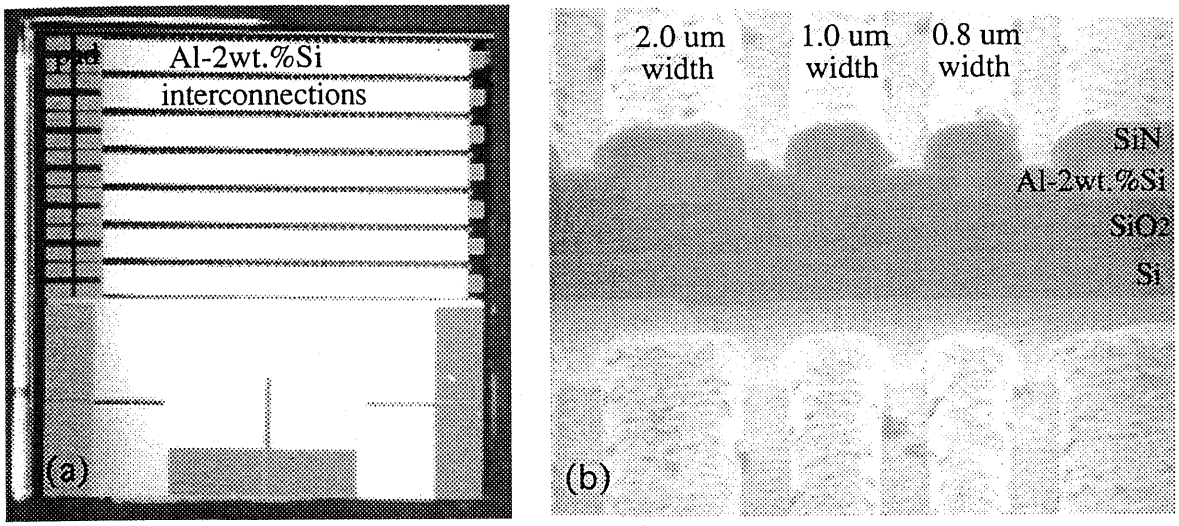


Fig. 2-2. Micrographs of the samples: (a) the sample for electrical resistivity measurements and (b) the cross section of the sample for observations of interconnection surface.

commonly used fabrication process throughout this work.

For measurements of the electrical resistivity, interconnections of 0.5 m length, 0.8 um thickness and from 0.8 to 3.0 um wide were designed. For observations of the interconnection surfaces, interconnections of 5 mm length, 0.8 um thickness and from 0.8 to 10 um wide were designed. The micrographs of the samples are shown in Fig. 2-2: Figure 2-2(a) shows the sample used for electrical resistivity measurements and Fig. 2-2(b) shows the cross section of the sample used for observations of the interconnection surface.

2-2-2 Experimental method

Measurements of the resistivity change for 60-minutes storage were carried out between -198 to 350 ℃. The resistivity was measured at room temperature before and after the storage. The time dependence of the resistivity change was also measured at temperatures between 125 to 350 ℃. To reduce resistivity measurement errors due to the change of the ambient temperature during the measurement at room temperature, the measurement values were corrected using the resistivity of a reference sample. Consequently, the experimental

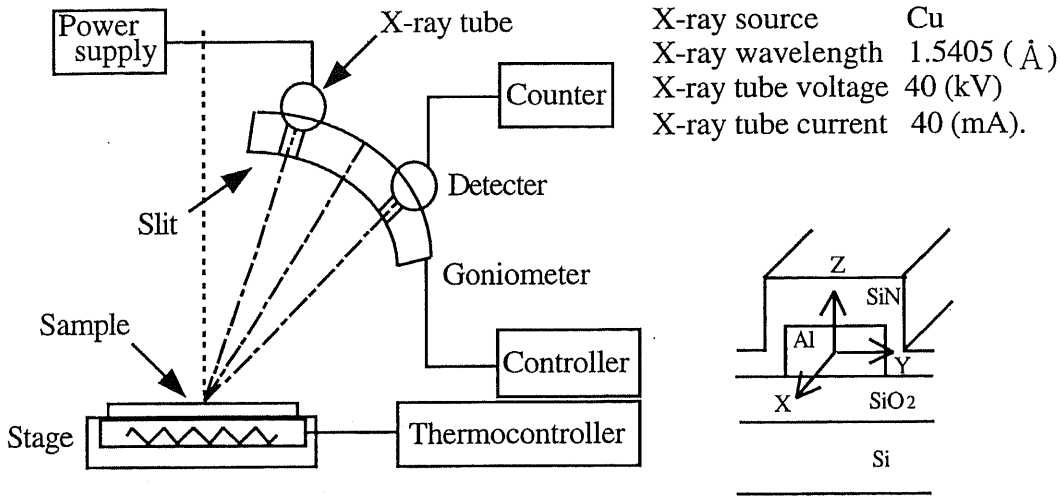
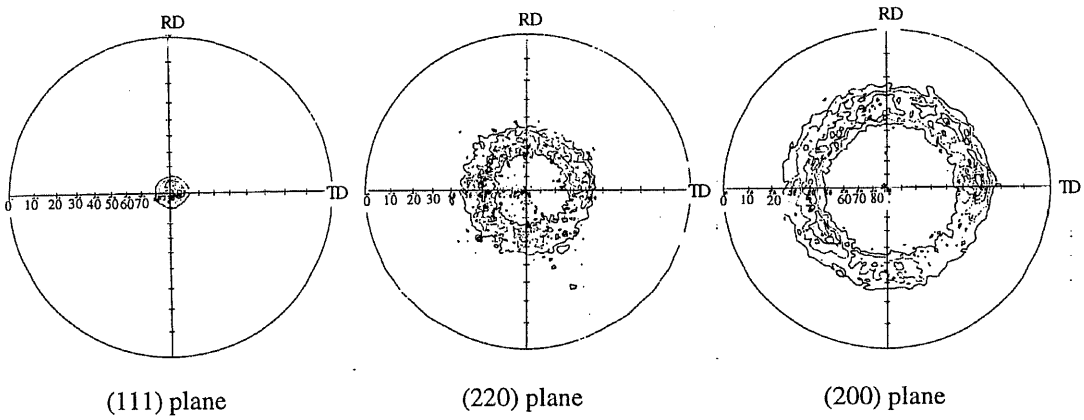


Fig. 2-3. Schematic of X-ray diffraction measurement system.



(111) plane (220) plane (200) plane

Fig. 2-4. X-ray diffraction pole figures of interconnections: (a) Al (111) plane, (b) Al (220) plane and (c) Al (200) plane. Maximal X-ray intensity: (a) 792 (arb. units), (b) 46 (arb. units) and (c) 73 (arb. units).

error was reduced to less than 0.1 % for the samples of 5×10^{-6} Ω-cm.

Three-dimensional stress in interconnections was derived using the fundamental stress-strain relation of Hooke's law for three-dimensional strain measured by the X-ray diffraction method [8,14,15,19,21,33,34]. Figure 2-3 shows the X-ray diffraction measurement method system. The pole figures obtained from X-ray diffraction show that the samples had a {111} fiber texture parallel to the surface within a deviation of a few degrees, as shown in Fig. 2-4.

in (222) orientation was measured for three different directions: normal to the surface, tilted 70.5° tilted from the Z-axis along the X-axis, and tilted 70.5° from the Z-axis along the Y-axis. Since the spot size of the X-ray beam at the sample surface was about 5 mm×5 mm, the obtained values were for the average stress in several hundred interconnections. The experimental error was less than ±10 MPa.

The sample observation was performed using a secondary electron microscope (SEM) and a transmission electron microscope (TEM). The SiN passivation layer was removed from the sample surface for the SEM and TEM observations using a dry-etching method at room temperature.

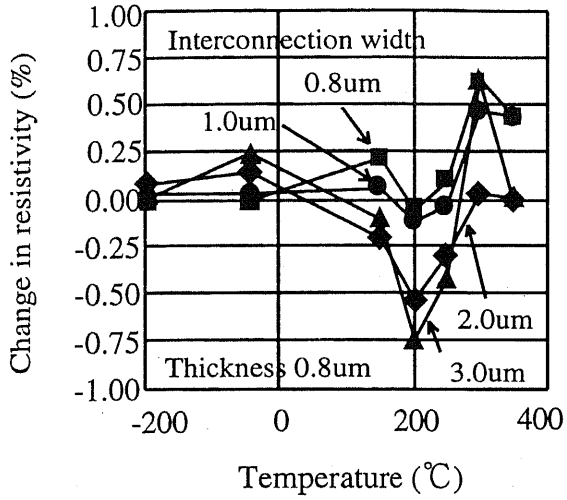


Fig.2-5. Change in the electrical resistivity of Al-2wt.%Si interconntection for 60 min storage. Resistivity is measured at room temperature.

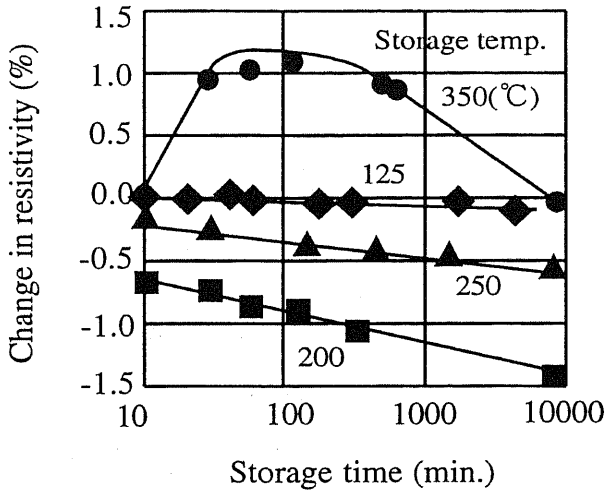


Fig. 2-6. Time dependence of the resistivity change by high-temperature storage. Line width is 1.0um and thickness is 0.8um. Resistivity is measured at room temperature.

2-3 Experimental results

2-3-1 Electrical resistivity change during short-term storage

Figure 2-5 shows changes in the electrical resistivity in the temperature range from -198 to 350 ℃ for 60-minutes storage. The resistivity change was $(\rho_1 - \rho_0) / \rho_0$, where ρ_0 and ρ_1 are resistivities before and after storage, respectively. The results are summarized as follows.

(1) The resistivity does not change in the temperature range from -198 to 150 ℃.

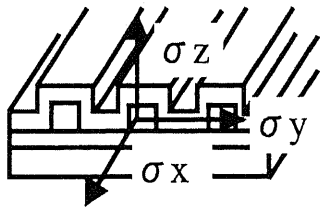
(2) When the temperature rises beyond 150 ℃, the resistivity first decreases in the temperature range from 150 to 200 ℃ and then increases in the range from 200 to 300 ℃.

(3) In addition, the resistivity at 350 ℃ is less than that at 300 ℃.

(4) The resistivity change of narrower interconnections tends to be smaller than that of broader interconnections.

Table 2-1
Thermal stress in interconnections.

Storage temp.(℃)	Storage time	Thermal stress (MPa)		
		σ x	σ y	σ z
	initial state	457	239	145
250	133 hours	479	291	185
	500 hours	446	266	155
350	1 hour	547	303	195



Positive sign indicates tensile stress.

2-3-2 Time dependence of resistivity change on storage time

Figure 2-6 shows the change in the electrical resistivity with the temperature. The sample interconnections were of 0.5 m length, 0.8 um thickness and 1.0 um width. The results are summarized as follows.

(1) The resistivity at temperatures below 250 ℃ decreases with time, and the magnitude of this resistivity reduction is increasingly significant in the order of 200, 250, and 125 ℃.

(2) The resistivity change at 350 ℃ exhibits a different behavior from there at the other temperatures; the resistivity increases up to about 100 minutes, and then starts to decrease, just as in the case of temperature below 250 ℃.

2-3-3 Change in thermal stress

The average thermal stress values in interconnections was measured at 250 and 350 ℃, as summarized in Table 2-1. The sample interconnections were of 0.5 m length, 0.8 um thickness and 1.0 um width. The results are summarized as follows.

(1) When the storage temperature is 250 ℃, the stress increases slightly during the

initial 133 hours, and then decreases during the subsequent 500 hours.

(2) When the storage temperature is 350 ℃, the stress increases significantly during the initial 60-minutes, which coincides with the rapid increase in resistivity shown in Fig. 2-6.

2-3-4 Sample observation

Figure 2-7 shows the grain growth of Al-2wt.%Si in the interconnections at 200 and 350 ℃. The grain growth at 350 ℃ is grater than that at 200 ℃. It is noted that degenerations considered to be due to a pileup of dislocations are observed at grain boundaries only in the sample of 60-minutes storage at 350 ℃.

Figure 2-8 shows many dislocations within the grain near the edges of the interconnection, observed after 60-minutes storage at 350 ℃. This condition corresponds to the maximal increase in resistivity shown in Fig. 2-6.

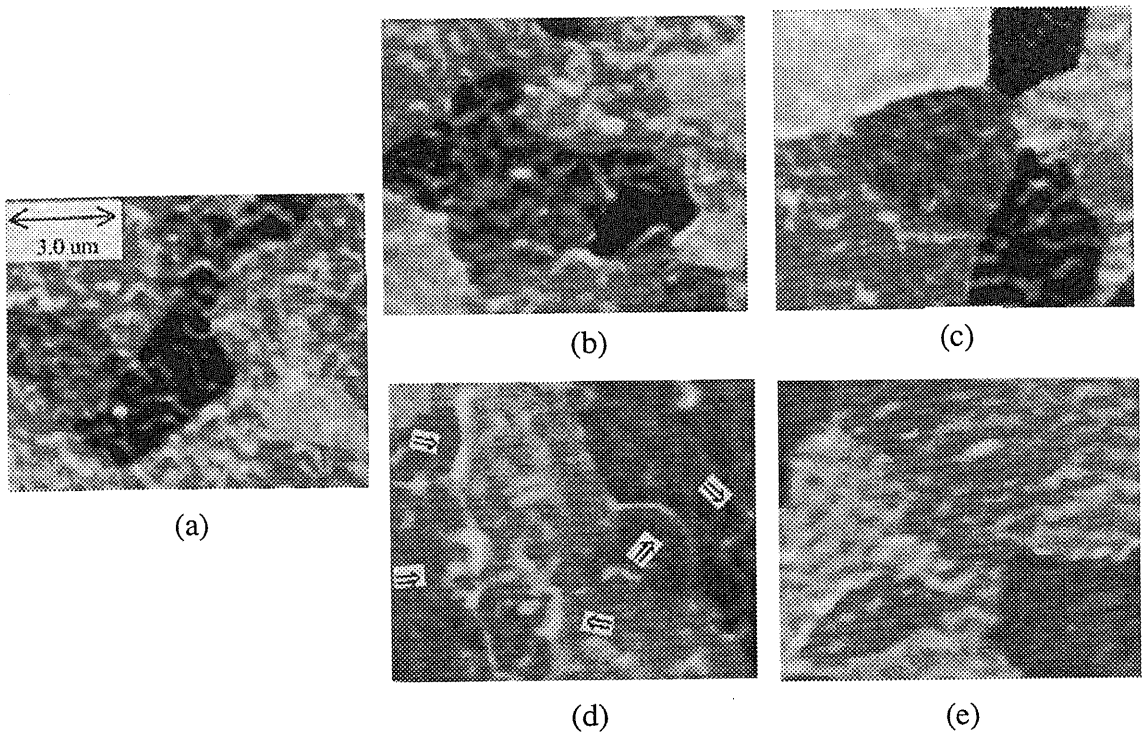


Fig. 2-7. SEM micrographs of grain growth. (a) Initial sample. Grain size is 2.7 um. (b) After 60 min at 200℃. Grain size is 2.7 um. (c) After 3.5 hours at 200 ℃. Grain size is 3.5 um. (d) After 60 min at 350 ℃. Grain size is 3.7 um. ⇒ shows pileup of dislocations. (e) After 3.5 hours at 350 ℃. Grain size is 4.2 um.

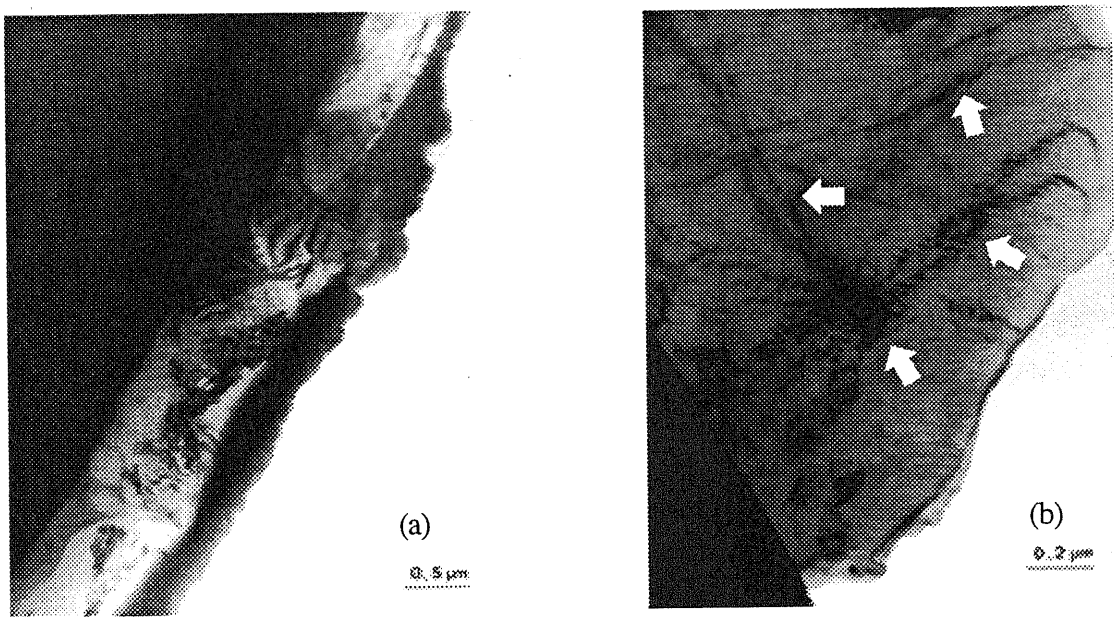


Fig. 2-8. Micrographs of the dislocation. (a) Initial sample. (b) After storage at 350 ℃ for 60 min. ⇨ shows dislocations.

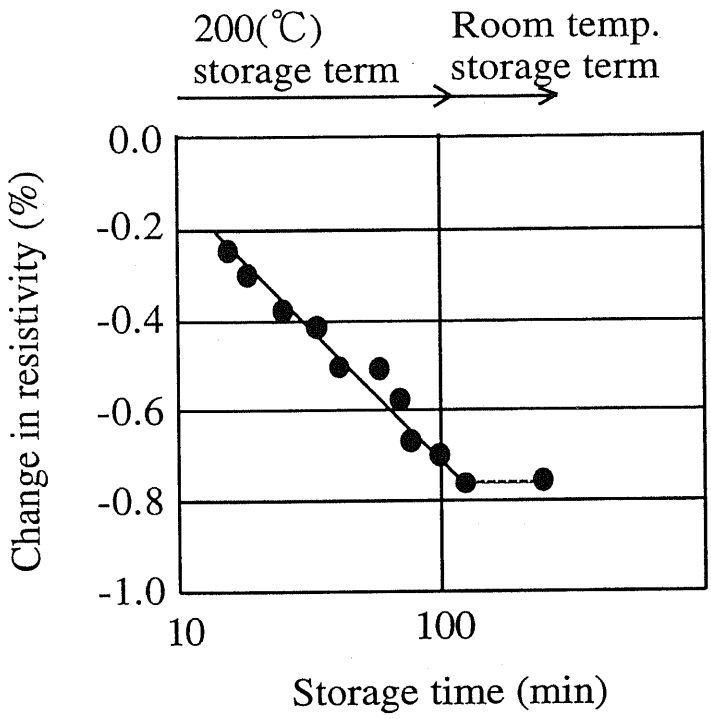


Fig. 2-9. Resistivity change during high-temperature and room-temperature storage. Line width is 1.0 um and thickness is 0.8 um. Resistivity is measured at a high temperature.

2-4 Discussion

2-4-1 Time periods of resistivity change

In the experiments, the resistivities were measured at room temperature, therefore the time period of the actual change in the electrical resistivity can not be determined from Figs. 2-5 and 2-6. It is considered that the change in resistivity occurred during the period of temperature rise or fall or during storage. Knowledge of the time period of the actual change in the electrical resistivity is important to understand the stress-induced migration phenomenon.

Figure 2-9 shows the change in resistivity, measured during storage at 200 ℃ for 120 minutes, followed by storage at room temperature for 120 minutes. The sample interconnections were of 0.5 m length, 0.8 um thickness and 1.0 um width. The standard point of the resistivity change, ρ_0, during 200 ℃ storage is the resistivity at 200 ℃, which was

measured immediately after the temperature at the interconnections reached 200 ℃. The standard point of resistivity change, ρ_0, during room-temperature storage is the resistivity just after 200 ℃ storage. The resistivity change decreases with time during 200 ℃ storage, and is constant at room temperature. These results reveal that the resistivity change occurs during 200 ℃ storage.

Moreover, the change in the resistivity was within the values of experimental error, even after a heat cycle test of 350 cycles ranging from -55 to 150 ℃.

Consequently, it is determined that the resistivity does not change during the periods of temperature rise and fall, but rather during the high-temperature storage. In the high-temperature long-term storage tests, samples are frequently taken out of or put into a constant temperature box to measure their resistivity. These changes in temperature do not influence the resistivity of the samples.

2-4-2 Mechanisms of resistivity change

There is a critical point of resistivity change at around 200 ℃, as shown in Figs. 2-5 and 2-6. To clarify the mechanism of resistivity change around the critical temperature, the change in the grain boundary of the interconnections was observed using a SEM.

In the case of 350 ℃ storage, degenerations were observed near the grain boundary for 60-minutes storage, as shown in Fig. 2-7(d), and furthermore, Fig. 2-8 shows the dislocations near the grain boundary for 60-minutes storage. These defects disturb the flow of electrons, which results in the increase of resistivity, as shown in Fig. 2-6. After 3.5 hours, degenerations almost disappear, as shown in Fig. 2-7(e), and the resistivity decreases, as shown in Fig. 2-6.

In the case of temperatures below 200 ℃, the grain growth becomes dominant without any degeneration near the grain boundary, as shown in Figs. 2-7(b) and 2-7(c). The grain growth results in a decrease in the density of the grain boundaries, so that the resistivity

decreases, as shown in Fig. 2-6.

From the above discussions, the complex behavior of the resistivity change can be considered to be determined by a competition between two phenomena.

(1) The degenerations near the grain boundary, such as dislocation pileup, increase the resistivity of the interconnection.

(2) The disappearance of degenerations near the grain boundary and the grain growth decrease the resistivity.

The resistivity started to decrease after 100 min at 350 ℃. This decrease may have been due to the saturation of the pileup of dislocations, as shown in Fig. 2-7(e), so that the grain growth became dominant, similar to that at temperatures below 250 ℃.

The change in the resistivity of the narrower interconnections tended to be less than that of the broader interconnections, as shown in Fig. 2-5. Narrower interconnections, under 1.0 um wide, resemble bamboo structures, so that the number of grains and grain boundaries in the narrower interconnections are fewer than that in the case of broader interconnections. Consequently, in the case of narrower interconnections it is harder for the resistivity to change with temperature.

2-4-3 Mechanisms of stress change

The thermal stress increases during the early stages at temperatures of 250 and 350 ℃, as summarized in Table 2-1. It is considered that this increase in stress is mainly due to the grain growth, because the number of Al and Si atoms remains unchanged in the interconnections, as shown in Fig. 2-10. With grain growth, the tensile stress in the interconnections increases, and the number of grain boundaries decreases. In the case of 350 ℃, the grain growth is more significant compared with that at 200 ℃, as shown in Fig. 2-7, so that the tensile-stress increases more significantly.

Thermal stress begins decreasing after 500 hours at 250 ℃ storage, which is caused by

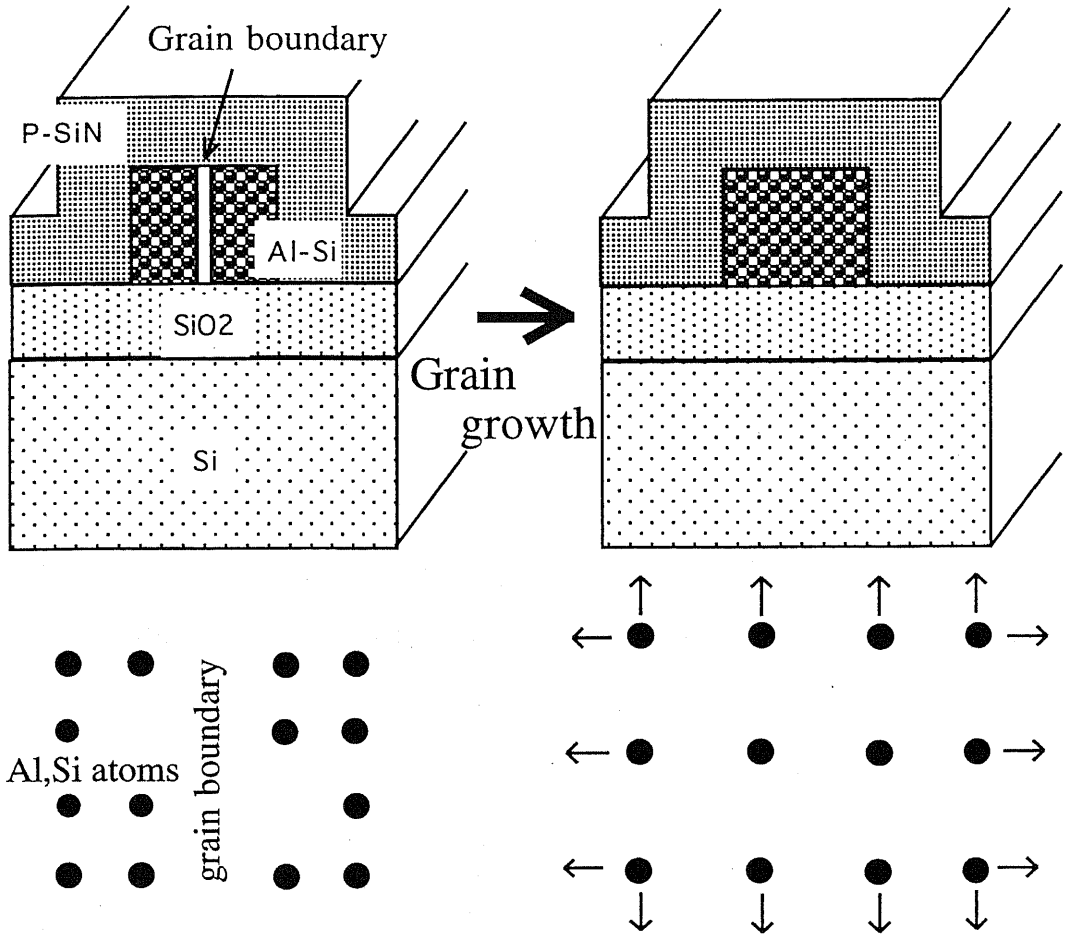


Fig.2-10. Schematic of relation between the grain growth and the tensile stress. Since the number of Al and Si atoms in the interconnection remains unchanged, if the grain boundary density decreases due to the grain growth, the tensile stress should increase.

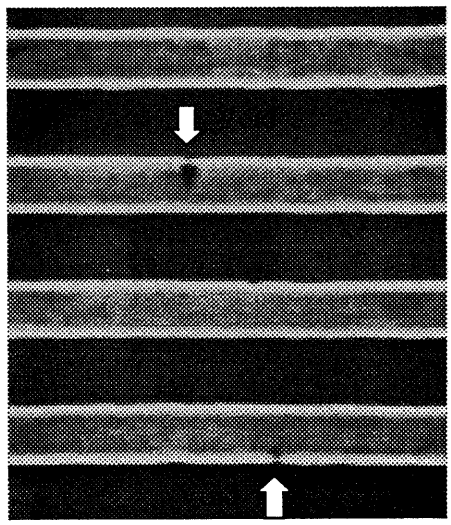


Fig. 2-11. Micrograph of voids formed at a temperature of 200 ℃ maintained for 500 hours.

the formation of microvoids in the interconnections, as shown in Fig. 2-11. Voids in the interconnections induce stress relaxation. It is considered that voids are generated by stress-induced migration.

It is considered that the change in the thermal stress is determined by a competition between the above-mentioned phenomena.

2-4-4 The relation between lifetime and resistivity change at the initial stage

Among the cases of storage temperatures below 250 ℃, the decrease in the resistivity change at 200 ℃ was the most significant. This distinctive feature is consistent with the open failure rate of the interconnection and other reports [5,8,11]. This indicates the possibility that the open failure rate of the interconnection is related qualitatively to the change in the electrical resistivity during the initial stage of the stress-induced migration. The relation between lifetime and resistivity change will be discussed in chapter 7.

2-5 Conclusion

The characteristics of the initial stage of the stress-induced migration vary markedly with the storage temperature and period.

The resistivity change can be considered to be determined by a competition between two phenomena.

(1) The disappearance of degenerations near the grain boundary and the grain growth decrease the resistivity.

(2) The degenerations near the grain boundary, such as dislocation pileup, increase the resistivity of the interconnection.

The latter tends to saturate after a certain time in high-temperature storage, after which the former becomes dominant.

The change in the thermal stress is determined by a competition between two phenomena.

(1) The micro void decreases the thermal stress.

(2) The grain growth increases the thermal stress.

The latter tends to saturate after a certain time in high-temperature storage, after which the former becomes dominant.

CHAPTER 3

VACANCY FORMATION ENERGY

3-1 Introduction

It is considered that void formation and fractures are caused by vacancy migration to vacancy sinks [1-3], so that the vacancy concentration distribution in interconnections is one of the most important issues to study to clarify the mechanism of stress-induced migration. Knowledge of the vacancy formation energy is necessary to determine the vacancy concentration distribution, because the vacancy concentration is calculated using the vacancy formation energy. The vacancy formation energy can be measured using a quenching technique which freezes vacancies generated at high temperatures. Several investigations related to the quenching of lattice vacancies in aluminum have been reported using a resistometric technique which is based on the resistivity change of samples [35-39], because the resistivity change of quenched-in samples is proportional to the quenched-in vacancies [35-39]. In this method, the change in resistivity, $\triangle \rho$, immediately after the quenching, is given by

$$\Delta \rho = A \exp\left(-\frac{E_F}{k T_q}\right), \quad (3-1)$$

where A is a constant, Tq is the absolute temperature of samples just before quenching, k is Boltzmann's constant and E_F is the energy required for single-vacancy formation.

Using eq. (3-1), Bradshaw and Pearson reported $E_F = 0.76 \pm 0.04$ eV [35], Federighi and Gatto reported $E_F = 0.74 \pm 0.03$ eV [36], DeSorbo and Turnbull reported $E_F = 0.79 \pm 0.04$ eV [37] and Furukawa et al. obtained a value of $E_F = 0.702 \pm 0.003$ eV [38]. These single-vacancy formation energies are obtained using the quenching technique with pure aluminum

wire or foil.

Single-vacancy formation energy in aluminum or aluminum-alloy interconnections on semiconductor devices, however, has not yet been reported. In this case, the single-vacancy formation energy value may differ from the above values, because interconnections are subjected to tensile stress due to the passivation layer.

In this chapter, the vacancy formation energy for Al-2wt.%Si interconnections on semiconductor devices is studied using the quenching technique, and a theoretical calculation procedure for the vacancy concentration in this case, taking into account the strain force in interconnections, is discussed; as a result, the author proposes a stress-induced vacancy model which indicates the relation between the stress and the vacancy concentration.

3-2 Sample preparation

Sample fabrication was performed using the same processes as described in chapter 2. Here, these processes are briefly described. Al-2wt.%Si of 0.8 um thickness was sputter-deposited on thermally oxidized silicon wafers at 300 ℃. A thermal oxidization layer of 1.4 um thickness was grown at 1000 ℃ in H_2O ambient. Patterns of interconnections of 3.0 um width were formed by the plasma etching method. After patterning the interconnections, the wafers were annealed at 400 ℃ for 20 min in H_2 ambient, and subsequently covered with a SiN layer of 1.0 um thickness formed by plasma chemical vapor deposition at 360 ℃, T_{SiN}. The wafer was scribed into chips of 5 mm×5 mm size, and finally, the chips were mounted on small ceramic packages.

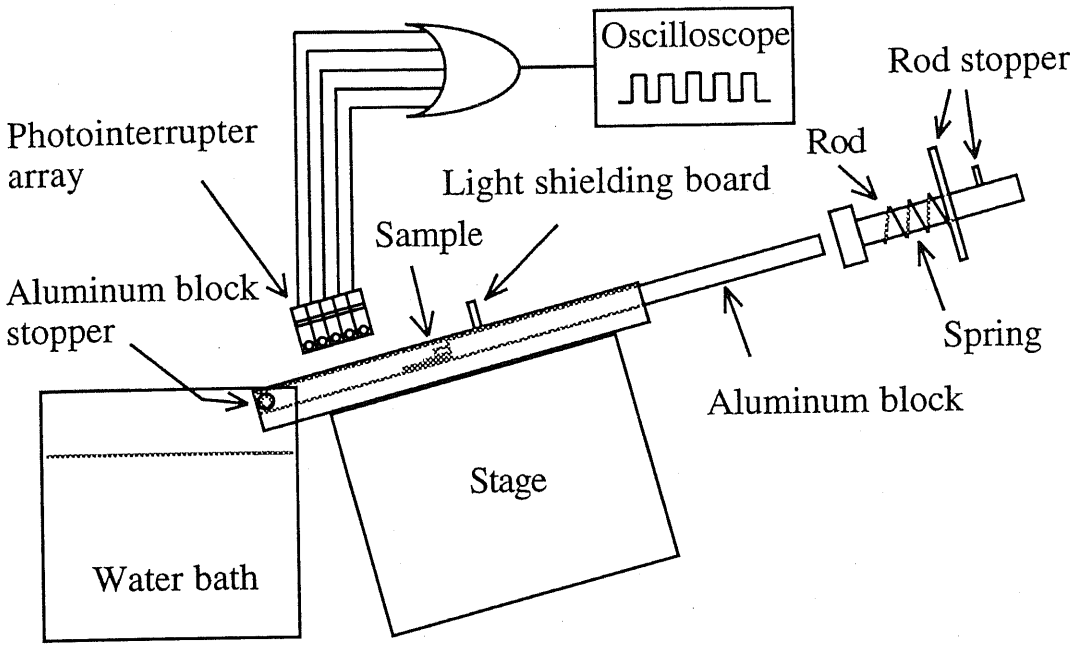


Fig. 3-1. Quenching apparatus. The samples are placed on a heated sample stage, and plunged into a water bath by the recoil of the spring. The temperature of the heated stage is varied from 200 to 300 ℃ and the temperature of the water is 1.5±0.3 ℃. The speed of the moving samples is detected by the photointerrupter.

3-3 Experimental method

3-3-1 Quenching technique

Figure 3-1 shows the quenching apparatus composed of a heated sample stage, a sample plunger mechanism, a detector of the sample pushing speed and a water bath. The samples were placed on the heated stage at a temperature *Tq* which was controlled from 200 to 300 ℃ with an accuracy of ±1.0 ℃.

In the experiments, the samples were kept on the heated stage for 5 min, so that the vacancies reached an equilibrium concentration at *Tq*, as shown in Fig. 3-2. The samples were then plunged into the water bath which was at a controlled temperature of 1.5±0.3 ℃. The author measured the quenching speed using monitor samples, which are used to measure the transient resistivity directly. From the transient resistivity change of the monitor samples, the author confirmed that the quenching speed was more than 2.8×10^4 (℃ / s).

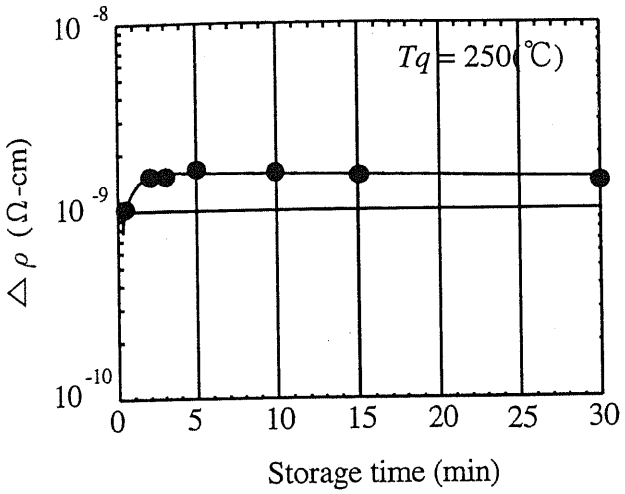


Fig. 3-2. Resistivity change, △ ρ , with storage time dependence.

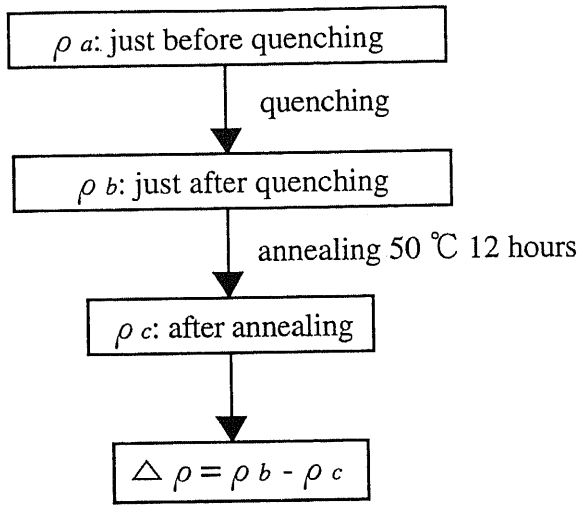


Fig. 3-3. Measurement procedure

For this experiment, it is sufficient to freeze the vacancies generated at *Tq* [40].

3-3-2 Measurement procedure

First, the electrical resistivity of samples, ρ_a, was measured just before quenching. Next, the samples were quenched using the apparatus shown in Fig. 3-1, and the resistivity of quenched-in samples, ρ_b, was measured again. Finally, the samples were kept at 50 ℃ for 12 hours to anneal out quenched-in vacancies, and then the resistivity of samples, ρ_c, was measured after annealing. This procedure is illustrated in Fig. 3-3.

Thus, the author measured three values of resistivity, ρ_a, ρ_b and ρ_c, for each sample. The resistivity change ($\rho_b - \rho_a$) is due to two kinds of phenomena: vacancy increase and aluminum crystal structure change caused during sample storage at *Tq* for 5 minutes. The resistivity change ($\rho_b - \rho_c$) is caused only by quenched-in vacancies, because the annealing at 50 ℃ for 12 hours does not change the crystal structure of aluminum, as discussed in chapter 2, but anneals out quenched-in vacancies [35,37,38]. Hereafter, we use the resistivity

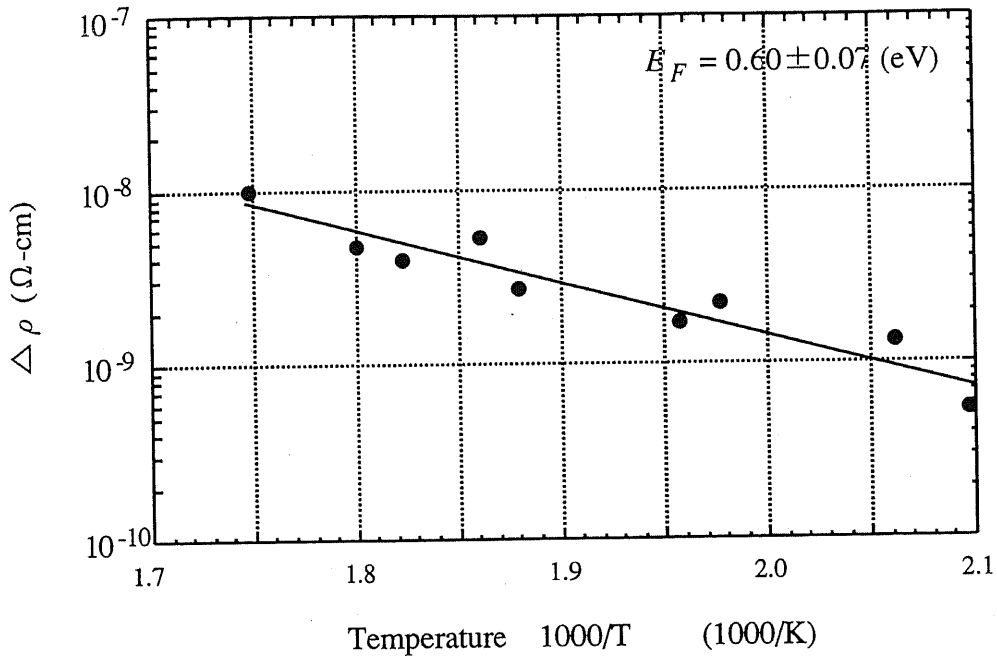


Fig. 3-4. Resistivity change, △ ρ , in Al-2wt%Si interconnections with a SiN passivation layer. The interconnection is of 0.8 um thickness, 3.0 um width and 0.5 m length. The passivation layer is 1.0 um thick. The vacancy formation energy is estimated to be 0.60±0.07 eV.

change (ρ_b - ρ_c) (≡△ ρ) to estimate the total number of quenched-in vacancies.

3-4 Experimental results

Figure 3-4 shows a plot of the resistivity change, △ ρ , resulting from the quenched-in vacancies, as a function of the reciprocal of *Tq*. From this plot, the single-vacancy formation energy E_F is derived as 0.60±0.07 eV in the temperature range of 200 to 300 ℃, where Al-2wt.%Si interconnections were of 0.8 um thickness, 3.0 um width and 0.5 m length.

3-5 Vacancy concentration in interconnections without stress

There is ample evidences [35-40], both theoretical and experimental, that in some of the lattice sites in pure metals or alloys there exist single vacancies. The theoretical evidence is based on a thermodynamic argument; that the free energy of pure metals is at a minimum if it contains a specific concentration of single vacancies.

This concentration can be calculated as follows [41-43]. There are n single vacancies in pure metal containing N metallic-atom sites, and if n vacancies are arranged at random among N metallic-atom sites, the probability W of any such arrangement is

$$W=\frac{(n+N)!}{n!\,N!} \quad . \quad (3-2)$$

By using Stirling's approximation and the Boltzmann relationship, the author obtains the mixing entropy as

$$S_{mix}=k\{(n+N)\ ln(n+N)-N\,ln\,(N)-n\,ln(n)\} \quad . \quad (3-3)$$

The change in free energy F due to vacancies in pure metals is given by

$$F=n\,E_F-n\,T\,S_F-k\,T\ \{(n+N)\ ln(n+N)-N\,ln\,(N)-n\,ln(n)\} \quad . \quad (3-4)$$

Here, E_F is the single-vacancy formation energy required to create a single vacancy, S_F is the single-vacancy formation entropy required to create a vacancy and S_{mix} is the mixing entropy required to mix vacancies and metallic atoms, as shown by eq. (3-2).

The free energy of pure metal is minimum if it contains a specific concentration of vacancies, namely,

$$\frac{\partial F}{\partial n}=0 \quad , \quad (3-5)$$

but

$$\frac{\partial F}{\partial n} = E_F - S_F\, T - k\, T\, ln\left(\frac{n+N}{n}\right), \quad (3-6)$$

and therefore the equilibrium single-vacancy concentration is given by

$$C = \frac{n}{n+N} = exp\left(-\frac{E_F}{k\,T}\right) exp\left(-\frac{S_F}{T}\right). \quad (3-7)$$

Equation (3- 7) gives the relationship between the temperature and the single-vacancy concentration in pure metals without stress.

In the case of dilute alloys without stress [39], the single-vacancy concentration for solvent metals, C_{SOLV}, is given by

$$C_{SOLV} = (1 - Z\, C_S)\; exp\left(-\frac{E_F}{k\,T}\right) exp\left(\frac{S_F}{k}\right), \quad (3-8)$$

where Z is the number of first-nearest-neighbors to the vacant site and C_S is the solute concentration.

The vacancy concentration for solute metals, C_{SOLU}, is given by

$$C_{SOLU} = Z\, C_S\; exp\left(-\frac{E_F}{k\,T}\right) exp\left(\frac{S_F}{k}\right) exp\left(\frac{E_{FB}}{k\,T}\right) exp\left(-\frac{S_B}{k}\right), \quad (3-9)$$

where E_{FB} is the binding energy between vacancies and solute atoms and S_B is the entropy of vacancies near solute atoms. Equation (3-9) shows that the binding energy and the entropy of vacancies near solute atoms are decreased in the vacancy formation energy and vacancy formation entropy.

Consequently, the single-vacancy concentration for dilute alloys can be obtained as the sum of eq. (3-8) and eq.(3-9).

$$C = (1 - Z\, C_S)\; exp\left(-\frac{E_F}{k\,T}\right) exp\left(\frac{S_F}{k}\right) + Z\, C_S\; exp\left(-\frac{E_F}{k\,T}\right) exp\left(\frac{S_F}{k}\right) exp\left(\frac{E_{FB}}{k\,T}\right) exp\left(-\frac{S_B}{k}\right) \quad (3-10)$$

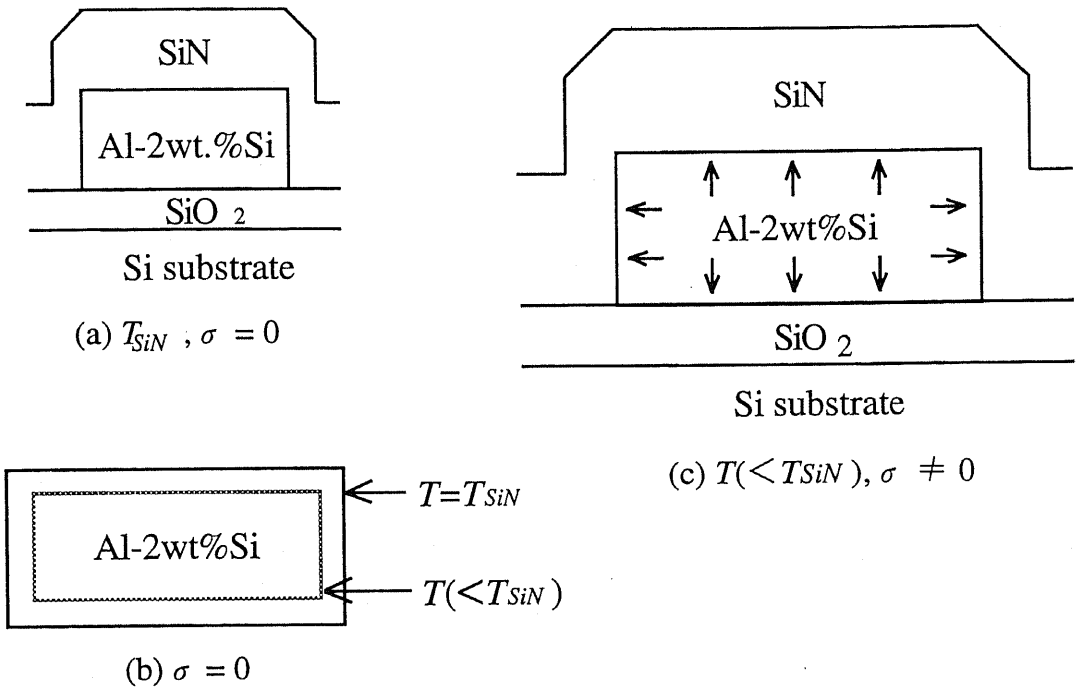


Fig. 3-5. Schematic of the relation between the temperature and the stress in the aluminum interconnection. (a) Cross section of the sample. It is assumed that the stress, σ, in the aluminum interconnection is zero at T_{SiN}. (b) Aluminum interconnection without the passivation and the underlayer is shown by a solid line at T_{SiN}. When the temperature is cooled to a value (T) below T_{SiN}, the aluminum interconnection shrinks without stress, as shown by a dotted line. (c) When the temperature of the sample shown in Fig. 3-5(a) is cooled to T, below T_{SiN}, the aluminum interconnection can not shrink and is subjected to tensile stress.

3-6 Proposal of stress-induced vacancy model

Interconnections on semiconductor devices are usually covered with a passivation layer, as shown in Fig. 3-5(a). Without the underlayer and the passivation layer, the aluminum film would be free from stress at any temperature, as shown in Fig. 3-5(b), so that the vacancy concentration in the interconnections of bulk Al-2wt.%Si can be calculated using eq. (3-10). The strain force in interconnections, however, can not be neglected, when the passivation layer is present, as shown in Fig. 3-5(c), because interconnections restrained by SiN can not shrink upon cooling from T_q. This is attributed to the fact that the thermal expansion coefficient of aluminum is about six times larger than that of SiN at Tq [25-27], Interconnections are subjected to tensile stress owing to this difference.

The free energy of one vacancy under tensile stress, G_V, is defined by [41]

$$G_V = E_F - S_F T + \sigma V . \quad (3-11)$$

Here, stress σ is defined as positive for compressible stress. The tensile stress enhances the generation of vacancies since it probably decreases the vacancy formation energy. The vacancy concentration in this case is given by

$$C = (1 - Z C_S) \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right) + Z C_S \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(\frac{E_{FB}}{kT}\right) \exp\left(-\frac{S_B}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right), \quad (3-12)$$

where σ is the local stress in interconnections and V is the vacancy volume. The stress is defined as positive for compressible stress. Equation (3-12) is a stress-induced vacancy model for dilute alloys.

If pure metals are used to form the interconnections, C_S in eq. (3-12) is zero. Equation (3-12) becomes the vacancy concentration for pure metals with stress, namely

$$C = \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right) . \quad (3-13)$$

Equation (3-13) is a stress-induced vacancy model for pure metals.

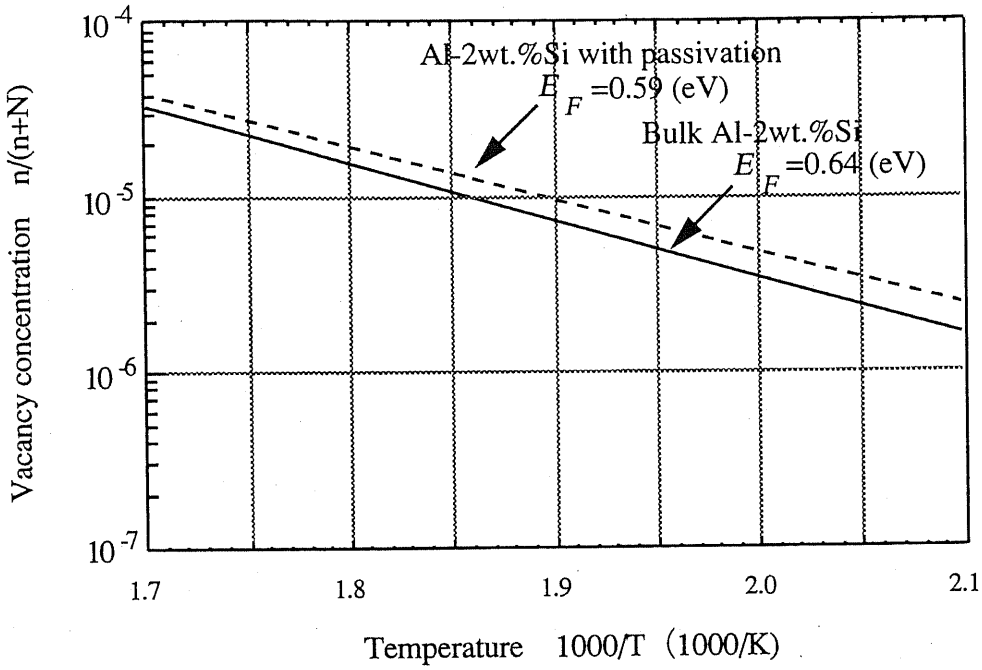


Fig. 3-6. Theoretical calculation of the single-vacancy concentration *n/(n+N)*, where *n* and *N* are the numbers of vacancies and lattice sites, respectively. The vacancy formation energy for bulk Al-2wt.%Si is 0.64 eV and that for the Al-2wt.%Si interconnection with a SiN passivation layer is 0.59 eV.

3-7 Discussion

Using the values E_F = 0.702 eV [38], S_F = 1.69k [38], E_{FB} = 0.07 eV [44], S_B = -1.7k [44], Z = 12 and C_S = 1.9 at% for Al-2wt.%Si, the calculated results of vacancy concentration using eq. (3-10) are shown in Fig. 3-6 by a solid line. The single-vacancy formation energy is obtained as 0.64 eV in the temperature range of 200 to 300 ℃.

Under the assumption that the thermal expansion coefficient of aluminum is isotropic and the interconnection is surrounded only by SiN, σV is estimated from the relation [41]

$$\sigma V = \left(\alpha_{AlSi} - \alpha_{SiN}\right)\left(T_{SiN} - T\right) E_{AlSi} V , \quad (3-14)$$

where E_{AlSi} is Young's modulus of Al-Si alloy and α_{AlSi} and α_{SiN} are the thermal expansion coefficients of Al-Si alloy and SiN, respectively. Substituting eq. (3-14) into eq.

(3-12), one obtains the vacancy concentration in the aluminum interconnection with a passivation layer.

The calculated results obtained using the values $\alpha_{AlSi} = 27.7 \times 10^{-6}$ K^{-1}, $\alpha_{SiN} = 4.8 \times 10^{-6}$ K^{-1} and $E_{AlSi} = 55 \times 10^{9}$ Pa, [25-27] are shown in Fig. 3-6 by a dotted line. Thus the vacancy formation energy for the passivated Al-2wt.%Si interconnections is 0.59 eV in the temperature range of 200 to 300 ℃.

This activation energy is smaller than that of bulk Al-2wt.%Si of 0.64 eV. The difference in the vacancy formation energy, $\triangle E_F = 0.05$ eV, is caused by the strain force in Al-2wt.%Si interconnections. The calculated result of 0.59 eV agrees with the experimental result of 0.60 ± 0.07 eV shown in Fig. 3-4.

3-8 Conclusion

The single-vacancy formation energy in Al-2wt.%Si interconnections on semiconductor devices with a SiN passivation layer is studied using the quenching technique. We find that the single-vacancy formation energy is 0.60 eV in the temperature range of 200 to 300 ℃, where the interconnection is of 0.8 um thickness, 3.0 um width and 0.5 m length.

The theoretical calculation of the single-vacancy formation energy based on the stress-induced vacancy model is 0.64 eV for bulk Al-2wt.%Si, and 0.59 eV for the Al-2wt.%Si interconnection with the SiN passivation layer. This difference is attributed to the fact that the thermal expansion coefficient of Al-Si is larger than that of SiN, so that the interconnection is tensiled due to the difference in expansion. The tensile force enhances the generation of vacancies. The theoretical calculation indicates a vacancy formation energy of 0.59 eV in the case of the presence of tensile stress, which is in agreement with the experimental result of 0.60 ± 0.07 eV.

CHAPTER 4.

VACANCY DISTRIBUTION

4-1 Introduction

The vacancy generation in interconnections is enhanced by thermal stress due to the difference in thermal expansion between interconnections and passivation layers, as described in the previous chapter; therefore the stress distribution in interconnections is a key issue in clarifying the mechanism of stress-induced migration. The overall stress in interconnections can be measured via X-ray diffraction techniques [8,13,14,17-21,28] or wafer curvature measurements through laser-scanning techniques [15,16,22,23]. These techniques, however, can not be used to measure the microscopic stress distribution in interconnections on semiconductor devices, because of the relatively large spot sizes of the X-ray and laser beams. Instead of these techniques, a thermal stress simulation based on a finite-element method (FEM) is used to estimate the stress distribution in microscopic interconnections on semiconductor devices [3,24-27].

In this chapter, the vacancy distribution in the interconnections is calculated by combining the thermal stress simulation based on FEM and the stress-induced vacancy model described in the previous chapter .

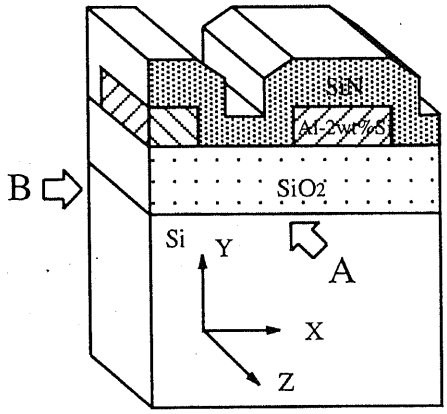


Fig. 4-1. Schematics of the structural model for FEM. Only the right half of the model is shown, because of the symmetrical-geometry.

4-2 Thermal stress simulation model

The thermal stress in interconnections is influenced by the sample structure. The cross section of these interconnection used in the thermal stress simulation is illustrated in Fig. 4-1. Here, Al-2wt.%Si interconnections are deposited on a thermally oxidized silicon layer 1.4 um thick and covered with a SiN passivation layer 1.0 um thick. The structure is similar to the experimental sample used in chapter 2. The boundaries A and B have a symmetry condition for symmetrical geometries, and the bottom boundary is restrained. The silicon substrate thickness was reduced to 10 um, although the actual thickness is 500 um; the author found that this reduction induces a maximum error of 2% for the stress calculation. The strains, $\triangle \varepsilon_x$, and stresses, $\triangle \sigma_x$, in the x-direction are expressed as [45,46]

$$\Delta\varepsilon_x = \alpha\,\Delta T + \frac{\Delta\sigma_x}{E} - \frac{\nu\,\Delta\sigma_y}{E} - \frac{\nu\,\Delta\sigma_z}{E} \qquad (4-1)$$

$$\Delta\sigma_x = \frac{E(1-\nu)}{(1+\nu)(1-2\nu)}\Delta\varepsilon_x + \frac{E\nu}{(1+\nu)(1-2\nu)}\left(\Delta\varepsilon_y + \Delta\varepsilon_z\right), \qquad (4-2)$$

where $\triangle \varepsilon_x$, $\triangle \varepsilon_y$ and $\triangle \varepsilon_z$ are the thermal strain in the x-, y- and z-directions, respectively.

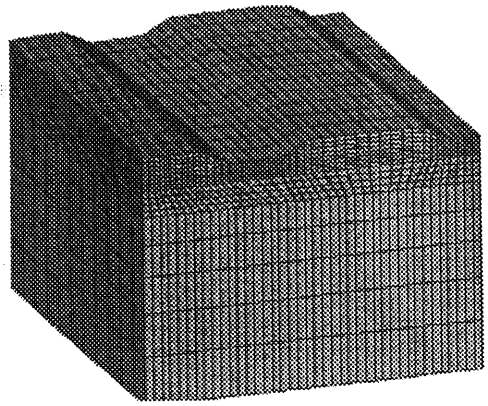


Fig. 4-2. Schematic of hexahedral meshes

Table 4-1 Summary of material properties

Property / Material		Temperature (℃) 20	100	150	200	260	320	370
Young's modulus								
Al-Si	(GPa)	69	68	66	62	55	49	42
SiN		250	250	250	250	250	250	250
SiO2		69	69	69	69	69	69	69
Si		130	130	130	130	130	130	130
Thermal expansion coefficient								
Al-Si	(10^{-6}/K)	22.5	24.2	25.3	26.5	27.7	28.9	30.0
SiN		2.2	3.4	4.0	4.4	4.8	5.2	5.6
SiO2		0.6	0.6	0.6	0.6	0.6	0.6	0.6
Si		2.3	3.4	4.0	4.4	4.8	5.2	5.6
Poisson's ratio								
Al-Si		0.33	0.33	0.33	0.33	0.33	0.33	0.33
SiN		0.2	0.2	0.2	0.2	0.2	0.2	0.2
SiO2		0.17	0.17	0.17	0.17	0.17	0.17	0.17
Si		0.28	0.28	0.28	0.28	0.28	0.28	0.28

$\triangle \sigma_x$, $\triangle \sigma_y$ and $\triangle \sigma_z$ are the thermal stress in the x-, y- and z-directions, respectively. α is the thermal expansion coefficient, ν is Poisson's ratio, E is Young's modulus and T is the absolute temperature. $\triangle T$ is defined as (T_{SiN} - T), where T_{SiN} is the SiN deposition temperature. The stresses and strains for the y- and z-directions are expressed in a similar manner.

The above-mentioned relations apply to the conventional thermal stress simulation based on FEM [47] in three dimensions using hexahedral meshes, as shown in Fig. 4-2. The material properties used in this simulation are Young's modulus, Poisson's ratio and thermal expansion coefficient, which are summarized in Table 4-1 with temperature dependence [25-27]. These figures are the values for bulk materials. Although the materials used in semiconductor devices are thin films, the properties of the thin films are not exactly known, and so the properties of the bulk were used in this simulation. The stress simulation was carried out assuming that (1) materials used in the simulation are isotropic and homogeneous, (2) the stress in interconnections is zero at a deposition temperature of T_{SiN} and (3) stress relaxation does not occur.

4-3 Stress-induced vacancy model

In the previous chapter, for Al-2wt.%Si interconnections on semiconductor devices, we demonstrated that the stress-induced vacancy model for a dilute alloy as a relation between the stress and the vacancy concentration was

$$C=(1-Z\,C_S)\,exp\left(-\frac{E_F}{kT}\right)exp\left(\frac{S_F}{k}\right)\,exp\left(-\frac{\sigma V}{kT}\right)$$
$$+\,Z\,C_S\,exp\left(-\frac{E_F}{kT}\right)exp\left(\frac{S_F}{k}\right)exp\left(\frac{E_{FB}}{kT}\right)exp\left(-\frac{S_B}{k}\right)\,exp\left(-\frac{\sigma V}{kT}\right). \quad (4-3)$$

Here, C is the vacancy concentration, Z is the number of the first-nearest neighbors to the vacant site, C_S is the solute concentration, E_{FB} is the binding energy between vacancies and solute atoms, S_B is the entropy of vacancies near solute atoms, E_F is the single-vacancy formation energy, S_F is the vacancy formation entropy, V is the vacancy volume and σ is the local stress in interconnections. σ is defined as positive for a compressive stress.

In this chapter, we calculated the vacancy concentration distribution in interconnections using eq. (4-3), where stress σ was obtained from the results of the thermal stress simulation.

4-4 Calculation results

The maximal axial stresses in Al-2wt.%Si interconnections upon cooling from T_{SiN} are shown in Fig. 4-3; Figs. 4-3(a), (b) and (c) show the maximal stresses in the x-, y- and z-directions, respectively, for 0.8-um-thick interconnections with width ranging from 0.8 to 2.0 um. Figures 4-3(d), (e) and (f) show the maximal stresses in the x-, y- and z-directions, respectively, for 1.5-um-wide interconnections with thickness ranging from 0.2 to 0.8 um. The stress is considered as positive for tensile stresses.

The maximal stresses in the x- and y-directions varied depending on the width and the thickness, while the maximal stress in the z-direction was almost constant for all the various values of width and thickness considered. The maximal stress values in the y-direction were the smallest as compared to other directions.

Figures 4-4 to 4-9 show axial-stress distributions in the cross section. The interconnection width was varied from 0.8 to 2.0 um, thickness was varied from 0.2 to 0.8 um. Only the right half is illustrated because of the symmetric geometry. The maximal stress for the y- and z-direction axial-stress occurred near the sidewalls, and the x-direction axial-stress was it maximum at the top-center except for 0.2 um width. The axial-stress distribution for the other samples also showed qualitatively, similar distributions.

The stress σ in interconnections is composed of three axial-stresses, as shown in Fig. 4-3, along with three shear stresses [48,49] which are not illustrated in this thesis. However, eq. (4-3) assumes hydrostatic stress described as σV work. Therefore, we employed an equivalent of the stress value which is the mean value of the three principal stresses calculated from the six stresses values obtained in the simulation.

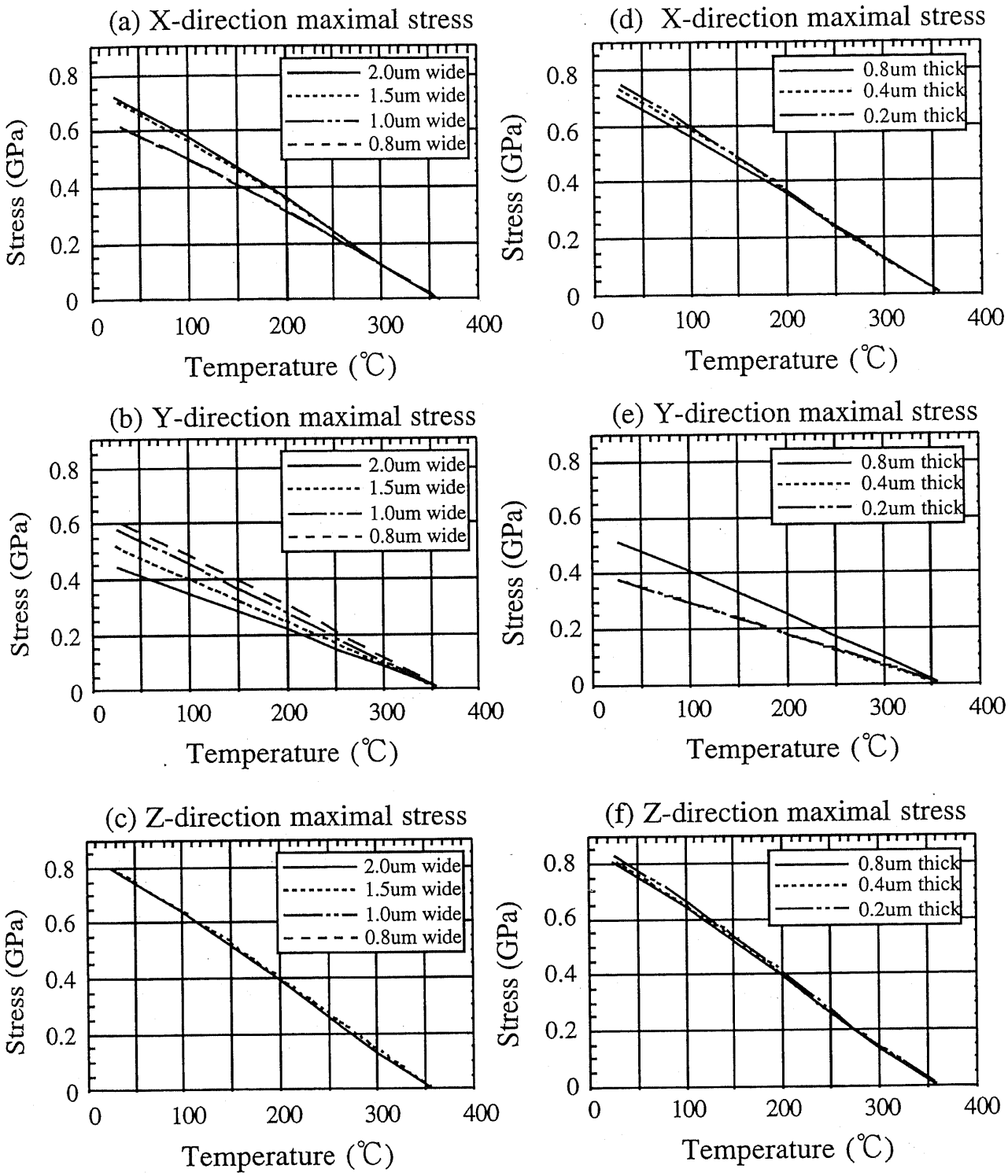


Fig. 4-3. Calculated maximal axis stress in interconnections. Figures 4-3(a) to (c) show the maximal stress in interconnections for 0.8-um-thick interconnections with width of 0.8 to 2.0 um. Figures 4-3(d) to (f) show the maximal stress in interconnections for 1.5-um-width interconnections with thickness of 0.2 to 0.8 um. The sign of stresses is positive for a tensile stress.

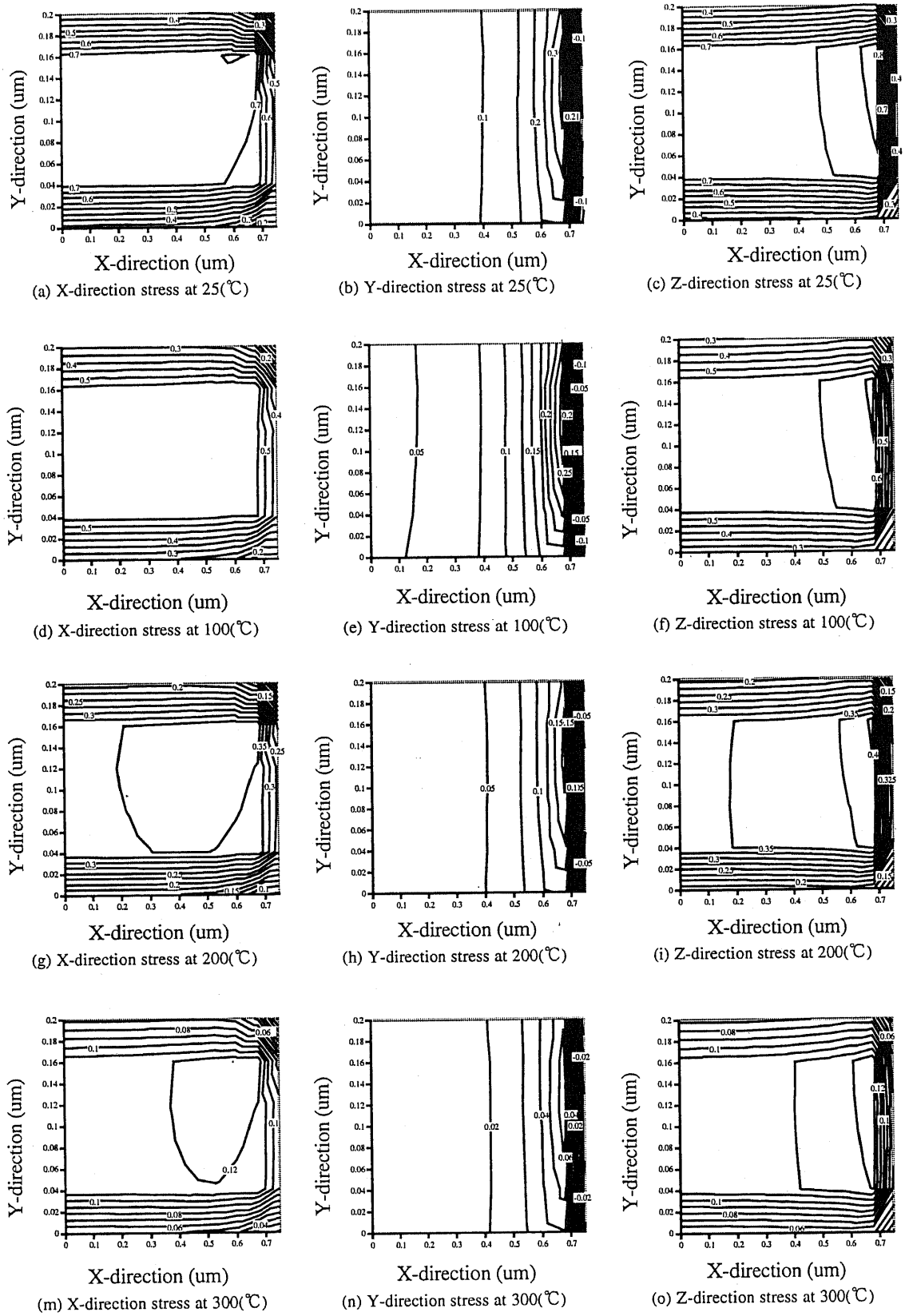


Fig. 4-4. The calculated x-, y- and z-direction stress distributions in the interconnection with 1.5 um width and 0.2 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

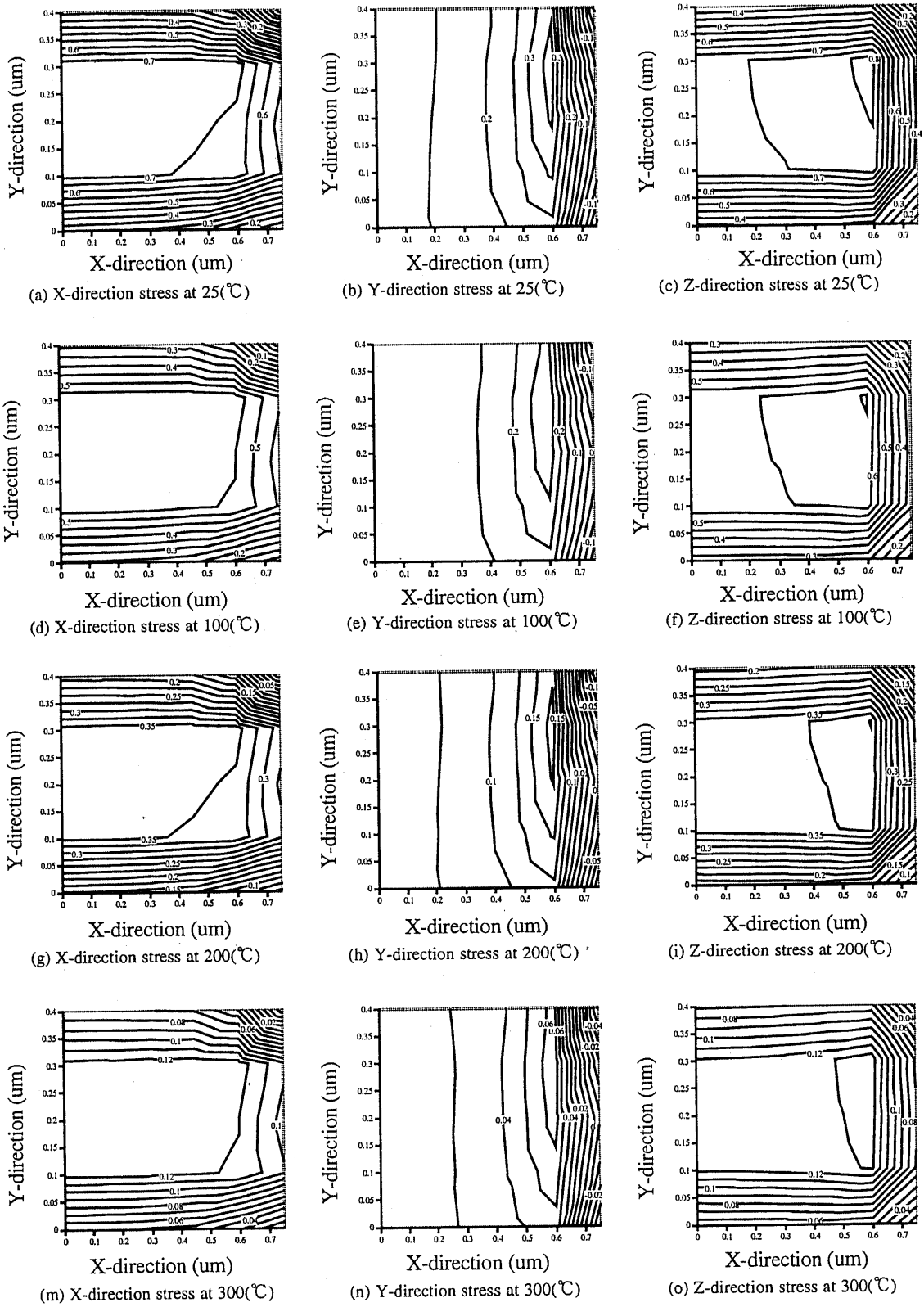


Fig. 4-5. The calculated x-, y- and z-direction stress distributions in the interconnection with 1.5 um width and 0.4 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

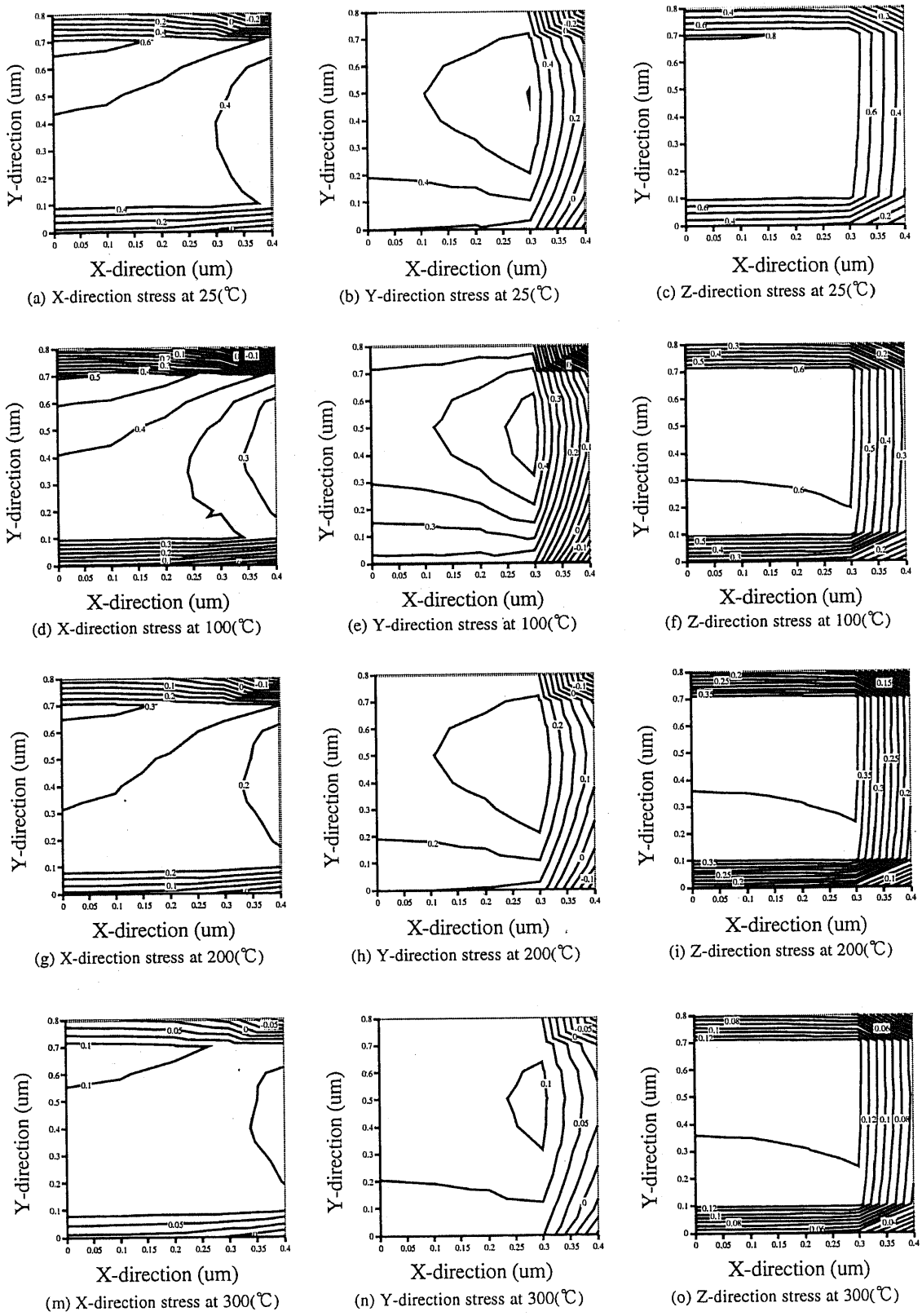


Fig. 4-6. The calculated x-, y- and z-direction stress distributions in the interconnection with 0.8 um width and 0.8 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

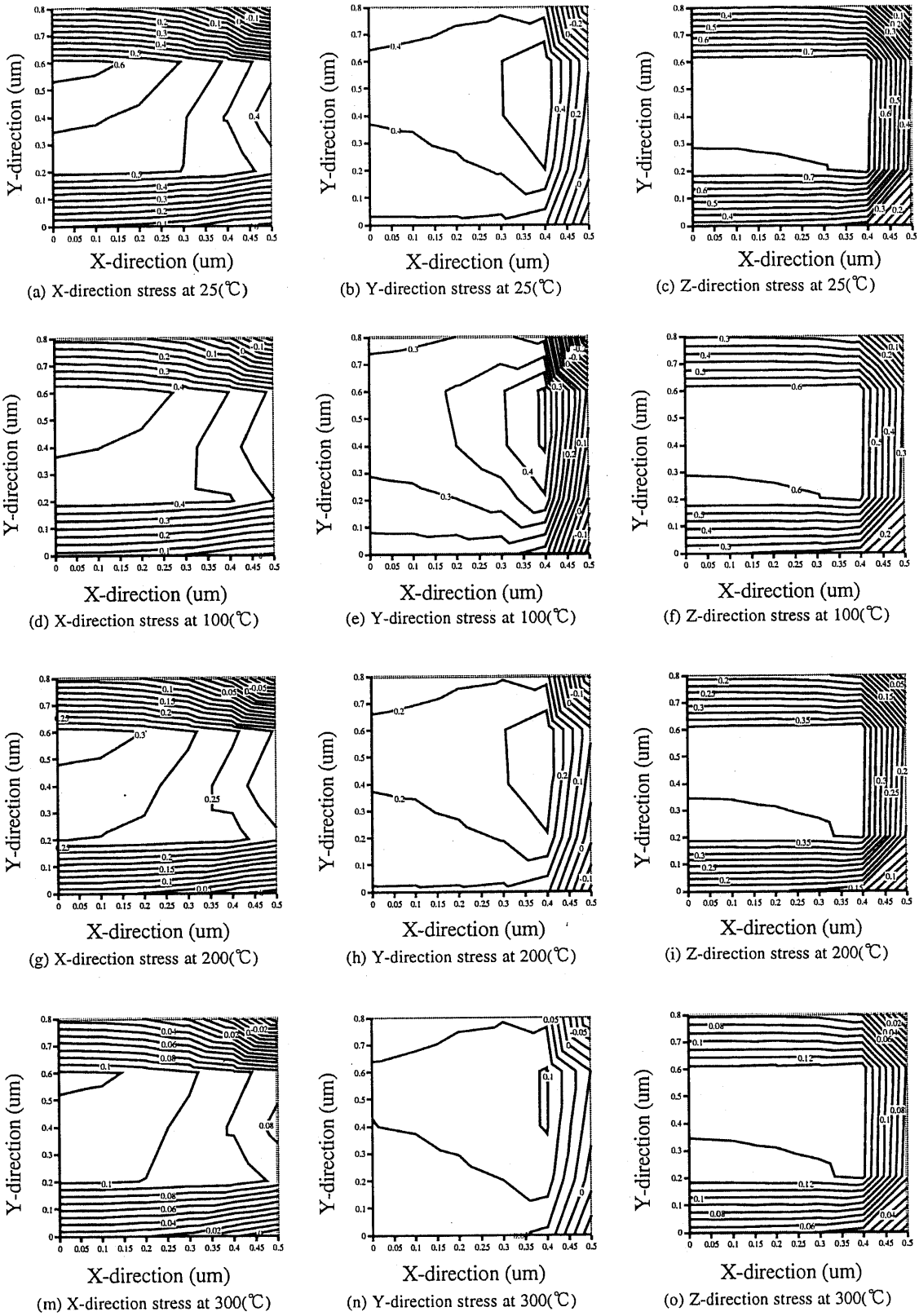


Fig. 4-7. The calculated x-, y- and z-direction stress distributions in the interconnection with 1.0 um width and 0.8 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

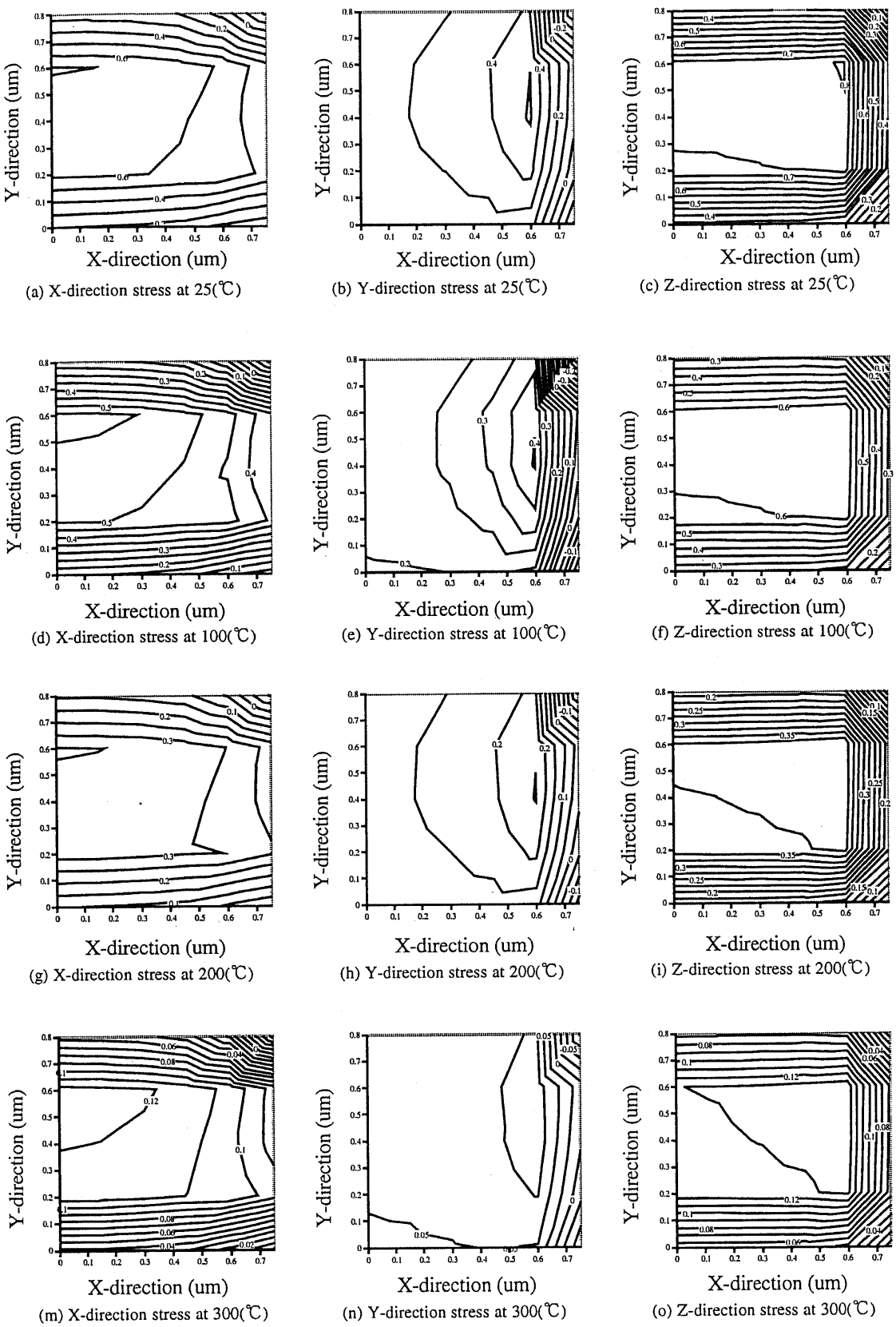


Fig. 4-8. The calculated x-, y- and z-direction stress distributions in the interconnection with 1.5 um width and 0.8 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

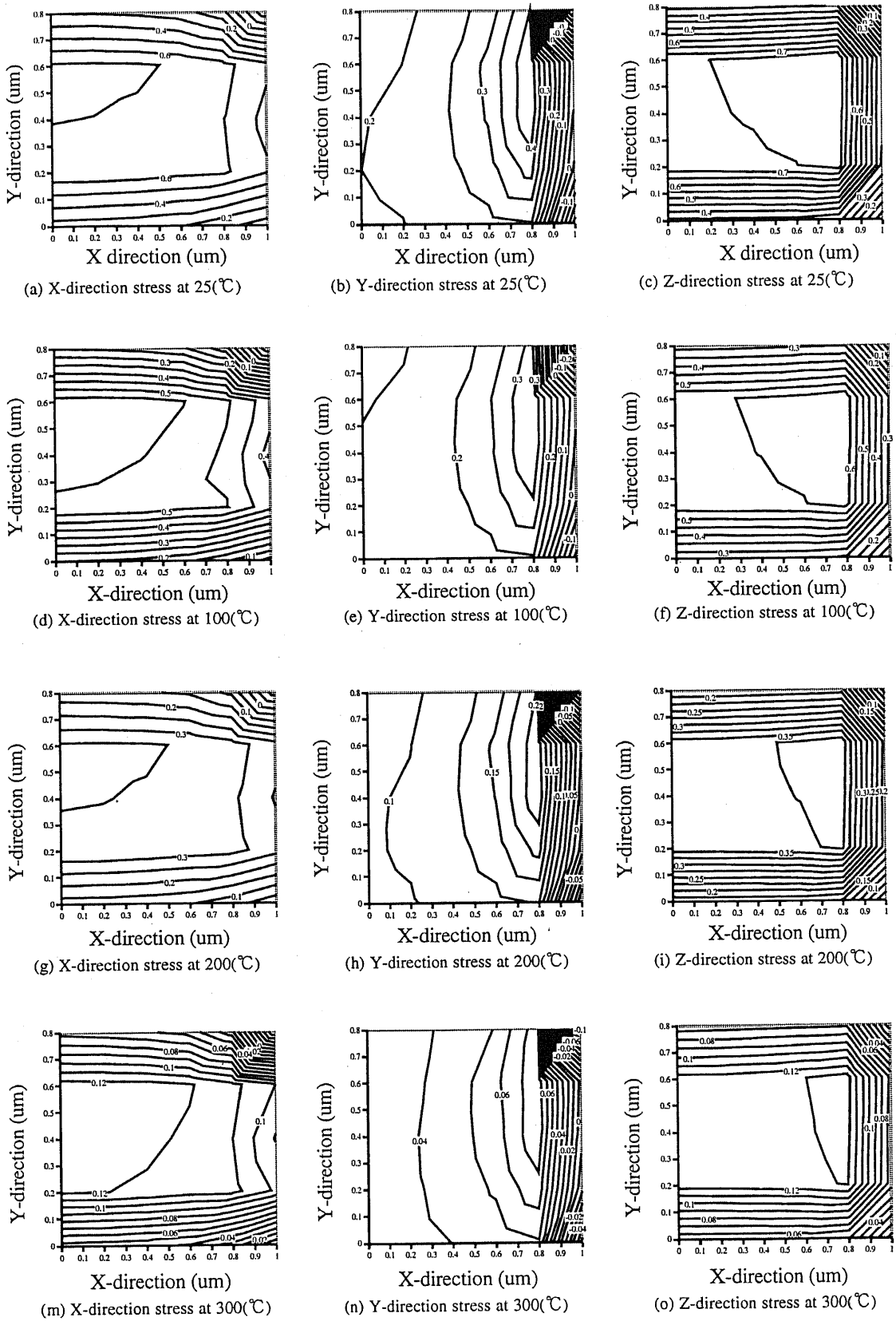


Fig. 4-9. The calculated x-, y- and z-direction stress distributions in the interconnection with 2.0 um width and 0.8 um thickness. Only the right half of the interconnection is shown, because of the symmetric geometry. The sign of stress is positive for a tensile stress. Stress unit is GPa.

Using the above approximation, we calculated the distributions of vacancy concentration from the stress distributions. The equivalent stress distribution and the vacancy concentration are illustrated in Figs. 4-10 to 4-21. The interconnection width was varied from 0.8 to 2.0 um, thickness was varied from 0.2 to 0.8 um. Here, E_F is 0.702 eV [38], S_F is $1.69k$ [38], E_{FB} is 0.07 eV [44], S_B is $-1.7k$ [44], Z is 12, C_S is 1.9 at% and the vacancy volume V is assumed to be the Al atomic volume without stress.

The vacancy distribution is similar to the stress distribution, as determined from eq. (4-3). The vacancies and stress in the interconnections are concentrated near the sidewalls. At the corners, the vacancy concentration is minimum and the stress is compressible. The gradients of stress and vacancy concentration are directed toward the corners and sidewalls in interconnections. These calculated results indicate that voids are formed by the stress-induced migration at corners and sidewalls in interconnections, because voids are generated as a result of a vacancy accumulation. Void formation and growth, however, must be considered that vacancies migrate to vacancy sinks. The relation between the vacancy migration and voids, vacancy sinks, will be discussed in chapter 6.

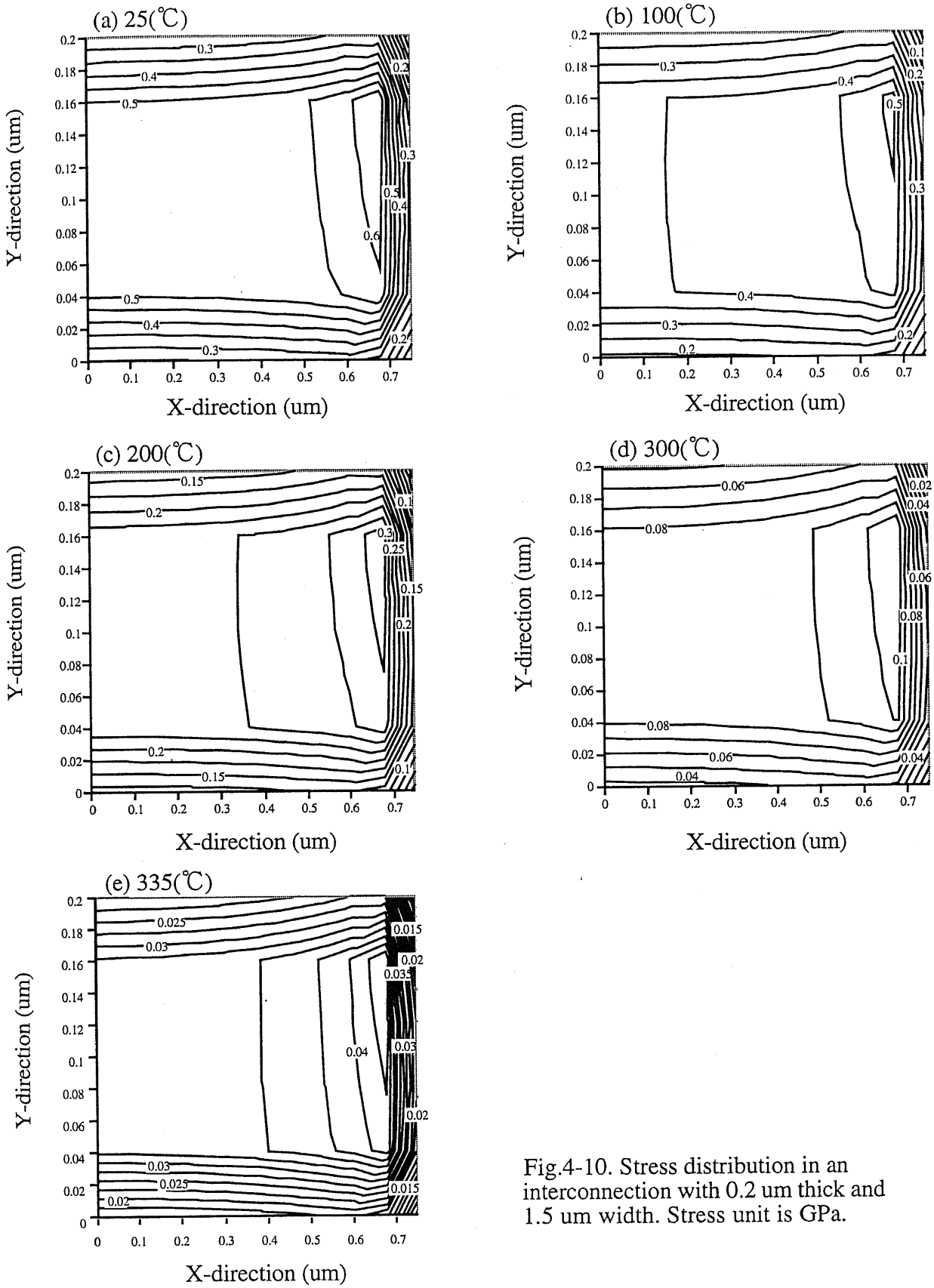


Fig.4-10. Stress distribution in an interconnection with 0.2 um thick and 1.5 um width. Stress unit is GPa.

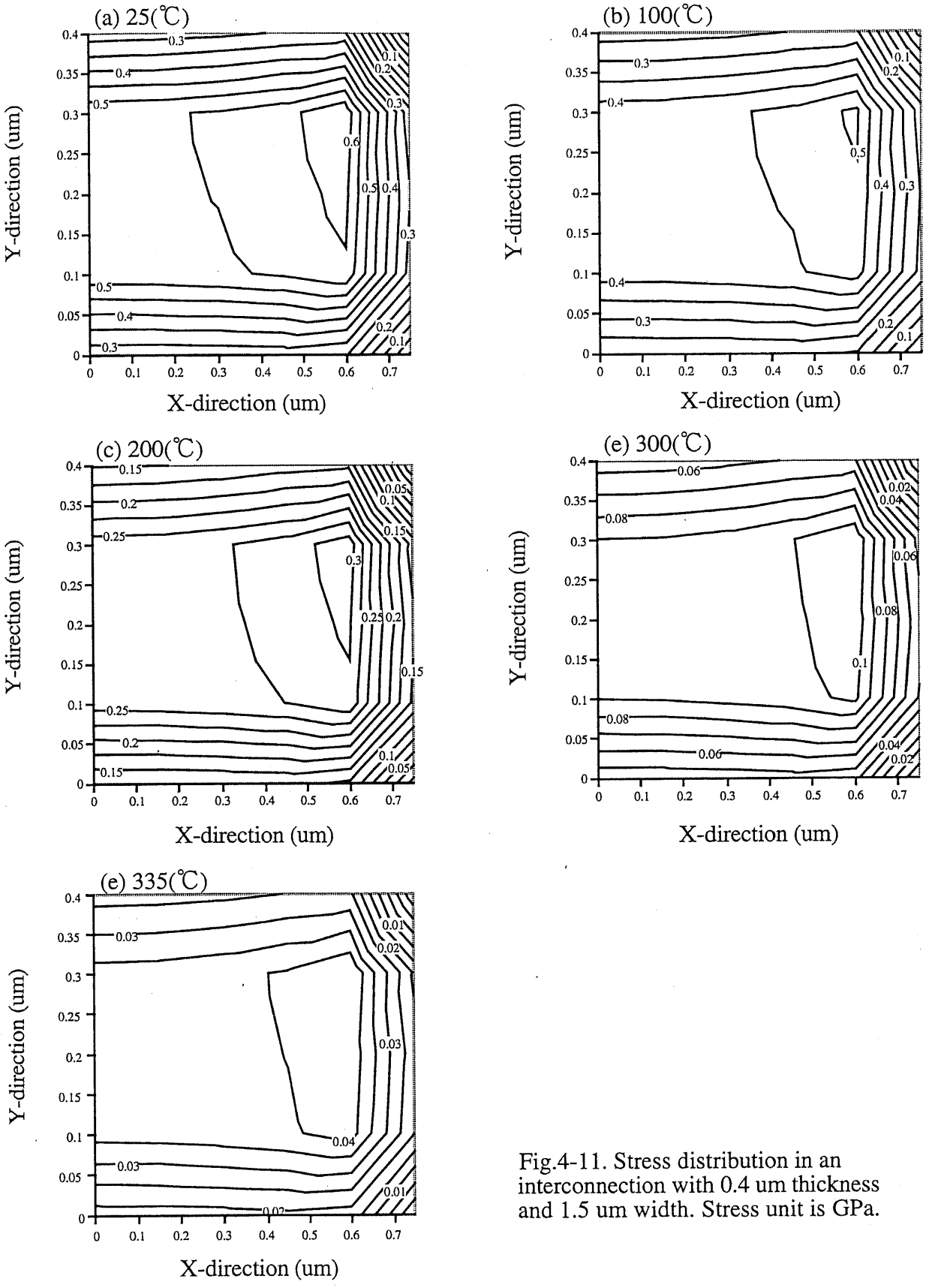


Fig.4-11. Stress distribution in an interconnection with 0.4 um thickness and 1.5 um width. Stress unit is GPa.

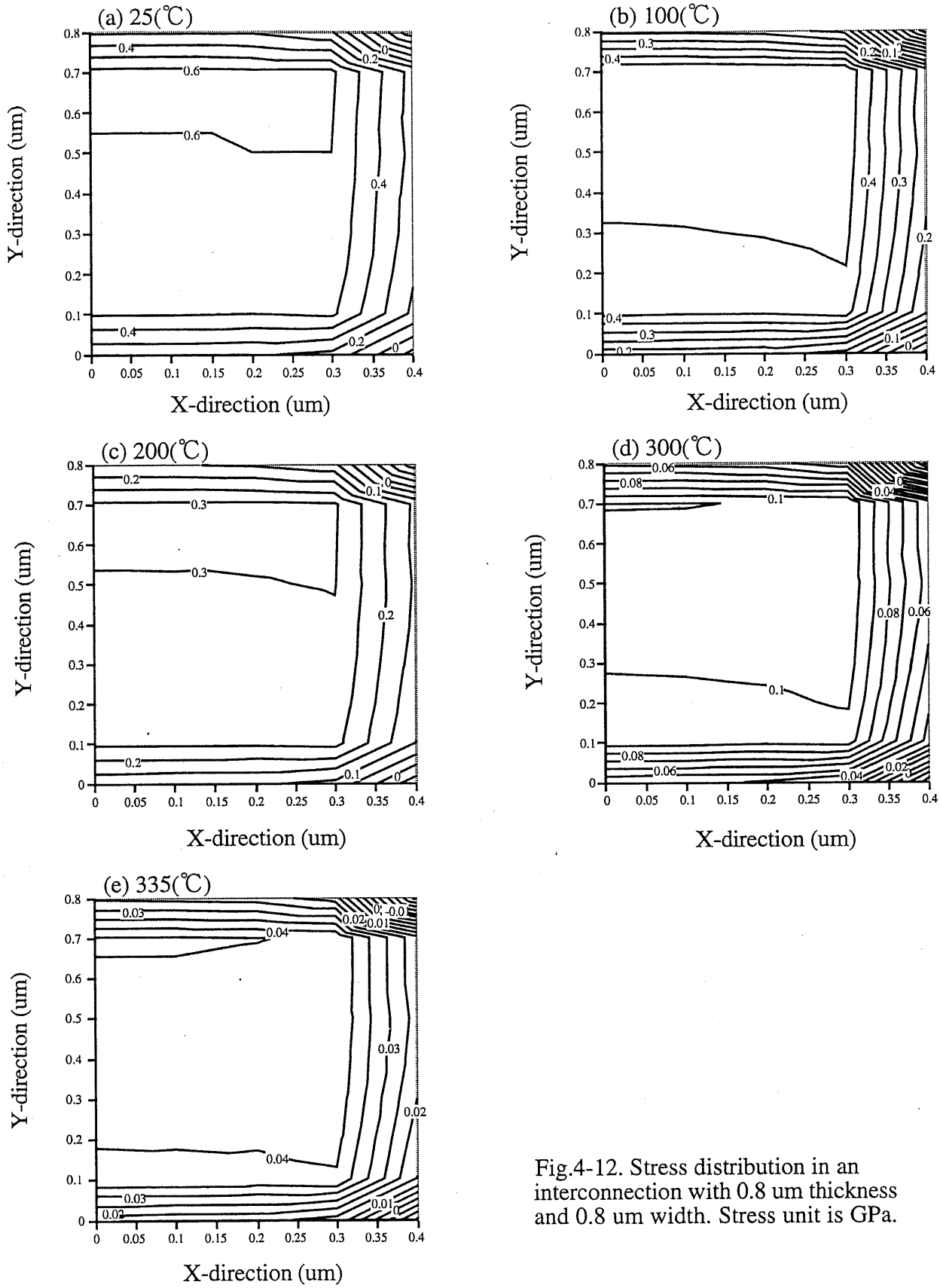


Fig.4-12. Stress distribution in an interconnection with 0.8 um thickness and 0.8 um width. Stress unit is GPa.

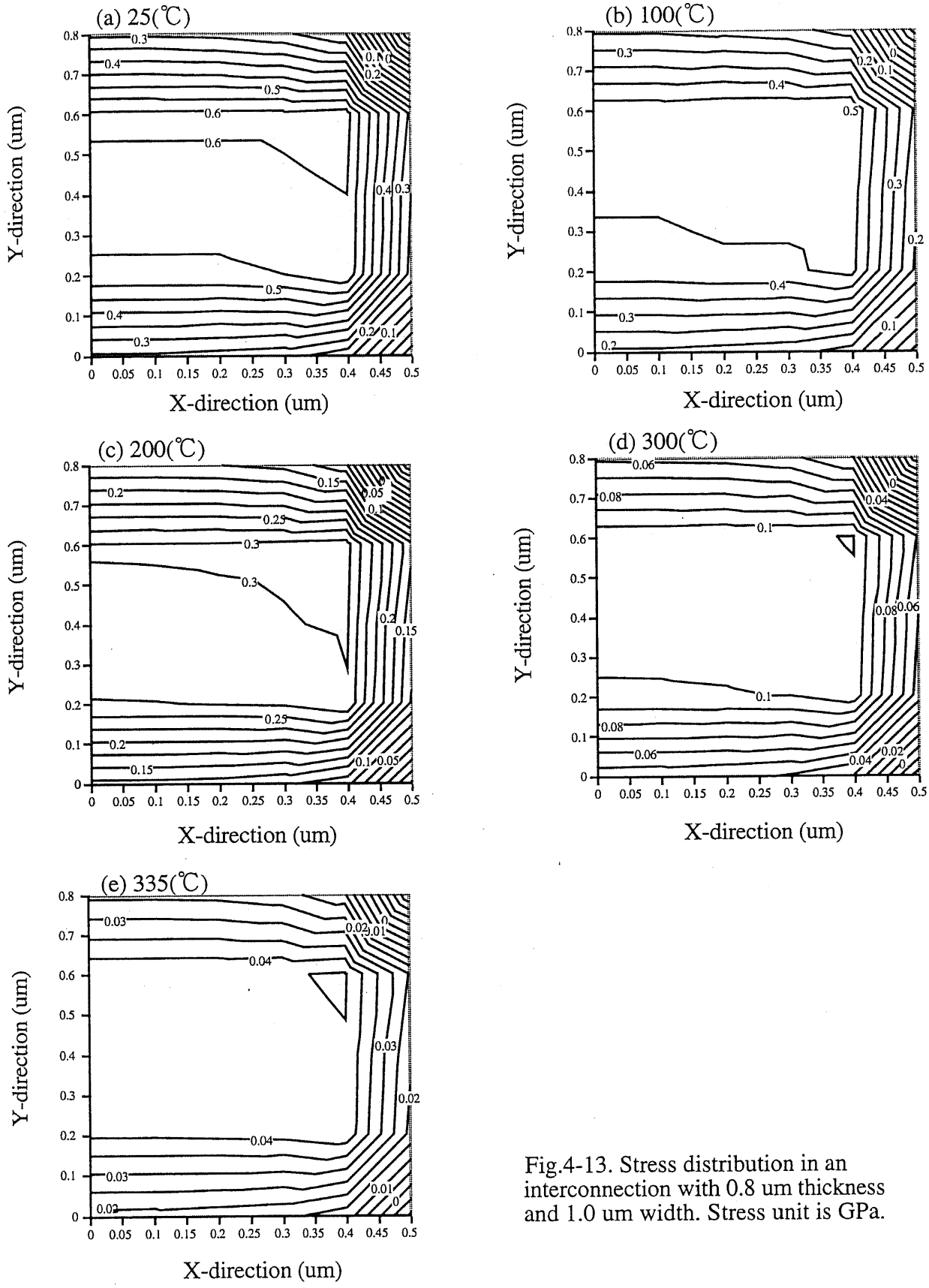


Fig.4-13. Stress distribution in an interconnection with 0.8 um thickness and 1.0 um width. Stress unit is GPa.

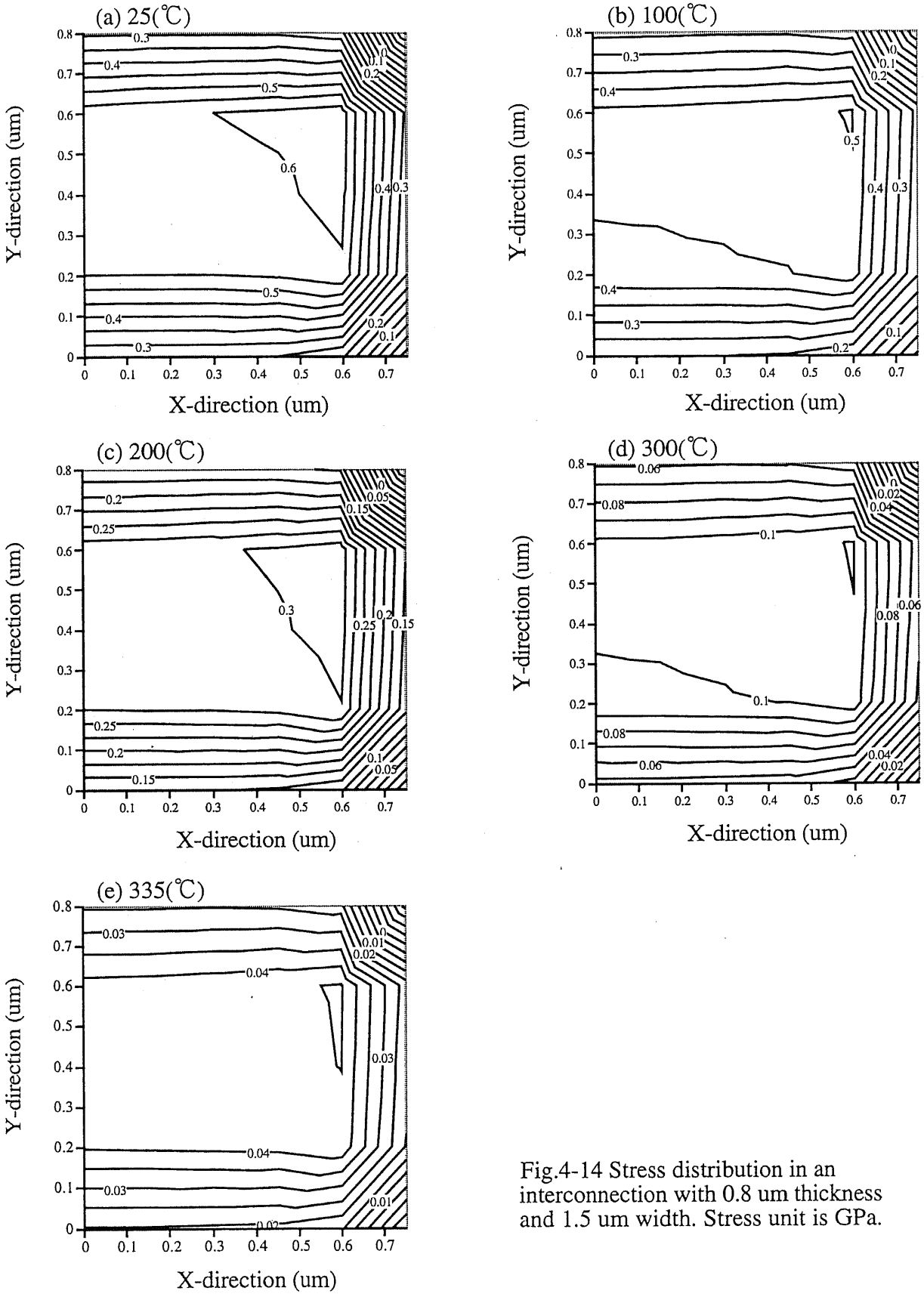


Fig.4-14 Stress distribution in an interconnection with 0.8 um thickness and 1.5 um width. Stress unit is GPa.

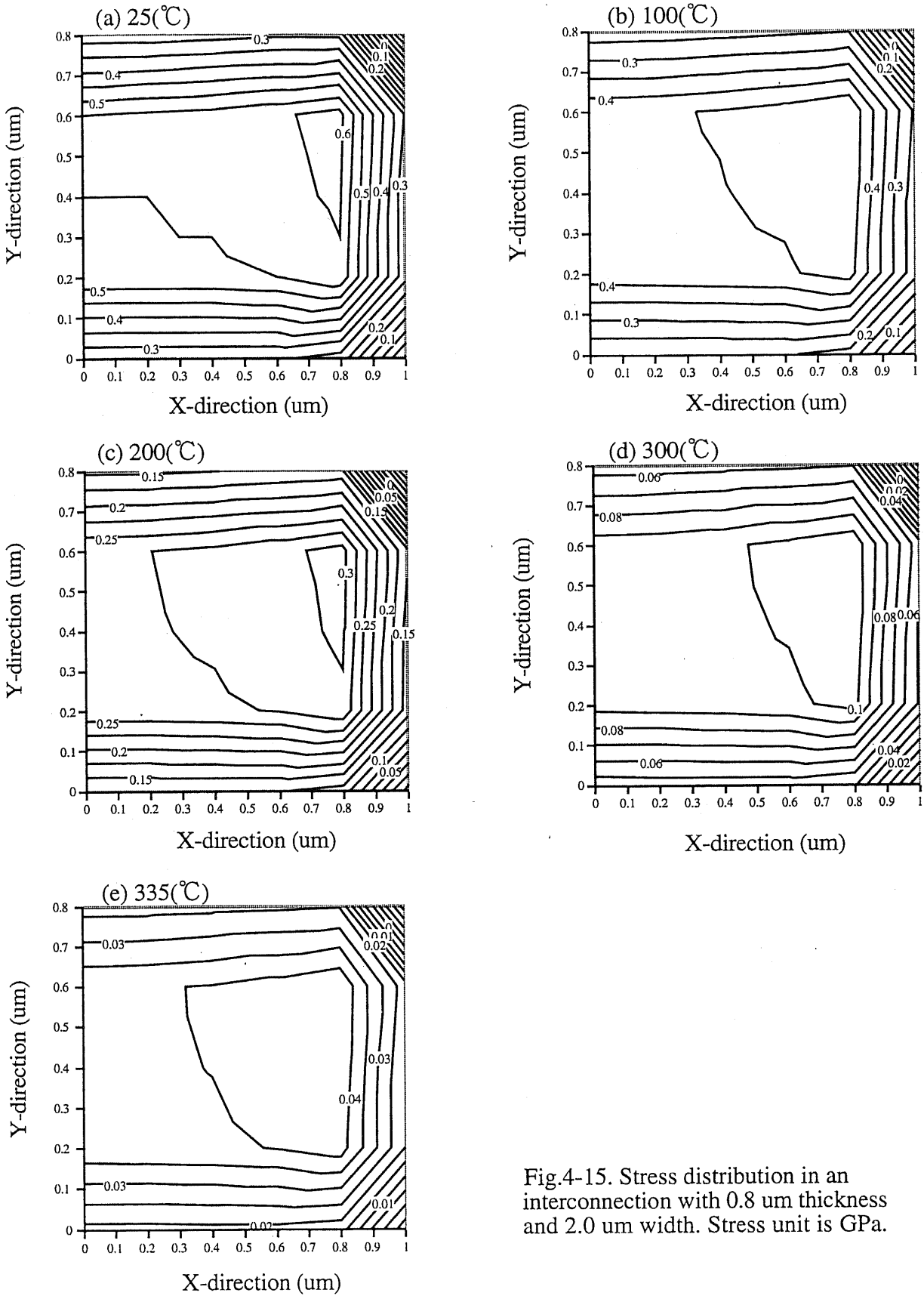


Fig.4-15. Stress distribution in an interconnection with 0.8 um thickness and 2.0 um width. Stress unit is GPa.

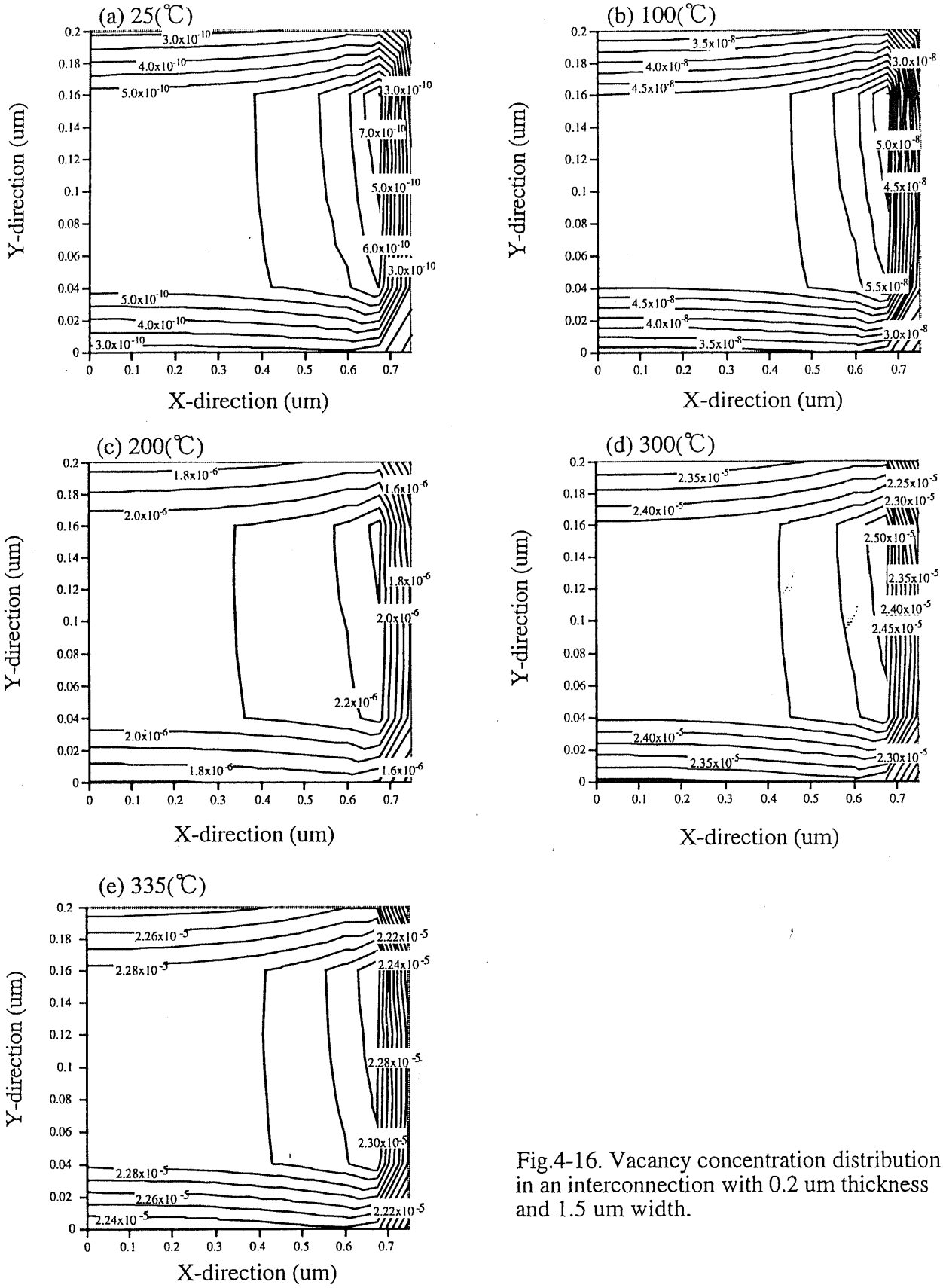


Fig.4-16. Vacancy concentration distribution in an interconnection with 0.2 um thickness and 1.5 um width.

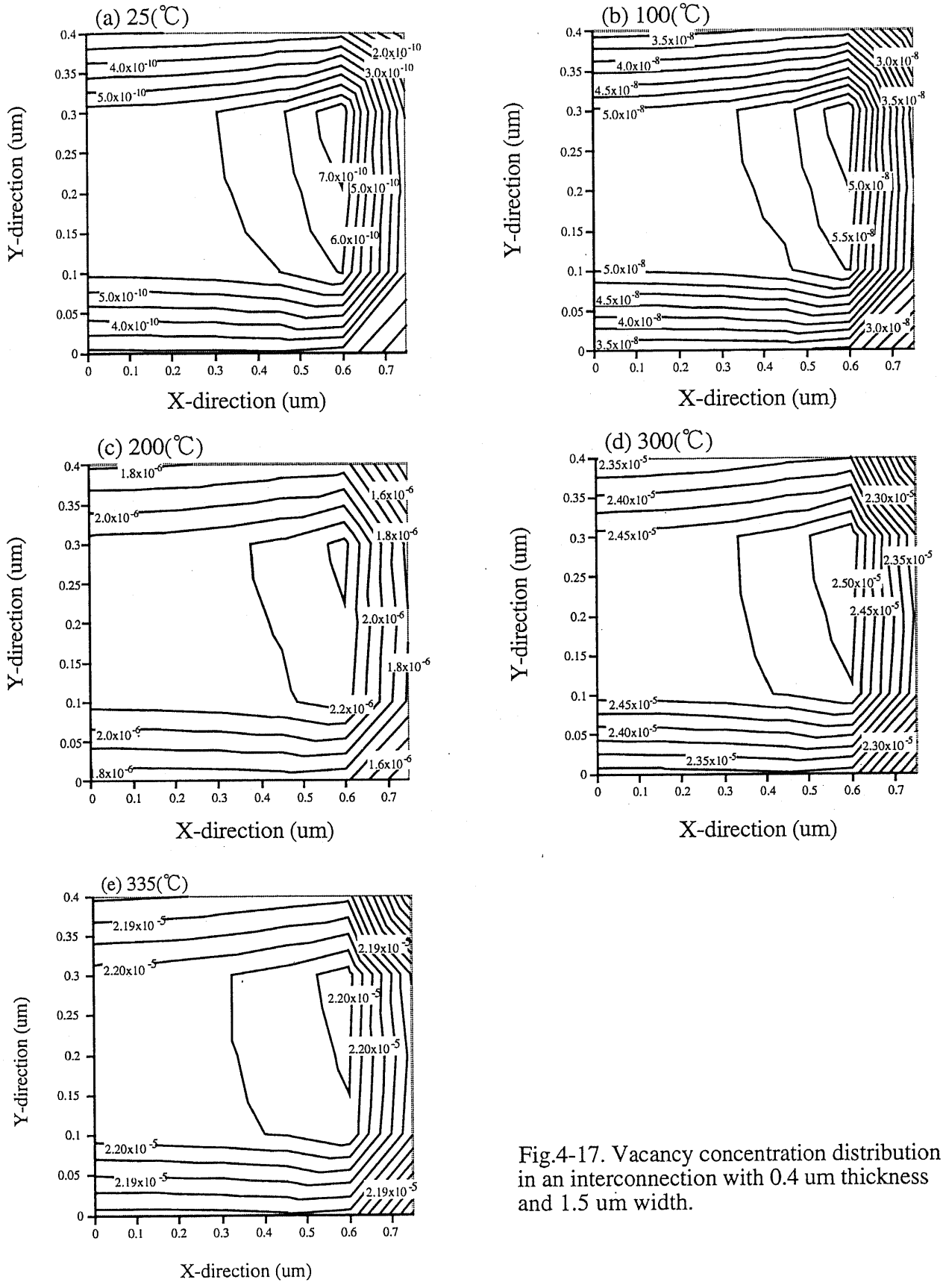


Fig.4-17. Vacancy concentration distribution in an interconnection with 0.4 um thickness and 1.5 um width.

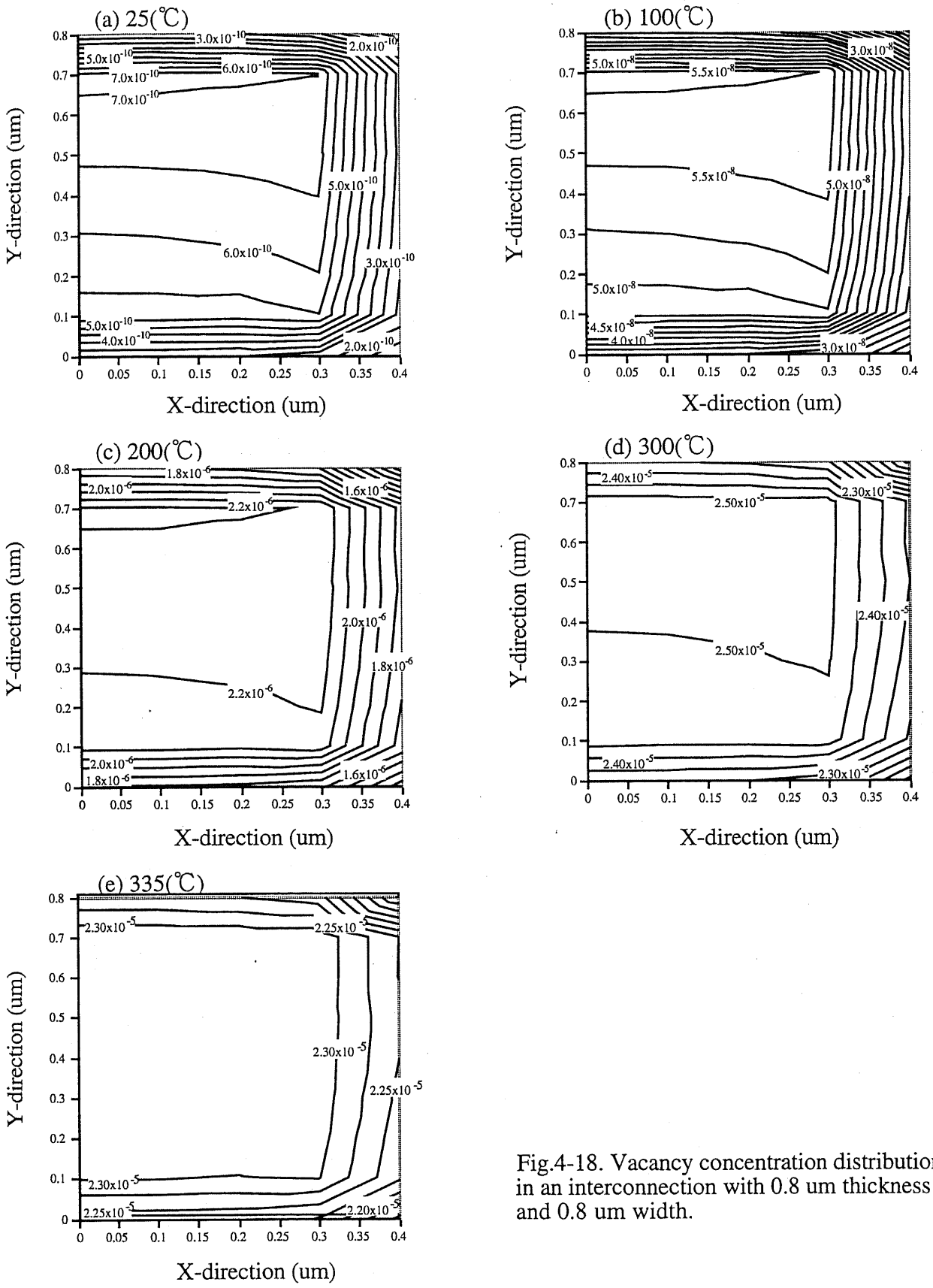


Fig.4-18. Vacancy concentration distribution in an interconnection with 0.8 um thickness and 0.8 um width.

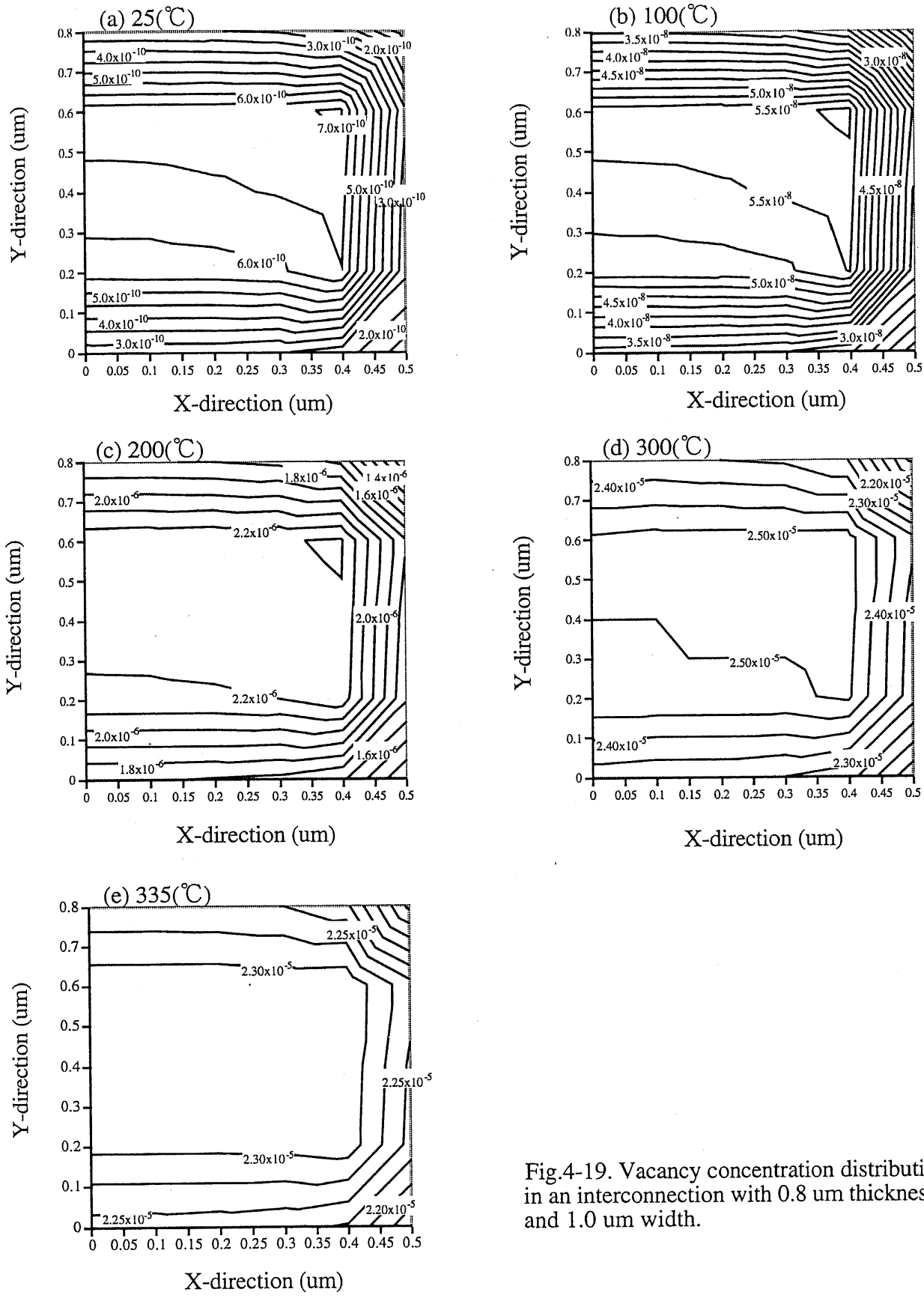


Fig.4-19. Vacancy concentration distribution in an interconnection with 0.8 um thickness and 1.0 um width.

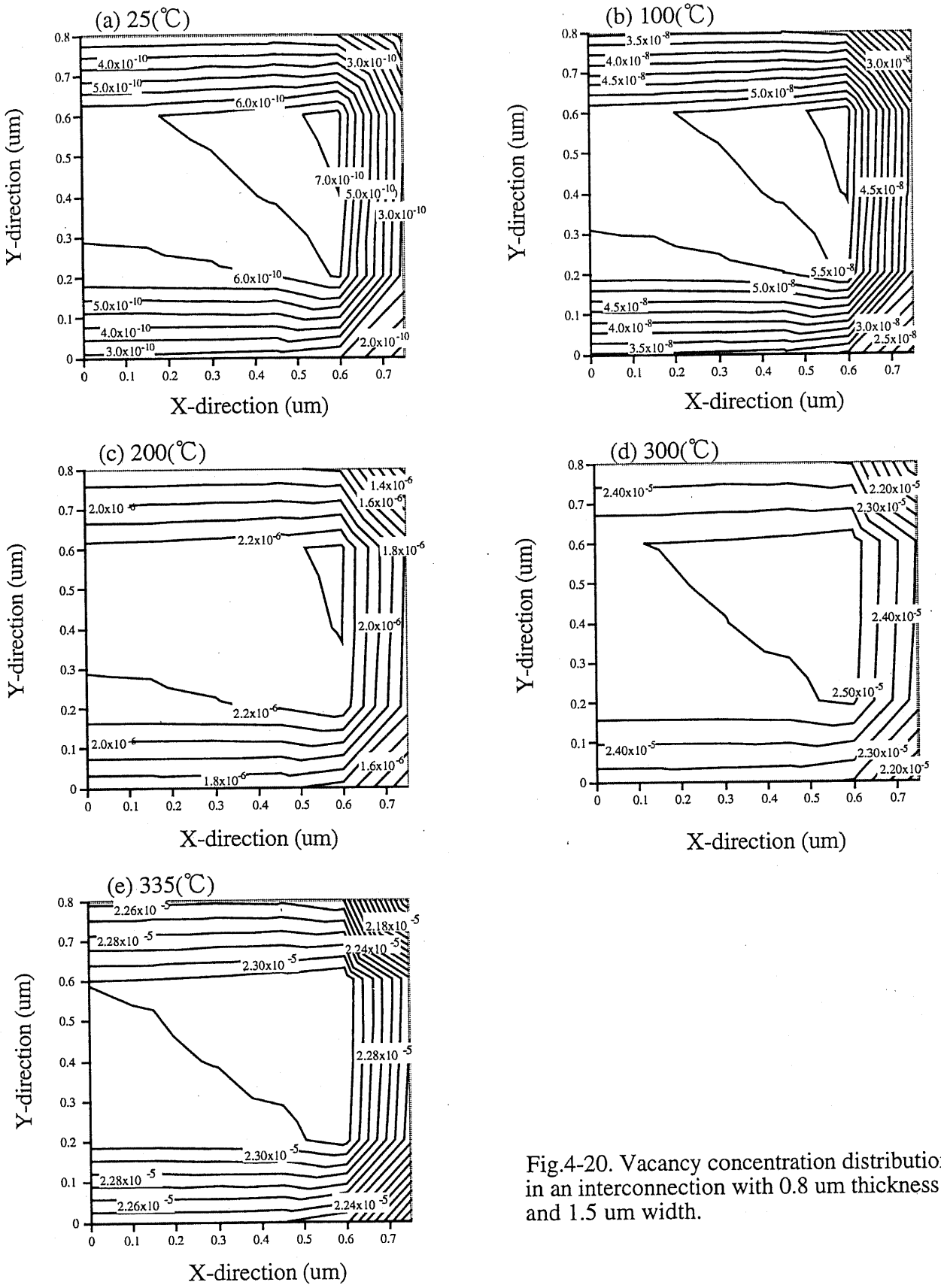


Fig.4-20. Vacancy concentration distribution in an interconnection with 0.8 um thickness and 1.5 um width.

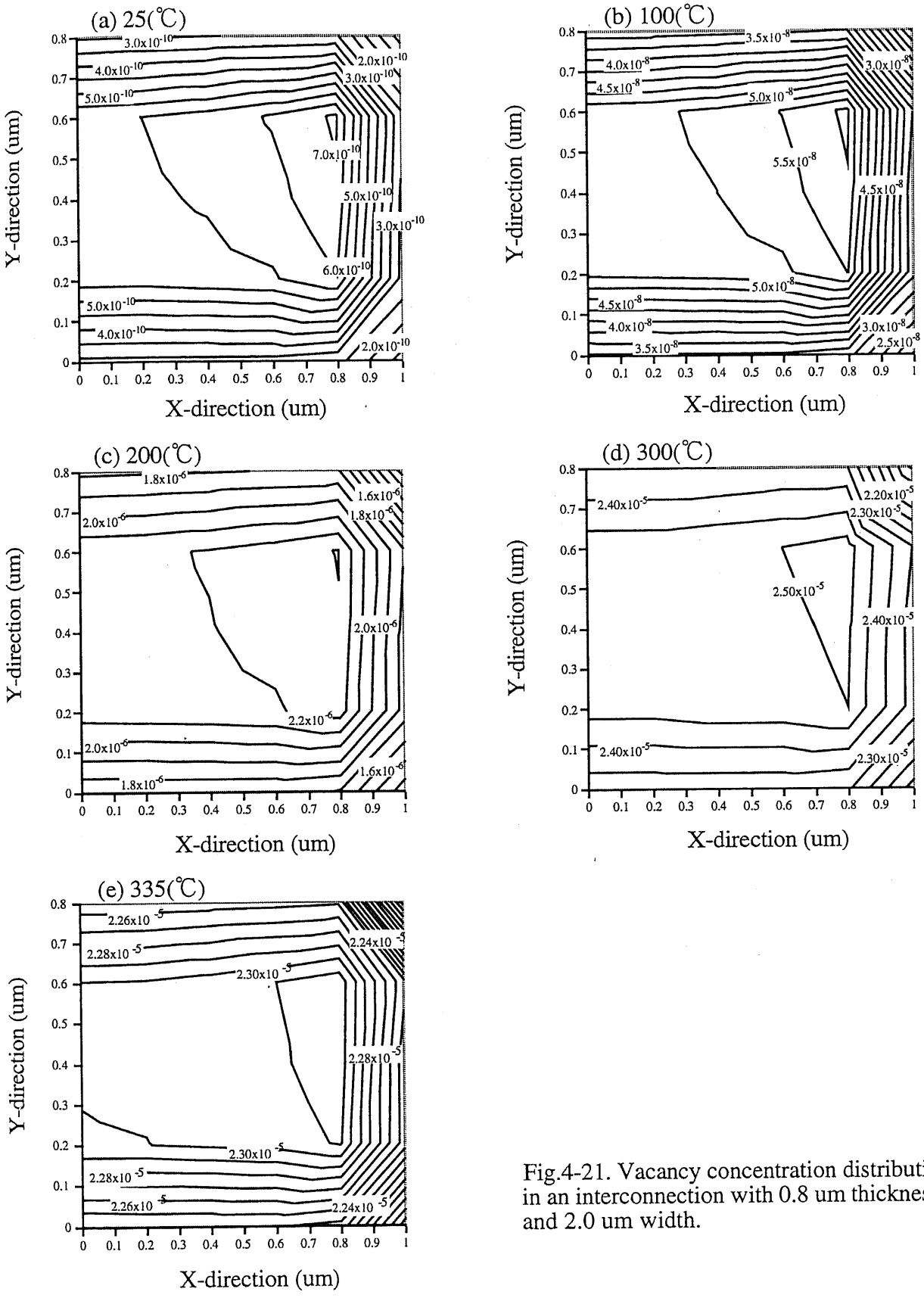


Fig.4-21. Vacancy concentration distribution in an interconnection with 0.8 um thickness and 2.0 um width.

4-5 Conclusion

The vacancy distribution in Al-2wt.%Si interconnections covered with a SiN passivation layer on semiconductor devices has been calculated for the first time. The calculation of the vacancy distribution is based on the stress distribution in interconnections, since the vacancy concentration is influenced by the local stress.

From the results of the stress simulation, the vacancy distribution was calculated using the stress-induced vacancy model. The results showed that both stress and vacancies are concentrated near interconnection sidewalls, and their gradients are directed toward the corners and sidewalls in interconnections.

CHAPTER 5.

STRESS-INDUCED MIGRATION MODEL

5-1 Introduction

The availability of thermal energy results in random motion of vacancies in a lattice of aluminum or aluminum alloy. Since the movement direction of each vacancy is random, the average thermal motion of whole vacancies is zero. However, directed motion of vacancies to vacancy sinks such as defects and grain boundaries is caused by vacancy diffusion and vacancy drift [45,50-53]; vacancy diffusion is due to a vacancy concentration gradient, and vacancy drift is due to a vacancy free-energy gradient. Voids and fractures are considered to be formed as a result of vacancy accumulation, so that the diffusion and drift of vacancies in interconnections is also a key issue for clarifying the mechanism of stress-induced migration.

In this chapter, a stress-induced migration model in interconnections on semiconductor devices is proposed.

5-2 Vacancy diffusion

The vacancy flux due to diffusion, J_{di}, which is the number of vacancies crossing a unit area per unit time, is usually expressed as [42,43,48,50,51]

$$J_{di} = -D \nabla C_V , \quad (5-1)$$

where D is the diffusion constant of vacancies and C_V is the number of vacancies per unit volume under stress.

Equation (5-1) shows that vacancies flow from the high concentration region to the low concentration region; namely, vacancies flow from the tensile stress region to the compressible stress region.

5-3 Vacancy drift

The free energy of vacancy, G_V, shows gradients in interconnections because of the presence of a stress gradient. Vacancies drift due to the force resulting from the free energy gradient, and the force, F_{dr}, is defined as [48]

$$F_{dr} = - \nabla G_V . \quad (5-2)$$

If a mobility, A_V, is defined as a vacancy velocity per unit force, then the vacancy flux due to the drift, J_{dr}, which is the number of vacancies crossing a unit area per unit time, is expressed as [48]

$$J_{dr} = -A_V C_V \nabla G_V . \quad (5-3)$$

The free energy of a vacancy under thermal stress, G_V, is defined by [41-43]

$$G_V = E_F - S_F T + \sigma V . \quad (5-4)$$

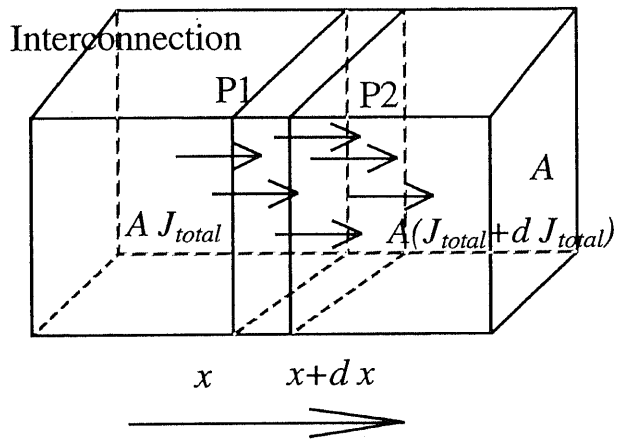


Fig. 5-1. Schematic of vacancy flux.

Here, stress σ is a hydrostatic stress and defined as positive for compressible stress. Substituting eq. (5-4) into eq. (5-3) and applying the Einstein mobility relation, one obtains the vacancy flux due to the drift, J_{dr}, as [54]

$$J_{dr} = -\frac{D}{kT} C_V \nabla (\sigma V) . \quad (5-5)$$

Here, we assumed that E_F and S_F are constant.

Equation (5-5) shows that vacancies flow from the compressible stress region to the tensile stress region.

5-4 Vacancy continuity equation

From eqs. (5-1) and (5-5), the total vacancy flux, J_{total}, is

$$J_{total} = -D \nabla C_V - \frac{D}{kT} C_V \nabla (\sigma V) . \quad (5-6)$$

Under the thermal equilibrium with stress and without vacancy sink, the vacancy flux due to the diffusion and drift compensate each other, so that the total vacancy flux is zero.

Fick's second law is derived by applying considerations of vacancy continuity to eq. (5-6). Consider the flow of vacancies in interconnection of cross section A, between planes P_1 and P_2 separated by dx, as shown in Fig. 5-1. The rate of accumulation of vacancies in the region between planes is $A(\partial C_V/\partial t)dx$. This can also be written as the difference between the fluxes flowing into and out of the region. The vacancy flux entering the region at P1 is AJ_{total}, and the vacancy flux leaving the region at P2 is $A(J_{total}+dJ_{total})$; the net flux entering the region is thus $-A\, dJ_{total}$. Hence

$$A \frac{\partial C_V}{\partial t} dx = -A\, dJ_{total} + A\, U\, dx \ , \quad (5-7)$$

where U is a vacancy generation/annihilation term which allows for the vacancy generation or annihilation rate per unit volume in the region. Equation (5-7) can be written as [49]

$$\frac{\partial C_V}{\partial t} = -\nabla J_{total} + U \ . \quad (5-8)$$

The term U for an excess concentration of vacancies compared to the equilibrium value under thermal stress can be introduced as

$$U = -\frac{C_V - C_{Ve}}{\tau_S} \ , \quad (5-9)$$

where C_{Ve} is the number of vacancies in a unit volume in equilibrium under thermal stress and τ_S is a life time of a vacancy.

Substituting eqs. (5-6) and (5-9) into eq. (5-8), one obtains the vacancy continuity equation

$$\frac{\partial C_V}{\partial t} = -\nabla \left(-D \nabla C_V - \frac{D}{kT} C_V \nabla(\sigma V)\right) - \frac{C_V - C_{Ve}}{\tau_S} \ . \quad (5-10)$$

If the diffusion constant D is not a function of the vacancy concentration and the vacancy volume V does not depend on the stress, eq. (5-10) is reduced to

$$\frac{\partial C_V}{\partial t} = D \nabla^2 C_V + \frac{D}{kT} V C_V \nabla^2 \sigma - \frac{C_V - C_{Ve}}{\tau_S} . \quad (5-11)$$

From eqs. (3-12) and (3-11), C_{Ve} can be written as follows:

for pure metal

$$C_{Ve} = N_{pure} \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right), \quad (5-12)$$

and for alloy

$$C_{Ve} = N_{alloy} (1 - Z C_S) \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right)$$
$$+ N_{alloy} Z C_S \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(\frac{E_{FB}}{kT}\right) \exp\left(-\frac{S_B}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right), \quad (5-13)$$

where N_{pure} is the number of lattice sites in a unit volume for pure metal and N_{alloy} is the number of lattice sites in a unit volume for alloy.

5-5 Proposal of stress-induced migration model

The vacancy continuity equation, the stress-induced vacancy equation and the thermal stress simulation model compose the stress-induced migration model. The vacancy continuity equation and the stress-induced vacancy equation are rewritten as follows.

The vacancy continuity equation is

$$\frac{\partial C_V}{\partial t} = D \nabla^2 C_V + \frac{D}{kT} V C_V \nabla^2 \sigma - \frac{C_V - C_{Ve}}{\tau_S} . \quad (5-14)$$

The stress-induced vacancy equation for pure metal is

$$C_{Ve} = N_{pure} \exp\left(-\frac{E_F}{kT}\right) \exp\left(\frac{S_F}{k}\right) \exp\left(-\frac{\sigma V}{kT}\right), \quad (5-15)$$

and that for alloy is

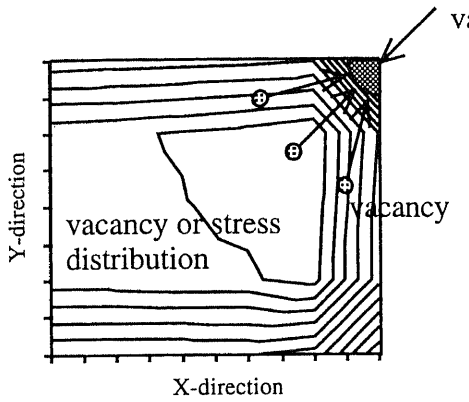


Fig. 5-2. Transportation of vacancies to the vacancy sink by the vacancy diffusion and drift.

$$C_{Ve}=N_{alloy}\,(1-Z\,C_S)\,exp\left(-\frac{E_F}{kT}\right)exp\left(\frac{S_F}{k}\right)\,exp\left(-\frac{\sigma V}{kT}\right)$$
$$+\,N_{alloy}\,Z\,C_S\,exp\left(-\frac{E_F}{kT}\right)exp\left(\frac{S_F}{k}\right)exp\left(\frac{E_{FB}}{kT}\right)exp\left(-\frac{S_B}{k}\right)\,exp\left(-\frac{\sigma V}{kT}\right). \quad (5-16)$$

The thermal stress simulation model was briefly described in chapter 4.

These equations shows the stress-induced migration for vacancies with the stress relaxation due to the generated vacancies, because C_V is directly reflected by the stress relaxation phenomenon. The stress-induced transport of vacancies changes not only the local vacancy concentration but also the local stress, so that the stress calculation is important for the stress-induced migration.

For solving these equations, vacancy sinks must be considered in the interconnection, and the vacancies are transported to vacancy sinks, as shown in Fig. 5-2. Moreover, these equations and the thermal stress simulation should simultaneously be computed through a three-dimensional numerical simulation. Voids and fractures caused by the stress-induced migration, however, are mainly surrounded by crystal planes of (111) orientation with peculiar shapes, which will be shown in chapter 7 [6,12,55,56]. It is difficult to simulate the stress-induced migration model within that boundary condition.

In the proposed model, the author assumed that (1) the vacancies generated at T_{SiN} vanish and the vacancies corresponding to a certain temperature, T, generate, because the life time

of vacancies is several minutes [57-61] and (2) single vacancies do not change into vacancy clusters such as voids, stacking faults and dislocation loops [57-61] until vacancies reach vacancy sinks.

The author has attempted the analytical application of the stress-induced migration model to the voids and fractures, in chapters 6 and 7.

5-6 Conclusion

In this chapter, the author proposed the stress-induced migration model with the stress relaxation due to the generated vacancies. The model is constituted of the vacancy continuity equation and the stress-induced vacancy equation, along with the thermal stress model. For solving the stress-induced migration model the proposed equations should simultaneously be computed and void formation and growth must be considered that vacancies migrate to vacancy sinks.

CHAPTER 6.
VOID FORMATION

6-1 Introduction

The stress distribution and vacancy concentration distribution in interconnections were discussed in chapter 4. The stress and vacancy concentration were concentrated near interconnection sidewalls, and their gradients were directed toward sidewalls and corners in the interconnections. These indicate that vacancies would migrate toward sidewalls and corners in interconnections due to a gradient force caused by both the vacancy distribution and the stress distribution, so that it is considered that voids due to stress-induced migration are generated at sidewalls and corners in interconnections. The void formation and growth, however, must be considered that vacancies migrate to vacancy sinks.

If the stress-induced migration model described in the previous chapter can be adapted to the void formation, it may be possible to demonstrate the process of void generation and growth quantitatively. In order to solve these equations based on a numerical calculation, it must be considered that voids are mainly surrounded by crystal planes of (111) orientation [6,12,55,56]. For numerical calculation, however, this treatment is complicated.

In this chapter, the stress-induced migration model is adapted to analyze the void formation and growth mechanism in interconnections on semiconductor devices, and moreover, the relation between the void growth and an initial void size will be discussed.

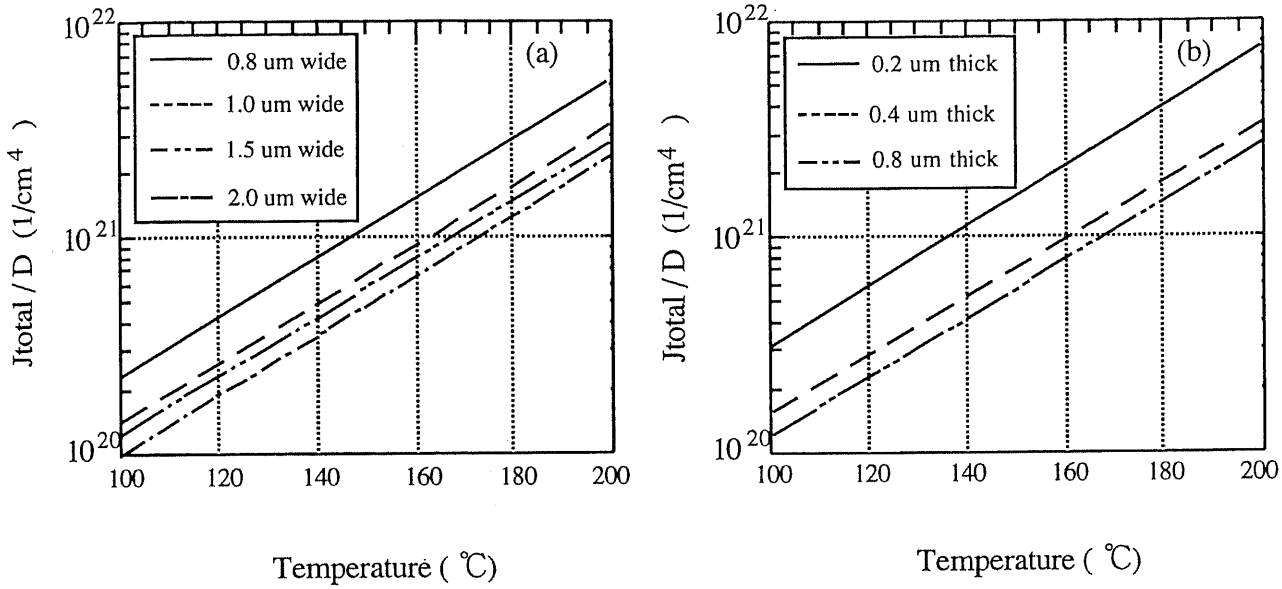


Fig. 6-1. Total vacancy flux normalized by *D*. (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um, (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

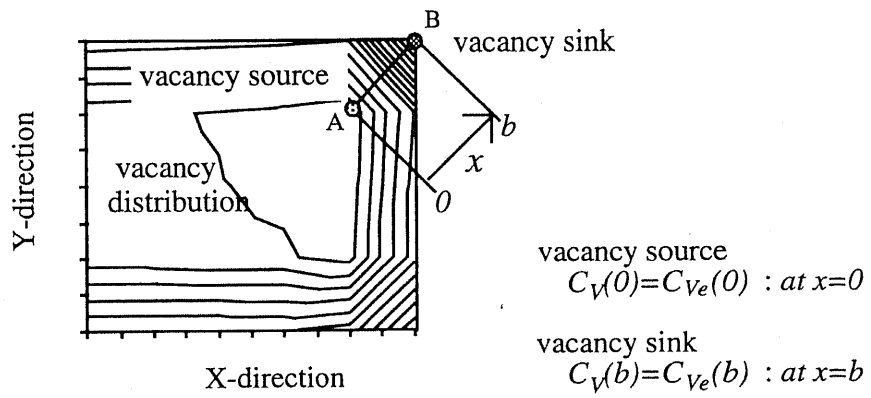


Fig. 6-2. Definition of the boundary conditions for solving stress-induced migration model.

6-2 Void formation model

Figures 6-1(a) and 6-1(b) show the theoretical calculation results of the total vacancy flux normalized by *D* for a thickness of 0.8 um and a width of 1.5 um, respectively.

The magnitude of the total vacancy flux for 0.8-um-thick interconnections increases in the order of width of 0.8, 1.0, 1.5 and 2.0 um, but the discrepancies in 1.0-, 1.5- and 2.0-um-thick samples are small. The magnitude of the normalized total vacancy flux for 1.5-um-wide

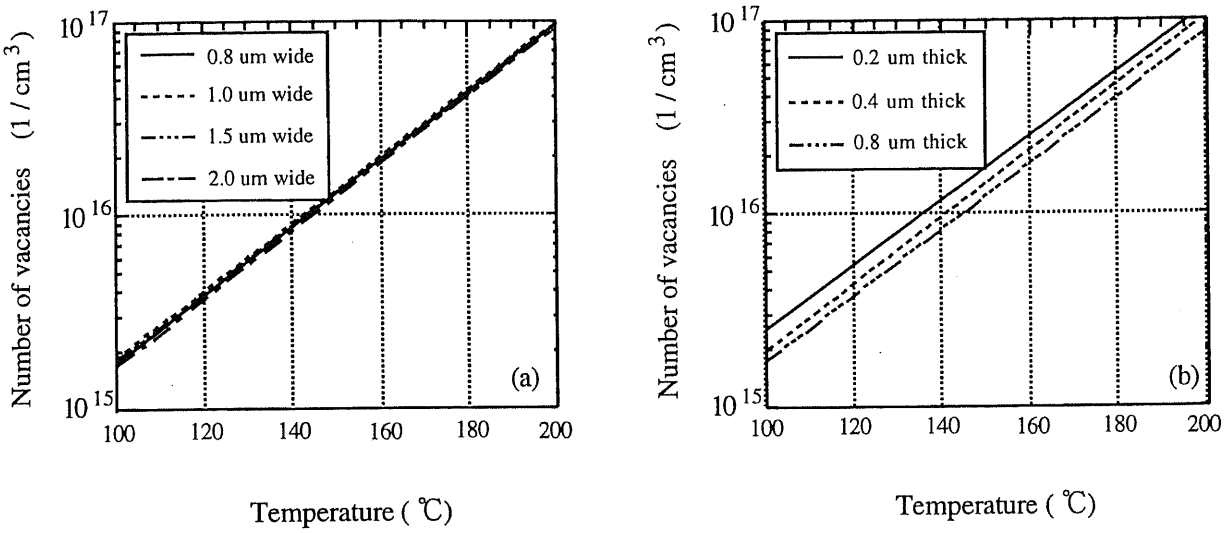


Fig. 6-3. Vacancy concentration. (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um, (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

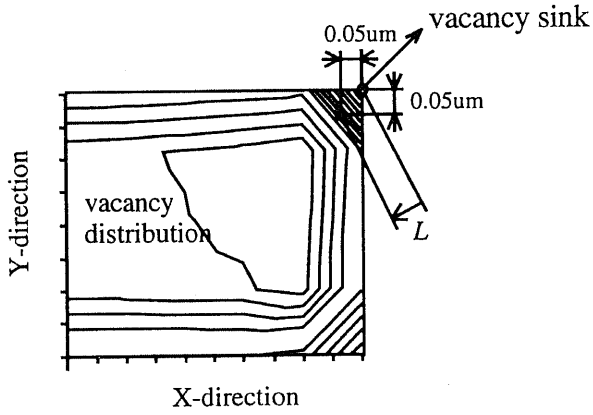


Fig. 6-4. Definition of the position for calculating the number of vacancies.

interconnections increases in the order of thickness of 0.2, 0.4 and 0.8 um, but the discrepancies in 0.4- and 0.8-um-thick samples are also small.

Here, the boundary conditions for solving the stress-induced migration model were defined as shown in Fig. 6-2. The author assumed that (1) the vacancy sink exists at the corner of the interconnection, (2) the vacancy source exists at the point of maximal vacancy concentration and (3) only the vacancy diffusion in the steady-state, J_{di}, was considered to first approximation, because solving eq. (5-14) subject to the above boundary conditions is analytically

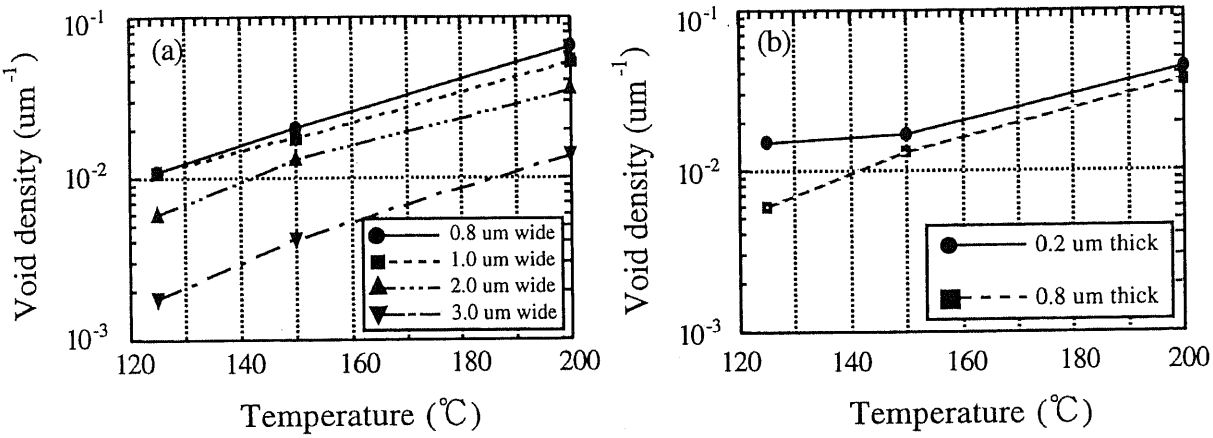


Fig. 6-5. Void density at the interconnection corners and sidewalls for samples which were kept at 125, 150 and 200 ℃ for 2000 hours: (a) 0.8-um-thick interconnections with width of 0.8 to 3.0 um and (b) 1.5-um-wide interconnections with thickness of 0.2 and 0.8 um.

impossible. From these assumptions, the total vacancy flux by D is approximate by the vacancy concentration gradient in the initial stage of stress-induced migration. These approximations may give the larger total vacancy flux, because the vacancy drift, J_{dr}, is not counted in; however, a certain degree of approximation may be obtained.

Figures 6-3(a) and 6-3(b) show the theoretical calculation results of the number of vacancies at the certain position defined in Fig. 6-4 for a thickness of 0.8 um and a width of 1.5 um, respectively. The number of vacancies increases with temperature. The discrepancies in the number of vacancies for 0.8-um-thick interconnections are much small. The magnitude of the number of vacancies for 1.5-um-wide interconnections increases in the order of thickness of 0.2, 0.4 and 0.8 um, but the discrepancies are small.

The distance, L, defined in Fig. 6-4 is a three times as long as a diffusion length of vacancies given by $\sqrt{(D\ \tau_S)}$, where the diffusion constant, D, is $1.71 \times exp(-1.44 / (kT))$ (cm^2/sec) [42], lifetime, τ_S, is 60 sec [57-61] and temperature is 300 ℃.

Figure 6-5 shows the void density which is experimentally obtained during long-term high-temperature storage tests. Figure 6-5(a) shows the void density at the corners and

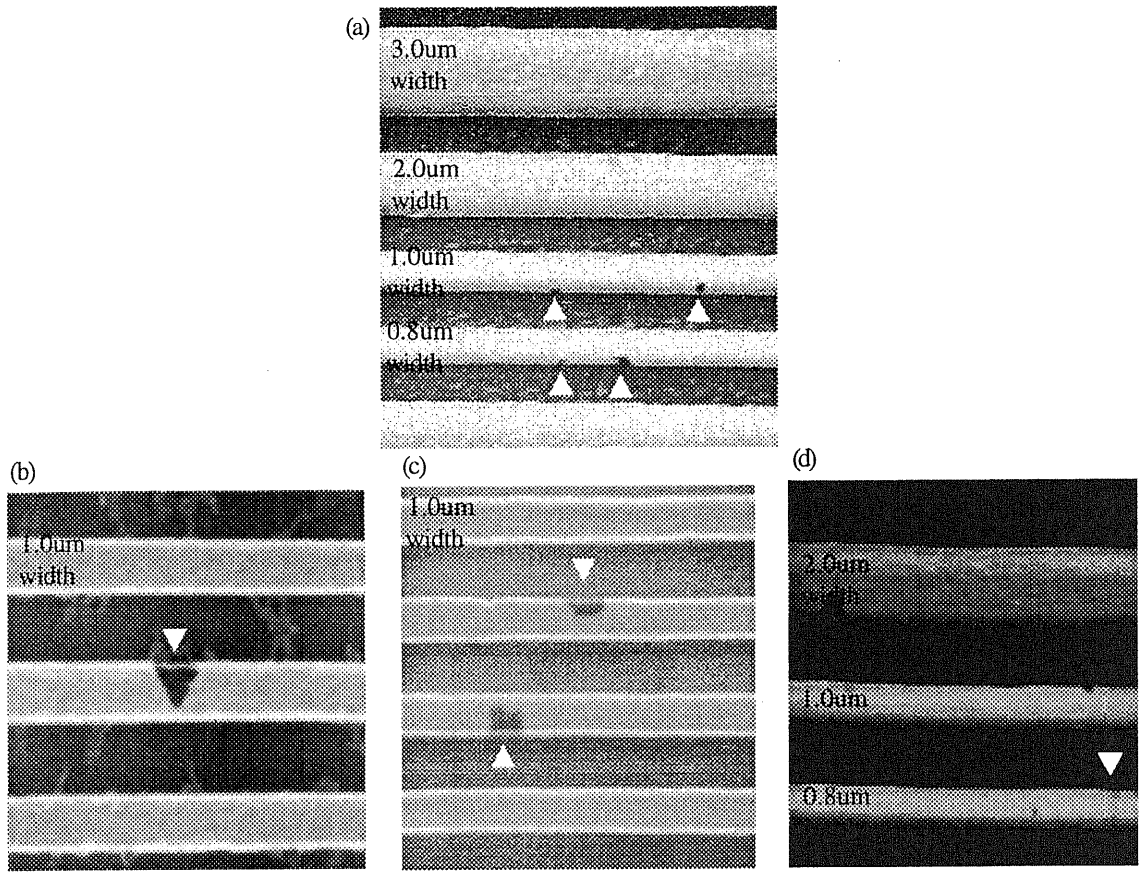


Fig.6-6. Micrographs of voids using a scanning electron microscope, for the sample of 0.8 um thickness kept at 200 ℃ for 5000 hours: (a) microscopic voids at 45° angle, (b) wedge-shaped void, (c) chamfer-like voids and (d) slit-like voids.

sidewalls of interconnections for 0.8-um-thick samples with width of 0.8 to 3.0 um. Figure 6-5(b) shows that for 1.5-um-wide samples with thickness of 0.2 and 0.8 um. Here, samples were kept at 125, 150 and 200 ℃ for 2000 hours. The sample fabrication process was the same as the process described in chapter 2. Voids were counted using a laser microscope. The void density in Fig. 6-5 is qualitative agreement with that in Figs. 6-1 and 6-3(b). These results show that the void formation is dominated by the vacancy concentration gradient. If the samples, however, keep on leaving in a high-temperature chamber until the stress relaxation due to the stress-induced migration becomes perfect, the void density may be agreement with that in Fig. 6-3(a), because Fig. 6-3(a) shows the providing ability of vacancies. For more detailed analysis of the relation between the vacancy concentration

gradient and the number of vacancies, the numerical simulation is necessary.

Voids formed by stress-induced migration are usually observed at corners and sidewalls in interconnections [6,12,21,62]. Figure 6-6 shows voids in interconnections which were kept at 200 ℃ for 5000 hours. Voids are observed at corners and sidewalls. Figure 6-6(a) shows microscopic voids at corners and sidewalls at a 45° angle, Fig. 6-6(b) shows a wedge-shaped void, Fig. 6-6(c) shows chamfer-like voids and Fig. 6-6(d) shows a slit-like void. These voids are mainly surrounded by crystal planes of (111) orientation [6,12,55,56].

These experimental results agree with the theoretical model. (1) Voids are more easily generated at narrower and thinner interconnections than at broader and thicker interconnections. (2) Voids are generated at corners and sidewalls in interconnections. Void generation and growth, however, must be considered that vacancies migrate to vacancy sinks.

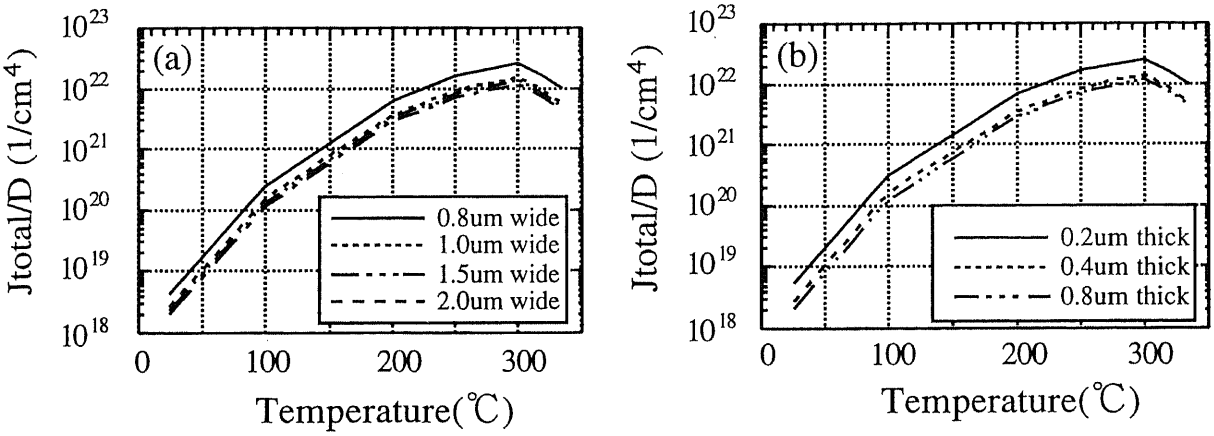


Fig. 6-7. Total vacancy flux normalized by D in the temperature range of 25 to 335 ℃: (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um and (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

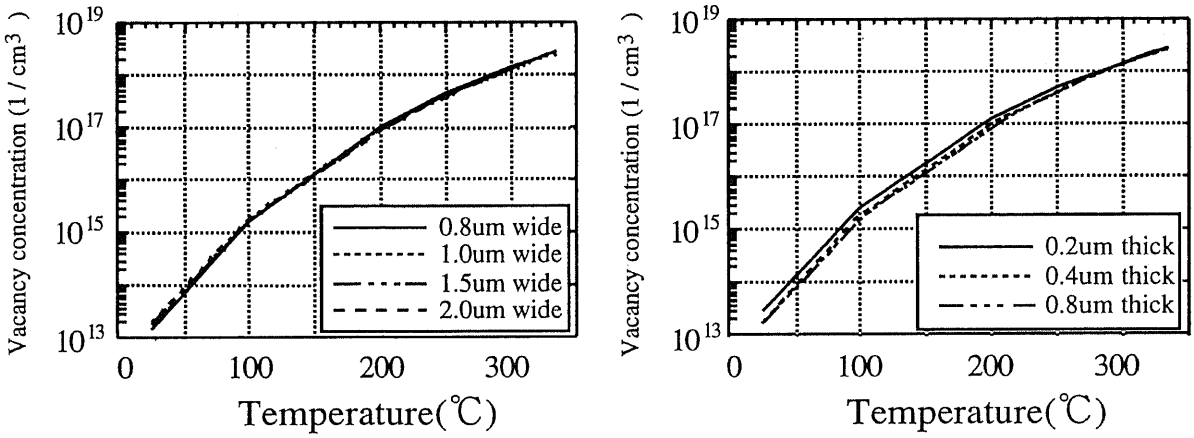


Fig. 6-8. Vacancy concentration in the temperature range of 25 to 335 ℃: (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um, (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

6-3 Restriction on void growth

6-3-1 Temperature and stress

Figure 6-1 showed the total vacancy flux normalized by D in the temperature range of 100 to 200 ℃. When the temperature extends over the range of 25 to 335 ℃, the total vacancy flux normalized by D decreases beyond 300 ℃ as shown in Fig. 6-7, because the thermal stress gradient and vacancy concentration gradient in interconnections decrease with

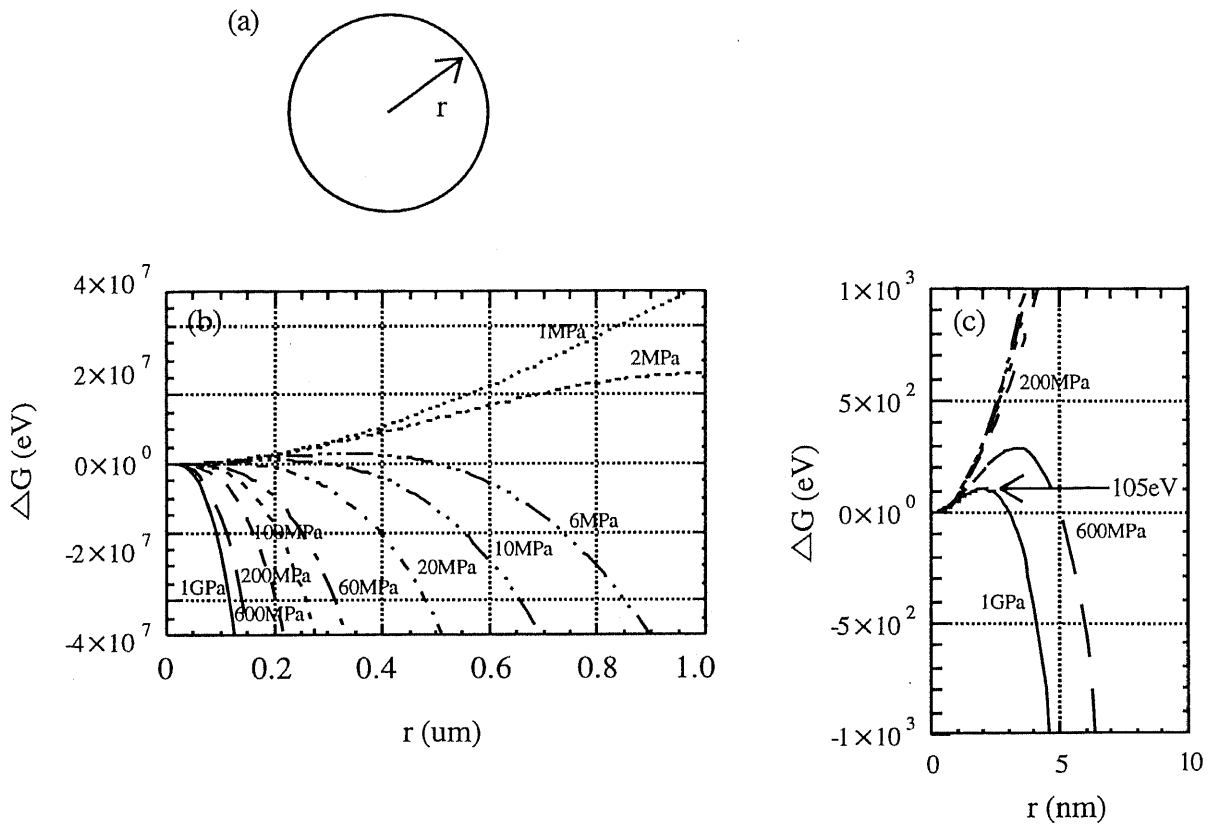


Fig. 6-9. $\triangle G$ of a spherical void as a function of radius: (a) shape of a spherical void, (b) $\triangle G$ of a spherical void as a function of radius and (c) partial magnification of Fig 6-6(b) [57] .

increasing temperature. The vacancy concentration increases with temperature as shown in Fig. 6-8. The void growth, however, is influenced by the vacancy concentration gradient as mentioned above, so that the void growth is restricted by the critical temperature.

6-3-2 Free energy of void formation

Under tensile stresses, the formation of voids in interconnections results in a decrease in free energy which is equal to σV work. The formation of the void surface, however, requires an increase of free energy which is equal to the surface area, S, with the energy per unit area, γ_m. The total change in free energy of void formation, therefore, is a competition between the decrease of free energy due to σV work and the increase of free energy due to S

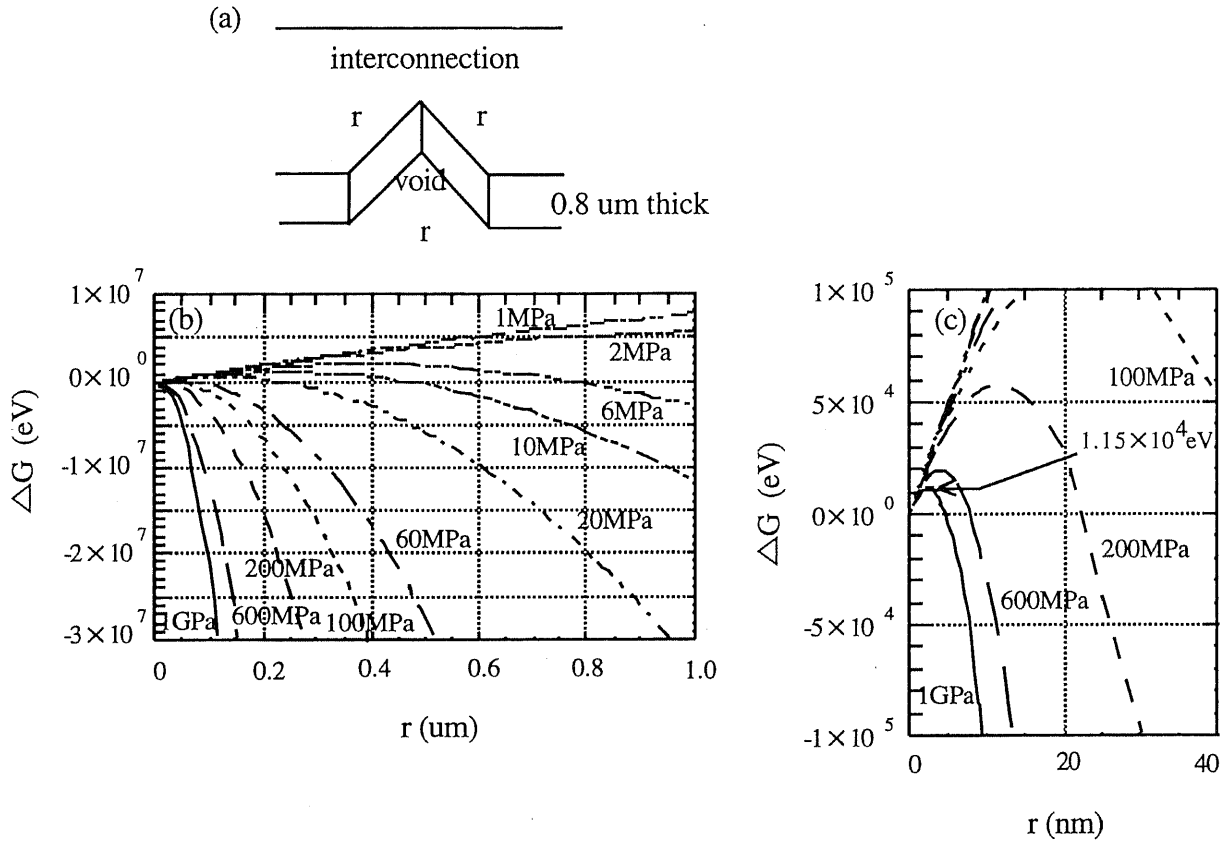


Fig. 6-10. $\triangle G$ of a trigonal prism void as a function of side length: (a) shape of a trigonal prism void, (b) $\triangle G$ of a trigonal prism void as a function of radius and (c) partial magnification of Fig. 6-7(b).

γ_m. For a spherical void with radius r, the surface area is $4\pi r^2$ and the volume is $4\pi r^3/3$. Thus, the total free energy change, $\triangle G$, is given by [62]

$$\triangle G = 4\pi r^2 \gamma_m - \frac{4\pi}{3} r^3 \sigma . \quad (6-1)$$

In the case of assuming a γ_m value of 1 (J/m2) [56,62], the total free energy change with tensile stresses is shown in Fig. 6-9.

The free energy change initially increases, because the surface area initially increases faster than the volume. For the void growth, this increasing free energy acts as a barrier. When the stress (taken here to be hydrostatic) is 1 GPa, the barrier is 105 eV which is very high relative

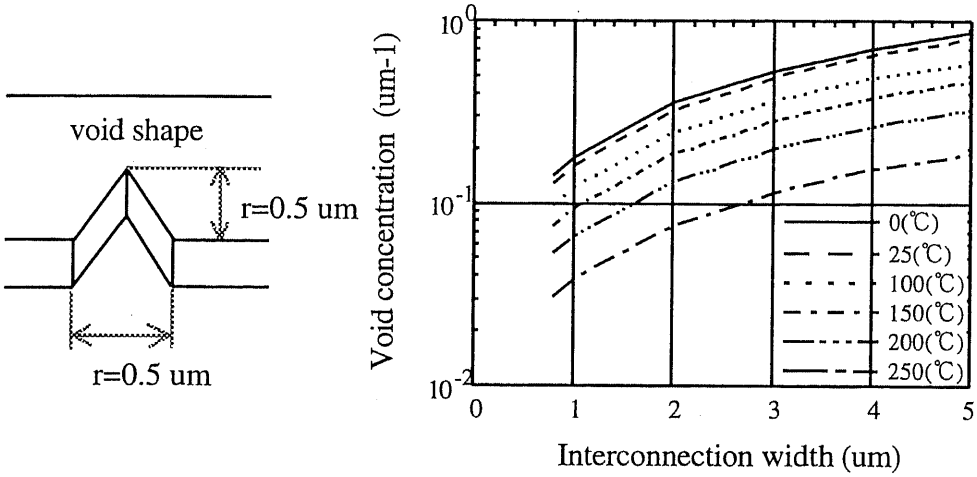


Fig. 6-11. Calculation of the superior limit of void concentration for 0.8-um-thick Al-2wt%Si interconnection.

to the thermal energy.

When the void shape is a trigonal prism, as shown in Fig. 6-9(a), the total free energy change, $\triangle G$, is given by

$$\triangle G = 2\,r\,t\gamma_m - \frac{\sqrt{3}}{4} r^2\,t\sigma, \quad (6-2)$$

where t is interconnection thickness, and the void growth is assumed to be hydrostatic. The total free energy change with tensile stress is shown in Fig. 6-10.

When the stress is 1 GPa, the barrier is 1.15×10^4 eV which is also very high relative to the thermal energy.

If voids grow to beyond the critical size, the free energy becomes negative and void growth is limited by the void formation model.

6-3-3 Stress relaxation

Interconnections on semiconductor devices are covered with a passivation layer and an underlayer. When the passivation layer is deposited at T_{SiN}, the volume of the interconnec-

tions, *V1*, expands until the SiN deposition temperature. After the passivation deposition process, if the temperature is decreased to a value (T) below T_{SiN}, the interconnection can not shrink, because interconnections are restrained by the passivation layer. After all, if the stress relaxation is not considered, the volume of interconnection, *V1*, is maintained below T_{SiN}. In the case of interconnections without the passivation layer and the underlayer, the volume of interconnections, *V2*, varies with temperature.

The difference between *V1* and *V2* causes a thermal stress in interconnections covered with the passivation layer. The thermal stresses are relaxed by generating voids due to the stress-induced migration. Consequently, if a void has a constant volume, V_{void}, the number of voids in the interconnection can be calculated as $(V1-V2)/V_{void}$ which is the maximum limit of the void concentration due to the stress-induced migration.

Assuming that the void is wedge-shaped, the void concentration in interconnections is shown in Fig. 6-11. The maximum limit of the void concentration is obtained as approximately 0.1 um^{-1}.

6-4 Discussion

As shown in Figs. 6-9 and 6-10, the initial change in free energy with void growth is positive and the thermodynamic barrier to void growth is very high, so void growth due to both the thermal energy and the effect of thermal tensile stress can not occur.
Some voids caused by the stress-induced migration, however, exist practically in interconnections, as shown in Figs. 6-5 and 6-6. It is considered that defects larger than the critical size must exist initially in the interconnections. The defects larger than the critical size act as vacancy sinks, because the free energy of vacancy growth becomes negative.

For example, if the initial defect sizes are 0.01 um and 0.05 um, the corresponding stresses required for void growth are over 500 MPa and 60 MPa. The stresses of 500 MPa and 60 MPa correspond to the temperature of 175 and 340 ℃, respectively. Therefore, the critical temperature at which void growth may be influenced by the initial defect size, as shown in Fig. 6-7.

The defects are considered to be small particles of contaminants [62], grain boundaries, lattice defects and imperfect adhesions at the interconnection/passivation interface. Especially, grain boundaries and imperfect adhesions are most interesting defects, because voids are observed at the corners of interconnections, as shown Fig. 6-6. Therefore, the following guidelines are proposed to suppress the stress-induced migration.

(1) Low-temperature process to reduce the thermal stress.

(2) Clean process to reduce the number of small-particle contaminants.

(3) Single-crystal interconnection to reduce grain boundaries.

(4) Perfect adhesion at interconnection/passivation interface.

6-5 Conclusion

The stress-induced migration model described in the previous chapter were adapted to analyze the void formation and growth in interconnections on semiconductor devices. The results of the theoretical treatment, the void formation model, agree with the experimental results. (1) Voids are more easily generated at narrower and thinner interconnections than at broader and thicker interconnections. (2) Void growth is restricted by the critical temperature. (3) Total void volume is limited by the stress relaxation.

Under tensile stress, the formation of the void volume in interconnections results in a decrease in free energy. The formation of the void surface, however, requires an increase of free energy. The total change in free energy of void formation, therefore, is a competition between the decrease of free energy and the increase of free energy. The free energy initially increases, because the surface area initially increases faster than the volume. For void growth, this increasing free energy acts as a barrier. The barrier is high enough to prevent void growth, so void growth due to thermal energy and the effect of thermal stress is not possible. Some voids caused by the stress-induced migration, however, exist in interconnections. It is considered that defect larger than the critical size must exist initially in interconnections. The defects may be small particles of contaminants, grain boundaries and imperfect contacts at the interconnection/passivation interface.

If voids grow beyond the critical size, the free energy becomes negative and void growth is limited by the void formation model. The voids larger than the critical size act as vacancy sinks.

CHAPTER 7

FRACTURE

7-1 Introduction

Void formation in interconnections was discussed in the previous chapter, and the stress-induced migration model was proposed in chapter 5. These indicate that vacancy migration occurs due to the gradient force caused by both the vacancy distribution and the stress distribution. If the stress-induced migration model is adapted to the fracture, open failure, of interconnections based on a numerical calculation, it may be possible to quantitatively demonstrate the fracturing process. For solving these equations, a grain boundary condition must be considered, because fractures are generated at grain boundaries through slit-like voids [3,4,9,11,12,24,63]. For numerical simulation, however, this treatment is difficult.

In this chapter, the stress-induced migration model are adapted to analyze the process of open failure.

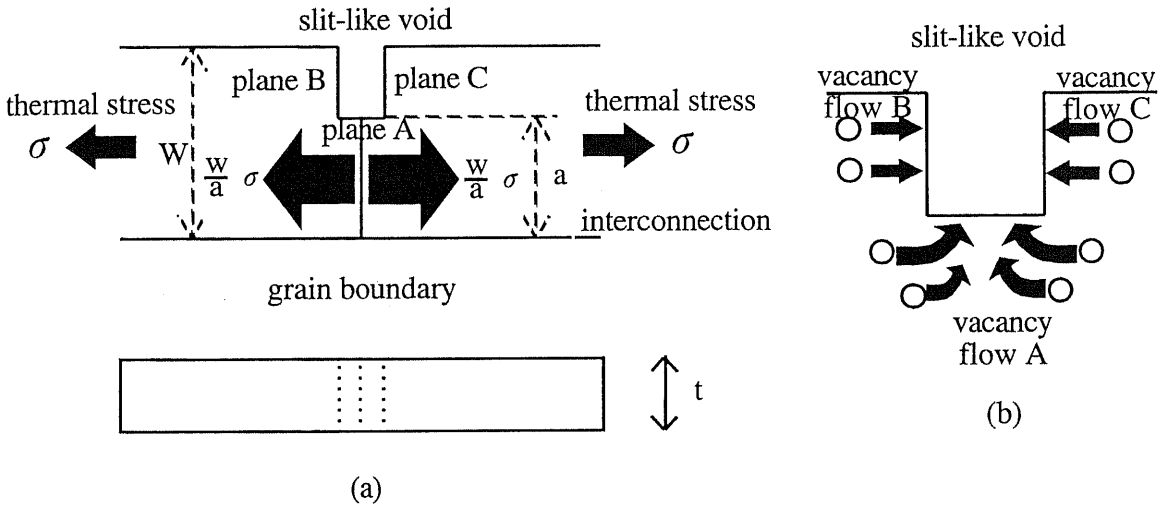
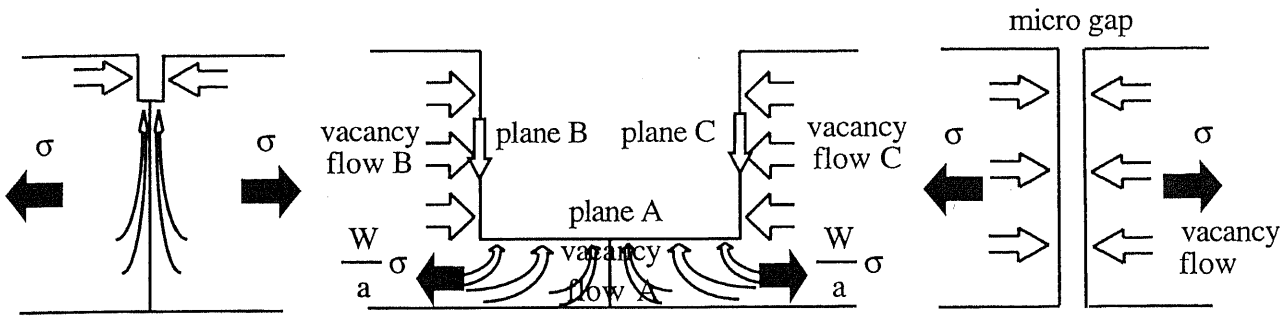


Fig. 7-1. Schematic of the fracture model

7-2 Fracture model

Fractures, open failures, caused by the stress-induced migration are usually observed at grain boundaries through slit-like voids [3,4,9,11,12,24,63]. Grain boundaries act as the nuclei for the void formation discussed in chapter 6, because some grain boundaries may be imperfect adhesions at the interconnection/passivation interface and larger than the critical size, and moreover, the diffusion constant of vacancies at the grain boundary is larger than that of volume diffusion [42,43].

Figure 7-1(a) illustrates a fracture model. The tensile stress around the slot-like void is *W/a* times as large as the tensile stress at other positions, because the cross-sectional area of the interconnection at the slit-like void is *a/W* times as large as that at other positions. Here, the stress intensity factor [45,46] is not considered, for the sake of simplicity. The difference between the local stresses in the interconnection induces a vacancy migration, as shown in chapters 5 and 6. For this reason, vacancies travel toward the slit-like void, as shown in Fig. 7-1(b).



(a) Initial stage (b) Steady state (c) Final stage

Fig. 7-2. Schematic of vacancy flow.

Figure 7-2(a) shows the vacancy flow near the grain boundary at the initial stage of the fracture. The vacancies travel toward the micro silt-like void, because the stress near the micro slit-like void in the interconnection is slightly larger than that at other positions and the stress on planes A, B and C are slightly less than that at other positions because of free surfaces. The vacancy flow mechanism is similar to the void formation mechanism included the stress relaxation, except that the vacancy flow is faster than the volume diffusion because of grain boundary diffusion and surface diffusion. Therefore, the initial stage of fracture can be qualitatively described using the void formation model discussed in chapter 6.

In the steady-state term of the fracture, the areas of planes B and C increase with time, because the slit-like void advances with time, so that the vacancy flow from planes B and C increases with time, as illustrated in Fig. 7-2(b). The tensile stress near the slit-like void is *W/a* times as large as that at other positions, so that the vacancy flow from plane A also increases with time. Consequently, the vacancy flow in the steady-state term is the total flow from planes A, B and C, and is larger than the vacancy flow in the initial stage of the fracture.

In the case of the open failure due to the stress-induced migration, the vacancy flow may be dominated by these processes. In order to solve this process, the stress-induced migration

model equations must be simulated based on the numerical calculation.

In the final stage of the fracture, grain boundaries are spread by the vacancy accumulation due to the stress-induced migration, and then the interconnections are split up, as shown in Fig. 7-2(c). Vacancy migration occurs due to the gradient force caused by both the stress distribution and the vacancy distribution. When grain boundaries are assumed to be microgap, as shown in Fig. 7-3(a), vacancy flow may be dominated by the z-axis stress distribution and vacancy distribution. The z-axis stress distribution in the interconnection is as shown in Fig. 7-4. The stress distribution was calculated using the conventional FEM. Figure 7-3(b) shows a schematic of the structural cross section of the interconnection used in FEM. Here, Al-2wt.%Si interconnections are deposited on a thermally oxidized silicon layer 1.4 um thick and covered with a SiN passivation layer 1.0 um thick. The structure is similar to the experimental sample used in chapter 2. Boundaries A and B have a symmetry condition for symmetric geometry, except in the case of the surfaces of interconnections because of microgap, as shown in Fig 7-3(b).

Figure 7-5 shows the z-axis stress distribution in the interconnection. Here, the z-axis stress at a certain position from the interconnection surface shows the average value of the z-axis stress at a certain z-axis position. All of the z-axis stress distribution curves show qualitatively similar characteristics.

Figure 7-6 shows the vacancy concentration distribution along the z-axis in the interconnection. Here, the vacancy concentration at a certain position shows the average value of the vacancy concentration distribution at a certain z-axis position. The vacancy concentration was calculated using the average value of the three-principal stresses. All of the vacancy concentration distribution curves show qualitatively similar characteristics.

Figures 7-7(a) and 7-7(b) show the total vacancy flux normalized by D for a thickness of 0.8 um and a width of 1.5 um, respectively. Equation (5-14) was used to calculate the vacancy flux and the boundary conditions defined as shown in Fig. 7-8. The assumptions and approximations for calculations are the same manners described in chapter 6.

The magnitude of the normalized total vacancy flux for 0.8-um-thick interconnections increases in the order of width of 0.8, 1.5, 1.0 and 2.0 um except in the case of temperature at 335 ℃, but the discrepancies are small. The magnitude of the normalized total vacancy flux for 1.5-um-wide interconnections increases in the order of thickness of 0.4, 0.8 and 0.2 um, but here too, the discrepancies are small.

A peak of the normalized total vacancy flux appears at about 300 ℃. This trend is similar to that for void formation.

Figures 7-9(a) and 7-9(b) show the number of vacancies at x=0.5 um from the surface. The number of vacancies increases with temperature and the discrepancies in the number of vacancies are much small.

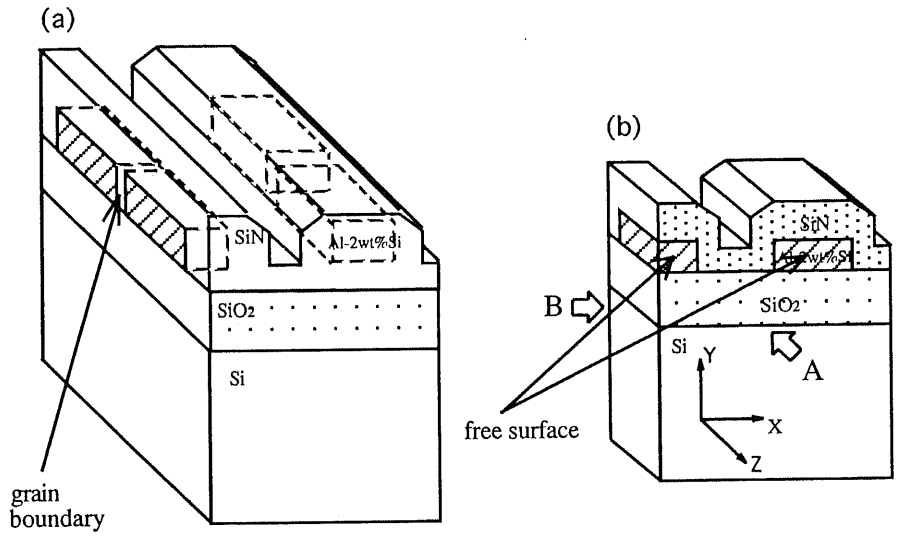


Fig. 7-3. Schematic of the structure model: (a) Model for grain boundary, microgap, (b) model for FEM. Only the right half of the model is shown, because of the symmetric geometry.

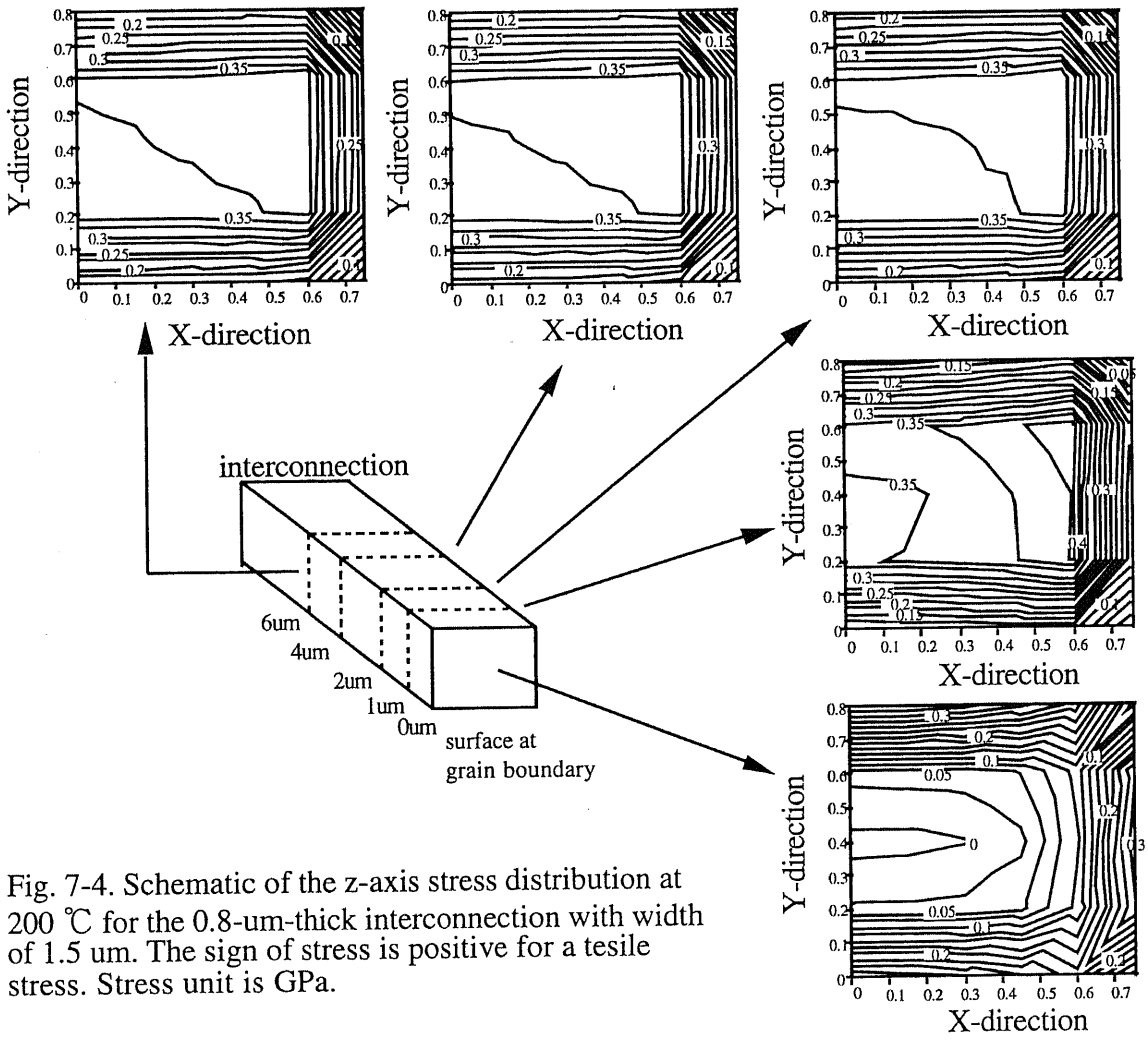


Fig. 7-4. Schematic of the z-axis stress distribution at 200 ℃ for the 0.8-um-thick interconnection with width of 1.5 um. The sign of stress is positive for a tesile stress. Stress unit is GPa.

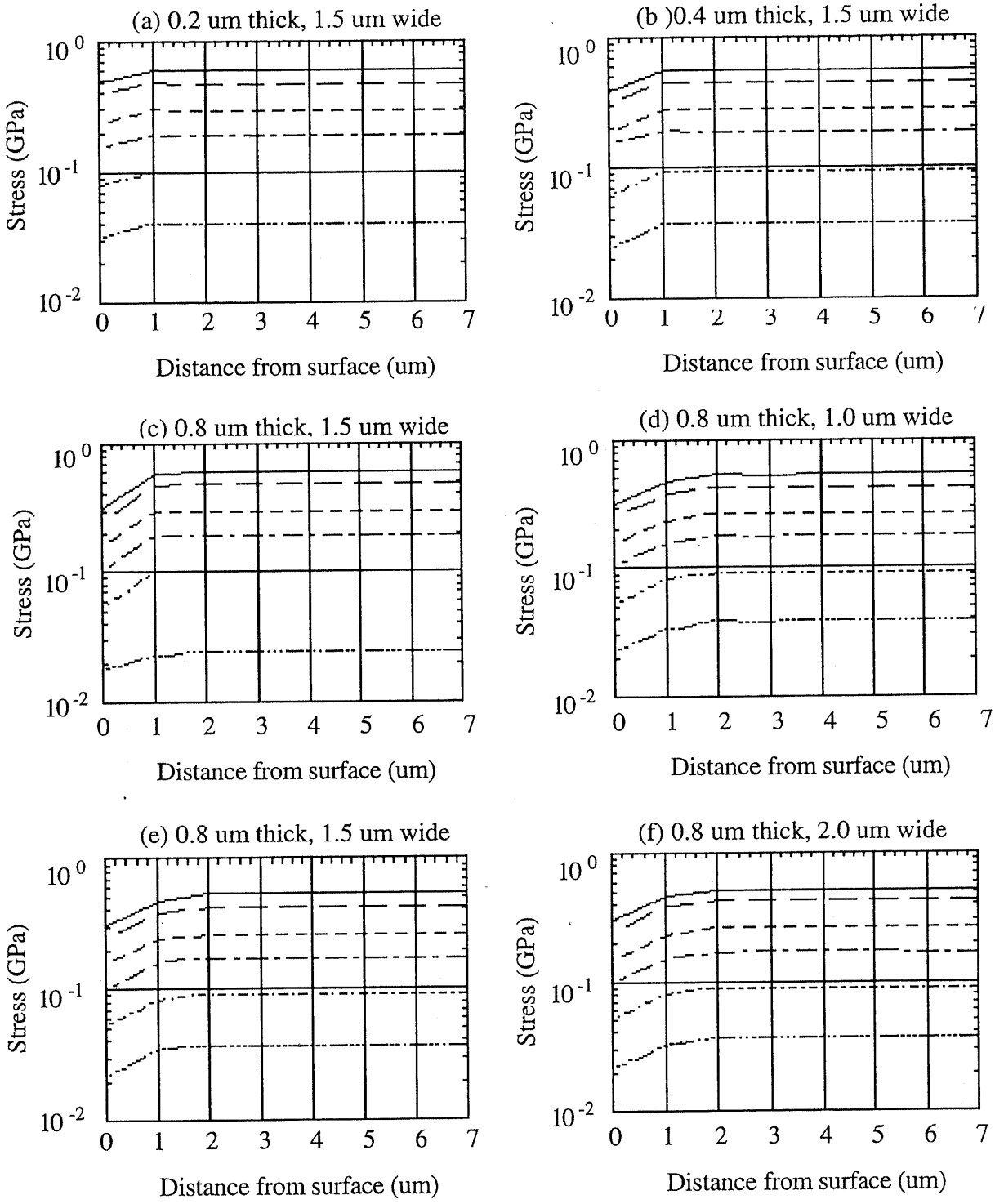


Fig. 7-5. Z-axis stress distribution. The sign of stress is positive for a tesile stress.

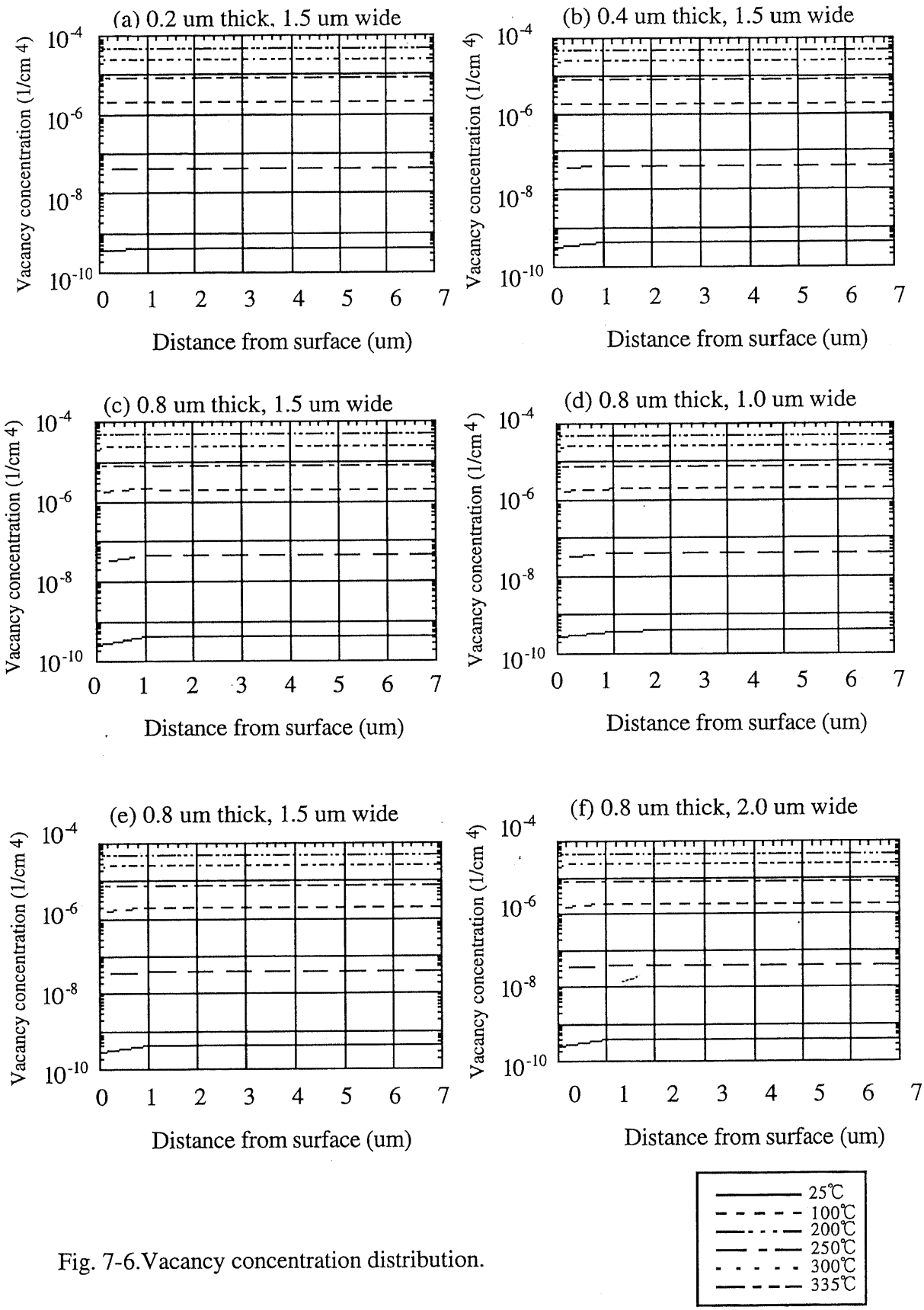


Fig. 7-6.Vacancy concentration distribution.

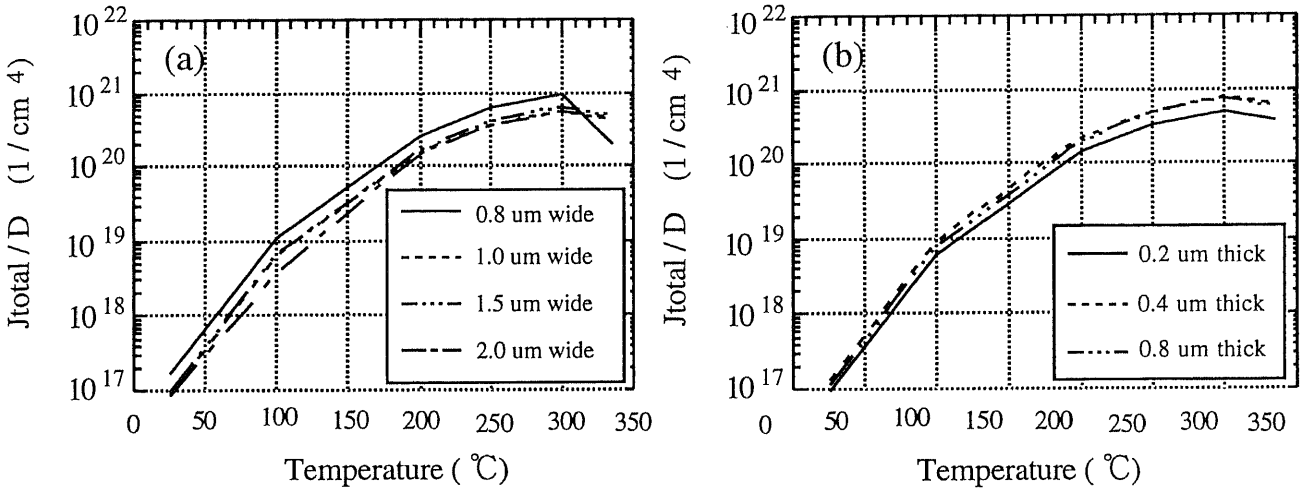


Fig. 7-7. Total vacancy flux normalized by *D*: (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um and (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

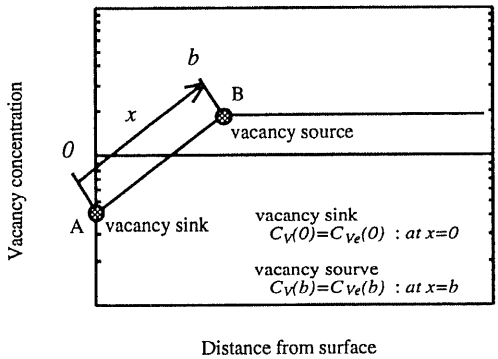


Fig. 7-8. Definition of the boundary conditions for stress-induced migration model.

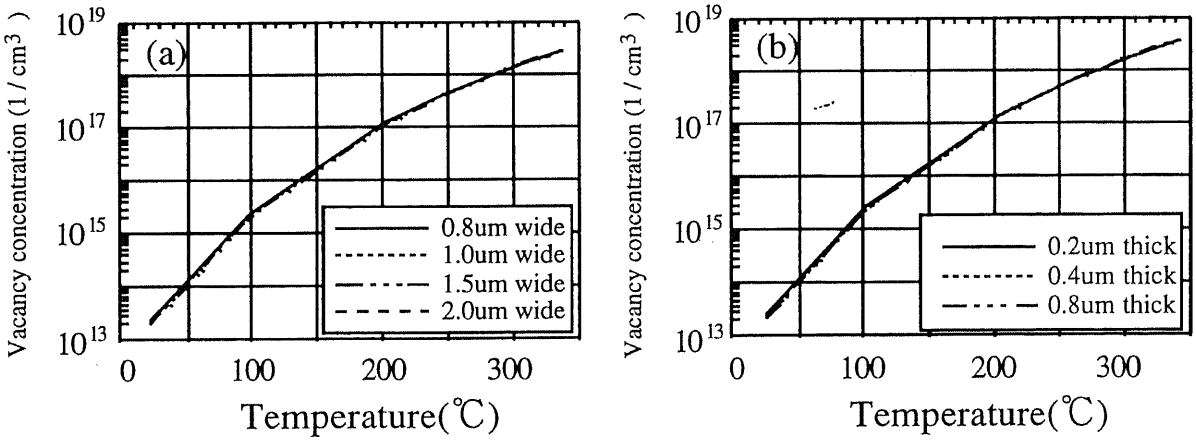


Fig. 7-9. Vacancy concentration in the temperature range of 25 to 335 ℃. (a) 0.8-um-thick interconnections with width of 0.8 to 2.0 um, (b) 1.5-um-wide interconnections with thickness of 0.2 to 0.8 um.

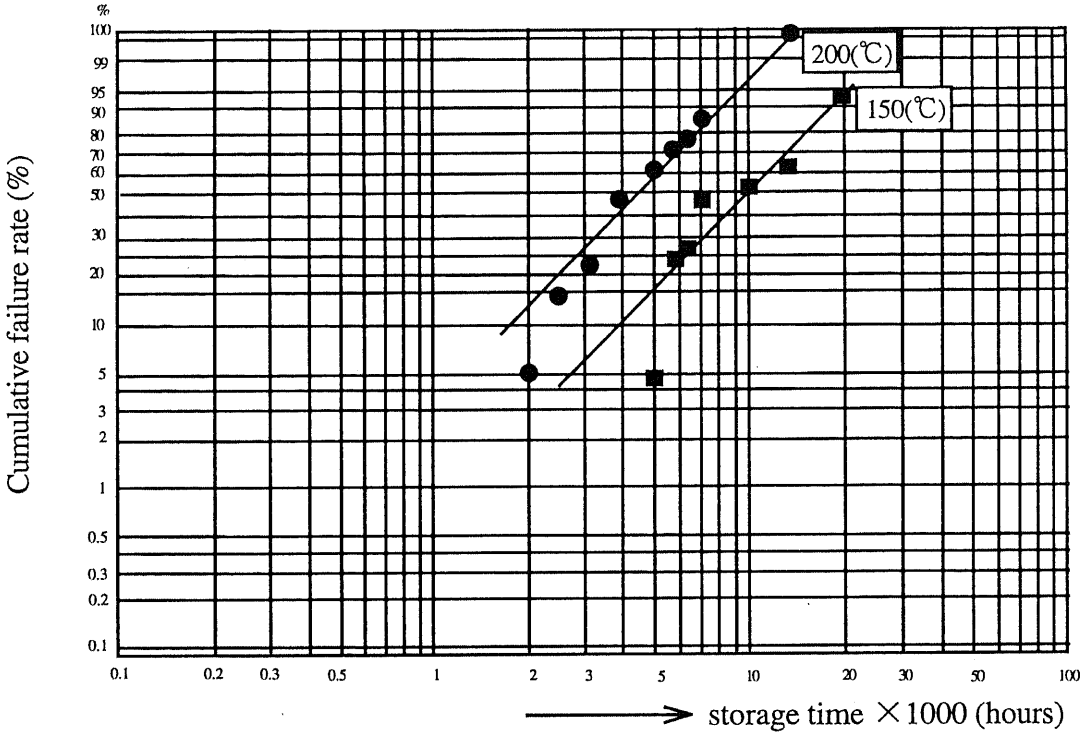


Fig. 7-10. Cumulative failure rate vs storage time during high-temperature storage tests. The interconnection width is 1.0 um and thickness is 0.2 um. Passivation layer is 1.0-um-thick SiN.

7-3 Lifetime tests

Lifetime tests, high-temperature long-term storage tests, were carried out at 125, 150, 200 and 250 ℃ for approximately 20000 hours to measure the failure rate defined as the electrical open failure. The interconnection width was varied from 1.0 to 3.0 um, thickness was varied from 0.2 to 0.8 um, and length was 0.5 m. The sample fabrication process was the same as that described in chapter 2.

Figure 7-10 shows the cumulative failure rate in a Weibull plot. Only the interconnection 0.2 um thick and 1.0 um wide broke down between 150 and 200 ℃; the peak failure rate occurs in the temperature range from 150 to 200 ℃. This experimental result agrees with the

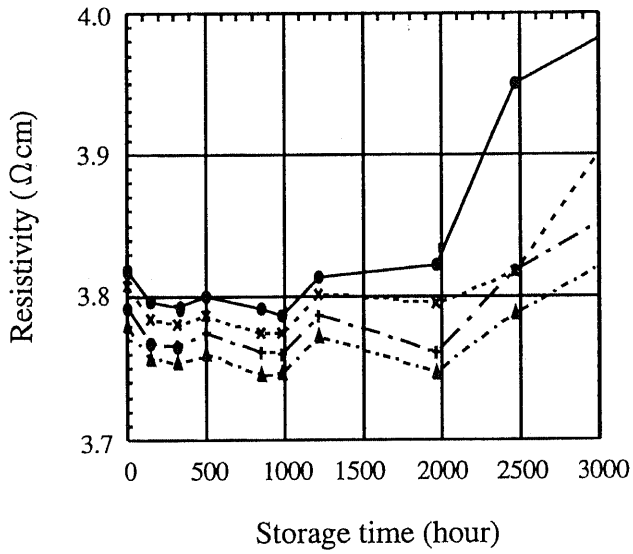


Fig. 7-11. Resistivity change during 200 ℃ storage. Thickness of interconnections was 0.2 um and width was 1.0 um.

reported values [5,8,11] and the theoretical model in that a peak failure rate exists. The temperature of the peak failure rate, however, does not agree with that of the theoretical model,. 300 ℃.

No relation between the lifetime and the interconnection geometry, thickness and width, was obtained in the experiments. The fact, however, that only the interconnection 0.2 um thick broke down is qualitative agreement with the void formation model.

Figure 7-11 shows the resistivity change during 200 ℃ storage. All of the samples broke down within the following 5000 hours. The resistivity decreased up to 1000 hours, and then increased after 2000 hours, and finally, the interconnection broke down.

The decrease in resistivity up to 1000 hours is identical to the initial stage of stress-induced migration described in chapter 2. The open failure occurs after the decrease in resistivity. The temperature dependence of the resistivity change during the initial stage, as discussed in chapter 2, is qualitative agreement with that of the lifetime due to the stress-induced migration. It is considered that the resistivity change during the initial stage is related to not only the crystal structure change, but also the stress and the vacancy/atom migration.

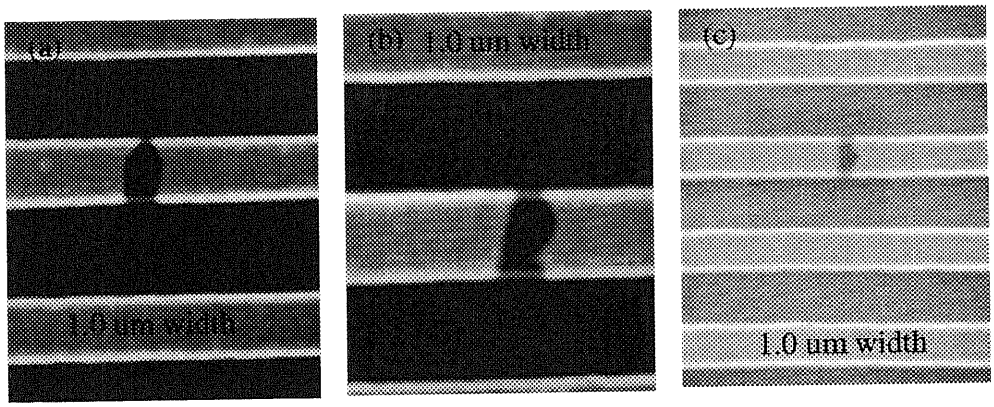


Fig. 7-12. SEM micrographs of fractures and a void in interconnections unlayered by removing SiN passivation layer: (a), (b) and (c) show fractures. Fractures were generated during 200 ℃ storage for 5000 hours. Interconnections are of 1.0 um width and 0.2 um thickness.

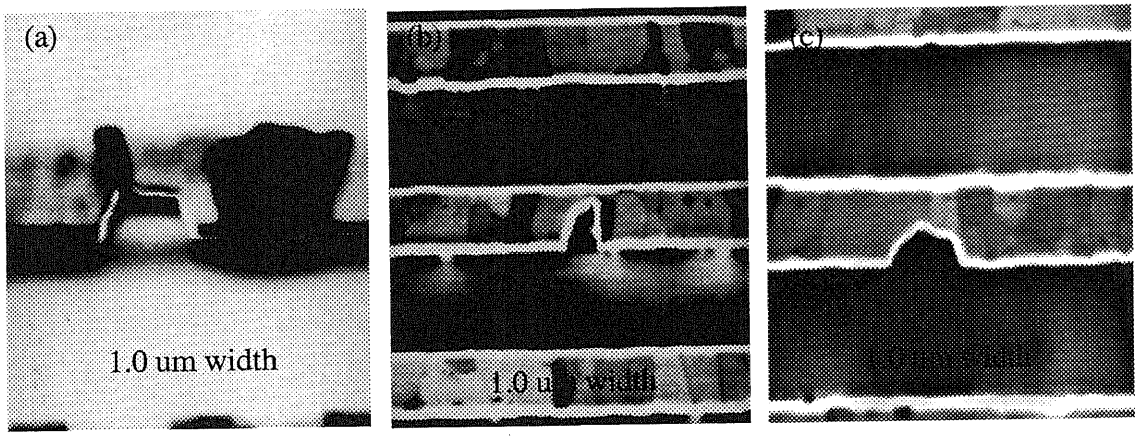


Fig. 7-13. SEM micrographs of voids in interconnections unlayered by removing SiN passivation layer. Interconnection surface was sputtered slightly using focused ion beam equipment. Voids were generated during 200 ℃ storage for 5000 hours. Interconnections are of 1.0 um width and 0.2 um thickness.

The flow of atoms which constitute the interconnections is opposite to that of the vacancies, but the mechanisms of atom flow is similar to that of vacancy flow.

Figure 7-12 shows micrographs of fractures. These micrographs indicate that fractures are not caused by the tearing by a force, but by the vacancy transport. Open failures are usually generated through slit-like voids [6,62]. In this experiments, however, fractures after expansion of the microgap were observed, as shown in Figs. 7-12 and 7-13.

Figure 7-13 also shows that the grain boundaries in the horizontal direction to the interconnection suppress the void growth and fracture. This result contradicts the findings in chapter 6 for the restriction of void generation as shown; grain boundaries in the transverse direction act as nuclei for the formation of voids.

7-4 Discussion

As described in chapter 1, discrepancies are found among the results reported by researchers on the storage temperature dependence of the interconnection lifetime. Mcpherson and Dunn [5], Tezaki et al. [8] and Kato et al. [11] reported that the peak failure rate occurs in the temperature range from 150 to 200 ℃. Hinode et al. [6] reported that the failure rate increases as the temperature rises up to 300 ℃. Mayumi et al. [4] reported that the failure rate is independent of temperature in the temperature range of 125 to 250 ℃.

The experimental results obtained by the author show that the peak failure rate occurs in the temperature range from 150 to 200 ℃. This is in agreement with the results of Mcpherson and Dunn [5], Tezaki et al. [8] and Kato et al. [11] The theoretical results obtained by the author, however, show that the peak failure rate occurs at about 300 ℃. This is in agreement with the results of Hinode et al [6]. This discrepancy in the temperature range in which the peak failure rate occurs may be related to the critical size of the nuclei on grain boundaries and/or the difference between the calculated stress and the actual stress in interconnections. The value of actual thermal stress in interconnections is not identical to the result of the thermal stress simulation, because the thermal stress simulation is not considered the thermal stress between the interconnection and the under layer at the interconnection deposition.

Consequently, the temperature at which the peak of the failure rate occurs may be influenced by the processing conditions and structure of the samples.

7-5 Conclusion

The stress-induced migration model equations are adapted to analyze the fracture mechanism of interconnections on semiconductor devices. The results of theoretical treatment agree with the experimental results in that the peak failure rate occurs at a certain temperature. The temperature of peak failure rate occurrence, however, does not agree with the experimental results. This discrepancy may be related to the critical size of nuclei discussed in chapter 6 and/or the difference between the calculated stress and the actual stress in interconnections.

Grain boundaries in the horizontal direction to the interconnection suppress the void growth and fracture and grain boundaries in the transverse direction act as nuclei for the formation of voids and fractures.

CHAPTER 8

CONCLUDING REMARKS

The author has clarified the mechanisms of stress-induced migration in interconnections on semiconductor devices based on thermodynamics theory and experiments. Dramatic results were obtained and are summarized here.

- First, the characteristics of the interconnections during the initial stages of stress-induced migration were shown by means of the high-temperature short-term storage experiments. The characteristics, such as the electric resistivity, stress and crystal structure, vary markedly depending on the storage temperature and storage duration.

  The resistivity change can be considered to be determined by a competition between two phenomena. (1) Degenerations near the grain boundary such as dislocation pileups increase the resistivity of the interconnection. (2) The disappearance of degenerations near the grain boundary and the grain growth decrease the resistivity. The change in the thermal stress is also determined by a competition between grain growth and micro void formation.

- Second, the single-vacancy formation energy in Al-2wt.%Si interconnections on semiconductor devices with a SiN passivation layer was measured using the quenching technique. We found that the single-vacancy formation energy is 0.60 eV in the temperature range of 200 to 300 ℃. The theoretical calculation of the single-vacancy formation energy based on the stress-induced vacancy model, which shows the relation between the stress and vacancy concentration, is 0.64 eV for bulk Al-2wt.%Si and 0.59 eV for the Al-2wt.%Si interconnection with a SiN passivation layer. This difference is attributed to the fact that the thermal expansion coefficient of

Al-2wt.%Si is larger than that of SiN, so that the interconnection is tensiled due to the difference in expansion. The tensile force enhances the generation of vacancies. The theoretical calculation indicates a vacancy formation energy of 0.59 eV for the tensiled situation, which is agreement with the experimental result of 0.60 eV.

• Third, the vacancy concentration distribution in Al-2wt.%Si interconnections covered with a SiN passivation layer on semiconductor devices was shown for the first time. The calculation of the vacancy concentration is based on the thermal stress distribution in interconnections, because the vacancy concentration is influenced by the local stress. The thermal stress simulation based on a finite-element method (FEM) is used to estimate the stress distribution in microscopic interconnections.
From the results of the stress simulation, the vacancy distribution was calculated using the stress-induced vacancy model. The results showed that both the stress and vacancies are concentrated near the interconnection sidewalls, and their gradients are directed the toward corners and sidewalls in the interconnections.

• Fourth, the stress-induced migration model was proposed. The model equation is constituted of the continuity equation for vacancies and the stress-induced vacancy model equation, along with thermal stress model. The continuity equation for vacancies is based on the vacancy diffusion equation and vacancy drift equation.

• Fifth, the stress-induced migration model equations were adapted to analyze the void formation and growth mechanism in interconnections on semiconductor devices. The results of the theoretical treatment agree with the experimental results. (1) Voids are generated more easily in narrower and thinner interconnections than in broader and thicker interconnections. (2) Void growth is restricted by a critical temperature. (3) Total vacancy volume is limited by the stress relaxation.

• Sixth, under the tensile stresses, the formation of the void volume in interconnections results in a decrease in free energy. The formation of the void

surface, however, requires an increase of free energy. The total change in the free energy of void formation, therefore, is a competition between the decrease and increase of free energy. The free energy initially increases, because the surface area initially increases faster than the vacancy volume. This increasing free energy behaves as a barrier for void growth. This barrier is very high and therefore void growth due to thermal energy and the effect of thermal stress is not possible. Some voids caused by the stress-induced migration, however, exist in interconnections. It is considered that defects larger than the critical size must exist initially in the interconnections. The defects can be small particles of contaminants, grain boundaries and imperfect contacts at the interconnection/passivation interface. If voids become larger than the critical size, the free energy becomes negative and the void growth is only limited by the void formation model. Voids larger than the critical size act as vacancy sinks.

- Finally, the stress-induced migration model equations were applied to analyze the open failure mechanism of interconnections on semiconductor devices. The results of the theoretical treatment agree with the experimental results in that the peak failure rate occurs at a certain temperature. The temperature at which the peak failure rate occurs, however, does not agree with the experimental result. This discrepancy in the temperature of the peak failure rate may be related to the initial void size and/or the difference between the calculated stress and the actual stress in interconnections.

Based on the results of this work, the following guidelines can be proposed to suppress the stress-induced migration.

(1) Low-temperature process to reduce the thermal stress in interconnections.

(2) Clean process to reduce the number of small-particle contaminants which act as nuclei of voids.

(3) Perfect adhesion at interconnection/passivation interface.

The solutions to some of the problems described in chapter 1 have been given in this

thesis and solutions to the remaining problems may be obtained using the proposed stress-induced migration model with numerical simulation.

For solving the complicated practical problems, the stress-induced migration model and concepts proposed in this thesis will be useful as a base of future study.

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