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Dissertation
学位請求論文

Simulation-based Device Characterization and its Application to Device Parameter Optimization

(計算機シミュレーションによる集積デバイスの特性抽出およびデバイスパラメータ最適設計)

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Chapter 1

Introduction

1.1 Roles of Computer Simulations in Semiconductor Device Design

In recent years, a VLSI(Very Large Scale Integrated circuit) contains a huge number, even over millions, of circuit elements and the integration scale is continuously growing as well as the integrated devices are continuously shrinking. Now, computer-aided design(CAD) techniques are important and indispensable skills all over the research, development and fabrication stages of such integrated circuits.

CAD tools used in VLSI development contains many kinds of simulation, synthesis and design tools(fig.1.1). In the lower level, there are process simulator, device simulator and parameter extractor, which mainly concern the fabrication stages of VLSIs. In the higher level, there are high-level synthesizer, circuit synthesizer, logic simulator, circuit simulator and layout tools, which concern the VLSI design stages.

This dissertation concentrates on the circuit and the device simulation techniques, which evaluate performance of circuits and semiconductor de-

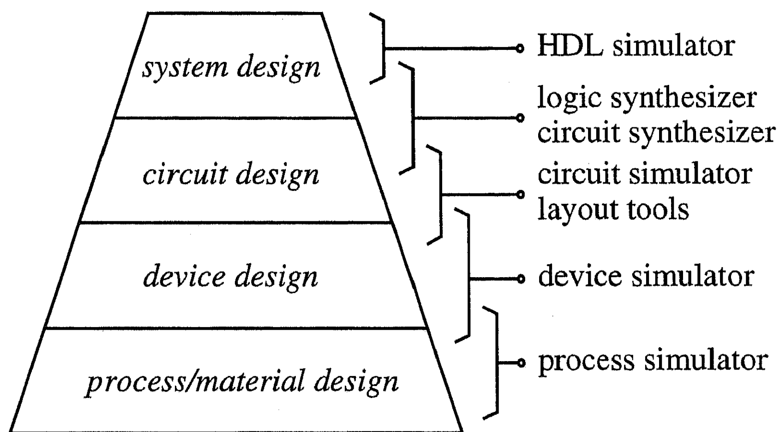

Figure 1.1: Computer-Aided Design techniques in VLSI development

vices.

Relations between the simulation and the fabrication stages of VLSI development are illustrated in fig.1.2 on the device simulation case, for example.

In the development flow, the device simulation works as a prediction tool for device characteristics such as static I-V characteristics, transient responses and reliabilities, etc.. Those device characteristics are fed back and examined to improve the device design for desired performance. Simulation tools also concern the real fabrication processes or the real device characteristics, in the calibration processes for the simulation models.

As well as device simulation, circuit simulation predicts the performance of manually or automatically designed circuits and also the characteristics are fed back to the design stage.

From the iterations of the design and the simulation stages, optimized circuit and device designs are obtained and real products of devices and VLSIs are to be fabricated. This is the computer-aided fabrication flow.

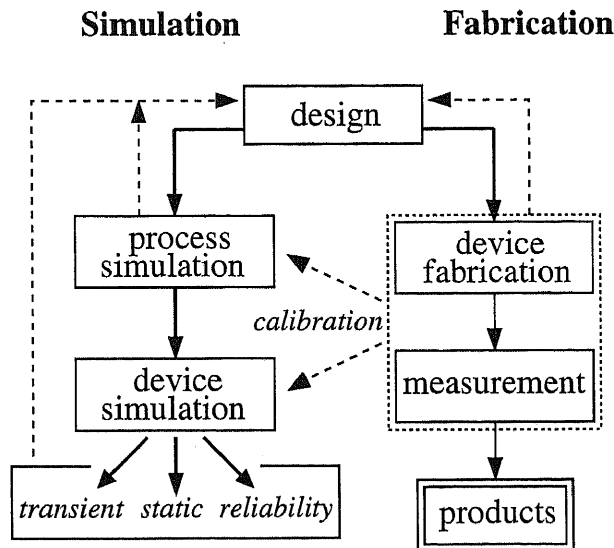

Figure 1.2: Simulation and fabrication stages on VLSI development

In this dissertation, optimization schemes in VLSI design are discussed especially in terms of semiconductor device design by optimization of device parameters. The key techniques in device and circuit evaluation with the computer simulations is the device modeling. In the following section, a history of semiconductor device modelings in both analytical and numerical ways are summarized briefly. Then, the goal of this work is presented with the outline of this dissertation in the last section of this chapter.

1.2 A Brief History of Analytical and Numerical Modeling of Semiconductor Devices

The history of analytical 'compact' modeling of semiconductor devices has begun at the same time as the concept of junction field-effect transis-

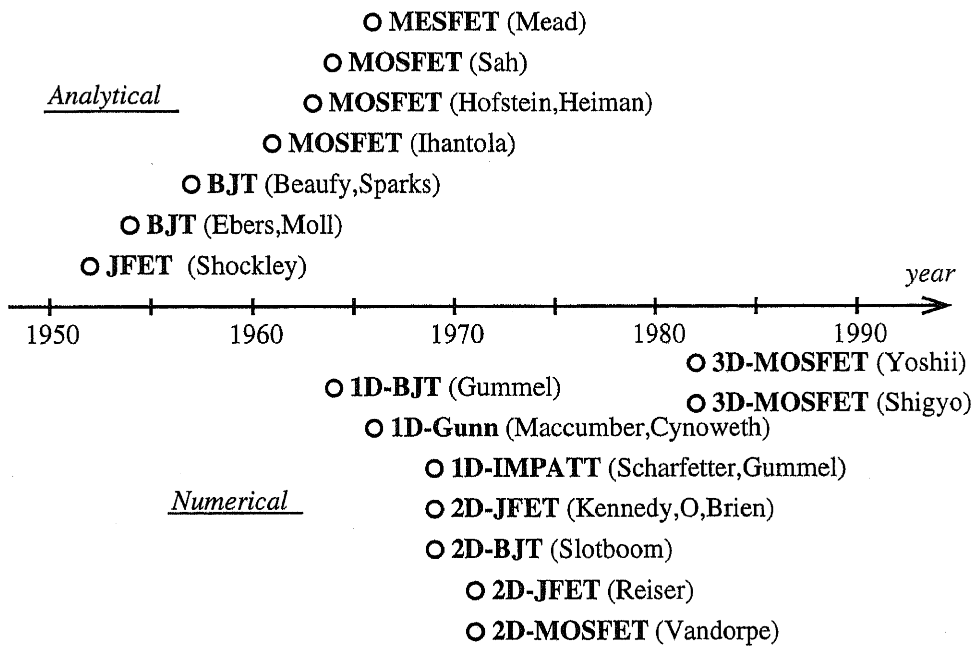

Figure 1.3: Early history of analytical and numerical semiconductor modeling

tor(JFET) was proposed by Shockley in 1952[1.1].

An analytical model for bipolar junction transistor(BJT) was presented by Ebers and Moll in 1954[1.2]. In 1957, the charge control model of BJT was presented by Beaufy and Sparks[1.3].

Metal-semiconductor field-effect transistor(MESFET) was firstly proposed by Mead in 1966[1.4]. The operation principle of a MESFET was similar to that of a JFET.

Another idea for field-effect controlled semiconductor devices is metal-oxide-semiconductor field-effect transistor(MOSFET), which has very old history down to 1930s. Device characteristics of MOSFETs were studied by Ihantora and Moll[1.5][1.6], Sah[1.7], and Hofstein and Heiman[1.8] in the

early 1960s. Since MOSFETs are suitable for integration in VLSIs, the minimum feature length has been shrunk continuously. Then, the short-channel effects such as the threshold shift or other scaling problems have become the important matters of modelings[1.9] and a lot of works have been proposed for the sake of establishing accurate models for device and circuit analysis.

Circuit simulators have also been investigated and developed to analyze circuit performance with the compact models. The most famous circuit simulation tool is SPICE (Simulation Program with Integrated Circuit Emphasis) which had been developed in University of California, Berkeley in 1973[1.10]. SPICE was evolved into SPICE2 in 1975[1.11], and currently SPICE3 and the improved versions of it are widely used among circuit engineers all over the world.

Numerical methods for semiconductor device modeling have their own history for about 30 years, which are described with fundamental device physics but requires a large amount of computer resources.

The numerical semiconductor device simulation based on the partial differential formulation of the drift-diffusion model was firstly presented in 1964 by Gummel with one-dimensional static analysis of BJT[1.12]. MacCumber and Chynoweth analyzed the Gunn oscillation of GaAs device by one-dimensional transient simulation in 1966 [1.13]. In 1969, Scharfetter and Gummel proposed, in analysis of Read IMPATT diode, a discretization scheme for the continuity equations with physically based expressions, which has been widely made use of in numerical simulation programs [1.14].

A two-dimensional numerical simulation of JFET was presented in 1969 by Kennedy and O'Brien with Poisson equation and one continuity equation[1.15]. BJT was simulated two-dimensionally in 1969 by Slotboom[1.17] with Poisson and both continuity equations. The transient

behavior of JFET was investigated by Reiser in 1971 with two-dimensional simulation[1.16] Also in 1971, two-dimensional simulation of MOSFETwas demonstrated by Vandorpe[1.18].

A lot of investigations have been attempted especially on two-dimensional numerical analysis of MOS devices, because the two-dimensional model has been believed to have enough ability to reproduce the characteristics of those devices.

Activities on three-dimensional numerical simulation have appeared in 1980s with requirement for analyzing three-dimensional effects in small geometry devices, such as the narrow channel effects, for example ref.[1.19] and [1.20]. The dramatic evolution of the computational power was one of the driving force for those activities.

Nowadays, a lot of commercial products for semiconductor device simulation based on three basic equations have been developed and are widely used in design, development and research stages of semiconductor devices.

On the opposite side of the partial differential method of the drift-diffusion model stands the Monte-Carlo method. The Monte-Carlo method has been known as a general mathematical method for solutions of various natural- and social-scientific problems based on random numbers and samplings since the early this century [1.21].

In 1966, Kurosawa has applied the Monte-Carlo method to simulation of the transport of electrons under high electric field[1.22]. Through 1970s and 1980s, many investigations of semiconductor devices with the Monte-Carlo methods have been carried out, for example ref.[1.24],[1.24],[1.23] and [1.26]. However, it was not a popular approach to model semiconductor devices with the Monte-Carlo method because the Monte-Carlo method based simulations require a large amount of computational time.

In the late 1980s, as computers had had a great improvement and as the limits of the drift-diffusion modeling of small geometry semiconductor devices had become frequently mentioned, the Monte-Carlo scheme became an important and an indispensable technique for semiconductor device simulations.

1.3 Outline of This Thesis

The aim of this dissertation is to present the design methodology of small geometry integrated semiconductor devices, especially CMOS devices, for high speed, low power and low energy operation. Analytical and numerical characterization methods are discussed in terms of the optimum design and the estimation of device parameters. As well as the simulation-based characterization methods, simulation methods themselves are investigated for efficient analyses.

In this dissertation, following works are presented and summarized.

In the first part, design methodology of MOSFETs for low power and low energy optima is discussed based on circuit simulation with compact models. In chapter 2, an evaluation method of power and energy consumption of CMOS circuits is presented using circuit simulation of a inverter circuit with physically based analytical models. In chapter 3, device design parameters are optimized to minimize energy consumption during a switching or to minimize the gate delay under restricted chip power.

In chapter 4, a one-dimensional numerical simulation of SOI MOSFETs for modeling the subthreshold characteristics is presented. Using the simulator, real device structural parameters of SOI MOSFETs are estimated by the curve fitting.

In chapter 5, stable and efficient schemes for two- and three-dimensional simulation of SOI MOSFETs are discussed. In the first half, a Quasi-Transient device simulation formulation is presented for stable and efficient SOI simulation. The Single-Transistor Latch(STL) phenomena are successfully reproduced by the method. In the latter half, matrix calculation problems of iterative linear solutions in SOI simulation are investigated and efficiency of a data-dependent scaling criterion is reported.

In chapter 6, quantum-mechanical considerations for thin-film SOI devices are introduced to the one-dimensional simulator presented in chapter 4, with electron mobility models by the relaxation time approximation. The parameter fitting is also demonstrated and necessity of the quantum-mechanical considerations in the analysis of thin-film devices is discussed.

Finally, in chapter 7, the studies on computational analyses for VLSI device design are summarized and discussed for the conclusion of this dissertation.

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Chapter 2

Evaluation of Power Consumption of CMOS Circuits with Physics-based Models

2.1 Introduction

In recent years, more and more MOSFETs and other circuit elements are integrated in a VLSI. A large number of circuit elements with high density integration cause large power consumption with thermal problems. They are especially noticeable in portable equipments with battery operations, such as PCS(Personal Communication System) terminals or note-book type PCs(Personal Computers), which have rapidly grown in number in this couple of years.

Many researches have been reported aiming to reduce power consumption of VLSIs, proposing new circuit designing methodology, evolving device and process technologies or optimizing signal/supply voltages.

In this chapter, we take a inverter circuit for an example and give a

generalized formulation of power consumption from simulated characteristics of the circuit with physically based device models.

From the simulation results, the supply voltage optima can be found from the view points of the switching energy minimization or the speed maximization under restricted power. These methods are applicable for device/process design of CMOS VLSIs considering the circuit characteristics.

2.2 Formulation of Power Consumption in CMOS Circuits

2.2.1 Power consumption in CMOS circuits

The power consumed in a CMOS circuit is composed of two parts, the dynamic power due to the load capacitance's charging/discharging and the static power due to the leak current of stand-by devices.

It is often mentioned that especially in a CMOS logic circuit the dominant part of the consumed power is the dynamic power, because the leak current of MOSFETs is extremely small when threshold voltages of MOSFETs are sufficiently low comparing with the supply voltage of the circuit.

However, in the recent trend of low supply voltage application for power saving, it is impossible to keep enough margin between the threshold voltage and the supply voltage. The decrease of the supply voltage also causes decrease of the active current, which results increase of the gate delay of a CMOS circuit.

As the result, the contribution of the static power to the whole power consumption is relatively increased in low-voltage circuits and it isn't always effective to reduce the supply voltage for saving the circuit power.

2.2.2 Dynamic power consumption

To evaluate the dynamic power consumption, a transient simulation of switching of a CMOS inverter circuit is carried out(fig.2.1(a)). From the simulation, the supplyed current of the inverter are obtained as a function of time, $I(t)$, along with the gate delay time, τ.

The dynamic power, P_{dyn}, is formulated as eq.(2.1), which is the product of effective frequency of the circuit switching, $\tilde{f}$, and switching energy, E_{sw}.

$$P_{dyn} = \tilde{f} \cdot E_{sw} \tag{2.1}$$

For the effective frequency, we assume that the mean time between switch-

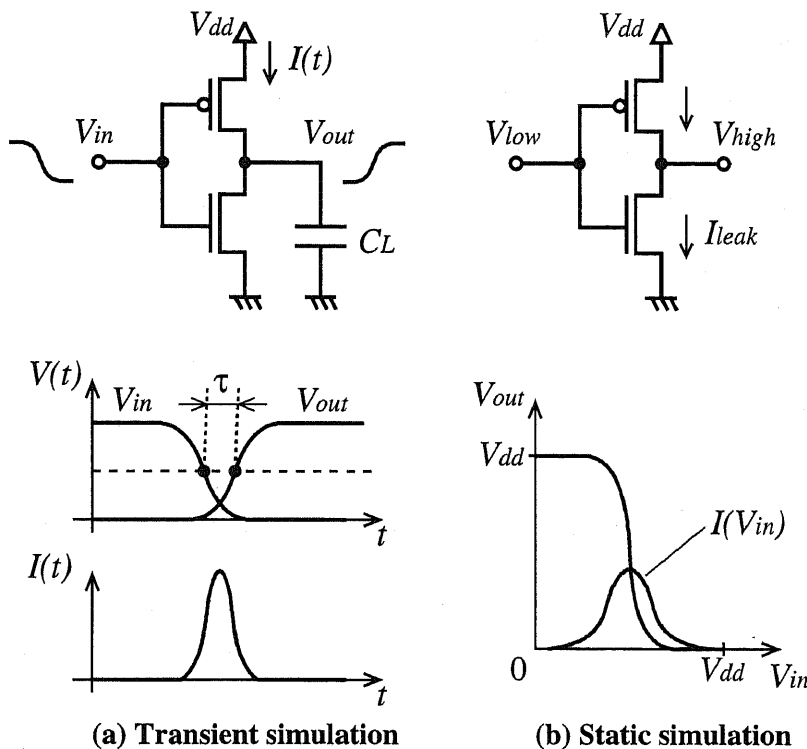

Figure 2.1: Inverter characterization by circuit simulation

ings is determined with the delay time, τ. Then, supposing N_f is a constant which represents the gate activity, $\tilde{f}$ is formulated as eq.(2.2).

$$\tilde{f} = (N_f \cdot \tau)^{-1} \tag{2.2}$$

The switching energy is derived from the supplyed voltage, V_{dd}, and the supplyed current during a switching, $I(t)$, as eq.(2.3).

$$E_{sw} = \int_0^T I(t) \cdot V_{dd} \, dt \tag{2.3}$$

Here, T denotes the period when the switching completes.

2.2.3 Static power consumption

To evaluate the static power consumption, a DC static circuit simulation is carried out and V_{out}-V_{in} characteristics are obtained. Among the characteristics, the input voltage, V_{in}, whose output voltage, V_{out}, is equal to V_{dd}-V_{in} is looked for. Then the leak current, I_{leak}, is given as the supplyed current at this input voltage.

The static power, P_{stat}, is formulated in proportional to the supply voltage and the leak current as eq.(2.4).

$$P_{stat} = I_{leak} \cdot V_{dd} \tag{2.4}$$

2.2.4 Total power and energy consumption

The total power consumption of a CMOS inverter circuit, P_{total} is formulated as the sum of eq.(2.1) and eq.(2.4).

$$\begin{aligned} P_{total} &= P_{dyn} + P_{stat} \\ &= \tilde{f} \cdot E_{sw} + I_{leak} \cdot V_{dd} \end{aligned} \tag{2.5}$$

As the same way, the total energy per switching is formulated as follows.

$$
\begin{aligned}
E_{total} &= \frac{P_{total}}{\tilde{f}} \\
&= E_{sw} + (N_f \cdot \tau) I_{leak} \cdot V_{dd} \qquad (2.6)
\end{aligned}
$$

2.3 Circuit Element Modeling

2.3.1 Requirement of physics-based accurate models

For the accurate device modeling down to sub-threshold gate voltage, we adopt Dunlop's model[2.1] for the MOSFET model in this study, which keeps the continuity of derivatives of the drain current in any region of gate/drain terminal voltage. The fact that the model is described simply with device structural parameters and has few fitting parameters is also favorable for our analysis.

The MOSFET model has a single-drain structure and a uniform channel doping profile as shown in fig.2.2.

The load capacitance, C_L, is also modeled with the device structural parameters with simple assumptions of the gate and drain shape.

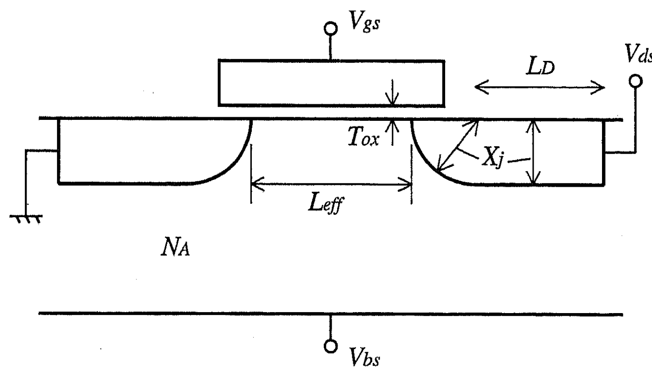

Figure 2.2: Schematic of MOSFET

2.3.2 Drain current modeling of MOSFET

Subthreshold current

The subthreshold drain current is modeled as eq.(2.7) with following equations.

$$I_d^{\text{sub}} = \frac{q\mu_0 W_{eff}}{L_{eff}} \cdot \frac{n_i L_{Bi}}{\sqrt{2}\beta} \cdot \frac{e^{\beta(b'-1)\phi_F} - 1}{\sqrt{\beta(\phi_F - V_{bs}) - 1}} \times e^{-\beta\phi_F/2} \cdot (1 - e^{-\beta V_{ds}}) \quad (2.7)$$

$$b' = b - (1/\beta\phi_F) \cdot \ln(e^{\beta(b-2)\phi_F} + 1) \quad (2.8)$$

$$b \cdot \phi_F = (V_{gs} - V_{FB}) + (F \cdot \gamma)^2 - F\gamma\sqrt{(V_{gs} - V_{FB}) - V_{bs} + \frac{(F\gamma)^2}{4}} \quad (2.9)$$

Here, the parameters presented in above equations are given as follows.

$$\beta^{-1} = \frac{kT}{q} \quad \text{thermal voltage}$$

$$L_{Bi} = \sqrt{\frac{\varepsilon_{si}}{\beta q n_i}} \quad \text{(intrinsic Debey-length)}$$

$$\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} \quad \text{(Fermi potential)}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si} N_A}}{C_{ox}} \quad \text{(body effect coefficient[2.3])}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad \text{(gate-oxide capacitance per unit area)}$$

The flat-band voltage, V_{FB}, is formulated as follows, assuming the n-type polysilicon gates for nMOSFETs.

$$V_{FB} = -0.56 + \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (2.10)$$

The short-channel effect, F[2.4], will be described later.

Linear region

The drain current in the linear region is modeled as follows;

$$I_d^{\text{lin}} = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \{(V_{gs} - V_{on})V_{ds} - \frac{a{V_{ds}}^2}{2}\} \tag{2.11}$$

Here, body-effect coefficiency, a, is assumed 1.0. V_{on} is defined as eq.(2.12) and is equivalent to V_{th} when $b' = 2(b \geq 2$: strong inversion).

$$V_{on} = b'\phi_F + V_{FB} + \gamma F\sqrt{b'\phi_F - V_{bs}} \tag{2.12}$$

This formulation is applicable when $V_{ds} \leq V_{gs} - V_{on}(\equiv V_p)$.

Saturation region

The drain current in the saturation region ($V_{ds} \geq V_p$) is modeled as follows.

$$I_d^{\text{sat}} = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \{(V_{gs} - V_{on})V_p - \frac{a{V_p}^2}{2}\} \tag{2.13}$$

Short-channel effects

To model the short channel effects, we consider the charge sharing model[2.4] in the channel depletion layer(fig,2.3). Then, the short-channel coefficient,

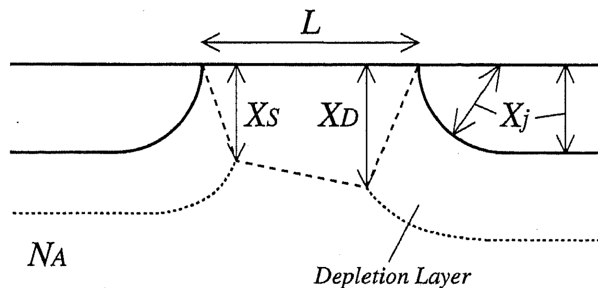

Figure 2.3: Charge sharing model

F, is formulated with following equations.

$$F = 1 - \frac{1}{2}\{F(X_S) + F(X_D)\} \tag{2.14}$$

$$F(X_S) = \frac{X_j}{L}\left(\left\{1 + \frac{2}{X_j}\left[\frac{2\varepsilon_{si}(2\phi_F - V_{bs})}{qN_A}\right]^{\frac{1}{2}}\right\}^{\frac{1}{2}} - 1\right) \tag{2.15}$$

$$F(X_D) = \frac{X_j}{L}\left(\left\{1 + \frac{2}{X_j}\left[\frac{2\varepsilon_{si}(2\phi_F - V_{bs} + V_{ds})}{qN_A}\right]^{\frac{1}{2}}\right\}^{\frac{1}{2}} - 1\right) \tag{2.16}$$

Total current expression

The total drain current, I_d, is expressed as the sum of the subthreshold current and the 'on'-current for the linear or the saturation region. An example of I_d-V_{gs} characteristics of an n-type MOSFET is shown in fig.2.4.

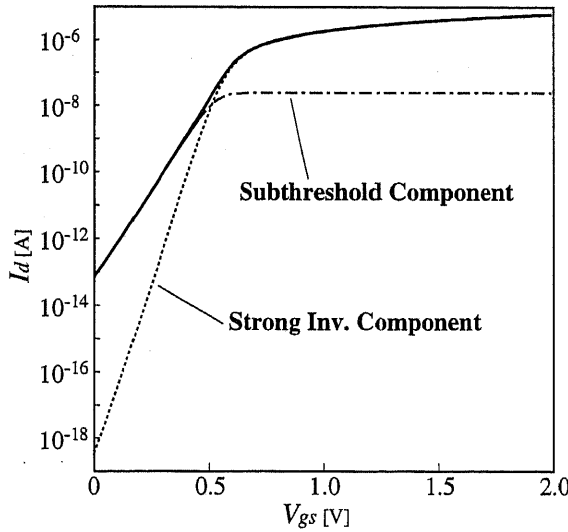

Figure 2.4: I_d-V_{gs} characteristics of nMOSFET
(L_{eff}=W_{eff}=1.0μm, N_A=1.6 $\times$ 10^{16}cm^{-3}, T_{ox}=50nm, V_{ds}=0.1V, V_{bs}=0.0V)

2.3.3 Load capacitance model

To model the load capacitance, we take into account the intrinsic gate capacitance and drain junction capacitance. The gate fringe capacitance and the metal wire capacitance are neglected simply because these are deeply dependent on the process technologies.

The intrinsic gate capacitance is formulated as eq.(2.17), assuming F_o is the effective fan-out number.

$$C_{inv} = C_{ox} \cdot W_{eff} \cdot L_{eff} \times 2 \times F_o \tag{2.17}$$

For the junction capacitance, we estimate difference of the maximum and the minimum thickness of depletion layer from the supplyed voltage and the spatial charge in the intermediate region, ΔQ, with eq.(2.18)(fig.2.5).

$$\Delta Q = qN_A W_D [L_D(W_{max} - W_{min}) + \frac{\pi}{4}\{(W_{max} + X_j)^2 - (W_{min} + X_j)^2\}^{\frac{1}{2}}] \tag{2.18}$$

$$W_{min} = \left[\frac{2\varepsilon_{si}(2\phi_F - V_{bs})}{qN_A}\right]^{\frac{1}{2}} \tag{2.19}$$

$$W_{max} = \left[\frac{2\varepsilon_{si}(2\phi_F - V_{bs} + V_{dd})}{qN_A}\right]^{\frac{1}{2}} \tag{2.20}$$

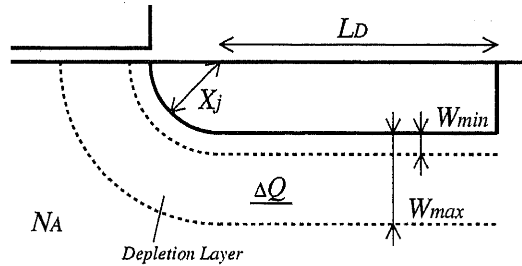

Figure 2.5: Junction capacitance modeling

In eq.(2.18), the first term of right hand is for the plate capacitance below the drain diffusion and the second term is for the rounded capacitance at the edge of the drain-channel junction.

Then the junction capacitance is formulated as follows.

$$C_{junc} = \frac{\Delta Q}{V_{dd}} \tag{2.21}$$

2.4 Calculation Results

2.4.1 Basic characteristics of a CMOS inverter circuit

Examples of simulated basic characteristics of a inverter circuit, the switching energy, E_{sw}, the delay time, τ, and the static leak current, I_{leak}, are shown

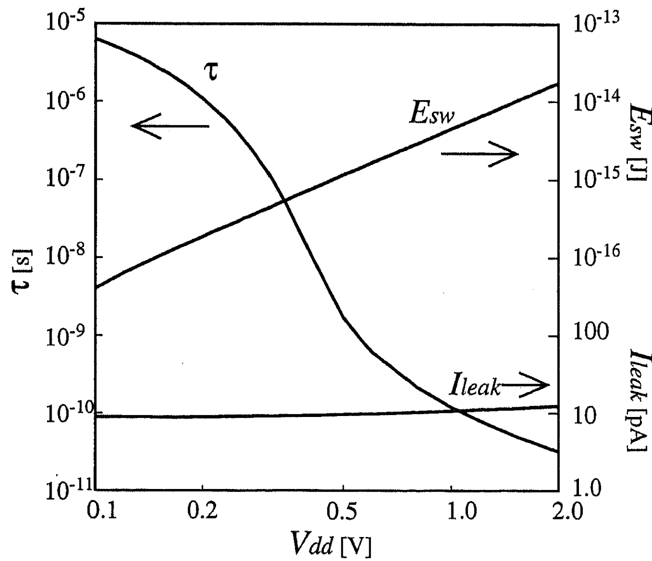

Figure 2.6: Basic characteristics of CMOS inverter circuit (L_{eff} = 0.7μm,$W_{eff} = 1.0\mu$m, $N_A = 4.0 \times 10^{16}$cm^{-3}, T_{ox} = 16nm)

in fig.2.6, for the functions of the supply voltage, V_{dd}. In this analysis, the junction depth, X_j, is fixed to $0.1[\mu m]$.

The threshold voltage of the device is estimated to 0.28[V]. The switching energy, E_{sw}, increases in proportional to the square of the supply voltage, V_{dd}. The leak current, I_{leak}, shows slight increase with V_{dd} increase. The delay time, τ, increases dramatically with V_{dd} decrease. When $V_{dd} < 0.5$[V], τ is inversely proportional to the logarithm of V_{dd}, while the logarithm of τ is inversely proportional to the logarithm of V_{dd} when $V_{dd} > 0.5$[V].

2.4.2 Evaluation of consumed energy per switching

Figure 2.7 shows the characteristics of the total energy consumption per switching, E_{total}, for three cases of the channel dopant density, N_A. E_{total} decreases as V_{dd} decreases for higher supply voltage than 0.5[V], and turns to increase for lower supply voltage due to the fact that the leak current becomes dominant compared to the switching energy. The minimum switching energy is realized at a supply voltage ranging from 0.2[V] to 0.5[V] depending on N_A. In this analysis, the constant for the effective frequency, N_f, is set to 1000.

Figure 2.8 shows the characteristics of E_{total} for three cases of the gate oxide thickness, T_{ox}. As same as the N_A cases, the minimum switching energy is also realized at a supply voltage for each device.

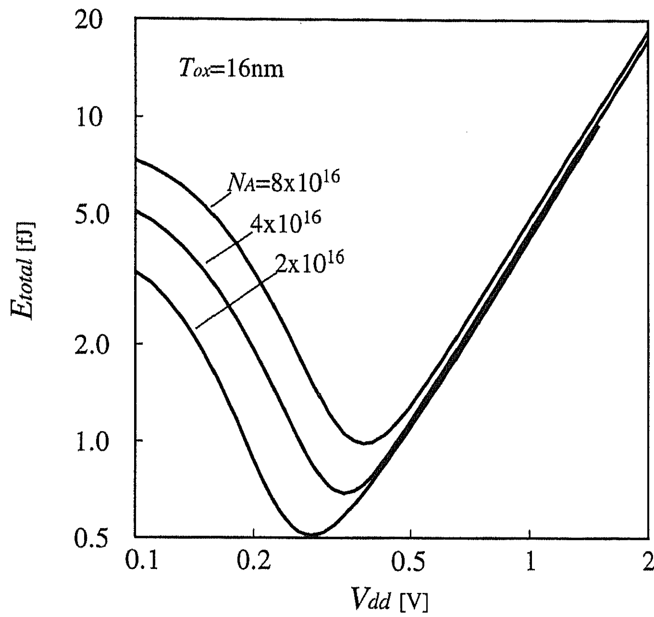

Figure 2.7: Total switching energy of inverter circuit, N_A as parameter ($L_{eff} = 0.7\mu$m,$W_{eff} = 1.0\mu$m)

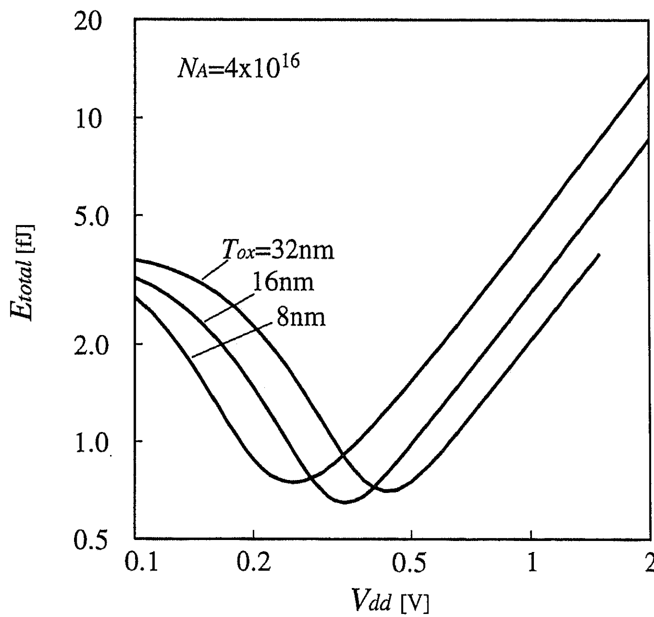

Figure 2.8: Total switching energy of inverter circuit, T_{ox} as parameter ($L_{eff} = 0.7\mu$m,$W_{eff} = 1.0\mu$m)

2.5 Conclusion

In this chapter, following works were presented.

1. Evaluation methods for the energy consumption per switching and the power consumption of CMOS circuits were presented using circuit simulation with physically based analytical models.

2. As shown in sample results of a CMOS inverter circuit, existence of the optimum supply voltage for the energy consumption minima was proved.

3. From the results of devices with different design parameters, it was proved that the minimum switching energy and the optimum supply voltage are determined depending on device parameters

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Chapter 3

Device Parameter Optimization for Low Power VLSIs using Circuit Simulation

3.1 Introduction

As described in chapter 2, circuit performance deeply depends on the device parameters and the supply voltage of the circuit. Namely, optimizing the device parameters and the supply voltage is one way to realize well designed circuits.

In this chapter, we demonstrate an optimization scheme of MOSFETs with the energy and power consumption evaluation method using CMOS inverter simulation presented in chapter 2.

The device parameters are optimized in terms of the absolute minimum switching energy or the minimal delay time under a constraint of the maximum circuit power. Those criteria are useful in design of portable equipments which require less speed but longer operation time.

The parameters to be optimized are the channel dopant density, N_A,

and the gate oxide thickness, T_{ox}, along with the optimization of the supply voltage, V_{dd}.

3.2 Circuit Optimization Criteria

3.2.1 Switching energy optimization

The evaluation factor firstly introduced is the total energy per switching, E_{total}, described as eq.(2.6).

This criterion will be useful for absolute reduction of the operating power where battery lifetime is of the first importance.

With recent VLSI technologies, the requirement for high-speed operation of VLSIs is not as the matter as the requirement for long term operation, especially in portable machineries. Further more, low-speed circuits can be accelerated by the parallel operations. Then, it can be concluded that the most concerning factor for the low power operation of VLSIs is the total energy consumption per switching of each circuit element.

3.2.2 Power consumption and circuit speed optimization

The other evaluation factor is the power consumption which is formulated as eq.(2.5).

This evaluation is important in such case that chip power is a key factor to determine the package cost.

When the maximally acceptable power consumption per chip, P_{chip}, is given from thermal problems or battery limits, there is a maximally supplyable voltage, V_{dd}^{opt} and in most case it gives the minimum delay time of the circuit, τ_{min} (fig.3.1).

This restriction for the power consumption of a inverter circuit, P_{total}, is described as:

$$P_{total} \leq \frac{P_{chip}}{N_{inv}} \quad (3.1)$$

Here, N_{inv} is the effective number of CMOS logic gates in a chip, assuming all gates are inverters.

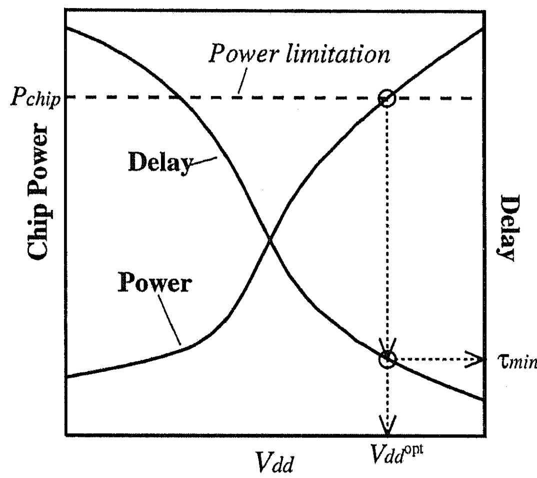

Figure 3.1: Circuit speed limitation with power restriction

3.3 Restrictions for Device Parameter Ranges

Device parameters have the maximum and the minimum limitations of values determined by several physical factors[3.1].

In this study, we take into consideration the limitations from the bulk punch-through phenomena and the drain-induced barrier lowering and the avalanche breakdown at the drain junction. The device parameters and the supply voltage are ranged in the accepted region.

3.3.1 Limitations from bulk punch-through phenomena

In short-channel MOSFETs, the depleted region of the drain junction and the source junction are grown by the drain and the substrate bias and often touch each other in the substrate and current flows through the depleted region, even if the channel does not induced at the oxide interface. This is the bulk punch-through phenomena.

The device parameter limitations from the bulk punch-through is formulated as follows with a model shown in fig.3.2[3.2].

$$L > \left[(X_j + W_S)^2 - W_C^2\right]^{\frac{1}{2}} + \left[(X_j + W_D)^2 - W_C^2\right]^{\frac{1}{2}} - 2X_j \qquad (3.2)$$

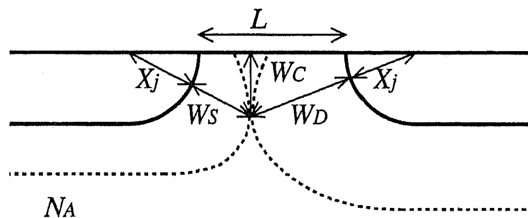

Figure 3.2: Bulk punch-through

Here, W_C is the depth where the punch-through occurs and it is obtained from the solutions of eq.(3.3). W_S and W_D are equivalent to W_{min} and W_{max} (eq.2.19 and 2.20) in chapter 2, respectively.

$$\begin{cases} W_C = \left[\dfrac{2\varepsilon_{si}(2\phi_S - V_{BS})}{qN_A}\right]^{\frac{1}{2}} \\ V_{GS} = V_{FB} + \phi_S + \dfrac{qN_A W_C}{C_{ox}} \end{cases} \tag{3.3}$$

3.3.2 Limitations from drain-induced barrier lowering

In short-channel MOSFETs, electric field by the drain potential reduces the channel potential and this causes various subthreshold characteristics degenerations. The parameter limitations from this drain-induced barrier lowering(DIBL) effect is modeled as follows in ref.[3.3].

$$L > 0.41\left[X_j T_{ox}(W_S + W_D)^2\right]^{\frac{1}{3}} \tag{3.4}$$

3.3.3 Limitations from avalanche break down

The avalanche break down at the drain junction has two critical regions, the first one is the junction corner and the second is the oxide surface.

The first limitation for the supply voltage from the corner break down is expressed as follows[3.4].

$$V_{BD} = 60\left(\frac{E_g}{1.1}\right)^{3/2}\left(\frac{N_A}{tens16}\right)^{-3/4}\gamma_{sp} \tag{3.5}$$

$$\gamma_{sp} = \zeta^2 + 2.14\zeta^{6/7} - (\zeta^3 + 3\zeta^{13/7})^{2/3} \tag{3.6}$$

$$\zeta = \frac{X_j}{W_d} \tag{3.7}$$

Here, E_g is the bandgap energy of bulk silicon and γ_{sp} represents the the spherical curvature effect at the drain junction corner.

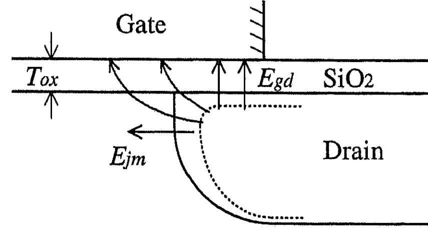

Figure 3.3: Surface avalanche breakdown concerning effective field

The second limitation by the surface break down is expressed as:

$$E_{dx} \leq E_{AV,crit} \tag{3.8}$$

where E_{dx} is the surface field parallel to the Si-SiO_2 interface at zero gate bias and $E_{AV,crit}$ (=1.4[MV/cm]) is the critical field for the surface avalanche breakdown[3.5]. E_{dx} is formulated as follows with E_{gd} and E_{jm}, which represent the vertical field at the drain-gate overlap region and the maximum lateral field at the drain-substrate junction, respectively[3.6](fig. 3.3).

$$E_{dx} = \frac{2}{\pi} E_{gd} + E_{jm} \tag{3.9}$$

$$E_{gd} = \left[\left(\frac{q N_D T_{ox}}{\varepsilon_{ox}} \right)^2 + \frac{2 q N_D (V_{BD} - V_{FB})}{\varepsilon_{si}} \right]^{1/2} = \frac{q N_D T_{ox}}{\varepsilon_{ox}} \tag{3.10}$$

$$E_{jm} = \left[\frac{2 q N_D (V_{BD} - V_{FB})}{\varepsilon_{si}} \right]^{1/2} \tag{3.11}$$

3.4 Device Parameter Optimization

3.4.1 Switching energy optimization

By the first optimization criterion(sec.3.2.1), the devices parameters and the supply voltage are optimized for the minimum total energy per switching, E_{total}.

In Fig.3.4, the minimum value of the total switching energy E_{total} is plotted with contours on the parameter space of (N_A, T_{ox}). Though the parameter space is limited by DIBL effect[3.1], the absolute minimum energy of a device with L_{eff}=0.25[μm] and W_{eff}=1.0[μm] is about 0.048[fJ] at $N_A = 1.65 \times 10^{16}$[cm^{-3}], T_{ox} = 19.4[nm] and the delay time of 0.33[ns] for

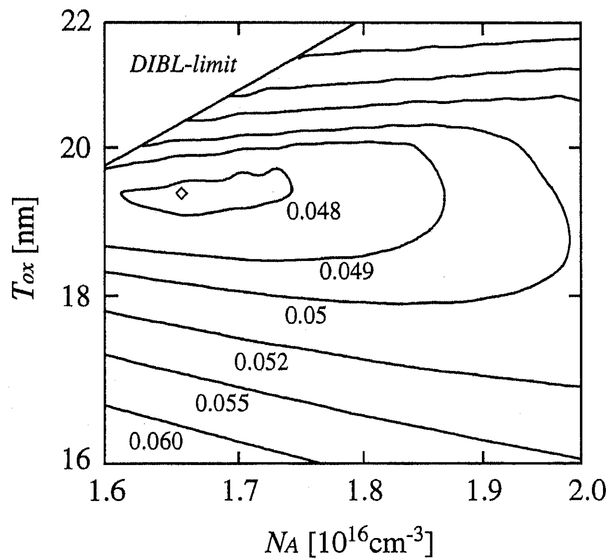

Figure 3.4: Minimum value of total switching energy [fJ]
($L_{eff} = 0.25\mu m$, $W_{eff} = 1.0\mu m$)

the supply voltage of V_{dd}=0.13[V]. In this analysis, N_f=100 is assumed.

Figure 3.5 shows the channel length, L_{eff}, dependent optimum device parameters for the minimum energy consumption. As the channel length is scaled down, the optimum gate oxide thickness decreases and the channel dopant density increases. The oxide thickness and the dopant density show the linear relationship in the logarithmic plot.

Figure 3.6 shows the minimum energy, E_{min}, the optimum supply voltage, V_{dd}^{opt}, and the delay time, τ^{opt}, for various channel length. As the channel length is scaled down, τ^{opt} decreases with a linear relation in the log-scale, but E_{min} and V_{dd}^{opt} show slight relationships with the channel length. This is because the optimum device with long channel has relatively thick gate

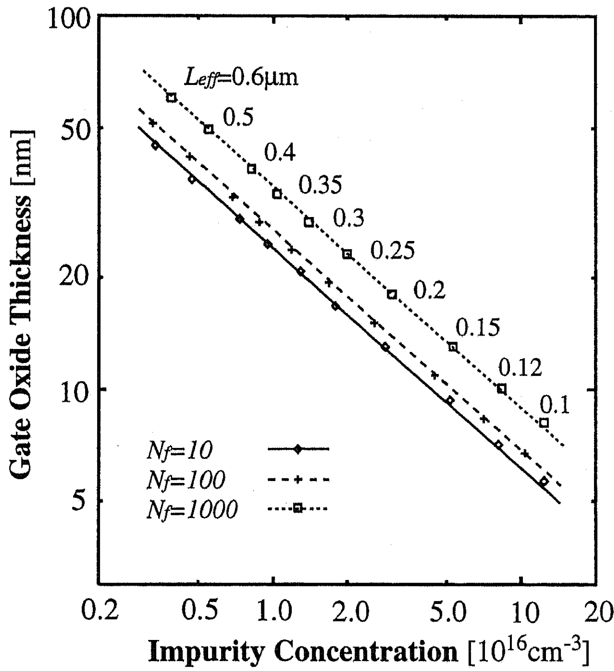

Figure 3.5: Channel length dependent optimum device parameters (N_A, T_{ox}) for the minimum energy consumption

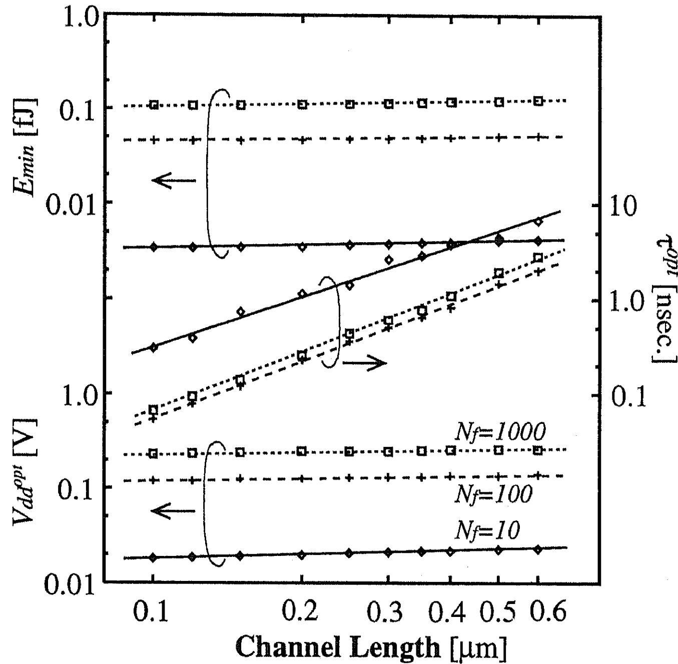

Figure 3.6: Dependence of the minimum energy, E_{min}, the optimum supply voltage, V_{dd}^{opt}, and the optimum gate delay, τ^{opt} on the channel length

oxide and has small gate capacitance per area, then, the total capacitance is almost at the same order in each device.

The energy minimizing optimum device parameters are shown in fig.3.7 for the fan-out(F.O.)=1,2 and 3. The optimum parameters are almost independent of the fan-out number.

Figure 3.8 shows the fan-out dependence of the minimum energy, E_{min}, the optimum supply voltage, V_{dd}^{opt}, and the delay time,τ^{opt}. V_{dd}^{opt} characteristics are also independent of the fan-out number. Thus, all of the device design parameters are optimized uniquely independent of the fan-out. The increase of τ^{opt} and E_{min} are simply explained by the increase of the load capacitance which are caused by increase of the gate capacitance.

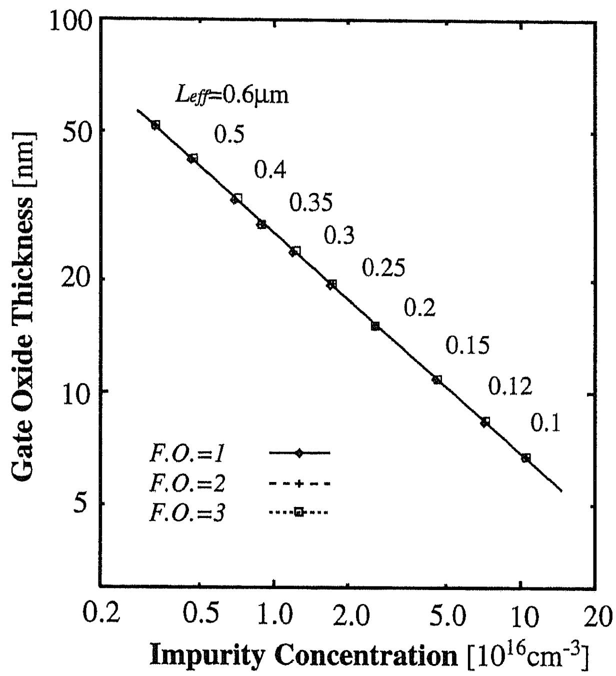

Figure 3.7: Channel length dependent optimum device parameters (N_A,T_{ox}) for fan-out(F.O)=1,2, and 3

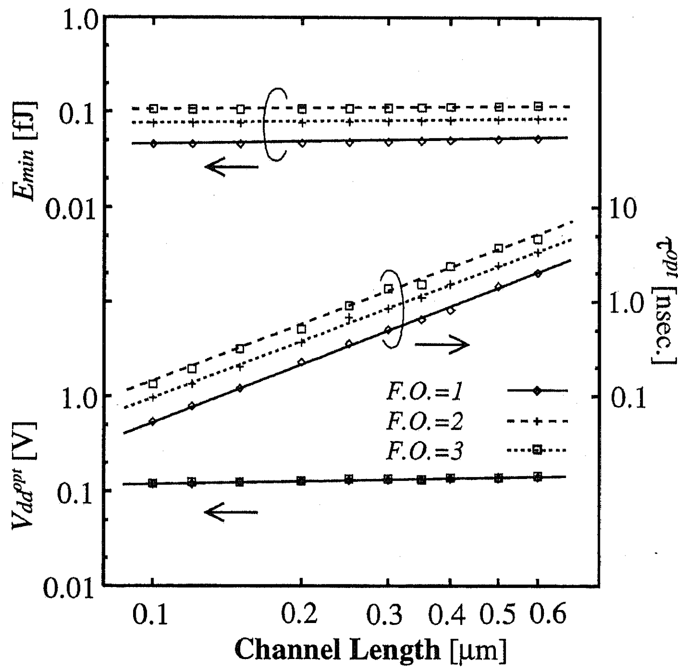

Figure 3.8: Fan-out dependent minimum energy, E_{min}, optimum supply voltage, V_{dd}^{opt}, and optimum gate delay, τ^{opt}

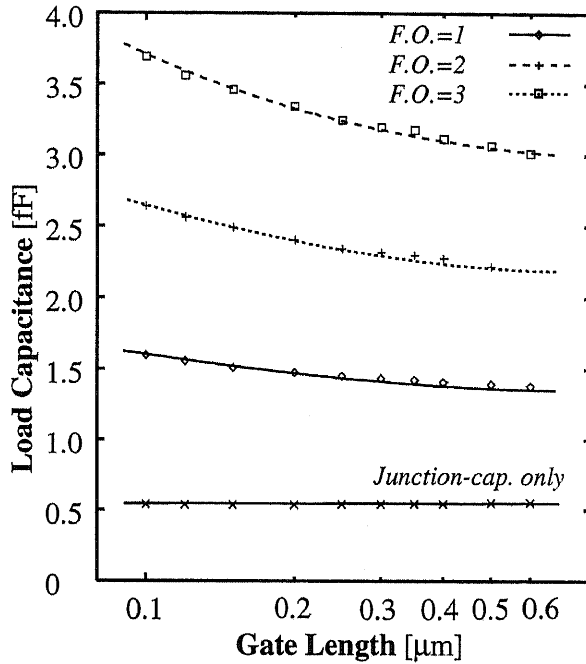

Figure 3.9: Channel length dependent optimum load capacitance, C_L, and junction capacitance, C_J, for the minimum energy (F.O.=1,2,3)

The optimized load capacitance, C_L, are shown in fig.3.9 for F.O.=1,2 and 3, along with the junction capacitance component, C_j, which is also included in the load capacitance. The optimum junction capacitance is independent of both the channel length and the fan-out number. The optimum load capacitance increases as the channel length decreases, because even the gate area decreases as the channel length shrinks, the optimum gate oxide thickness, T_{ox}, also decreases and the gate capacitance which is determined by the gate area and the oxide thickness increases consequently.

3.4.2 Delay time minimization under restricted chip power

By the second optimization criterion(sec. 3.2.2), the device parameters and the supply voltage are optimized for the minimum delay time under a restricted chip power.

In fig.3.10, the minimum delay time, τ_{min}, is plotted with contours on the parameter space of (N_A, T_{ox}). The optimum supply voltage is shown in fig.3.11 for the parameters. The absolute minimum delay of a device with L_{eff}=0.25μm and W_{eff}=1.0[μm] is about 4.4[ps] at N_A=5.0$\times 10^{16}$[cm^{-3}] and T_{ox}=7.8[nm] for the supply voltage of V_{dd}=1.1[V]. In this analysis, N_f=100, P_{chip}=10.0[W] and $N_{inv}=10^6$ are assumed.

In fig.3.12, the channel length, L_{eff}, dependent optimum device parameters for the minimum delay time are shown. The conditions for the analysis are as same as those described above. Similar to the energy optimum results, as L_{eff} is scaled down, the optimum gate oxide thickness decreases and the channel dopant density increases. The oxide thickness and the dopant density also show the linear relationship in the logarithmic plot.

Figure 3.13 shows the characteristics of the minimum delay time, τ_{min}, and the optimum supply voltage, V_{dd}^{opt}, on the channel length. τ^{min} and V_{dd}^{opt} decrease as the channel length is scaled down.

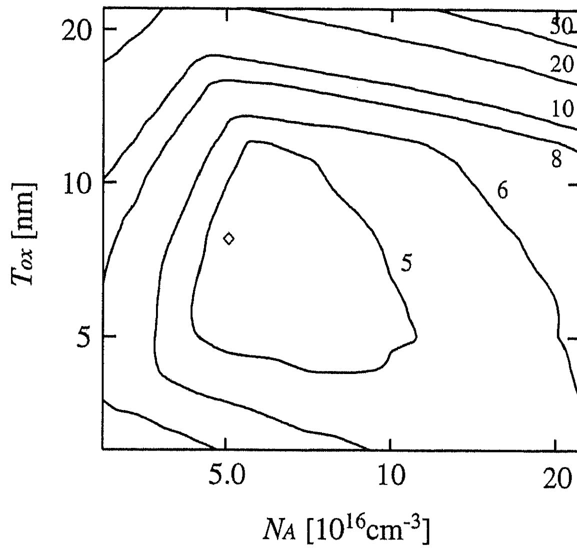

Figure 3.10: The minimum delay time ([ps]) under restricted chip power (L_{eff}=0.25μm, W_{eff}=1.0μm, P_{chip}=10.0μW)

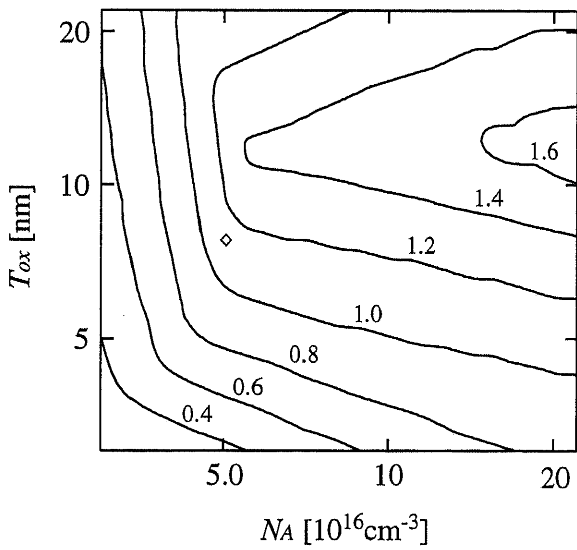

Figure 3.11: The optimum supply voltage for the minimum delay time under restricted chip power (L_{eff}=0.25μm, W_{eff}=1.0μm, P_{chip}=10.0μW)

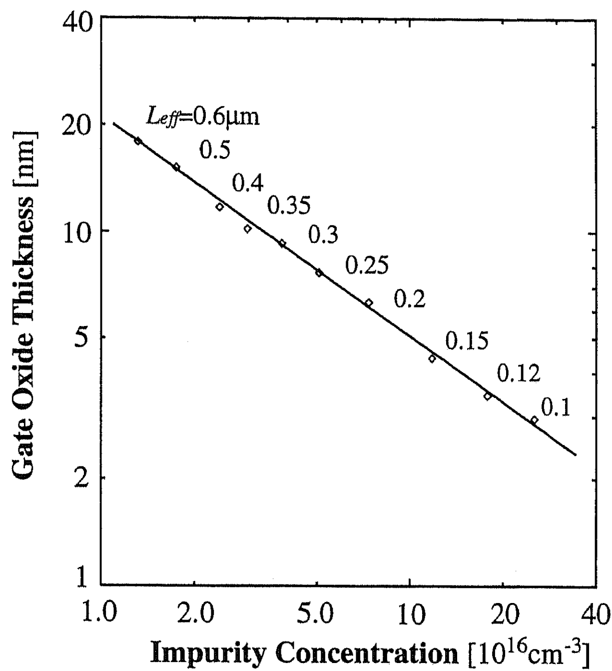

Figure 3.12: Channel length dependent optimum device parameters (N_A,T_{ox}) for the minimum delay time under restricted chip power

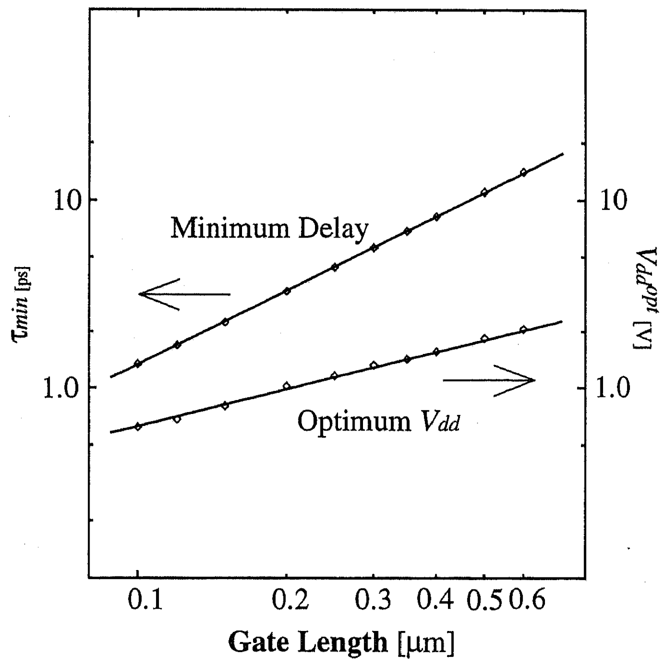

Figure 3.13: Dependence of minimum delay time, τ_{min}, and optimum supply voltage, V_{dd}^{opt}, under restricted chip power on the channel length

3.5 Conclusion

Following works were presented in this chapter.

1. Two optimization criteria for VLSI device parameters were presented based on the energy and power evaluation method with circuit simulation presented in chapter 2.

2. Device parameter optimization for the minimum switching energy was demonstrated with scaling of the channel length.

    - The minimum energy per switching was not scaled while the delay time was scaled down as the channel length decreases, in case the device width is not scaled down.
    - The optimized device parameters and the supply voltage are independent of the fan-out number of the logic gates.
    - The optimized load capacitance increases as the channel length shrinks.
    - It can be concluded that the essential merits of the channel length scaling of MOSFET are for the speed and the area advantages, not for the energy and the power advantages.

3. Device parameter optimization for the minimum delay under a given maximum power par chip was demonstrated.

    - The trends of the optimum device parameters and the supply voltage with the scaling of the channel length were shown.
    - The optimum supply voltage is scaled down as the channel length shrinks for the optimized minimum delay.

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Chapter 4

Device Parameter Estimation of SOI MOSFETs using One-Dimensional Numerical Simulation for Subthreshold Characteristics

4.1 Introduction

Semiconductor devices with SOI(Silicon-On-Insulator) structures were firstly introduced about 30 years ago. On their primitive stage, SOI devices were taken notice of for their capabilities for three-dimensional integrated circuits, their applicabilities for high voltage devices, and their performance of radiation hadness[4.1]. SOI devices were made on relatively thick silicon layers on their first stage.

SOI MOSFETs at that time have been developed in respect to the improved short-channel effects comparing with bulk MOSFETs, by suppressing the bulk-punch through and by reducing the parasitic capacitance and the

junction leak. In contrast, SOI devices with thick silicon layers suffered from the particular problems such as the kink-effects with the floating body features of SOI devices.

Fully-depleted SOI MOSFETs, firstly proposed by Malhi[4.2], have very thin silicon layers(thin-film SOI layers) of 10~100[nm] and are almost free from the kink effects. They also show the small parasitic capacitance, which enable fast and low-power circuit operations. But, as for other SOI features, they still have a lot of problems to be solved.

On the other hand, in thin-film SOI devices, the substrate bias has a great influence on the subthreshold characteristics of MOSFETs such as the threshold voltage, V_{th}, and the subthreshold swing, S. Those characteristics are also affected by the structural device parameters of the SOI multi-layer structure[4.3][4.4][4.5].

In this chapter, we present a one-dimensional Poisson equation based device simulation method for the subthreshold characteristics of SOI MOSFETs. Since only one-dimensional numerical calculations are needed in this simulator, extremely fast and efficient analyses can be realized.

Using the simulator, estimation of the device parameters of real SOI multi-layer structure is demonstrated by fitting the simulated characteristics with measured data. For the subthreshold characteristics to be fitted, substrate bias, V_{bs}, dependent threshold voltage, V_{th}, characteristics are measured on real devices and are also evaluated with the one-dimensional simulator.

4.2 One-Dimensional Numerical Simulation of SOI MOSFETs

4.2.1 Basic equations for One-dimensional Poisson equation based device simulation

In this section, a one-dimensional(1-D) device simulation method for SOI MOSFET is formulated basing on only the Poisson equation. While conventional two- or three-dimensional device simulators are composed of three basic equations of the Poisson equation and the continuity equations for electrons and holes, our one-dimensional subthreshold simulation needs only Poisson equation in one-dimensional form(eq.4.1) to be solved. The continuity equations of carriers are absent from the numerical model, by assuming the thermal-equilibrium conditions for electrons and holes(eq.4.2).

$$\frac{d}{dx}\left\{\varepsilon\frac{d}{dx}\psi(x)\right\} = -q\{N_A - n(x) + p(x)\} \tag{4.1}$$

$$\left\{\begin{array}{lll} n(x) & = n_i \exp\left[\frac{q}{kT}\psi(x)\right] & : \text{in SOI layer} \\ n(x) & = n_i \exp\left[\frac{q}{kT}\{\psi(x) - V_{bs}\}\right] & : \text{in substrate} \\ p(x) & = n_i^2/n(x) & \end{array}\right. \tag{4.2}$$

Here, N_A is the ionized impurity density in the SOI layer or in the substrate, and n_i is the intrinsic carrier density in bulk silicon.

The SOI multi-layer structure is modeled as fig.4.2, as the vertical cross section of an SOI MOSFET (**A—B** in fig.4.1). The finite differential method[4.6] is applied to solving the Poisson equation to obtain potential distribution, $\psi(x)$. The carrier density, $n(x)$ and $p(x)$, are calculated by eq.(4.2). The Poisson equation and the carrier equations are solved alterna-

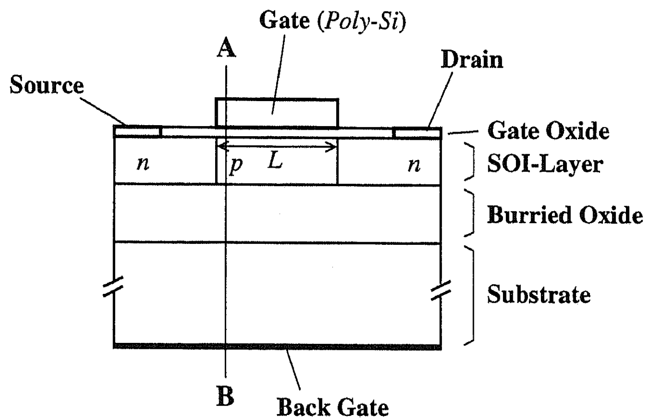


Figure 4.1: Schematic cross section of SOI MOSFET

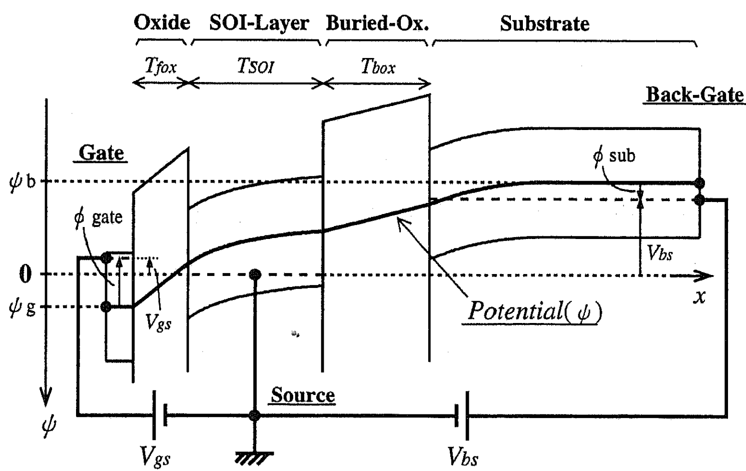


Figure 4.2: 1-D device simulation of SOI MOSFET with front/back bias conditions (cross-section **A**—**B** in fig.4.1)

tively until revisions of the potential distribution are sufficiently small, and then, the self-consistent solution is obtained.

Boundary conditions for the simulation are given as bias voltages for the gate(front-gate), V_{gs}, and for the substrate(back-gate), V_{bs}, as follows.

$$\begin{cases} \psi_{\mathrm{g}} &= V_{gs} - \phi_{\mathrm{gate}} \\ \psi_{\mathrm{b}} &= V_{bs} - \phi_{\mathrm{sub}} \end{cases} \tag{4.3}$$

Here, ϕ_{gate} is the work-function difference of silicon and n-type-doped polysilicon. ϕ_{sub} is shift of the Fermi level in the substrate by the ionized impurity, which is formulated as:

$$\phi_{\mathrm{sub}} = \frac{kT}{q} \log\left(\frac{N_{sub}}{N_i}\right) \tag{4.4}$$

assuming N_{sub} is the ionized impurity density in the substrate.

4.2.2 Drain current modeling

From the potential and the carrier distributions in the SOI layer, the drain current, I_d, is calculated as eq.(4.5), which is composed of only the diffusion current term. The drift current term is not taken into account because the major conduction mechanism is the carrier diffusion in the subthreshold region of MOSFET operations[3.4].

$$I_d = \frac{qW}{L} \int_0^{T_{SOI}} D(x)\{n_s(x) - n_d(x)\}dx \tag{4.5}$$

Here, $D(x)$ is the electron diffusibility and $n_s(x)$ and $n_d(x)$ are electron densities at depth of x from the front surface of SOI layer near source and drain, respectively.

In this analysis, $n_s(x)$ is calculated from the one-dimensional analysis based on the Poisson equation described above. On the other hand, $n_s(x)$ is assumed to be 0, because the carrier density near the drain is sufficiently

small comparing with that near the source, when the diffusion current is dominant.

The electron diffusibility, D, is proportional to the electron mobility, μ, by the Einstein's relationship as:

$$D(x) = \frac{kT}{q} \cdot \mu(x) \tag{4.6}$$

Consequently, the drain current is summarized as following form, where $n_s(x)$ is replaced with $n(x)$.

$$I_d = \frac{qW}{L} \cdot \frac{kT}{q} \int_0^{T_{SOI}} \mu(x)n(x)dx \tag{4.7}$$

We took into account the scattering effects by the lattice temperature, the ionized impurity[4.7] and the surface roughness[4.8] for the mobility model in this analysis.

Finally, we introduce the effective mobility for describing the relationship between the total carrier number and the drain current. The effective mobility, μ_{eff}, is defined as:

$$\mu_{eff} = \frac{1}{N_I} \int_o^{SOI} \mu(x)n(x)dx \tag{4.8}$$

where

$$N_I = \int_o^{SOI} n(x)dx \tag{4.9}$$

Here, N_I represents the sheet density of the electrons in the SOI layer.

Then, the drain current can be simply described as eq.(4.10) with the effective mobility and the sheet density of electrons.

$$I_d = \frac{qW}{L} \cdot \frac{kT}{q} \cdot \mu_{eff} \cdot N_I \tag{4.10}$$

4.3 Evaluation of One-Dimensional Device Simulator and Device Parameter Estimation

4.3.1 Accuracy of one-dimensional device simulator

One-dimensional simulation results of I_d-V_{gs} characteristics of n-type SOI MOSFETs with several channel length are shown in fig.4.3, along with the results by two-dimensional device simulation with the same model parameters.

For rather long-channel devices (1.0 and 2.0[μm]), the one-dimensional results show good agreement with the two-dimensional results in the subthreshold region. They show different results on the 0.3[μm] device because of the short-channel effects. In high gate voltage region where the drift current term is the major conduction mechanism, the one- and two-dimensional results show much differences, because of the absence of the drift term from the one-dimensional model.

Figure 4.4 shows substrate bias dependence of the subthreshold characteristics by the one- and the two-dimensional simulation for a device of L=1.0[μm]. They also show good agreement in the subthreshold region.

Calculation time of each curve is about 1 hour for two-dimensional simulations and less than 1 second for one-dimensional simulations.

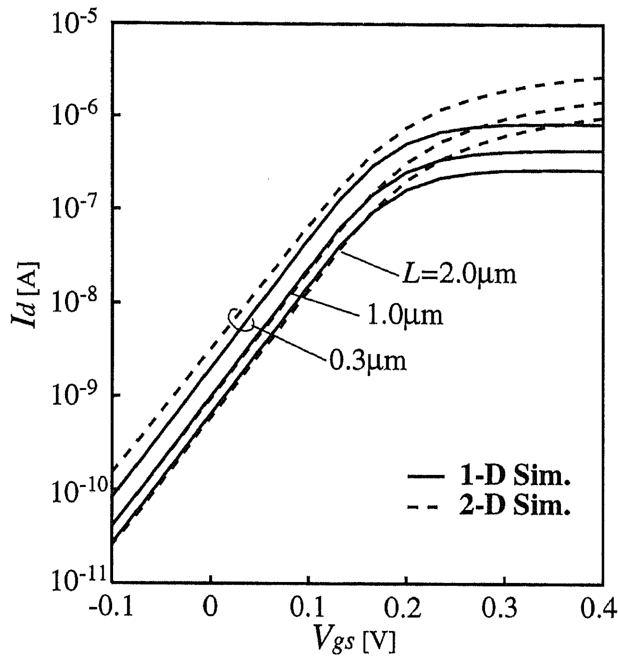


Figure 4.3: Channel length dependent I_d-V_{gs} characteristics of n-type SOI MOSFET; *solid-line: 1-D, dashed-line: 2-D* (W=1.0μm, N_A=1.5×10^{17}cm^{-3})

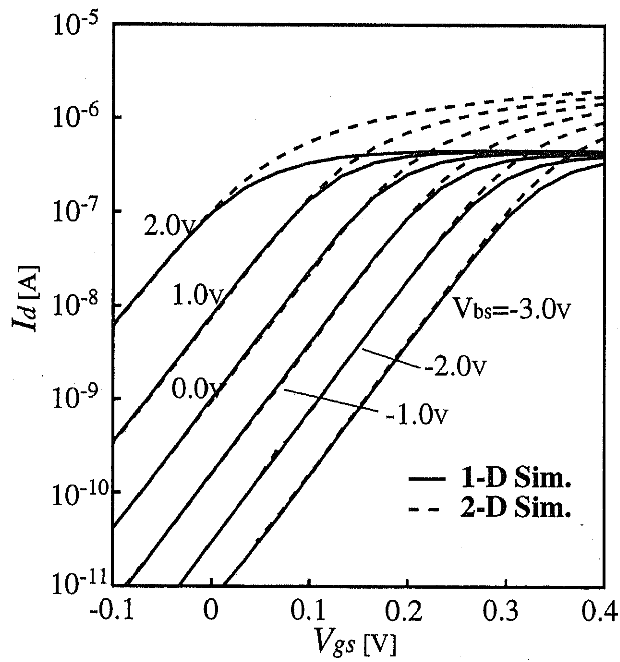


Figure 4.4: Substrate bias dependent I_d-V_{gs} characteristics of n-type SOI MOSFET; *solid-line: 1-D, dashed-line: 2-D* (W=1.0μm, N_A=1.5×10^{17}cm^{-3})

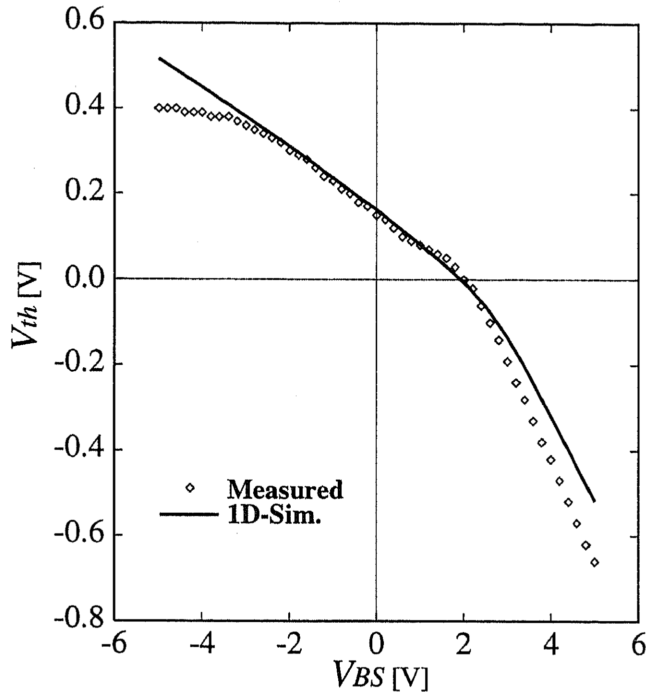


Figure 4.5: V_{th}-V_{bs} characteristics of n-type SOI MOSFET; *points: measured, line: 1-D simulation with 'designed' parameters* (L=W=100 μm)

4.3.2 Threshold voltage characteristics with substrate bias condition

V_{th}-V_{bs} characteristics were measured for n-type SOI MOSFETs fabricated by SIMOX technology[4.9]. Here, the threshold voltage is defined as the gate voltage where I_d=10[nA] for the device of L=W=100[μm]

Figure 4.5 shows the measured V_{th}-V_{bs} characteristics with the simulated characteristics by the one-dimensional subthreshold simulator. In this simulation, the device parameters were given as described in *'designed'* column of table 6.4. In these results, the measured and the simulated characteristics show much differences over the whole substrate bias region.

4.3.3 Device parameter estimation

The simulated V_{th}-V_{bs} characteristics curve was fitted with the measured data by tuning device parameters in the SOI multi-layer structure. The parameters fitted here were the channel dopant density, N_A, the thickness of gate oxide, T_{fox}, the thickness of SOI layer, T_{SOI}, and the thickness of buried oxide, T_{box}.

The curve fitting was carried out by the steepest descent method in the four-dimensional parameter space evaluating a mean-square error function;

$$\Delta = \sum_i \{V_{th}^{\mathrm{mes}}(V_{bs}^i) - V_{th}^{\mathrm{sim}}(V_{bs}^i)\}^2 \tag{4.11}$$

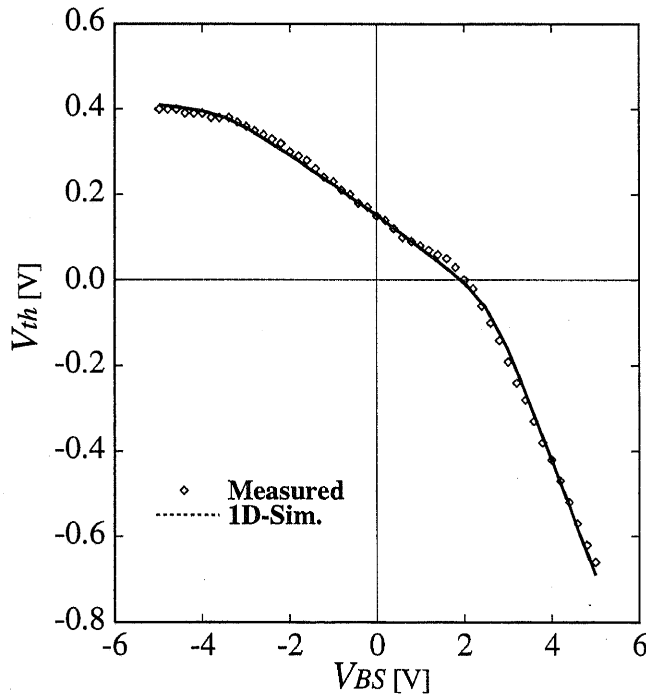


Figure 4.6: V_{th}-V_{bs} characteristics of n-type SOI MOSFET; *points: measured, line: 1-D simulation with 'fitted' parameters* (L=W=100 μm)

Table 4.1: Designed and estimated device parameters of SOI MOSFET

		designed	*fitted*
N_A	$[10^{17}\text{cm}^{-3}]$	—	2.36
T_{fox}	[nm]	7	6.43
T_{SOI}	[nm]	30	41.3
T_{box}	[nm]	80	70.7

Here, i denotes data index, V_{th}^{mes} and V_{th}^{sim} are the measured and the simulated threshold voltage at substrate bias, V_{bs}^{i}, respectively.

Figure 4.6 shows the fitted V_{th}-V_{bs} curve with the measured data. In table 4.1, designed and fitted device parameters are described.

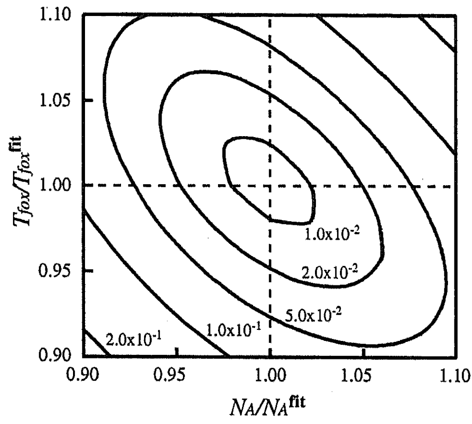
4.4 Property of parameter fitting results

Here, we examine the property of the parameter fitting results with the steepest descent method.

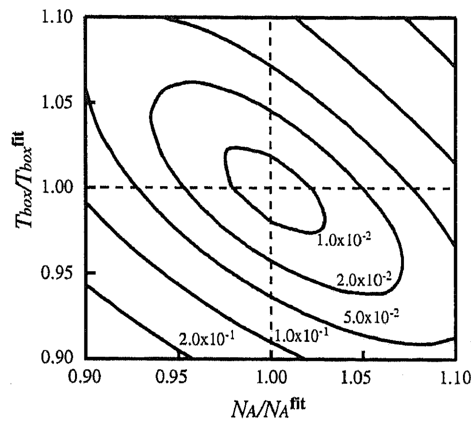
In fig.4.7, the mean-square errors are plotted with contours by two-dimensional cross sections of the four dimensional parameter space around the fitted parameter set. They show hyper-ellipsoid like distributions in the four-dimensional space.

To evaluate the efficiency and the property of the fitting results, the Laplacian matrix of mean-square errors around the optimum point is calculated numerically. In this analysis, the square roots of eigenvalues of the matrix represent length of axes of the hyper-ellipsoid. Then, the ratio of the longest axes and the shortest axes represents the sufficiency and the robustness of the steepest descent method.

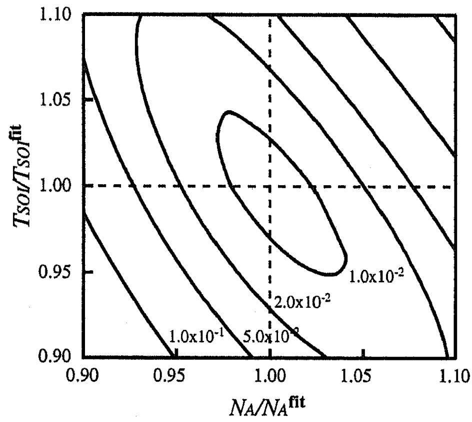
From the matrix analysis, we had the ratio of 2.9 and it can be concluded that the fitting was carried out successfully.



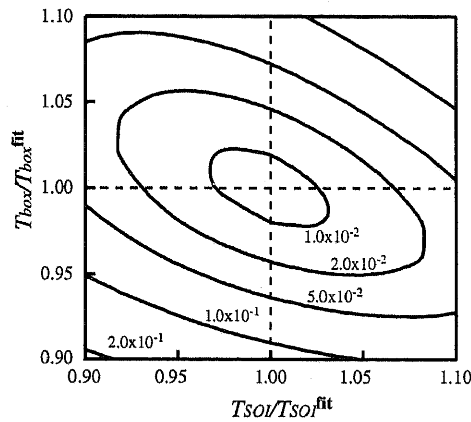
(a) (N_A,T_{fox})-space



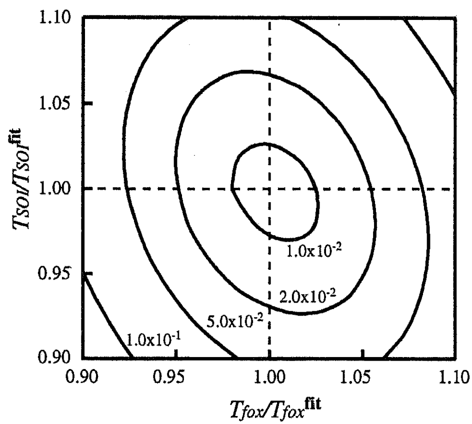
(b) (N_A,T_{box})-space



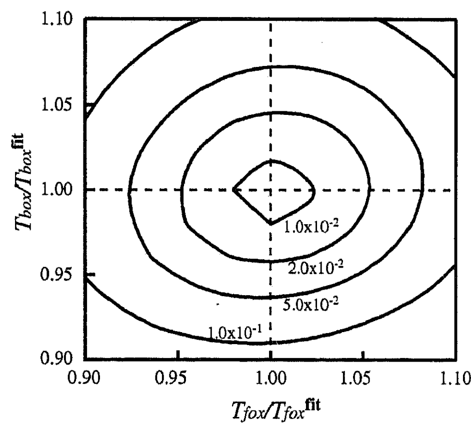
(c) (N_A,T_{box})-space



(d) (T_{SOI},T_{box})-space



(c) (T_{fox},T_{SOI})-space



(e) (T_{fox},T_{box})-space

Figure 4.7: Cross sections of mean-square error contours of measured and simulated V_{th}-V_{bs} characteristics

4.5 Conclusions

Following works were presented in this chapter.

1. A one-dimensional numerical simulation method for the subthreshold characteristics of SOI MOSFETs was presented basing on the Poisson equation assuming the thermal-equilibrium conditions.

2. One-dimensionally simulated drain current characteristics show good agreement with conventional two-dimensional results in the subthreshold region for long channel devices.

3. Efficiency of the one-dimensional simulation was proved by comparing calculation time with the two-dimensional simulation.

4. Device parameters of the SOI multi-layer structure were estimated using the one-dimensional simulation by fitting V_{th}-V_{bs} characteristics with the measured data.

5. Property of the curve fitting results by the steepest descent method was proved by eigenvalue analysis of the error function in the parameter space.

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Chapter 5

Numerical Methods for Robust and Efficient Two- and Three-Dimensional Device Simulation of SOI MOSFET

5.1 Introduction

Device simulation of SOI MOSFETs has several difficulties originating from their floating body features.

One of the problems is numerical unstability of solutions of carrier densities in the channel region due to the floating body effects, which is unlike conventional MOSFETs. Another problem is physical possibility of multiple solutions even at the same bias condition, which results in the hysteresis characteristics such as Single-Transistor Latch(STL) phenomena[5.8]. For the last of them, we have found that in SOI device simulation the iterative linear solutions show less efficiency than conventional bulk-MOS devices.

In this chapter, robust and efficient device simulation methods for SOI MOSFETs are studied from the numerical points of view.

To improve robustness of SOI simulation, we have developed a Quasi-Transient(QT) method for static(DC) mode analyses, and showed that fast and stable DC analyses are realized in device simulation of SOI MOSFETs. The QT method is suitable for analizing the floating body and the parasitic bipolar effects of thin-film SOI devices, and the STL phenomena of SOI MOSFETs are successfully simulated with the QT method.

In the latter half of this chapter, convergence efficiency of the iterative linear solution, especially ILU-CGS method, are investigated, along with evaluation of the formed matrices of the semiconductor equations in device simulation of SOI MOSFET. Eigenvalue analysis of the Jacobi matrices are carried out to clarify the differences of matrix characteristics for both SOI and bulk MOSFETs. And then, a data-dependent scaling scheme for efficient solutions of iterative linear solutions are presented and evaluated.

5.2 Robust simulation for the hysteresis phenomena of SOI MOSFET's by Quasi-Transient Method

5.2.1 Qusi-Transient device simulation

In conventional semiconductor device simulators three basic semiconductor equations, the Poisson equation(eq.5.1) and the continuity equations for carriers(eq.5.2 and 5.3) are applied.

$$\mathrm{div}(\varepsilon \cdot \mathrm{grad}\psi) = -q(N_D - N_A + p - n) \quad (5.1)$$

$$\frac{\partial n}{\partial t} + \mathrm{div}(\mu_n \cdot n \cdot \mathrm{grad}\psi - D_n \cdot \mathrm{grad}n) = \mathrm{GR} \quad (5.2)$$

$$\frac{\partial p}{\partial t} - \mathrm{div}(\mu_p \cdot p \cdot \mathrm{grad}\psi + D_p \cdot \mathrm{grad}p) = \mathrm{GR} \quad (5.3)$$

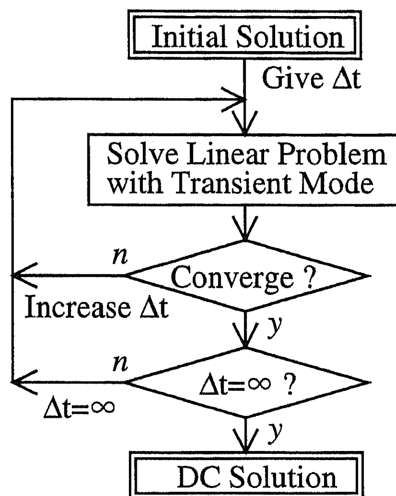


Figure 5.1: Flow-chart of Quasi-Transient method

Here, ψ is the electron potential and ε is the permittivity and N_A and N_D are the density of ionized acceptors and donors. n and p are electron and hole density. μ_n and μ_p are the carrier mobilities and D_n and D_p are the carrier diffusivity of electrons and holes, respectively. GR is the carrier generation and recombination rate.

To improve robustness and efficiency of the Newton's iterative calculation in SOI MOSFET device simulation for DC analysis with a numerical approach, we take a notice of the time-concerning *'transient'* terms in the continuity equations, which are used only in transient analyses in the conventional formulation in device simulation.

Figure 5.1 shows a generalized flow-chart of the Quasi-Transient device simulation. In the QT simulation, the solution of the former bias condition is used as the initial guess for new bias condition, as is in the conventional

method. The Newton's iterative calculation is carried out with the formulation for transient analyses. At this point, the initial guess is also assumed to be the former bias condition of qusi-time step, Δt, before. Then, Δt is gradually increased as the iterative loops are processed, and finally, the DC formulae with the condition of $\Delta t \rightarrow \infty$ are calculated, so that we can obtain the same solution as a DC simulation gives.

The advantages of this QT simulation are as follows.

1. The matrix becomes diagonally dominant as desired with the transient formulation using small Δt.

2. A stable simulation is realized even for an abrupt bias change.

3. The multiple solution problems like hysteresis phenomena are naturally avoided.

5.2.2 Efficiency of QT device simulation

Figure 5.2 compares convergence efficiency of the QT simulation with the conventional static simulation. Here, the simulations were carried out to solve the status of V_{gs}=1.0[V] with the solution of V_{ds}=0.5[V] and V_{gs}=0.5[V] as the initial guess. Details of simulated device are summerized in table 5.1.

The QT result shows shorter calculation time in each iteration of linear solution than the conventional method. The QT results also show a stable solution of carrier densities, while the conventional method obtains non-realistic solution with negative carrier densities, or even can not converge with MEDICI[5.8].

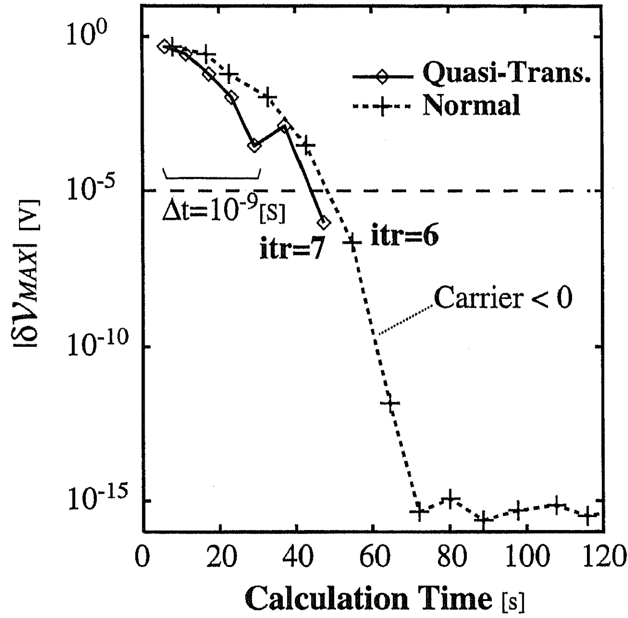


Figure 5.2: Comparison of convergence efficiency; *solid-line: QT, dashed-line: conventional*, (V_{ds}=0.5V, V_{gs}:0.5→1.0V)

Table 5.1: Device parameters used in evaluating QT method

Parameter	*Value*
type	n-type
gate length	0.6[μm]
gate oxide thickness	8[nm]
SOI layer thickness	50[nm]
buried oxide thickness	50[nm]
channel impurity density	2.0×10^{17}[cm^{-3}]
drain impurity density	1.0×10^{17}[cm^{-3}]
drain structure	single drain
grid size	$54 \times 27 = 1428$[grid^2]

5.2.3 Device Simulation of Single-Transistor Latch Phenomena

Figure 5.3 shows simulated I_d-V_{gs} characteristics of SOI MOSFET comparing simulation results including and excluding the impact-ionization mechanism of carrier generation. The gate length is 0.6[μm] and the thickness of the SOI layer is 50[nm].

In low drain voltage of V_{ds}=0.1[V], the including and the excluding results show no difference because the electric field at the drain junction is too small to generate electron-hole pairs by impact ionization.

At higher drain voltage, V_{ds}=1.0[V], the including and the excluding results show quantitative difference in both the threshold voltage and the sub-

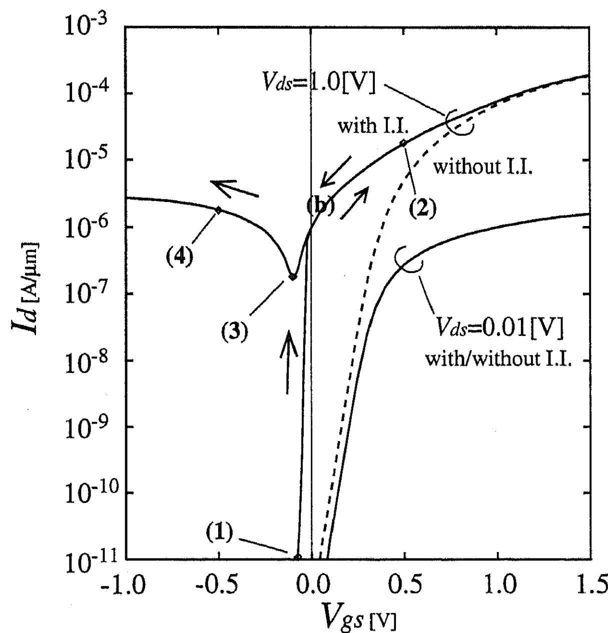


Figure 5.3: I_d-V_{gs} characteristics of n-type SOI MOSFET (V_{ds} as parameter, including/excluding I.I. model) (1) $\sim$ (4) are corresponding these in fig.5.5

threshold swing, and the STL phenomena is observed in the impact-ionization model. In the positive sweep (V_{gs} is increased from 0.1[V] to 1.5[V]), drain current, I_d, increases steeply in the subthreshold region and MOSFET turns on about V_{gs}=0.0[V]. In the negative sweep (V_{gs} is decreased from 1.5[V] to -1.0[V]), I_d decreases on the same curve as positive sweep in 'ON' region until V_{gs} is about 0.0[V]. The curve splits, however, below V_{gs}=0.0[V] by the floating body effects. In lower V_{gs} region (below -0.1[V]), holes accumulated in the body(base) region turn on the parasitic bipolar transistor and I_d increases as V_{gs} decreases.

Figure 5.4 shows simulated I_d-V_{gs} characteristics at several drain biases. When V_{ds}=0.7[V], the STL phenomena was not observed, while the FET is always in latch-up at V_{ds}=2.0[V].

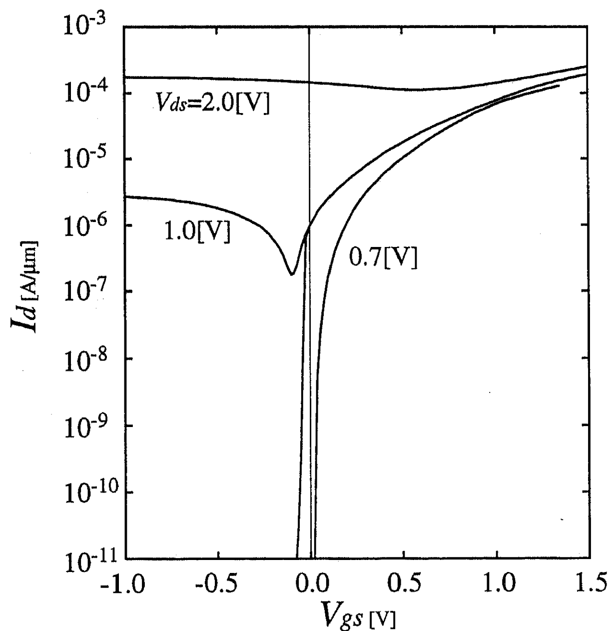


Figure 5.4: I_d-V_{gs} characteristics of n-type SOI MOSFET (V_{ds} as parameter)

Figure 5.5 shows the generation and recombination rates in SOI layer at V_{ds}=1.0[V], increasing V_{gs} from −0.1[V] to 0.5[V] and then decreasing 0.5[V] to −0.5[V]. The QT simulation shows robustness in the hysteresis of device status at the same bias where the multiple solutions are present.

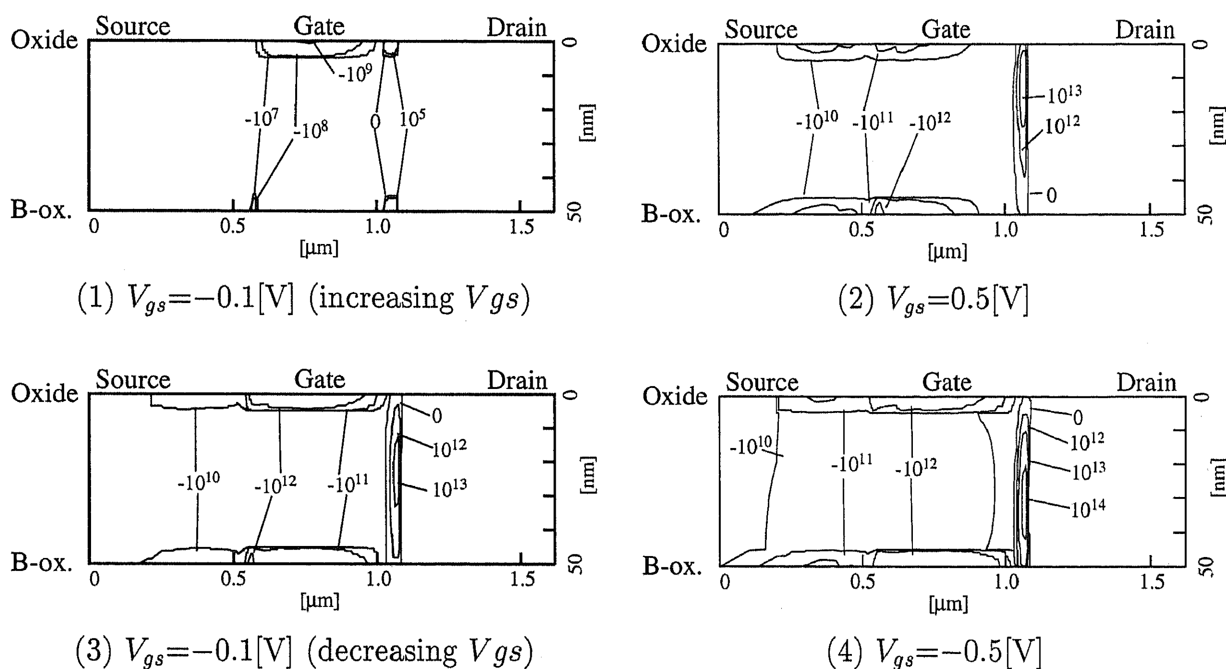


Figure 5.5: Generation (+) and recombination (−) rate in SOI layer [cm$^{-3}s^{-1}$] (V_{ds}=1.0V)

5.3 Device Structure Dependent Convergence Ability of Matrix Solutions

5.3.1 Problems in iterative linear solutions in device simulation of SOI MOSFETs

As mentioned before, device simulation of SOI MOSFET has several hardness in solutions. One of the problems well-known is that partially-depleted(PD) SOI devices show less convergence efficiency in the iterative solutions of the non-linear semiconductor equations by the Newton's iterative method than fully-depleted(FD) devices.

Furthermore, we found that PD devices show less convergence efficiency even in the iterative method of linear solutions(like SOR, CG or CGS

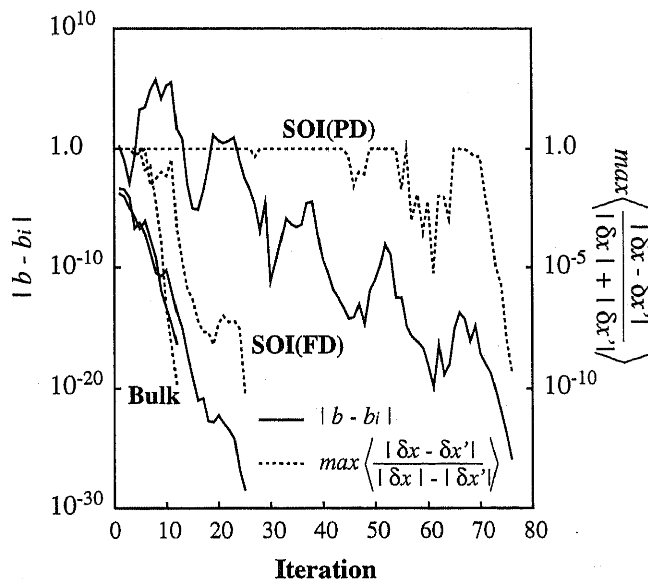


Figure 5.6: Convergence efficiency of iterative linear solutions by CGS method (*solid line: norm of revision vector of right hand side vector, dashed line: maximum quantity of revised data in solution*)

method[5.9]) than FD devices(fig.5.6).

In this section, we investigate the convergence efficiency of the iterative linear solutions concerning with device structures, especially with thickness of SOI layer which determines the device mode, PD or FD.

The iterative method we concentrate in this analysis is the Conjugate-Gradient Squared(CGS) method. The matrixes and the vectors solved by iterative solutions are pre-conditioned by the Incomplete Lower and Upper decomposition(ILU) method, as is often done, Thus, the iterative method used in this analysis is used to be called the ILU-CGS method.

5.3.2 Convergence efficiency iterative linear solutions with SOI layer thickness

To evaluate the convergence efficiency of iterative linear solutions, we prepare several device structure data of SOI MOSFETs which have same gate length and front- and buried-oxide thickness but have different SOI layer thickness each other, as illustrated in fig.5.7 and table 5.2.

Then, the convergence efficiency of the iterative linear solutions are evaluated for each device by the numbers of the iterations for convergence. The simulations are carried out for three gate bias conditions of V_{gs}=0.0, 0.1, −0.1[V]. The drain bias is V_{ds}=0.0[V]. Thus, no drain current flows in the MOSFET and the Newton's iterative method requires only 1 iteration for each of the solutions.

Figure 5.8 shows the convergence efficiency for V_{gs}=0.0[V]. The fastest convergence was realized in the bulk device. As for SOI devices, the devices with T_{SOI}=20∼40[nm] show similar convergence efficiency, 45 and 50[nm] devices show slower convergence and the device with 55[nm] SOI layer never converge.

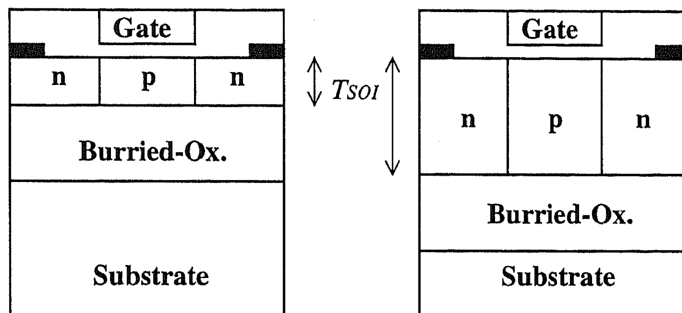


Figure 5.7: Simulated structures of SOI MOSFETs with different SOI layer thickness

Table 5.2: Device structure data for evaluating the convergence efficiency of iterative linear solution

Parameter	*Value*
type	n-type
gate length	0.3[μm]
gate oxide thickness	8[nm]
SOI layer thickness	20~70[nm]
buried oxide thickness	50[nm]
channel impurity density	2.0×10^{17}[cm^{-3}]
drain impurity density	5.0×10^{17}[cm^{-3}]
drain structure	single drain
grid size	$45 \times 34 = 1530$[grid^2]

The convergence efficiency for the gate bias conditions of V_{gs}=0.1[V] and −0.1[V] are shown in fig.5.9 and fig.5.10, respectively. They show similar dependency of the convergence efficiency on the thickness but critical SOI layer thickness is different for each bias condition.

Then, it can be claimed that the convergence efficiency depends not on the device structure nor the matrix features, but on the device status or feature of the data they contain.

In fig.5.11, distributions of eigenvalues of preconditioned matrixes by the ILU method, which are believed to rule the convergence efficiency of linear solutions[5.9], for the fast case of T_{SOI}=25nm and the worse case of T_{SOI}=50nm. No obvious difference can be seen between two results, but, as mentioned above, two matrixes showed quite different convergence efficiency in the linear solutions by the CGS method. This also supports the independence of the efficiency of the matrix features.

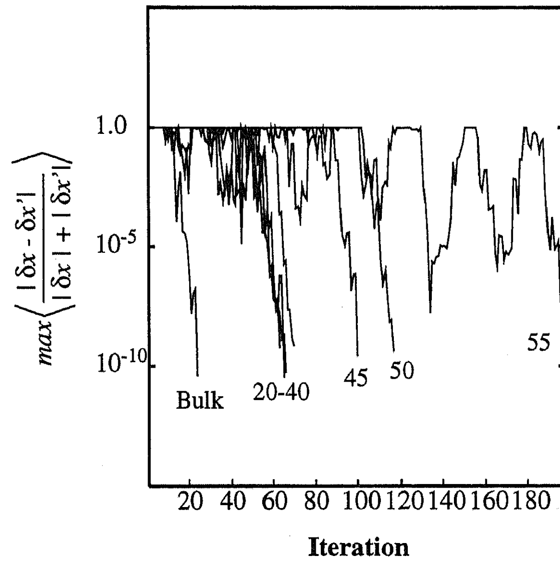


Figure 5.8: Convergence efficiency of linear solutions by CGS method (V_{gs}=0.0V, V_{ds}=0.0V)

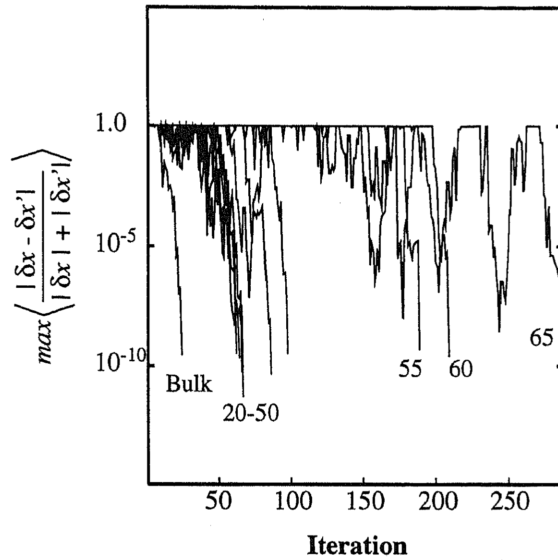


Figure 5.9: Convergence efficiency of linear solutions by CGS method (V_{gs}=0.1V, V_{ds}=0.0V)

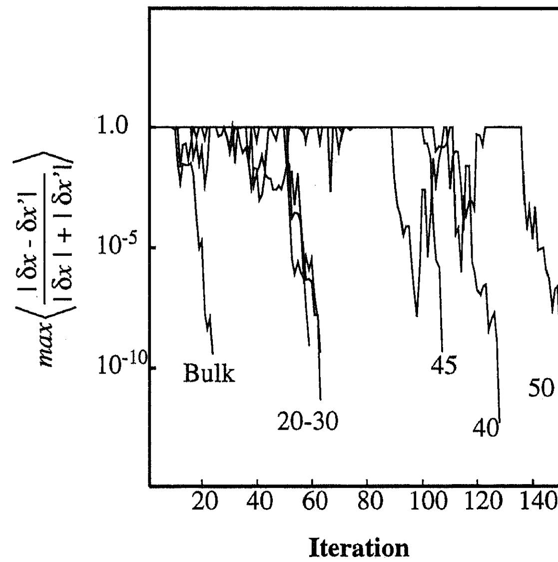
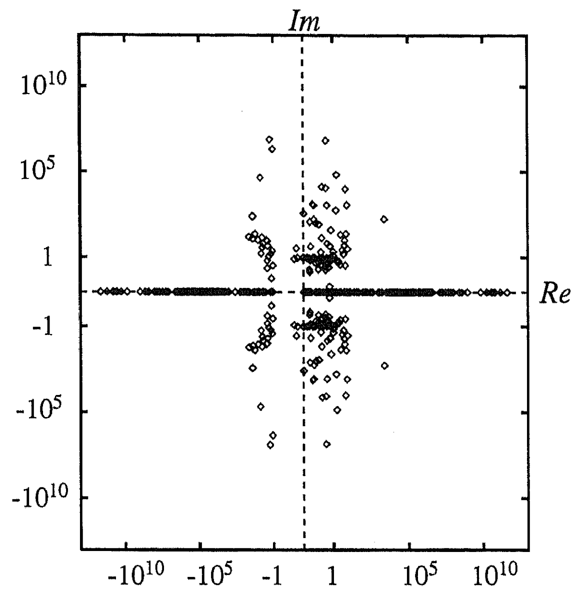
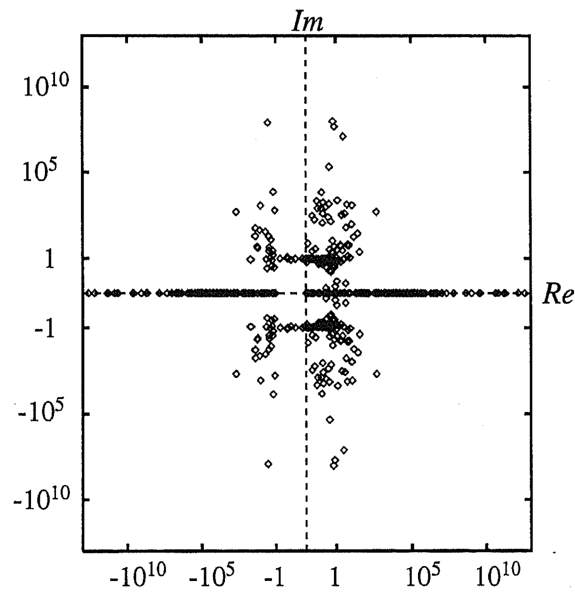


Figure 5.10: Convergence efficiency of linear solutions by CGS method (V_{gs}=−0.1V, V_{ds}=0.0V)



T_{SOI} = 25nm, degeneration in 1.0 = 61



T_{SOI} = 50nm, degeneration in 1.0 = 78

Figure 5.11: Eigenvalue analysis for ILU-preconditioned matrixes (Plotting e_i-1.0 in complex space, V_{gs}=0.0[V], V_{ds}=0.0[V])

5.3.3 Data dependent scaling scheme

As proved in the former section, the convergence efficiency of the iterative linear solutions are deeply dependent on the device status like the potential and the carrier densities. Here, we propose a scaling scheme for device simulation with data-dependent scaling factors and evaluate the efficiency of the method.

The data-dependent scaling scheme has a simple strategy of scaling carrier densities in the basic semiconductor equations (eq.5.1~5.3), by dividing the concerning elements in the formed matrix by the present carrier density n_0 or p_0(fig.5.12) so that elements in the solution vector are in the same order. Thus, it can be called *'normalized carrier scaling method'*.

The convergence efficiency was evaluated comparing the normalized carrier method with the conventional formulation, for devices of T_{SOI}=60[nm] and 25[nm](fig.5.13 and 5.14). For the 60[nm] device, the conventional for-

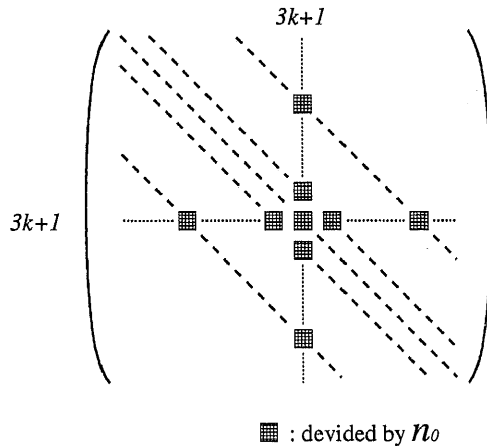


Figure 5.12: Normalized carrier scaling method

mulation could not converge the iterative solution, but by the normalized carrier formulation, the solution was obtained after about 360 iterations. On the other hand, for the 25[nm] device, both the conventional formulation and the normalized carrier formulation converged after about 65 iterations and no difference on convergence efficiency was seen between two formulation schemes. Then, it can be concluded that the normalized carrier scaling can realize robustness of linear solutions but can not contribute to efficiencies of them.

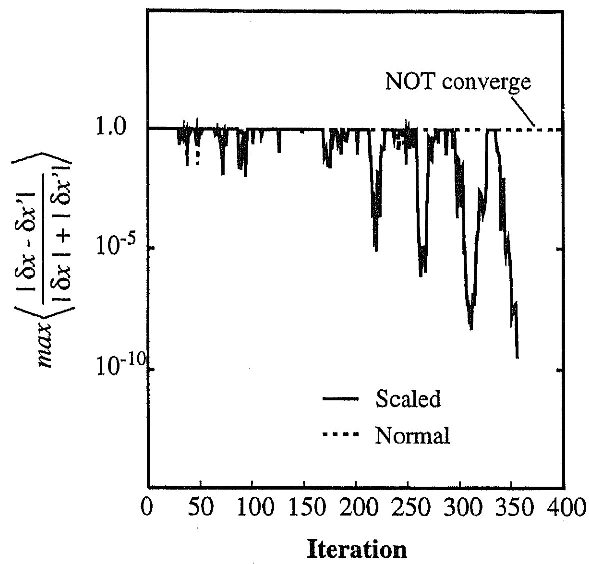


Figure 5.13: Convergence efficiency of linear solutions by CGS method (T_{SOI}=60nm, V_{gs}=0.0V, V_{ds}=0.0V)

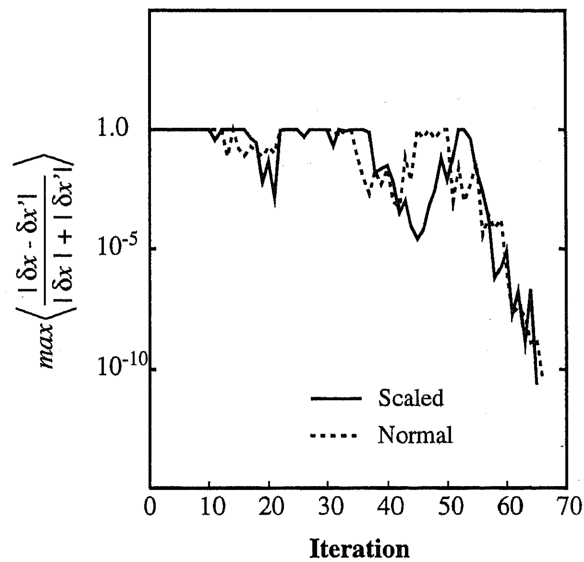


Figure 5.14: Convergence efficiency of linear solutions by CGS method (T_{SOI}=25nm, V_{gs}=0.1V, V_{ds}=0.0V)

5.4 Conclusions

Following works were presented in this chapter.

1. A Quasi-Transient formulation for robust and efficient DC analysis technique for device simulation of thin-film SOI MOSFET was presented

   - Robustness and efficiency of the QT method was proved comparing with conventional formulation of device simulation
   - With the QT method, Single-Transistor Latch phenomena with hysteresis I_d-V_{gs} characteristics were successfully simulated in DC analysis.
   - It is expected that simulations of multiple status for the same bias such as thyristor operations are also simulated using the QT method.

2. Convergence efficiency of the iterative linear solutions were evaluated with SOI layer thickness dependency

   - Data dependent convergence efficiency was concluded from simulation results and eigenvalue analyses
   - A data-dependent scaling scheme for formulation of semiconductor equations was proposed and demonstrated
   - The data-dependent scaling showed robustness in convergence of thick SOI devices

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Chapter 6

One-Dimensional Analysis of Subthreshold Characteristics of SOI-MOSFET Considering Quantum Mechanical Effects

6.1 Introduction

In chapter 4, we have presented a one-dimensional Poisson equation based device simulator for subthreshold analysis of SOI MOSFETs. It was revealed that the one-dimensional simulation is an efficient method for extracting the structural device parameters of SOI MOSFETs by fitting the simulated results with measured data.

On the other hand, it is often mentioned that quantum mechanical considerations are necessary for calculating accurate electron distribution in thin electron inversion layers or in thin SOI layers [6.1].

In this chapter, a self-consistent solver of the Poisson and the Schrödinger equations are implemented in the one-dimensional SOI MOSFET subthreshold device simulator. Mobility models are also modified so that the two-

dimensionally quantized transport phenomena are described in the quantized subband structures.

6.2 Quantum Mechanical Formulations

6.2.1 Two-dimensional electron calculation with self-consistent Schrödinger and Poisson equations

For the quantum-mechanical modeling of the two-dimensionally quantized electron inversion layer, we adopt a self-consistent method of Stern[6.2]'s with the Poisson equation(eq.6.1) and the Schrödinger equation(eq.6.2).

$$\frac{d}{dx}\left\{\varepsilon\frac{d}{dx}\psi(x)\right\} = -q\{N_A - n(x)\} \tag{6.1}$$

$$\left\{-\frac{\hbar^2}{2m^k}\frac{d^2}{dx^2} + q\psi(x)\right\}\phi_i^k(x) = E_i^k\phi_i^k(x) \tag{6.2}$$

Here, N_A is the ionized impurity density in the SOI layer and n_i is the intrinsic carrier density in bulk silicon.

In the Schrödinger equation, k denotes either lower(l) or higher(h) subband valleys in the inversion layer on a [100] surface of silicon(fig.6.1), and i denotes the subband index. $\phi_i^k(x)$ is the electron wave function and E_i^k is the energy level of ith subband of valley k, where $\phi_i^k(x)$ is the eigenfunction which concerns with the eigenvalue E_i^k of the equation. The lower valley, l, has the longitudinal electron mass, m^l, and the degeneracy of n_v^l=2, and the higher valley, h, has the transversal electron mass, m^h and the degeneracy of n_v^h=4(fig.6.1). These physical parameters are summarized in table 6.1.

In the Stern's method, the Poisson and the Schrödinger equations are solved alternatively, giving the inputs for the other in each calculation. The inputs for the Schrödinger equation are potential distributions, $\psi(x)$, which

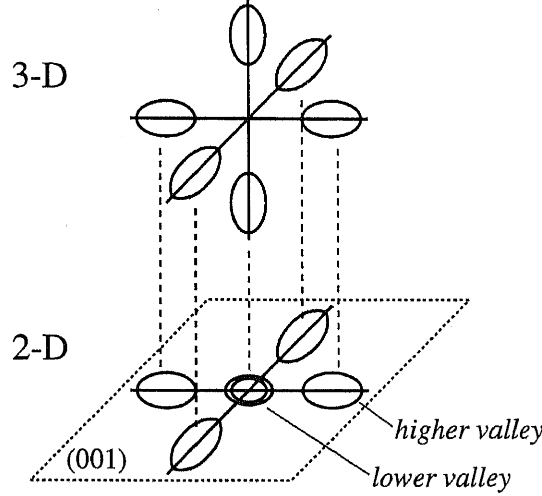

Figure 6.1: Schematic valley structure for 3-D and 2-D electron valleys

are the solutions of the Poisson equation. The inputs for the Poisson equation are the carrier distributions, which are calculated by eq.(6.3) and (6.4) with the subband structure, $\phi_i^k(x)$ and E_i^k, given by the Schrödinger equation.

$$n(x) = \sum_{k=l,h} \sum_{i} N_i^k \cdot |\phi_i^k(x)|^2 \quad (6.3)$$

$$N_i^k = \frac{n_v^k \cdot m_d^k \cdot kT}{\pi \hbar^2} \log \left[1 + \exp \left(\frac{E_F - E_i^k}{kT} \right) \right] \quad (6.4)$$

Here, m_d^k is the density-of-state mass for valley k. E_F is the Fermi energy in the SOI layer.

Figure 6.2 shows an example of the quantum mechanical result of subband diagrams in an SOI layer with the electron distribution functions, $|\phi_i^k(x)|^2$, for the lowest three subband levels of each valley.

In fig.6.3, shown are distributions of the electric potential and the electron density in the SOI layer for both classical and quantum-mechanical simulations, for a bias condition of V_{BS}=0.0[V] and V_{gs}=0.2[V]. In this case, the

Table 6.1: Physical parameters used in Schrödinger equation

Parameter	*Description*	*Value*
k	Boltzmann constant	1.38×10^{-23} [J/K]
$\hbar$	Plank constant/(2π)	1.05×10^{-34} [Js]
q	unit charge of electron	1.6×10^{-19} [C]
m_0	free-electron mass	9.11×10^{-31} [kg]
m^l	longitudinal electron mass	$0.98\ m_0$
m^h	transversal electron mass	$0.19\ m_0$
m_d^l	DOS mass for lower valley	$0.98\ m_0\ (=m_l)$
m_d^h	DOS mass for higher valley	$0.417\ m_0\ (=\sqrt{m_l m_h})$
m_c^l	conduction mass for lower valley	$0.19\ m_0\ (=m_h)$
m_c^h	conduction mass for lower valley	$0.315\ m_0\ (=m_l m_h/(m_l+m_h))$
n_v^l	valley degeneracy of lower valley	2
n_v^h	valley degeneracy of higher valley	4

structural device parameters which are used in the simulations are following; channel doping density, N_A=1.5×10^{17}[cm^{-3}], thickness of gate oxide, T_{fox}=7[nm], SOI layer, T_{SOI}=30[nm], and buried oxide, T_{box}=80[nm], which are *'designed'* parameters of our real devices.

It is notable that the classical simulation gives the maximum of the electron density at the front gate-oxide interface, while the quantum-mechanical result shows zero at the interface. Figure 6.3 also shows a slight difference in the electric potential distributions.

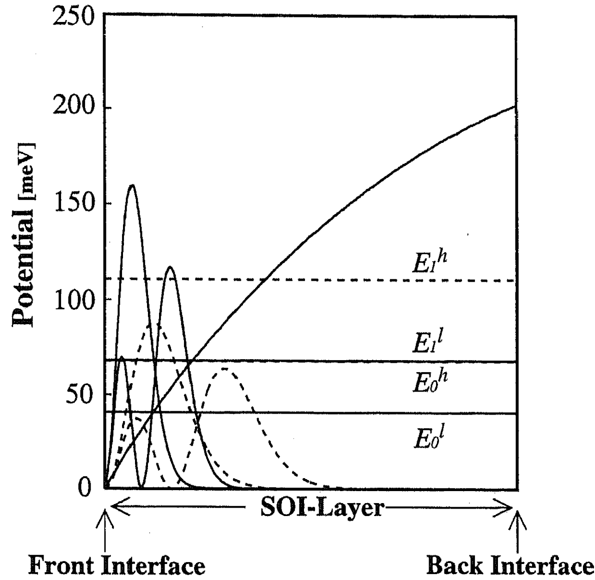

Figure 6.2: 2-D subband diagrams and electron wave functions in SOI layer by quantum mechanical simulation

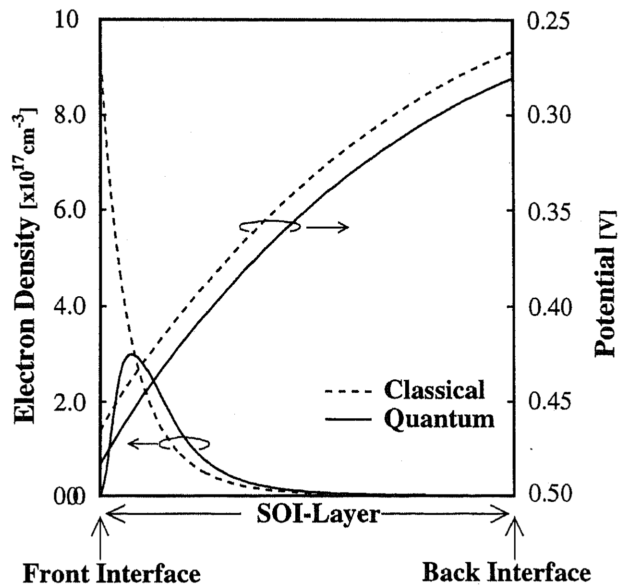

Figure 6.3: Simulated potential and electron distribution in SOI layer (V_{bs}=0.0V, V_{gs}=0.2V; *solid-line*: quantum mechanical, *dotted-line*: classical)

6.2.2 Quantum mechanical mobility modeling in two-dimensionally quantized electron layer

Quantum-mechanical considerations are also required for modeling of the electron mobility. To calculate the electron mobility from the quantum-mechanically obtained subband structures, two kind of approaches have been studied generally. One is the Monte Carlo simulation method[6.3][6.4], and the other is the relaxation time approximation[6.5] [6.6][6.7][6.8][6.9][6.10].

The Monte Carlo method needs much computational time to simulate each transport and scattering events for a lot of carriers under consideration. Carrier statistics are calculated after some time steps of simulations and current or other device conditions are obtained. The Monte Carlo simulation is suitable, for example, for the high energy carrier transport phenomena, where the thermal-equiliblium considerations are no more applicable.

In the relaxation time approximation, the mobility is derived directly from the subband structures and less computational time is required.

In this analysis, the relaxation time approximation is adopted and following intravalley phonon scattering, intervalley phonon scattering, ionized impurity scattering and surface roughness scattering are taken into consideration for the relaxation time calculation.

Relaxation time approximation

In the relaxation time approximation, the electron mobility of ith subband of valley k is calculated with the expectation of the momentum relaxation time over electron energy, E, as following formula[6.9].

$$\mu_i^k = \frac{q}{m_c^k}\left[\int_{E_i}^{\infty}(E - E_i^k)\tau_k^i(E)\frac{\partial f(E)}{\partial E}dE\right] \div \left[\int_{E_i}^{\infty}(E - E_i^k)\frac{\partial f(E)}{\partial E}dE\right] \quad (6.5)$$

Here, $\tau_i^k(E)$ is the momentum relaxation time for electrons with energy E in ith subband of valley k. m_c^k is the conductivity mass for valley k(tbl. 6.2). $f(E)$ is the Fermi-Dirac distribution function.

The momentum relaxation time, $\tau_i^k(E)$, is formulated as:

$$\frac{1}{\tau_k^i(E)} = \frac{1}{\tau_{ac,k}^i(E)} + \frac{1}{\tau_{in,k}^i(E)} + \frac{1}{\tau_{I,k}^i(E)} + \frac{1}{\tau_{SR,k}^i(E)} \tag{6.6}$$

$\tau_{ac,k}^i(E)$, $\tau_{in,k}^i(E)$, $\tau_{I,k}^i(E)$ and $\tau_{SR,k}^i(E)$ are the momentum relaxation time for the intravalley phonon scattering, the intervalley phonon scattering, the ionized impurity scattering and the surface roughness scattering, respectively. Those scattering models are described in following sections.

Intravalley phonon scattering

The intravalley phonon scattering rate for electrons in ith subband of valley k to jth subband of the same valley is modeled as eq.(6.7).

$$\frac{1}{\tau_{ac,k}^{i,j}(E)} = \frac{n_{ac}^k \cdot m_d^k \cdot (D_{ac}^k)^2 \cdot kT}{\hbar^3 \cdot \rho \cdot s_l^3} \cdot \frac{1}{W_{i,j}^k} \tag{6.7}$$

$$W_{i,j}^k = \left[\int \{\phi_i^k(x)\}^2 \{\phi_j^k(x)\}^2 dx\right]^{-1} \tag{6.8}$$

Here, n_{ac}^k is the valley degeneracy(n_{ac}^l=2 and n_{ac}^h=4), D_{ac} is the deformation potential of acoustic phonon, ρ is the mass density of crystalline silicon and s_l is the longitudinal sound velocity in crystalline silicon. $W_{i,j}^k$ represents the subband interaction between ith and jth subbands. Then, $W_{i,i}^k$ is interpreted as the effective electron layer thickness of ith subband of valley k.

The total intravalley phonon scattering rate for electrons in ith subband of valley k is calculated with following summation.

$$\frac{1}{\tau_{ac,k}^i(E)} = \sum_j \frac{u(E - E_i)}{\tau_{ac,k}^{i,j}(E)} \tag{6.9}$$

Here, $u(x)$ is the step function as:

$$u(x) = \begin{cases} 1 & (x >= 0) \\ 0 & (x < 0) \end{cases} \tag{6.10}$$

Intervalley phonon scattering

As shown in fig.6.4, the intervalley phonon scattering processes have two types of f and g, and different degeneracies for each valley and each type.

For the electrons in a lower valley, l, only f-type intervalley phonon scatterings to higher valleys are allowed and the degeneracy is $n^f_{l\to h}$=4. The scattering rate for the electrons in ith subband of a lower valley to jth subband of higher valleys is modeled as eq.(6.11)[6.9].

$$\frac{1}{\tau^{i,j}_{in,l\to h}(E)} = \frac{n^f_{l\to h}\cdot m^h_d \cdot (D^f_{in})^2}{\hbar\cdot\rho\cdot E^f_{in}}\cdot\frac{1}{V^l_{i,j}}\cdot\left(N(E^f_{in})+\frac{1}{2}\pm\frac{1}{2}\right) \times\frac{1-f(E\mp E^f_{in})}{1-f(E)}\times u(E\mp E^f_{in}-E^h_j) \tag{6.11}$$

$$V^l_{i,j} = \left[\int\{\phi^l_i(x)\}^2\{\phi^h_j(x)\}^2dx\right]^{-1} \tag{6.12}$$

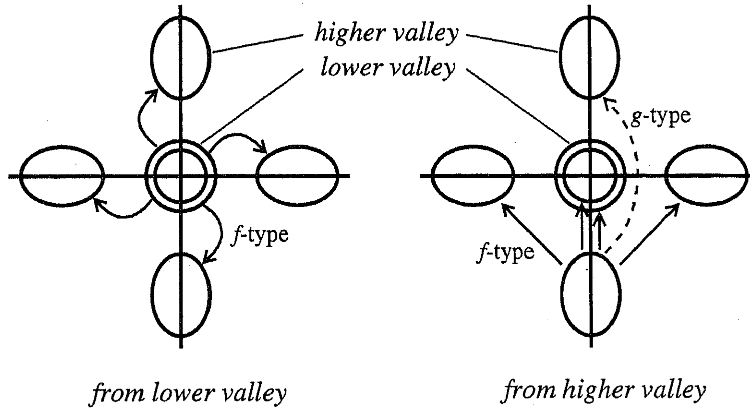

Figure 6.4: Inter valley scattering processes

Here, D_{in}^f is the deformation potential and E_{in}^f is the energy of f-type intervalley phonon, respectively. $V_{i,j}^l$ represents the subband interaction between ith subband of a lower valley and jth subband of a higher valley. $N(E)$ is the Bose-Einstein distribution function. $+$ and $-$ correspond to the phonon emission and absorption.

Finally, the total intervalley phonon scattering rate for electrons in ith subband of a lower valley is calculated with following summation.

$$\frac{1}{\tau_{in,l}^{i}(E)} = \sum_j \frac{1}{\tau_{in,l\to h}^{i,j}(E)} \tag{6.13}$$

For electrons in a higher valley, f-type scattering to higher and lower valleys and g-type scattering to a higher valley are allowed and the degeneracies are $n_{h\to h}^f$=2, $n_{h\to l}^f$=2 and $n_{h\to h}^g$=1. The scattering rate for electrons in ith subband of a higher valley to jth subband of other higher valleys is modeled as eq.(6.14), considering both f- and g-type intervalley phonons.

$$\begin{aligned}
\frac{1}{\tau_{in,h\to h}^{i,j}(E)} &= \frac{n_{h\to h}^f \cdot m_d^h \cdot (D_{in}^f)^2}{\hbar \cdot \rho \cdot E_{in}^f} \cdot \frac{1}{W_{i,j}^h} \cdot \left(N(E_{in}^f) + \frac{1}{2} \pm \frac{1}{2}\right) \\
&\quad \times \frac{1 - f(E \mp E_{in}^f)}{1 - f(E)} \times u(E \mp E_{in}^f - E_j^h) \\
&\quad + \frac{n_{h\to h}^g \cdot m_d^h \cdot (D_{in}^g)^2}{\hbar \cdot \rho \cdot E_{in}^g} \cdot \frac{1}{W_{i,j}^h} \cdot \left(N(E_{in}^g) + \frac{1}{2} \pm \frac{1}{2}\right) \\
&\quad \times \frac{1 - f(E \mp E_{in}^g)}{1 - f(E)} \times u(E \mp E_{in}^g - E_j^h)
\end{aligned} \tag{6.14}$$

$$W_{i,j}^l = \left[\int \{\phi_i^h(x)\}^2 \{\phi_j^h(x)\}^2 dx\right]^{-1} \tag{6.15}$$

Here, D_{in}^g is the deformation potential and E_{in}^g is the energy of g-type intervalley phonon, respectively. $W_{i,j}^l$ represents the subband interaction between ith subband of a higher valley and jth subband of a higher valley.

Table 6.2: Physical parameters used in intra- and inter-valley phonon scattering models

Parameter	*Description*	*Value*
ρ	crystal density of Si	2329 [kg/m^3]
s_l	sound velocity in Si	9037 [m/s]
D_{ac}	deformation potential of acoustic phonon	9.0 [eV]
D_{in}^f	def. pot. of f-type intervalley phonon	8.0 [$\times 10^8$eV/cm]
D_{in}^g	def. pot. of g-type intervalley phonon	8.0 [$\times 10^8$eV/cm]
E_{in}^f	energy of f-type intervalley phonon	59.0 [meV]
E_{in}^g	energy of g-type intervalley phonon	63.0 [meV]

The scattering rate for electrons in ith subband of a higher valley to jth subband of lower valleys is modeled as eq.(6.16).

$$\frac{1}{\tau_{in,h\to l}^{i,j}(E)} = \frac{n_{h\to l}^f \cdot m_d^l \cdot (D_{in}^f)^2}{\hbar \cdot \rho \cdot E_{in}^f} \cdot \frac{1}{V_{i,j}^h} \cdot \left(N(E_{in}^f) + \frac{1}{2} \pm \frac{1}{2}\right) \times \frac{1 - f(E \mp E_{in}^f)}{1 - f(E)} \times u(E \mp E_{in}^f - E_j^h) \tag{6.16}$$

$$V_{i,j}^h = \left[\int \{\phi_i^h(x)\}^2 \{\phi_j^l(x)\}^2 dx\right]^{-1} \tag{6.17}$$

Here, $V_{i,j}^h$ represents the subband interaction between ith subband of a higher valley and jth subband of a lower valley.

The physical parameters for the intervalley scattering are described in table 6.2 following Yamada's work[6.11].

Then, the total intervalley phonon scattering rate for electrons in ith subband of a higher valley is calculated with following summation.

$$\frac{1}{\tau_{in,h}^{i}(E)} = \sum_j \left(\frac{1}{\tau_{in,h\to h}^{i,j}(E)} + \frac{1}{\tau_{in,h\to l}^{i,j}(E)}\right) \tag{6.18}$$

Ionized impurity scattering

The scattering rate by the ionized impurity is modeled as eq.(6.19), being independent to the valley, the subband level and the electron energy[6.5].

$$\frac{1}{\tau^i_{I,k}(E)} = \frac{1}{\tau_I} = \frac{G \cdot q^4 \pi^2 N_c}{2\varepsilon^2 \hbar \cdot kT} \tag{6.19}$$

G is the multiplication factor for accounting the screening effects and N_c is the ionized impurity density in the channel region.

Surface roughness scattering

The rate of surface roughness scattering is modeled as follows[6.5].

$$\frac{1}{\tau^i_{SR,k}} = \frac{L^2 \delta^2 \hbar \cdot m^k_d \cdot 3^6}{16 \cdot (m^k)^2 \cdot W^6_j} \cdot e^{-k^2 L^2/2} \times \left[I_0(k^2 L^2.2) - I_1(k^2 L^2.2) \right] \tag{6.20}$$

$$W^k_i = \left[\int \{\phi^k_i(x)\}^4 dx \right]^{-1} \tag{6.21}$$

Here, δ is the mean-square height of the deviation of the surface and L is the lateral scale length of the fluctuation. k is the wave number of electron calculated as $k = \sqrt{2m^k_d(E - E^k_i)/\hbar^2}$. I_0 and I_1 are the 0th and 1st order Bessel functions of the first kind. W^k_i is the effective electron layer thickness of ith subband of valley k.

The physical parameters for the surface roughness scattering are chosen following Fischetti's work[6.4](tbl.6.3).

Table 6.3: Physical parameters used in surface roughness scattering model

Parameter	*Description*	*Value*
δ	mean-square height of the deviation	0.48 [nm]
L	lateral scale length of the fluctuation	1.3nm [nm]

6.2.3 Drain current modeling in quantum mechanical analysis

As the same way as the classical analysis, the drain current, I_d, is calculated with the diffusion current component. The current is calculated for each subband level, i, of each valley, k, as:

$$I_i^k = \frac{qW}{L} \cdot \frac{kT}{q} \cdot \mu_i^k \cdot N_i^k \tag{6.22}$$

Then, the total drain current is calculated with the summation of them as:

$$I_d = \sum_{k=l,h} \sum_i I_i^k \tag{6.23}$$

In the quantum-mechanical model, the electron mobility is determined for each subband of each valley as described above. Here, we define the effective mobility for the quantum-mechanical model to evaluate the relation between the total sheet density of electrons and the drain current.

The effective mobility, μ_{eff}, is formulated as the average of each subband's mobility weighted with the subband's electron population as:

$$\mu_{eff} = \frac{1}{N_I} \sum_{k=l,h} \sum_i N_i^k \cdot \mu_i^k \tag{6.24}$$

where

$$N_I = \sum_{k=il,h} \sum_i N_i^k \tag{6.25}$$

Here, N_I represents the total sheet density of electrons in the SOI layer.

Then, the drain current can be summarized as eq.(6.26) with the effective mobility and the sheet density of electrons, which is the same form as the classical modeling of eq.(4.10).

$$I_d = \frac{qW}{L} \cdot \frac{kT}{q} \cdot \mu_{eff} \cdot N_I \tag{6.26}$$

6.3 Mobility Evaluation of Quantum Mechanical Model

6.3.1 Back-bias dependent mobility characteristics

In fig.6.5, calculated back-bias(V_{bs}) dependent effective mobility characteristics are shown for the inversion electron density of N_I=10^{10}cm^{-2}, by the quantum-mechanical modeling(*Quantum*), the classical modeling(*Classical*) and the classical mobility model with the quantum-mechanical electron distribution(*Q+C*).

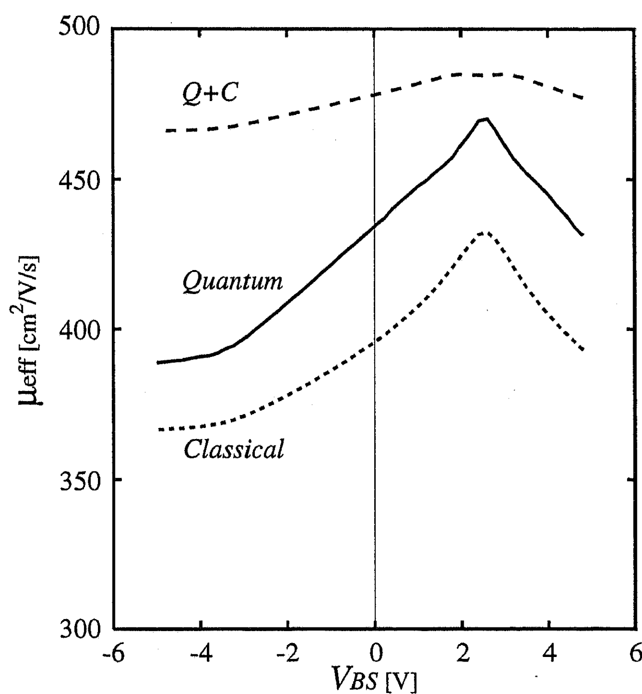

Figure 6.5: μ_{eff}-V_{BS} characteristics of SOI MOSFET (N_I=10^{10}cm^{-2}); *solid line: quantum-mechanical, dotted-line: classical, dashed-line: classical with QM electron dist.* (L=W=100 μm)

In low V_{bs} region, low μ_{eff} values are obtained by the vertical field effects or by the two-dimensionally quantized effects for electrons, with high electric field in the SOI layer because the electric potential at the back interface of the SOI layer and the buried oxide layer is lowered by the back-bias. In contrast, in high V_{bs} region, μ_{eff} characteristics are also lowered as the bias increases. This is because the current conduction occurs near the back interace of the SOI layer with high V_{bs} bias. Then, as V_{bs} gets higher, the vertical field effects in the SOI layer is also enhanced and results in the low conductivity. At about V_{bs}=2.5V, the effect from vertical electric field on the electron mobility is smallest and simultaneously, the conduction stage moves to the back interface from the front interface.

Comparing the Q+C results with others, the vertical field effects are not so obviously seen in Q+C simulation models, because as shown in fig.6.3 the electron distributions show quite different aspects especially at the interface where the vertical electric field affects most significantly to the mobility in the classical model. The classical results show very similar characteristics with the complete quantum-mechanical results. The quantitative difference between the quantum-mechanical and the classical mobilities are not discussed deeply here, because the difference of drain current by 20%~30% is easily resulted from the difference of V_{th} of only about 10mV in subthreshold analysis.

6.3.2 Mobility calculation for SOI and bulk MOSFET

In fig.6.6, mobility characteristics with sheet electron density, N_I, are shown comparing SOI and bulk results. The SOI results show higher mobilities by about 50 [cm^2/V/s] than bulk results over the whole density range.

Figure 6.7 compares electron distribution in the channel of SOI and bulk

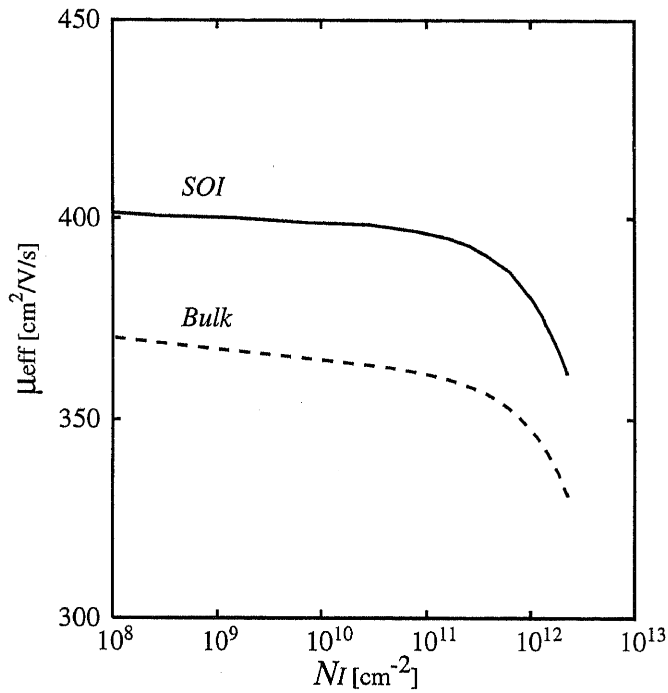

Figure 6.6: μ_{eff}-N_I characteristics of SOI and bulk MOSFET *solid line: SOI MOSFET, dashed-line: bulk MOSFET* (L=W=100 μm)

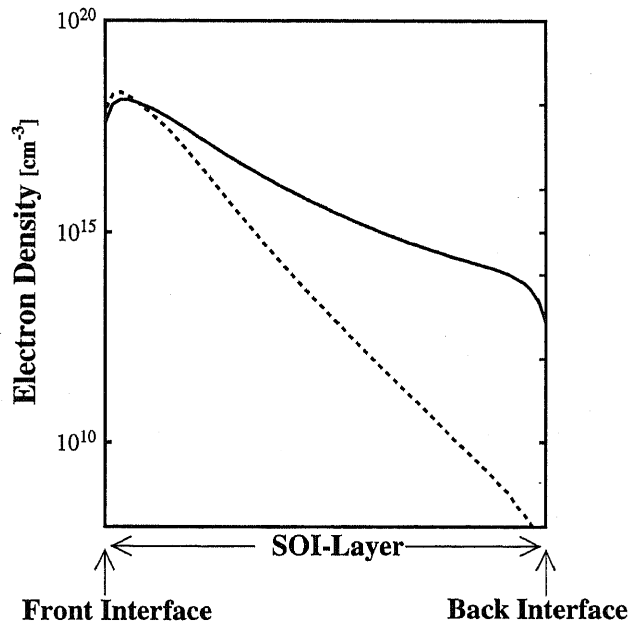

Figure 6.7: Electron distribution in channel(SOI) layer; N_I=5.0 $\times$ 10^{11}[cm^{-2}] *solid line: SOI MOSFET, dashed-line: bulk MOSFET*

MOSFET for N_I=5.0×10^{11}[cm^{-2}]. It shows significant difference of gradients of the electron distribution between SOI and bulk. The electron distribution represents the potential distribution, thus, higher electric field presents in the channel region of bulk MOSFET and results in the lower mobilities.

6.4 Device Parameter Estimation by Quantum Mechanical Models

6.4.1 Parameter fitting results

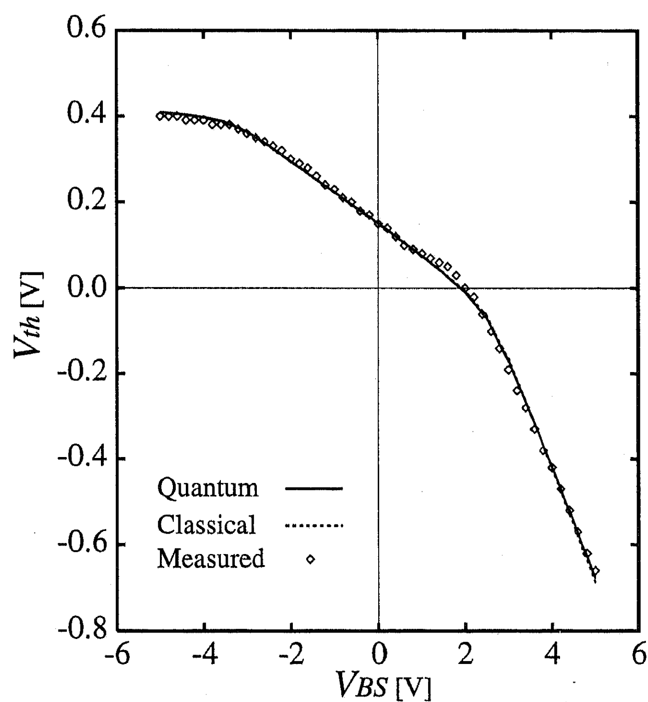

Figure 6.8: V_{th}-V_{bs} characteristics of n-type SOI MOSFET; *solid line: quantum mechanical, dashed-line: classical, points: measured* (L=W=100 μm)

Table 6.4: Estimated device parameters of SOI MOSFET

		designed	*quantum*	*classical*
N_A	$[10^{17}\text{cm}^{-3}]$	—	2.24	2.36
T_{fox}	[nm]	7	5.80	6.43
T_{SOI}	[nm]	30	43.3	41.3
T_{box}	[nm]	80	69.3	70.7

Device parameter estimation was demonstrated using the one-dimensional simulation with the quantum-mechanical model. With as same way as presented in sec.4.3.3, the simulated V_{th}-V_{bs} characteristics curve was fitted with the measured data by tuning the device parameters. The fitted parameters were also the channel dopant density, N_A, the thickness of gate oxide, T_{fox}, the thickness of SOI layer, T_{SOI}, and the thickness of buried oxide, T_{box}.

Figure 6.8 shows the V_{th}-V_{bs} curve fitted with the quantum-mechanical model, along with the classical results and the measured data. In table 6.4, designed and fitted device parameters are described, along also with the classical results and the designed values.

Comparing the quantum-mechanical results with the classical results, the thickness of silicon layer, T_{SOI}, is estimated thicker by the quantum-mechanical analysis while the thickness of oxide, T_{fox} and T_{box}, are estimated thinner by the quantum-mechanical analysis.

These results can be explained as follows; the electron distribution obtained from the classical analysis gives the maximum at the oxide interface but the real electron distribution shows the maximum at a little deep from the interface. Then, it can be said that so-called effective thickness[6.13][6.14] of the thinner silicon layer and the thicker oxide layers from the classical analysis, as illustrated in fig.6.9.

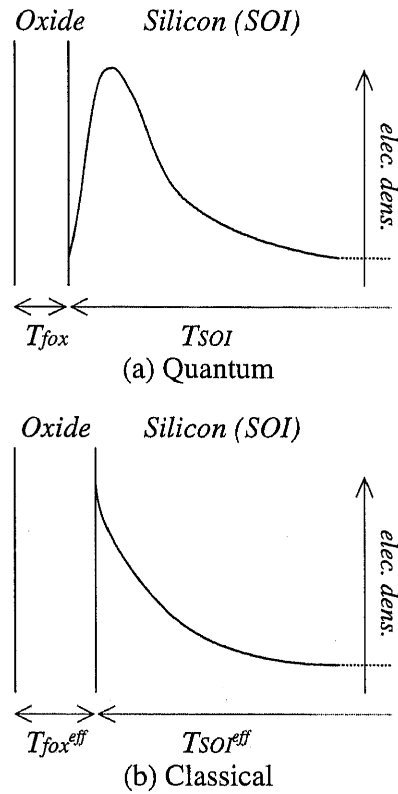

Figure 6.9: Difference of estimated device parameters from quantum-mechanical and classical analysis by the electron distribution aspects

The total sheet densities of the ionized impurity in the SOI layer, which are calculated as $N_A \times T_{SOI}$, are 9.69×10^{11}[cm^{-2}] for the quantum-mechanical model and 9.73×10^{11}[cm^{-2}] for the classical model. This results also support the effectively reduced thickness of the SOI layer by the classical analysis.

6.4.2 Effects of parameter fluctuation

For the four device parameters estimated above, the effects of the fluctuation of each parameter on the threshold characteristics are evaluated. Figure

6.10∼6.13 show the simulated results of V_{th}-V_{bs} characteristics using the device parameters one of which is modified by ±10% from the estimated value by the curve fitting.

In fig.6.10, relusts by the fluctuation of the gate oxide are shown. When V_{bs} is lower than about 2[V], V_{th} changes as described in basic MOS texts. When V_{bs} is higher than 2[V], this is the back-channel conduction case, the change of V_{th} is very small, because the gate bias acts as the substrate bias in the normal conduction.

In fig.6.11, relusts by the fluctuation of the SOI layer thickness are shown. In the middle of the V_{bs} range, V_{th} gets higher as the SOI layer gets thicker. This can be explained as follows; the series capacitance of the gate oxide, the SOI layer and the buried oxide gets bigger as the SOI layer gets thicker, then the ratio of the series capacitance and the gate capacitance gets bigger, resulting in the higher V_{th}. When V_{bs} is lower than about -3[V], the curves cross each other. This is because the back interface is almost accumulated with such deep back biases, so that the potential of the back interface is almost fixed, and then, the influence of the back bias is cancelled with the weak coupling of the front and back interface of thicker SOI devices.

Figure 6.12 shows relusts by the fluctuation of the buried oxide. In contrast to the front gate fluctuation results, the changes of V_{th} are significant in higher back bias conditions. This can also explained by basic MOS theories assuming the back-channel conduction with the buried oxide as the control gate oxide and the roles of V_{th} and V_{bs} are exchanged.

In fig.6.13, relusts by the fluctuation of the accepter density are shown. With denser accepter, higher V_{th} characteristics are obtained.

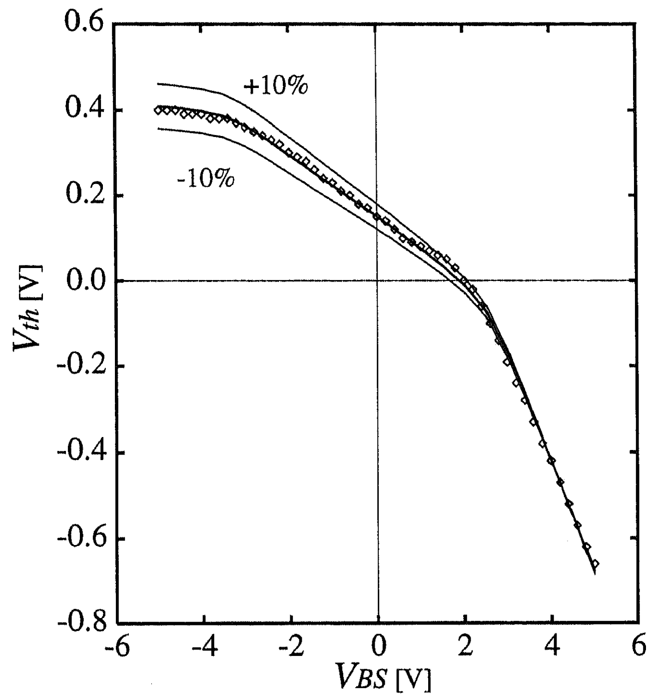

Figure 6.10: Fluctuation of V_{th}-V_{bs} characteristics by T_{fox} modulation

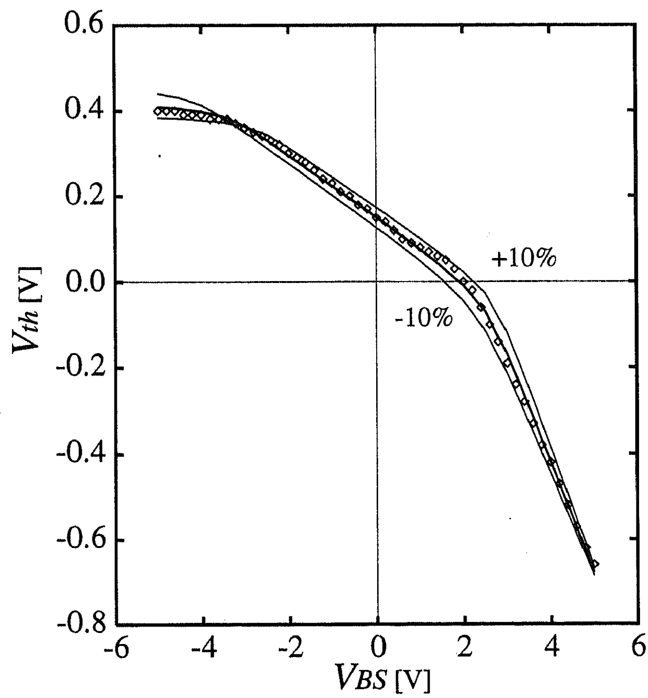

Figure 6.11: Fluctuation of V_{th}-V_{bs} characteristics by T_{SOI} modulation

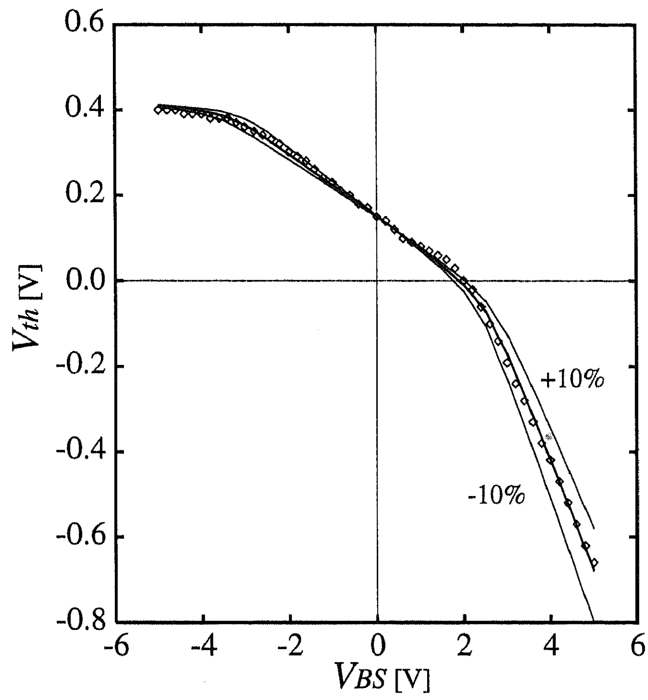

Figure 6.12: Fluctuation of V_{th}-V_{bs} characteristics by T_{box} modulation

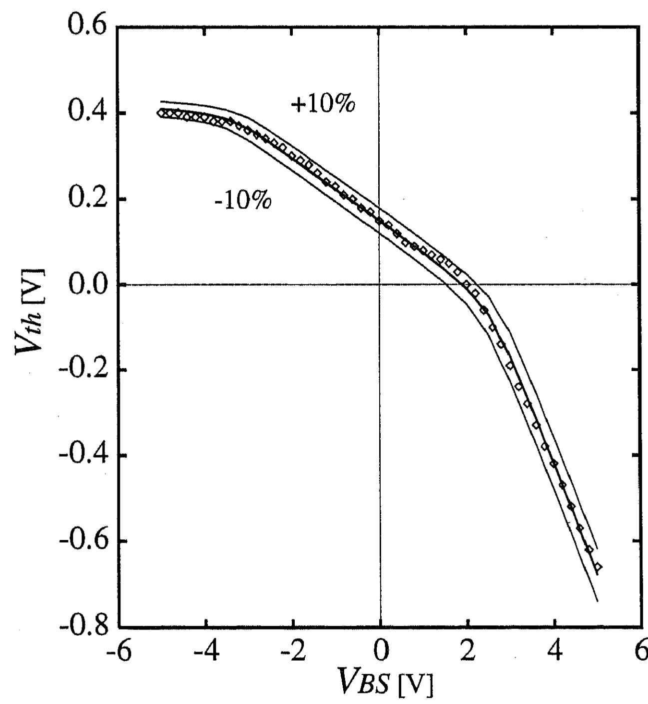

Figure 6.13: Fluctuation of V_{th}-V_{bs} characteristics by N_A modulation

6.4.3 Device-dimensional scaling and quantum mechanical effects

In fig.6.14, device parameters of the quantum mechanical model are compared with the classical model for scaled devices. The analyses were carried out in the following procedure.

Firstly, the scaled-down device parameters were assumed obeying the general scaling law[6.15], so that V_{th}-V_{bs} characteristics were calculated by the quantum mechanical model. In the next, the device parameter estimation was performed with the classical model, by fitting the classically calculated characteristics with the quantum mechanical results. From the fitting results, the differences can be evaluated between the quantum-mechanically and the

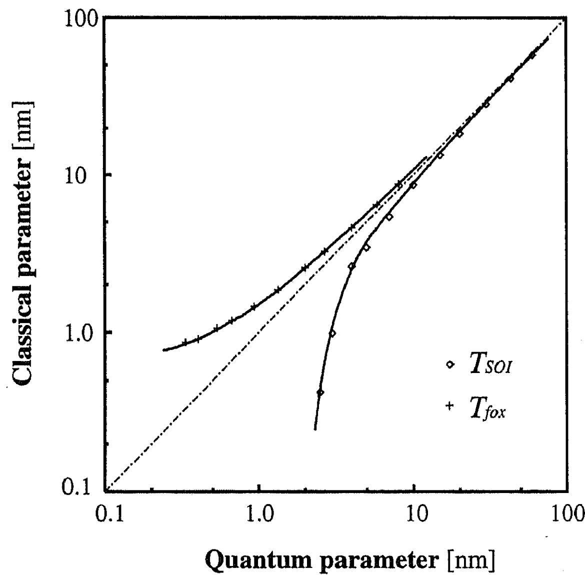

Figure 6.14: Comparing the scaled parameters given to the quantum mechanical simulation with the classically estimated device parameters

classically estimated device parameters for the same V_{th}-V_{bs} characteristics as shown in fig.6.14.

When T_{SOI} is less than about 5 nm or T_{fox} is less than about 1 nm, the classically estimated device parameters show much differences from those of the quantum mechanical simulations. Then, the necessity of quantum mechanical considerations are concluded especially in analysis of thin film devices like short-channel SOI MOSFETs.

6.5 Conclusion

Following works were presented in this chapter.

1. A one-dimensional numerical method for analysis of subthreshold characteristics of SOI MOSFETs was presented considering the two-dimensional quantization effects for electrons by a self-consistent scheme of the Poisson and the Schrödinger equations.

2. The electron transport is also modeled quantum-mechanically with the relaxation time approximation for the electron mobility model in the two-dimensionally quantized electron inversion layers.

3. Using the simulator, the device parameters of the SOI multi-layer structure of real SOI MOSFETs were estimated by fitting the simulated V_{th}-V_{bs} characteristics with the measured data.

4. Device parameter estimation was also performed with scaling down the device in-depth dimensions, proving the necessity of quantum mechanical considerations especially in analysis of devices with thin film regions.

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Chapter 7

Conclusion

In this dissertation, evaluation and design methodologies for integrated semiconductor devices were discussed by means of both analytical and numerical simulation. Also, numerical simulation methods themselves were investigated for realizing efficient analyses.

Activities which had been studied in this dissertation is summarized as follows;

Chapter 1 and 2. An evaluation method of power and energy consumption of CMOS circuits was presented using circuit simulation of a inverter circuit with physics-based analytical models.

Device parameter optimization of MOSFETs was demonstrated for low power and low energy optima with the evaluation method, to minimize energy consumption during a switching or to minimize the gate delay time under restricted chip power.

The trends of the optimum device parameters and the optimum supply voltage with the scaling of the channel length were shown for these optimization criteria. It was concluded that the essential scaling mer-

its of the channel length of MOSFETs were the speed and the area advantages, not the energy and power advantages.

Chapter 3 and 4. A one-dimensional numerical simulation method of SOI MOSFETs for modeling the subthreshold characteristics was presented.

Device structural parameters of SOI MOSFETs were estimated by curve fitting of the measured and the simulated V_{th}-V_{bs} characteristics using the subthreshold simulator.

The property of the curve fitting results with the steepest descent method was also proved by eigenvalue analysis of the Jacobian matrixes of the error function in the device parameter space.

Chapter 5. A stable and efficient scheme for two- and three-dimensional numerical simulation for SOI MOSFETs was presented with a Quasi-Transient formulation of device formulae for static simulation. The Single-Transistor Latch phenomena were successfully reproduced with the QT method.

Solution problems of iterative methods in linear matrix calculations in SOI simulation were investigated, with the device structural dependence. A data-dependent scaling criterion was presented and demonstrated as a efficient formulation scheme for linear matrix construction.

Chapter 6. Quantum-mechanical considerations for thin-film SOI devices were introduced to the one-dimensional simulator presented above. The electron mobility was also modeled quantum-mechanically by the relaxation time approximation.

The parameter fitting was also demonstrated and showed different fitting results than the classical results.

Device parameter estimation was also performed with scaling down the device in-depth dimensions, proving the necessity of quantum mechanical considerations especially in analysis of devices with thin film regions.

In fig.7.1, the positions of the studies which were discussed in this dissertation are illustrated as the components of computer-aided device design technologies, for the complete view of this dissertation.

As the conclusion of this dissertation, it can be concluded that following subjects had been made clear through this dissertation.

- Effectiveness of optimum design of device parameters of integrated

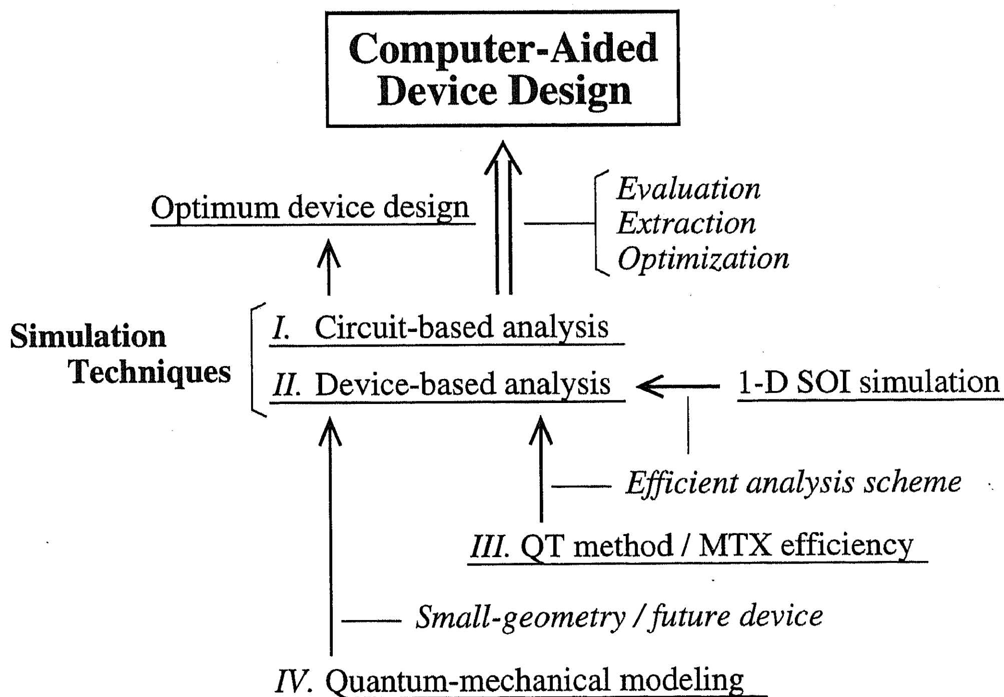

Figure 7.1: Complete view of this work

semiconductor devices for low-power VLSIs

- The trend and the essential merits on scaling of device feature size and device parameters
- Efficient numerical schemes for simulation-based evaluation and design of semiconductor devices
- Effectiveness of one-dimensional numerical analysis in extracting device parameters from measured characteristics
- Numerical schemes for stability and efficiency of two- and three-dimensional SOI device simulation
- Necessity of the quantum-mechanical considerations of electron inversion layers in analysis of thin-film SOI devices

List of Presentations and Publications

Chapter 2 and 3

- R.Ikeno and K.Asada, "Optimization of VLSI Process Parameters Using Circuit Simulation," IEICE Spring Conference, A-123, Mar. 1995.
- R.Ikeno and K.Asada, "Optimum Design of Device Parameters for Switching Energy Minimization using Circuit Simulation," *Trans. IEICE*C-II, vol.J79-C-II, pp.525–526, Oct. 1996.

Chapter 4

- R.Ikeno, T.Nakura and K.Asada, "Estimation of SOI MOSFET Threshold Voltage" Using 1-D Device Simulation Method," JSAP 42nd Spring Meeting, 28p-TF-4, Mar. 1995.
- R.Ikeno, H.Ito, T.Nakura and K.Asada, "Evaluation of SOI MOSFET Threshold Voltage using 1-D Device Simulation," IEICE Technical Report, SDM94-208, Mar. 1995.

Chapter 5

- R.Ikeno and K.Asada, "Stable Solution for SOI MOSFET Simulation by Quasi-Transient Method," JSAP 43rd Spring Meeting, 26p-H-3, Mar. 1996.
- R.Ikeno and K.Asada, "Robust simulation for the hysteresis phenomena of SOI MOSFET's by Quasi-Transient Method," 1996 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD '96), P-13, Sep. 1996.
- R.Ikeno and K.Asada, "Device Dependent Convergence-ability of Matrix Solution in Device Simulation," JSAP 57th Fall Meeting, 7a-V-4, Sep. 1996.

Chapter 6

- R.Ikeno, H.Ito and K.Asada, "Device Parameter Estimation by 1-D SOI Simulation Considering 2-D Quantum Effects," JSAP 56th Fall Meeting, 27a-ZQ-3, Aug. 1995.
- R.Ikeno, H.Ito and K.Asada, "One-Dimensional Analysis of Subthreshold Characteristics of SOI-MOSFET Considering Quantum Mechanical Effects," 4th International Workshop on Computational Electronics, P11, Oct. 1995.
- R.Ikeno, H.Ito and K.Asada, "SOI Device Parameter Estimation with 2-dimensionally Quantized Mobility Modeling in Electron Inversion Layer" JSAP 44th Spring Meeting, Mar. 1997(to be presented).

- R.Ikeno, H.Ito and K.Asada, "One-Dimensional Analysis of Subthreshold Characteristics of SOI-MOSFET Considering Quantum Mechanical Effects," Special Issue of *VLSI Design*, Gordon & Breach, 1997(to be published).

- R.Ikeno, H.Ito and K.Asada, "Device Parameter Estimation of SOI MOSFET using One-Dimensional Numerical Simulation Considering Quantum Mechanical Effects," submitted to *IEICE Trans. Electron.*

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