High-T_C Superconductive Switching Devices

高温超伝導スイッチングデバイス

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Contents

Synopsis

High-T_c superconductive quasi-particle injection devices aiming at the use for the interface between superconductor and semiconductor logic circuits were fabricated. YBCO was used as the material for the superconductive bridge and Au as the injector.

The fundamental characteristics of the device prototype were measured. When the device was operated in non-latching mode, the response time was 10~100 μs, but in latching mode, the response time was reduced to about 100 ns.

We tried to explain the electric characteristics of this device by thermal analysis. By the simulation, the behavior of the device was successfully explained. It was also proved that the response time can be shortened to the order of ~ns under an appropriate operation condition.

The results obtained from the measurement were not sufficient for the practical use as the interface devices, but the simulation results showed that a device with high performance can be realized with scaling and more accurate fabrication process.

Chapter 1

Introduction

1.1 Background

It is believed among the superconductor researchers that the superconductor computer system will be realized in the near future. It has a great advantage over the conventional semiconductor computers: the calculation speed is 2 orders of magnitude faster and the power consumption is 4 to 5 orders of magnitude smaller.

At the same time, superconductor has a well-known disadvantage. It is difficult, or almost impossible, to make a small superconductor computer system because a refrigerator is necessary to cool down the superconductor circuits.

Therefore, the superconductor computers and the semiconductor computers will exist together; the former for high-speed calculation, and the latter for mobile use, etc.

Taking this fact into consideration, we must think about the way of data transmission between these two different types of computers. In the complementary metal oxide semiconductor (CMOS) circuits, '0' and '1' signals are represented by the difference of the voltage, e.g. 0 V and 3.3 V. On the other hand, in the case of single flux quantum (SFQ) logic circuits, which is the most popular logic structure of superconductor computer, the signal '1' is represented by the existence of a single magnetic flux, and '0' by absence. A magnetic flux can be transformed to voltage by using a superconducting quantum interference device (SQUID), but the voltage generated from one flux is only a few mV or less. The aim of my research is to make an interface between SFQ and CMOS that can amplify the small voltage generated by a SQUID to a voltage large enough to operate CMOS circuits.

So far, a few articles about the interface systems are reported [1–3]. The system proposed in these articles can be divided into 2 components: one consists of many Josephson junctions or SQUIDs that are connected in series so that a few tens mV of voltage is generated, and the other one is a CMOS differential

amplifier that can amplify the voltage to CMOS level. Though this kind of system is reliable and high-speed (the slew rate is above 10 GHz), the circuits are complicated and thus the size of the whole system is rather large.

In order to overcome this drawback, we propose a new interface system that is very small and simple; it consists only of a high-T_c superconductive microbridge and a metal electrode. The microbridge can be switched to resistive state by applying small voltage to the metal electrode. Generally speaking, the switching speed of this kind of device is not thought to be so fast because the change of the state is accompanied with a process of heating and cooling, which takes relatively long time [6]. In the case of low-T_c superconductive devices, however, the switching speed is estimated to be less than 1 ns [7]; about the switching speed of state-of-the-art CMOS circuits. Therefore I expect the value above can be also achieved with high-T_c superconductive devices.

1.2 Contents

In chapter 2, the structure and the fabrication method of the devices are explained. The basic device structure is roughly the same as that of quasi-particle injection device. In order to inject large current, the contact resistance between the injector and the bridge must be small. For this purpose, we tried in-situ Au deposition and annealing process.

In chapter 3, the measurement results of the fundamental device characteristics are shown. The resistance–temperature characteristics of the $YBa_2Cu_3O_{7-x}$ film, the current–voltage characteristics of the superconductive microbridge, critical current–injection current characteristics, etc. were measured.

In chapter 4, the results of thermal analysis of this device are shown. We assumed that the electrical characteristics of the device were determined by the device temperature. Based on this hypothesis, the heat generation and the heat conduction were calculated and then the device characteristics were simulated.

In chapter 5, the switching characteristics are discussed. There are two types of operation modes: latching mode and non-latching mode. The measurement results and the simulation results of the switching characteristics in each mode were compared to show the plausibility of the simulation. Lastly, the scaling effect on the switching characteristics is also mentioned.

Chapter 6 is the conclusion of this thesis.

Chapter 2

Device Structure and Fabrication Process

2.1 Structure of the Device

2.1.1 Quasi-Particle Injection Device

First, we introduce quasi-particle injection devices because the structure of the device proposed in this research is similar to that of quasi-particle injection device.

The structure of the quasi-particle injection device is shown in Fig. 2.1. It consists of a superconductive bridge and a metal gate across the bridge. By the current injection from the gate electrode into the bridge, the critical current I_c of the bridge is reduced because the quasi-particles (= electrons that are not in the form of Cooper pair) injected from the gate will break the Cooper pairs that are flowing in the bridge. Consequently, the superconductivity of the bridge is weakened or broken.

Usualy, the current gain of this device, defined as

$$\text{(current gain)} \equiv \left| \frac{\Delta I_c}{\Delta I_{\text{inj}}} \right|, \tag{2.1}$$

is more than unity. In the case of the device fabricated with high-T_c superconductor, current gain of larger than 5 is reported [4,5].

So far, quasi-particle injection devices have been investigated by many researchers [4–6], but the main purpose of these researches is to study the physics of quasi-particle injection, such as the origin of current gain, the influence of the tunnel barrier thickness on the device characteristics, the process of Cooper-pair breaking, etc. However, this device is suitable for applications on electronics because quasi-particle injection device has a remarkable advantage over other superconductive devices; different from Josephson junctions, which have only two terminals, quasi-particle injection devices have three terminals. This is a great merit because three terminal devices are good at separation of input and output
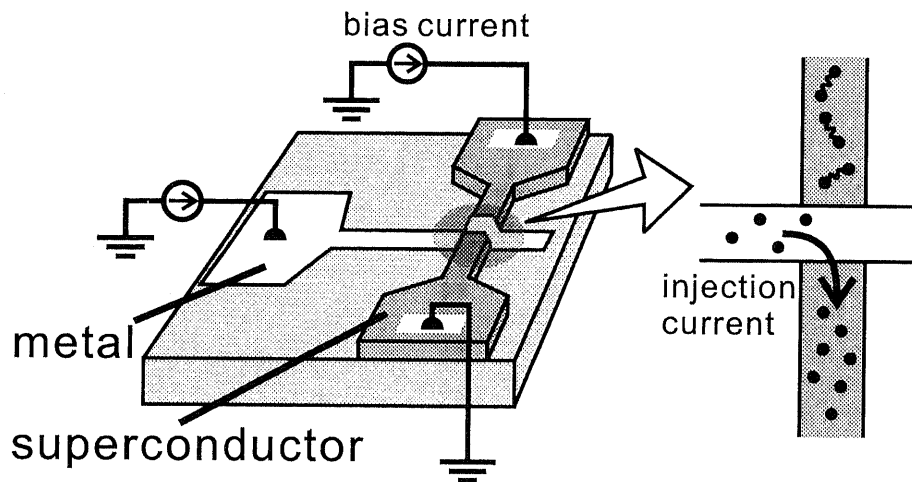
Figure 2.1: Quasi-particle injection device.

signals and appropriate for switching devices. This fact can be easily understood by the analogy with the semiconductor devices; the transistors are ideal devices for switching, but the diodes are not.

2.1.2 Proposed Device

The schematic picture of the proposed switching device is shown in Fig. 2.2. Basically, this device has the same structure as the quasi-particle injection device. The only difference is that the gate electrode is located close to the source, not in the middle of the bridge, so that the voltage gain V_{ds}/V_{gs} be as large as possible.

The operation procedure of this device is as follows. Bias current I_d is previously applied to the drain electrode. When a small voltage is applied to the gate, quasi-particles are injected to the $YBa_2Cu_3O_{7-x}$ (YBCO) bridge. Then the bridge area becomes resistive and high voltage appears at the drain electrode.

There are two reasons why we chose high-T_c superconductor as the material for this device. One is that the interface devices should be operated in high temperature; interface devices are directly connected to the semiconductor circuits which is used in room temperature. The other is that high-T_c superconductor has high resistivity compared with low-T_c superconductor and it helps us make smaller devices; the voltage appears at the drain electrode is determined by the product of the bias current and the resistance of the bridge.

2.2 Fabrication Process

Device fabrication process is shown in Fig. 2.3. The materials and the process conditions are listed in Tab. 2.1.
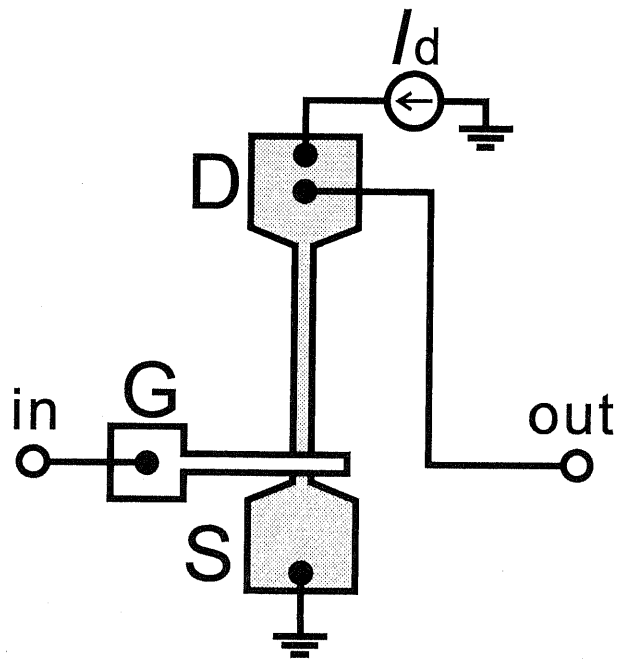
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Figure 2.2: Schematic of the interface device.

1. Deposit YBCO on $SrTiO_3$ (STO) substrate by pulsed laser deposition (PLD) method and anneal in 1 atm O_2 at 450 °C. The thickness of the YBCO film is about 100 nm.

2. Deposit Au by PLD method (in-situ) and anneal in 1 atm O_2 at 500 °C. The thickness of the Au film is a few nm.

3. Deposit Au by sputtering. The thickness is about 50 nm.

4. Lithography for YBCO bridge patterning.

5. Remove Au and YBCO by Ar ion milling.

6. Remove photo resist by acetone, oxygen ashing, and Ar ion milling.

7. Deposit Au by PLD method and anneal in 1 atm O_2 at 500 °C.

8. Deposit Au by sputtering. The thickness is about 100 nm.

9. Lithography for Au gate electrode patterning.

10. Make Au thinner by Ar ion milling.

11. Remove Au by wet etching using $KI+I_2$ solution.

12. Remove photo resist by acetone.

8

YBCO is the most popular high-T_c superconductor. The critical temperature of YBCO film was about 80 K.

The Au film deposited in the process (2) and (3) prevents the surface of YBCO from being polluted or damaged by dust, air, photo resist, etc. For this purpose, in-situ Au deposition is ideal, but the rate of in-situ Au deposition (PLD method) is as low as 10^{-3} nm/shot; about 1/100 of that of YBCO. Therefore we deposited Au by sputtering in addition to the in-situ Au.

According to a previous report, contact resistivity between YBCO and Au can be reduced to 10^{-10} Ωcm^2 or less by annealing in 1 atm O$_2$ at 650 °C [8]. In order to reduce the contact resistance at the gate–bridge contact area, we tried to anneal my samples in the condition described above, but the Au film was damaged when the annealing was done at the temperature higher than 500 °C. Thus, we annealed the samples at 500 °C, and the contact resistivity remained as high as 1.5×10^{-7} Ωcm^2.

Au film deposited by PLD method has particles on its surface (Fig. 2.4). They are called droplets and their origin is drops of Au liquefied by the laser. The Diameter varies from 1 μm to 5 μm. The density is about 100 droplets/mm^2 and it is not an obstacle to device fabrication so far, but when we integrate the devices in the future, we must reduce the density of droplets.

Sometimes it happened that the gate Au wire was snapped just at the side of the bridge after Au wet etching by KI+I$_2$ solution (Fig. 2.5); the solution had somehow flowed in under the photo resist. However, the difference in level at the point is about 100 nm (the thickness of YBCO and previously-deposited-Au), which value is thin enough for photo resist to be spread uniformly.

The cause of this snap was the abnormal growth of sputtered Au at the edges. As you see in Fig. 2.5, the growth rate of Au at the edge area is much higher than that at the flat area. Therefore the photo resist can not cover Au completely and KI+I$_2$ solution flows into the gap, and finally the Au wire is snapped (Fig. 2.6).

This problem was overcome by two modifications in process:

- Reflow of the photo resist

- Shortening of sputtering time

By high temperature postbake, photo resist becomes soft and plastic. This method is called 'reflow'. We tried reflow method because it was expected that the resist would transform and cover the uneven Au surface. Reflow was done at 150 °C for 3 min.

Along with the increase in sputtering time, the abnormal growth of Au becomes more and more obvious (Fig. 2.7). On the other hand, the Au wire resistance becomes large if the sputtering time is too short. After all, the sputtering time was decided to be 10 minutes considering both conditions.
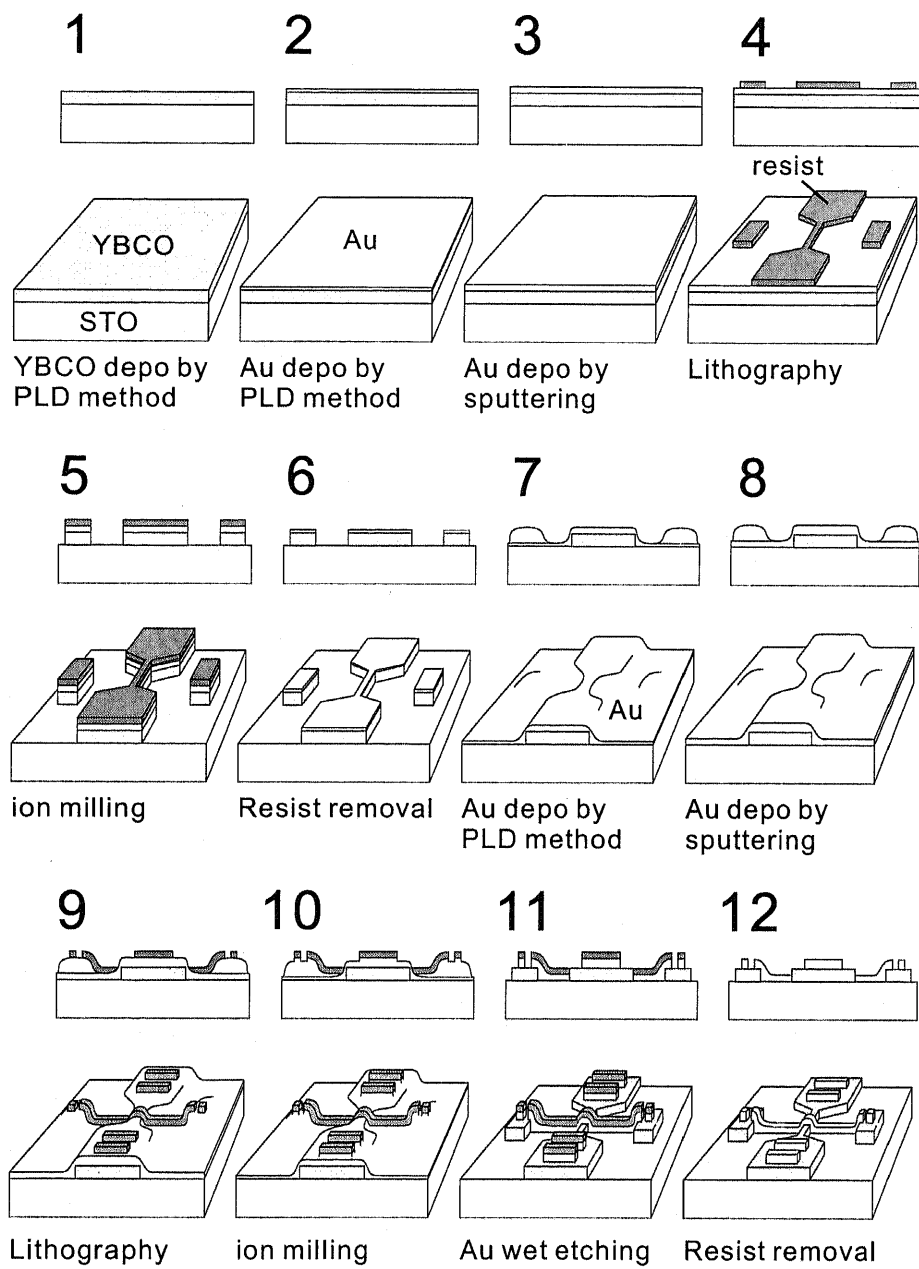
1

YBCO depo by
PLD method

2

Au depo by
PLD method

3

Au depo by
sputtering

4

resist

Lithography

5

ion milling

6

Resist removal

7

Au depo by
PLD method

8

Au depo by
sputtering

9

Lithography

10

ion milling

11

Au wet etching

12

Resist removal

Figure 2.3: Device fabrication process.

Table 2.1: Materials and process conditions

Materials	
substrate	$SrTiO_3$
superconductor	$YBa_2Cu_3O_{7-x}$
electrodes	Au

YBCO PLD	
pulsed laser energy	140 mJ/shot
pulse frequency	2 shots/s
atmosphere	O_2, 200 mTorr
substrate temperature	730 °C
deposition time	10 min

Au PLD	
pulsed laser energy	200 mJ/shot
pulse frequency	10 shots/s
atmosphere	vacuum ($\sim 10^{-6}$ Torr)
substrate temperature	200 °C
deposition time	10 min

Au sputtering	
atmosphere	Ar
acceleration voltage	1.4 kV
current	8 mA
deposition rate	10 nm/min

Lithography	
photo resist	AZ5214E
prebake	90 °C, 90 sec
developer	AZ300MF
rinse	water

ion milling	
atmosphere	Ar, 6×10^{-4} Torr
acceleration voltage	2 kV
current	40 mA
etching time	20 min

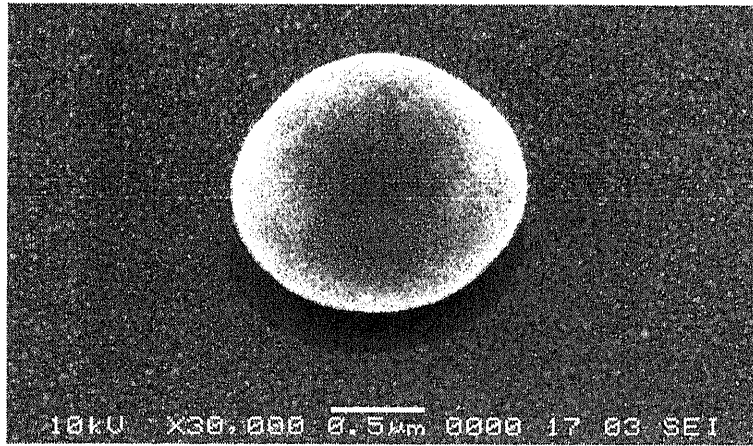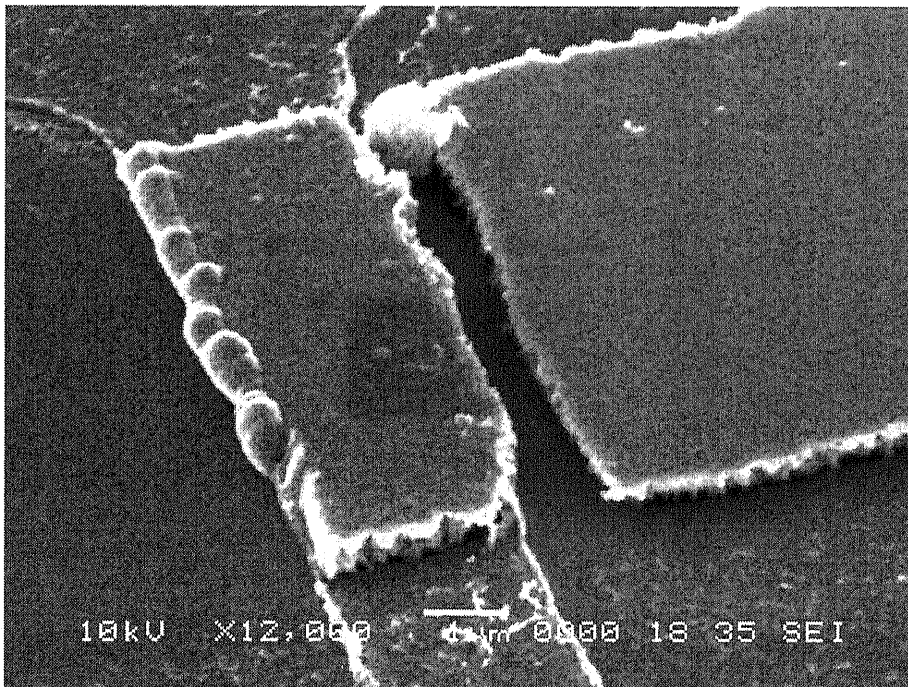| Ashing	
atmosphere	O_2, 50 mTorr
acceleration voltage	60 V
current	1.5 A
ashing time	2 hours

Figure 2.4: Au droplet produced by Au PLD.
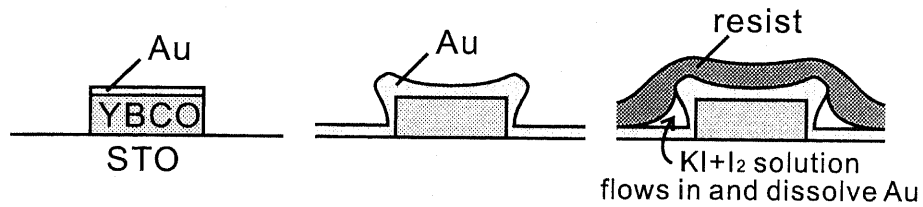

Figure 2.5: Snapped Au wire.

Figure 2.6: The process of Au wire snapping.

2.3 Micrographs

Photographs of the device is shown in Fig. 2.8 and 2.9. Fig. 2.8 is an optical microscope image of the device. The bridge can be seen at the center and the gate line is crossing over the bridge near the source. Fig. 2.9 is a scanning electron microscope (SEM) image of the contact area. Though being wet etched, the edge of the Au wire is quite smooth.

The dimensions of the devices are as follows.

- The length and the width of the bridge: (100 μm, 5 μm), (60 μm, 6 μm), (60 μm, 4 μm), (40 μm, 4 μm), (20 μm, 4 μm)

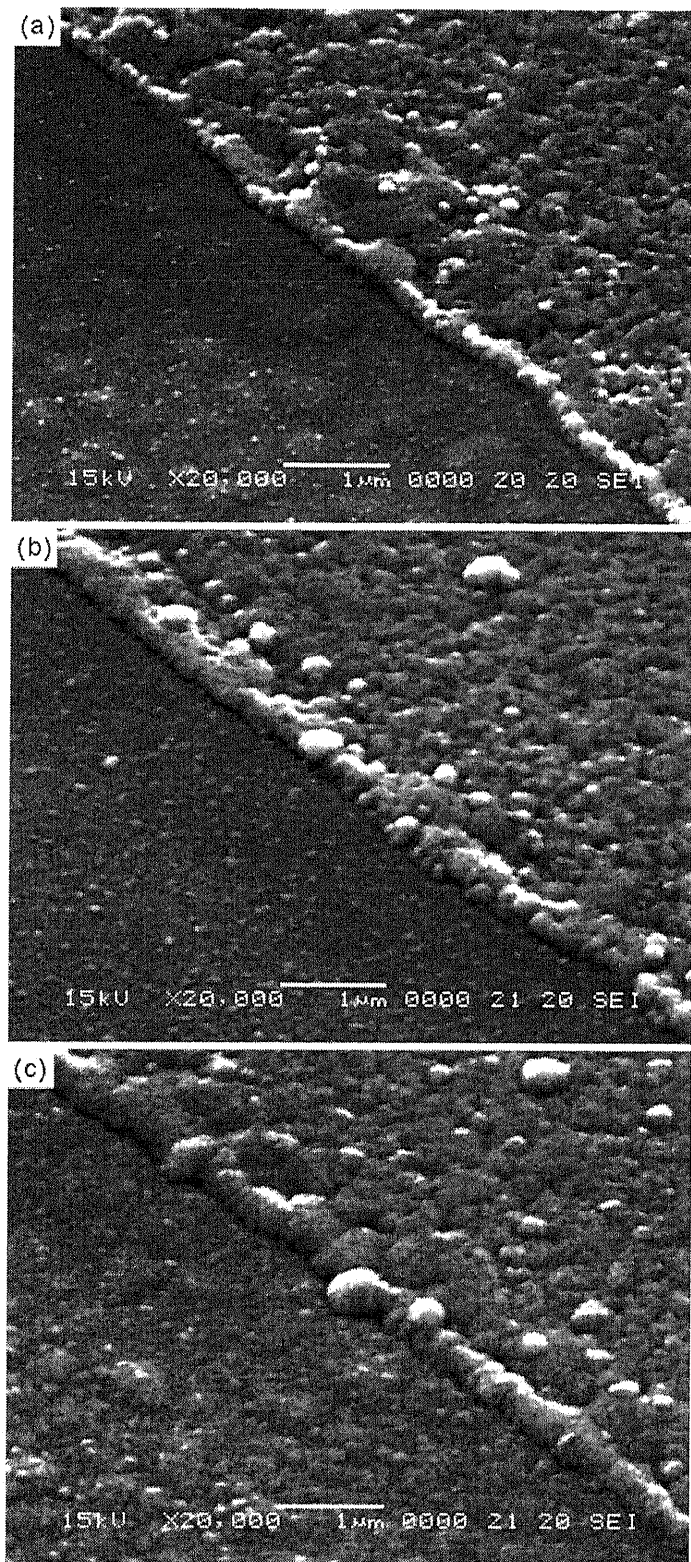- The width of the Au gate electrode: 10 μm, 5 μm

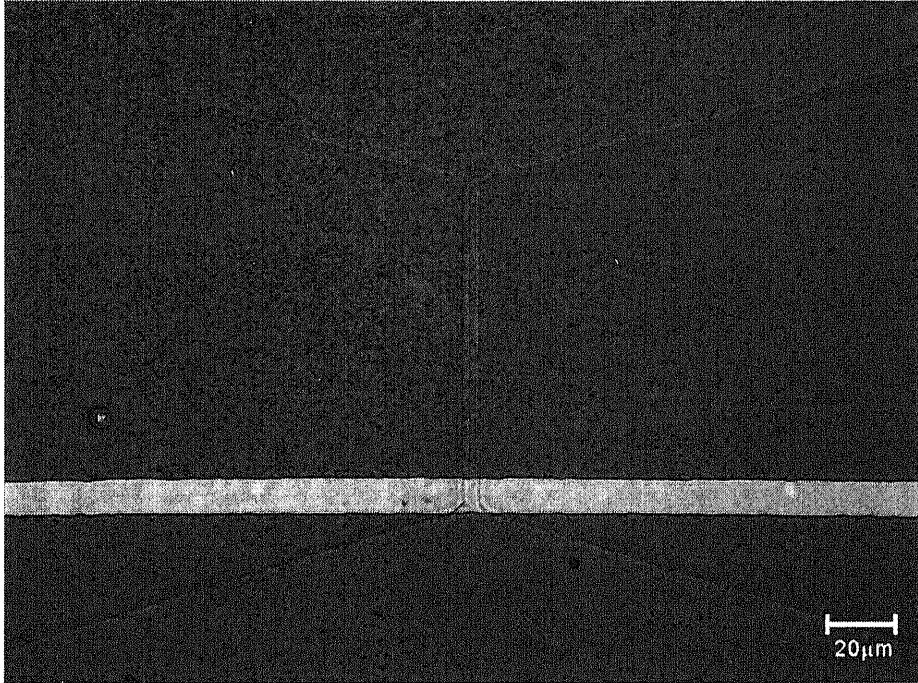Figure 2.7: Sputtering time dependence of Au growth at the edges. (a) 10 min. (b) 20 min. (c) 40 min.

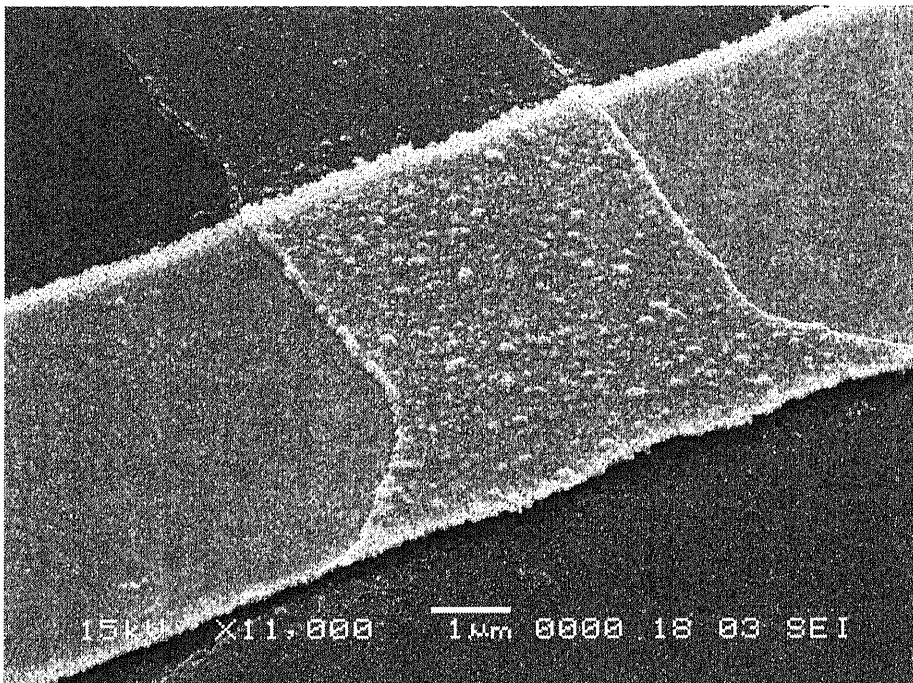Figure 2.8: Optical microscope image of the device.

Figure 2.9: SEM image of the gate–bridge contact area.

Chapter 3

Fundamental Device Characteristics

3.1   Measurement System

The measurement system of the device characteristics are shown in Fig. 3.1. We have measured five parameters: drain current I_d, injection current (= gate current) I_{inj}, drain–source voltage V_{ds}, gate–source voltage V_{gs}, and the thermal bath temperature T.

As for the power supply, we selected one among three, i.e. current source, AC voltage source (function generator), and DC voltage source, depending on the measurement object.

3.2 R–T Characteristics

First, the resistance–temperature characteristics of the bridge were measured. The measurement circuit is shown in Fig. 3.2-(a). The resistance R was measured with the four-probe method. Small current I_d was applied to the drain electrode and V_{ds} was measured at various temperature. I_d is the smaller the better because the intrinsic critical temperature T_c is determined by the T_c when $I_d=0$; T_c decreases with the increase in I_d.

The results are shown in Fig. 3.2-(b). The resistance falls to zero at 70~80 K.

3.3 I_d–V_{ds} Characteristics with No Injection

The electrical characteristics of the YBCO bridge were measured. The gate electrode was kept open-circuited. The circuit for measurement is shown in Fig. 3.3-(a). 40 Hz triangular wave was applied to the drain electrode.
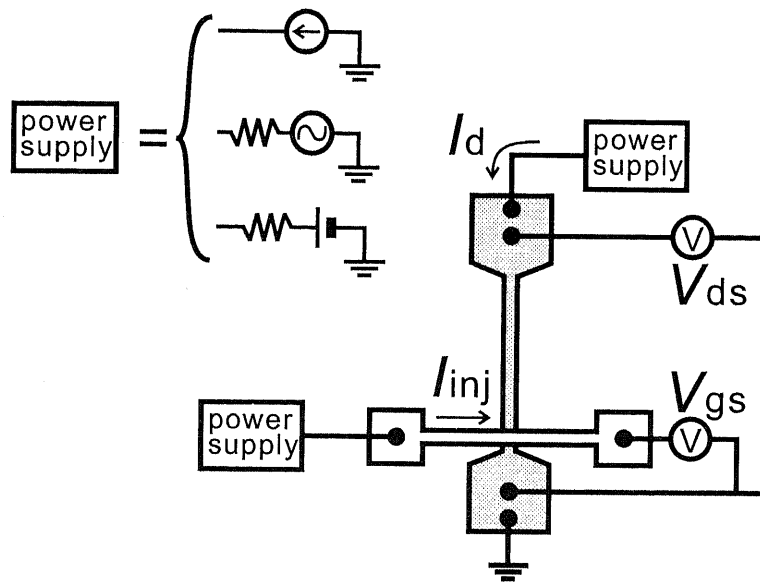
Figure 3.1: Measurement system.

Typical I_d–V_{ds} characteristics are shown in Fig. 3.3-(b). When I_d exceeds the critical current I_c, the bridge becomes resistive and large voltage appears at the drain electrode. As you see, I_d is almost constant when $V_{ds}>0$. Hereafter, we call this value I_n , the abbreviation of $I_{normal\ state}$. In chapter 4, we try to elucidate this peculiar characteristics.

I_d–V_{ds} characteristics dependence on the thermal bath temperature is shown in Fig. 3.4. The data of the device with the bridge length of 60 μm are shown in Fig. 3.4-(a) and 20 μm in Fig. 3.4-(b). As the temperature increases, both I_c and I_n decrease.

The shape of I_d–V_{ds} curve is roughly the same regardless of the bridge length, but a small difference appeared at higher temperatures. At 60 K, for example, I_d of 20 μm bridge device slightly increased along with V_{ds}, but that of 60 μm bridge device remained constant. The reason of this characteristics is also explained in chapter 4.

We also measured the time required to change the bridge from the superconductive state to the resistive state, and the reverse. For the measurement, we used the same circuit as the one shown in Fig. 3.3-(a), but in this time the input signal was rectangular wave, not triangular.

The results are shown in Fig. 3.5 and 3.6. The data in Fig. 3.5 were measured at 10 K and Fig. 3.6 at 60 K. Here, it must be noted that the values of I_d on these graphs were measured through a differential amplifier whose highest transmittable frequency (-3dB) is 1 MHz. Therefore the real I_d curves are steeper than those shown in these graphs.

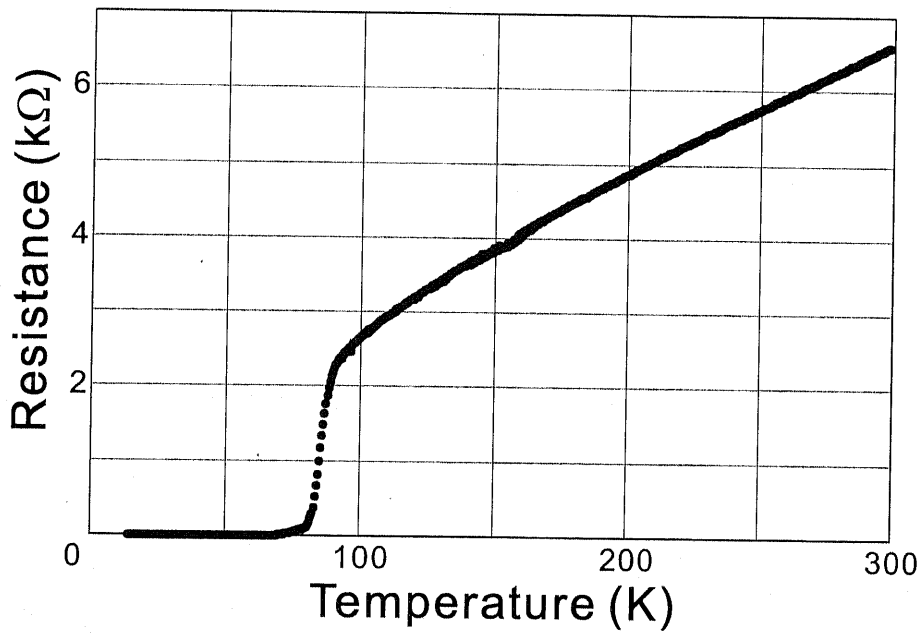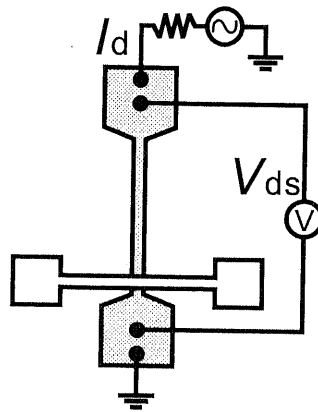As can be seen in these graphs, vibrations were observed when I_d and V_{ds}

(a)
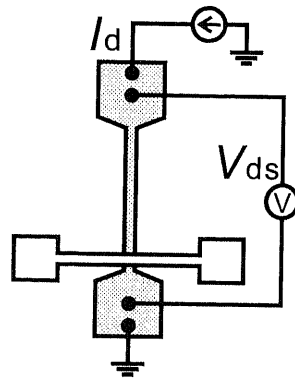
(b)

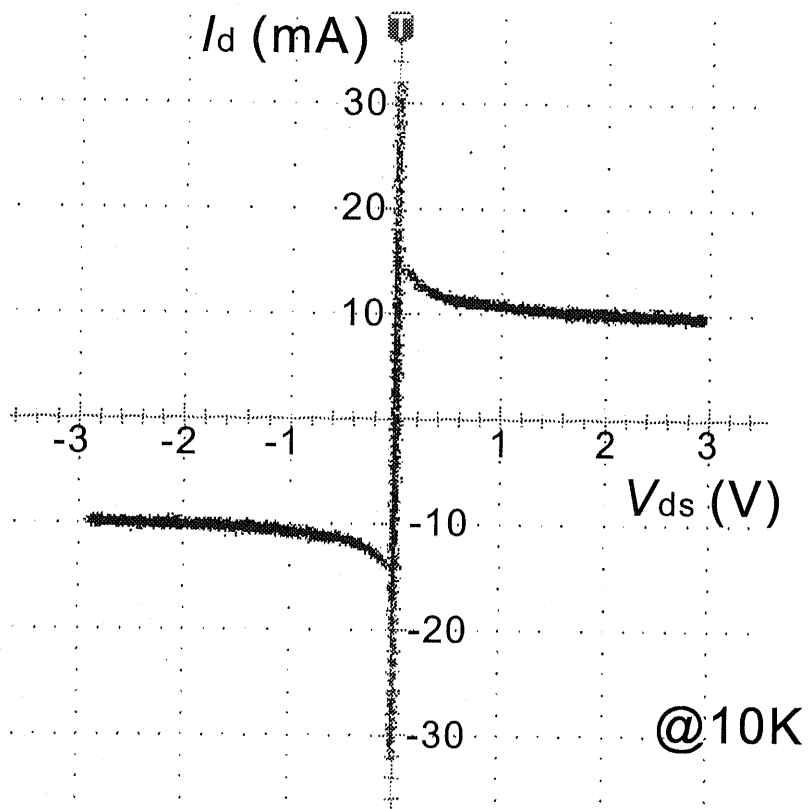Figure 3.2: (a) Circuit for measurement. (b) R–T characteristics.

(a)

I_d

V_{ds}

(b)

I_d (mA)

30

20

10

-3   -2   -1   1   2   3

V_{ds} (V)

-10

-20

-30   @10K

Figure 3.3: (a) Circuit for measurement. (b) I_d–V_{ds} characteristics. The bridge length was 60 μm and the bridge width was 4 μm.
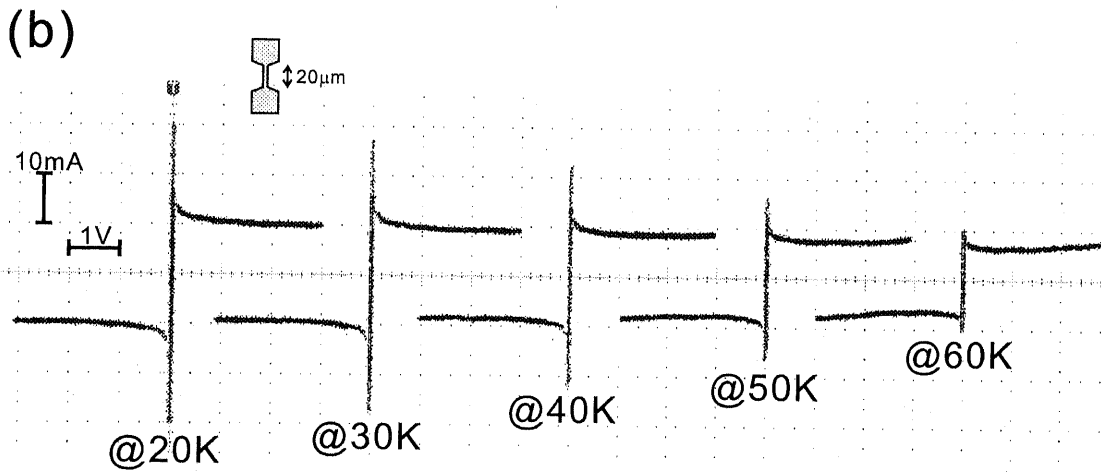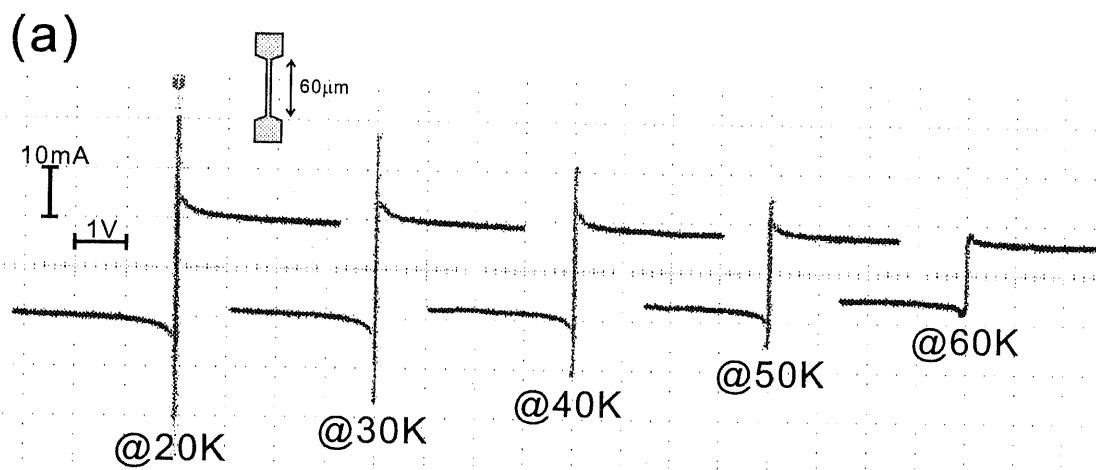
Figure 3.4: Temperature dependence. Bridge width = 4 μm. (a) Bridge length = 60μm. (b) Bridge length = 20μm.

swing. They are more obvious at low temperature because I_c is larger at low temperature and I_d must exceed that large I_c. This fast swing of I_d causes the vibrations.

According to Fig. 3.6, the slew rate is more than 20 V/μs at both the up edge and the down edge.

3.4 I_c–T Characteristics

We measured I_d–V_{ds} characteristics at various temperatures and plotted the I_c dependence on temperature (Fig. 3.7).

The value of I_c is almost constant when $T<20$ K, but it begins to decrease linearly above 20 K, and finally it becomes zero at 70~80 K.

3.5 I_d–V_{ds} Characteristics with Injection

We measured I_d–V_{ds} characteristics when gate current I_{inj} was injected. The circuit for measurement is shown in Fig. 3.8-(a). A current source was added to the circuit in Fig. 3.3-(a).

The results are shown in Fig. 3.8-(b). I_c decreases along with the increase in I_{inj}.

3.6 I_c–I_{inj} Characteristics

From the results of section 3.5, the I_c dependence on I_{inj} was acquired (Fig. 3.9). The curve in the first quadrant tells that the current gain $|\Delta I_c/\Delta I_{inj}|$ is no more than unity when $I_{inj}=0$~10 mA, and is 1.5~2 even at its maximum (I_{inj}~15 mA); this value is much smaller than the one referred to in section 2.1.1.

Such low current gain is derived from the absence of the barrier layer between Au and YBCO films. In the case of the device introduced in bibliography [4], there is an insulator layer of 3 nm. Therefore relatively high voltage is needed to inject quasi-particles and only the electrons whose energy is high enough to tunnel the barrier are injected. Such electrons that have high energy can break Cooper pairs efficiently and thus the current gain becomes large. However, we did not deposit insulator layer and tried to make the contact resistance between Au and YBCO as small as possible because the input voltage of this device, the voltage generated by a SQUID, is very small (~mV). As a result, the current gain remained small.

(a)

(V)

100ns

2

V_{ds} 1

0

(mA)

20

I_d 10

0

@10K

Ch1 1.00 V   Ch2 1.00 V   M 100ns   A Ch1 ∫ 300mV

(b)

(V)

100ns

2

V_{ds} 1

0

(mA)

20

I_d 10

0

-10
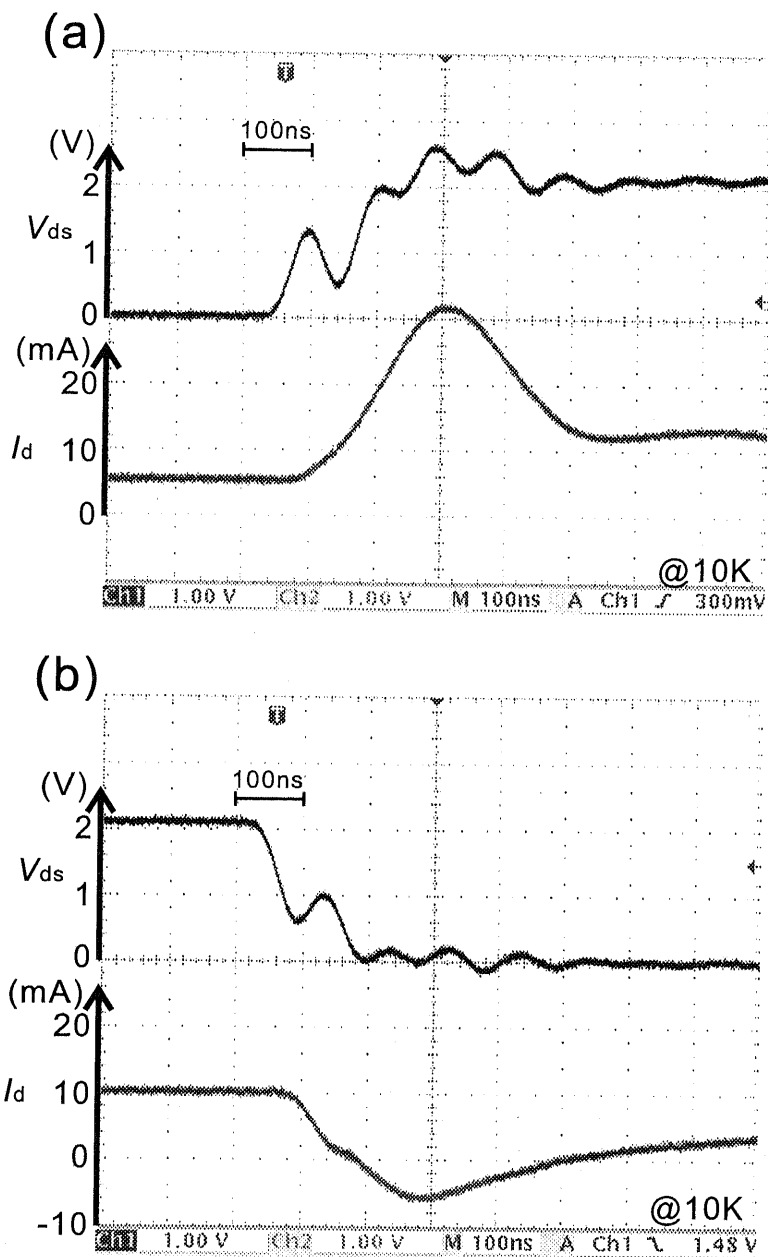
@10K

Ch1 1.00 V   Ch2 1.00 V   M 100ns   A Ch1 ⌐ 1.48 V

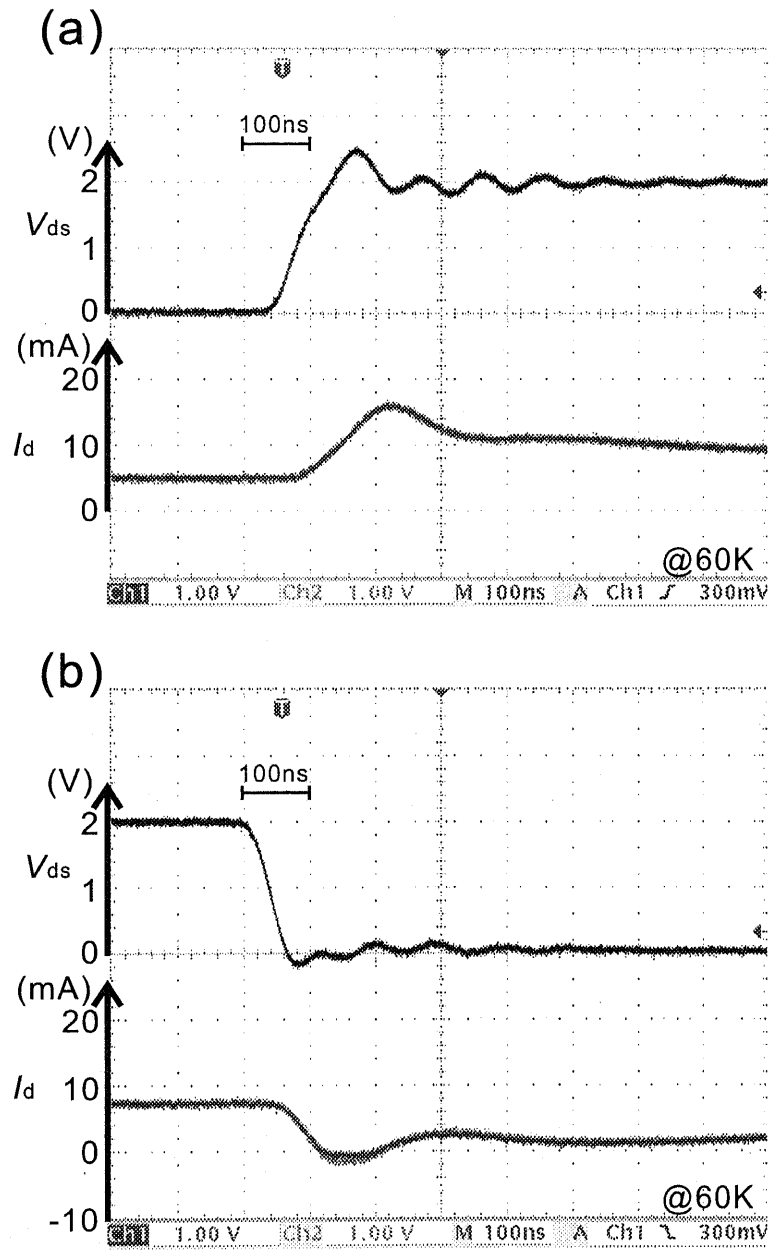Figure 3.5: I_d, V_{ds}–t characteristics @10 K. (a) Up edge. (b) Down edge.

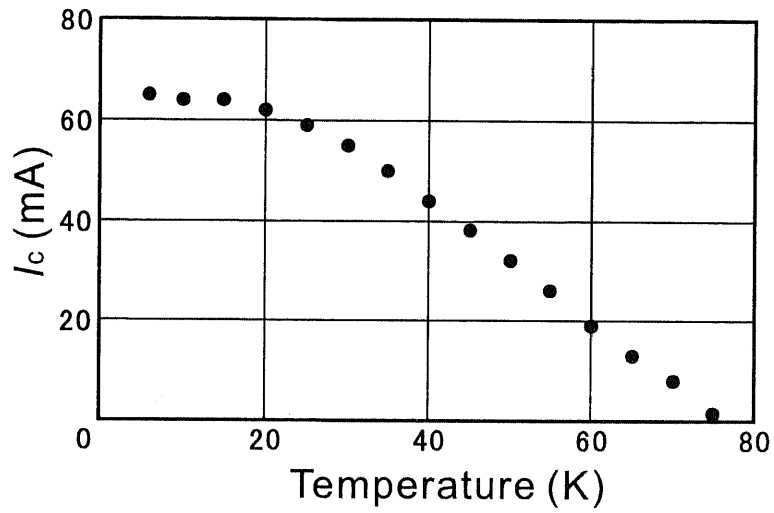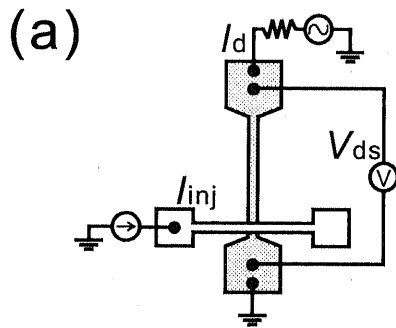Figure 3.6: I_d, V_{ds}–t characteristics @60 K. (a) Up edge. (b) Down edge.

23
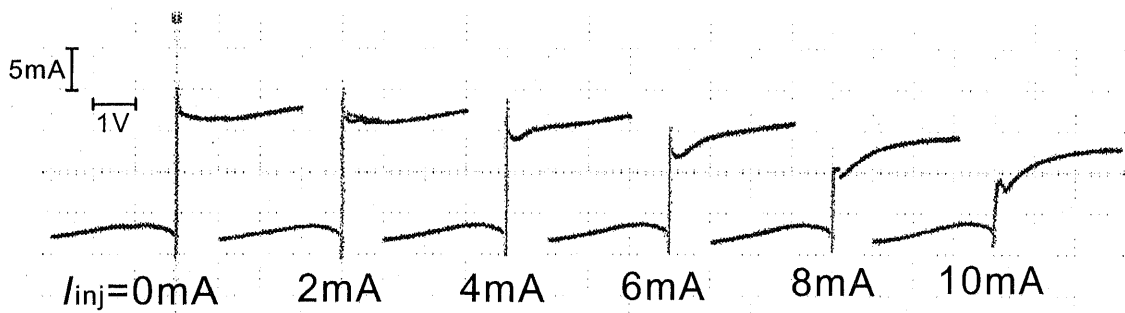
Figure 3.7: I_c–T characteristics.

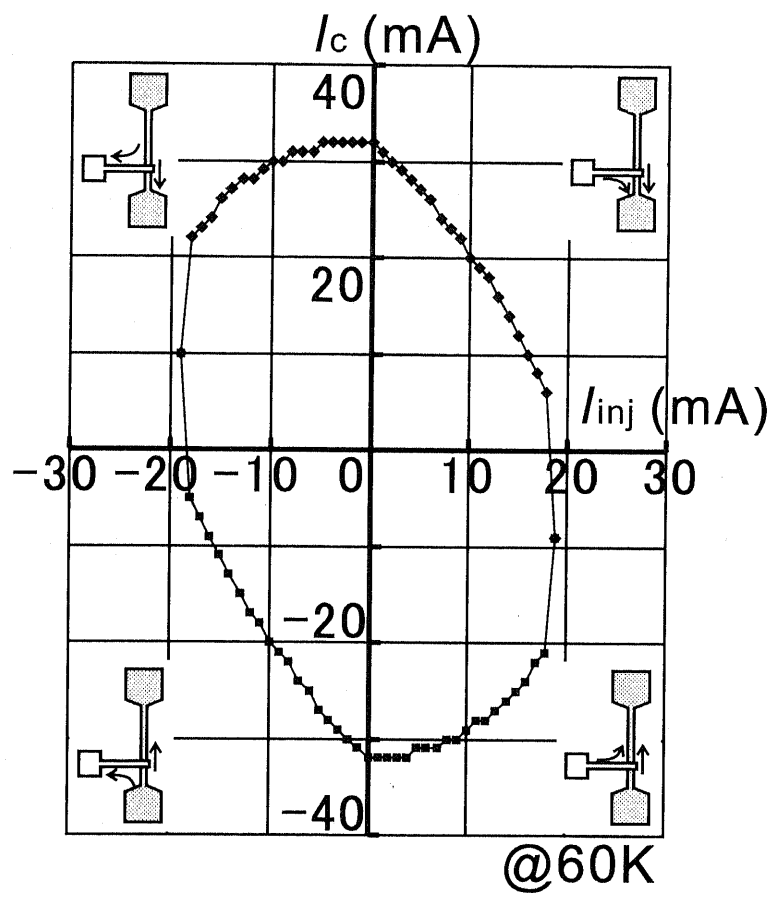Figure 3.8: (a) Circuit for measurement. (b) I_d–V_{ds} characteristics at various I_{inj}.

Figure 3.9: I_c–I_{inj} characteristics.

3.7 I_d, V_{ds}, V_{gs}—t

In order to observe the voltage distribution in the bridge, we made a device whose gate is in the middle of the bridge.

We measured I_d, V_{ds}, and V_{gs} with the circuit shown in Fig. 3.10-(a). The value of the voltage was expected to be

$$V_{gs} = \frac{V_{ds}}{2}, \tag{3.1}$$

because the gate is just in the middle of the bridge. However, Fig. 3.10-(b) does not agree with it; while V_{ds} is smaller than 3 V, V_{gs} remains much lower than $V_{ds}/2$, but when V_{ds} exceeds 3 V, V_{gs} begins to rise steeply and finally V_{gs} reaches $V_{ds}/2$ at about V_{ds}=5 V. This phenomenon means that not whole bridge becomes resistive at once; resistive area and superconductive area can exist juxtaposed at the same time. In the case of Fig. 3.10-(b),

- V_{ds}<3 V: only the area near the drain is resistive.

- 3 V<V_{ds}<5 V: the resistive area expands towards the source across the gate.

- 5 V<V_{ds}: whole bridge is resistive.

Of course, the opposite case may happen. In that case, V_{ds}=V_{gs} while V_{ds} is low. The mechanism of this phenomenon is explained by a simulation in chapter 4.
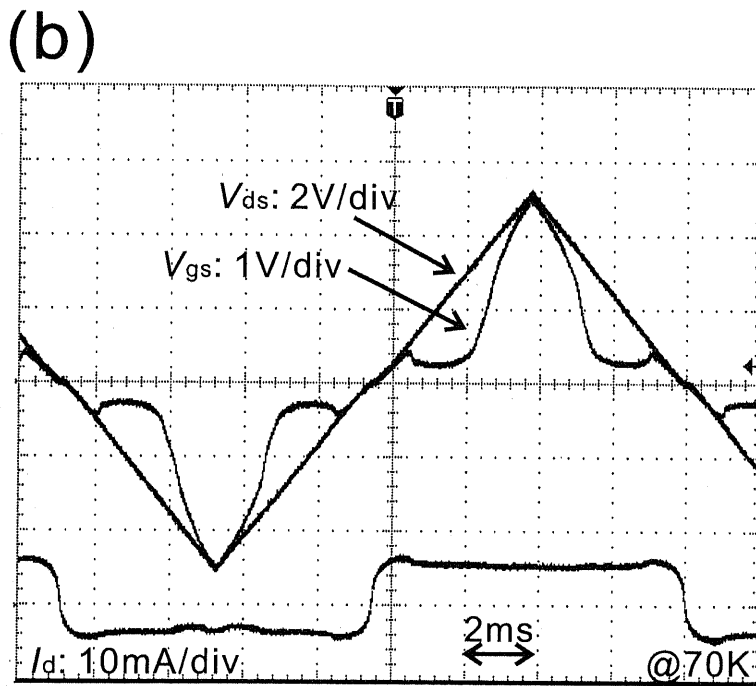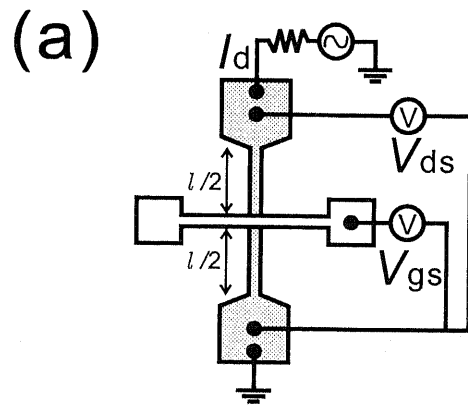
Figure 3.10: (a) Circuit for measurement. (b) I_d, V_{ds}, V_{gs}–t characteristics.

Chapter 4

Simulation for Device Analysis

4.1 Outline of the Analysis Method

We tried to explain the behavior of this device by means of the thermal analysis because the characteristics of this device are determined by the temperature of the bridge. In other words, the operation point (V_{ds}, I_d) can be calculated from the bridge temperature: when current I_d flows through the bridge, the area whose temperature is lower than the critical temperature $T_c(I_d)$ becomes superconductive and the area higher than $T_c(I_d)$ becomes resistive. The total resistance of the bridge R is given by the sum of the resistive area, and thus $V_{ds}=I_d \times R$ is obtained.

The analysis consists of two stages: heat generation process and heat conduction process. Detailed procedure is written in the following sections.

4.2 Heat Generation

Heat is generated at the resistive area in the bridge. The amount of the generated heat P is given by

$$P = \int_{\text{source}}^{\text{drain}} I^2 \cdot dR, \tag{4.1}$$

but it is not so easy to calculate the value of R at each point of the bridge. A few steps of calculation using the characteristics shown in Fig. 4.1 is necessary.

In Fig. 4.1-(a), I_c–T_c characteristics are shown. This graph is the same one as I_c–T characteristics shown in Fig. 3.7. From this graph, you can get T_c if you input I, and you can get I_c if you input T. Here we use this graph for the former usage.

Resistivity–temperature characteristics are shown in Fig. 4.1-(b). When $I=0$, resistivity ρ_r drastically changes at $T_c(0)$, but along with the increase in I, the change of ρ_r becomes smooth, as shown with dashed lines.
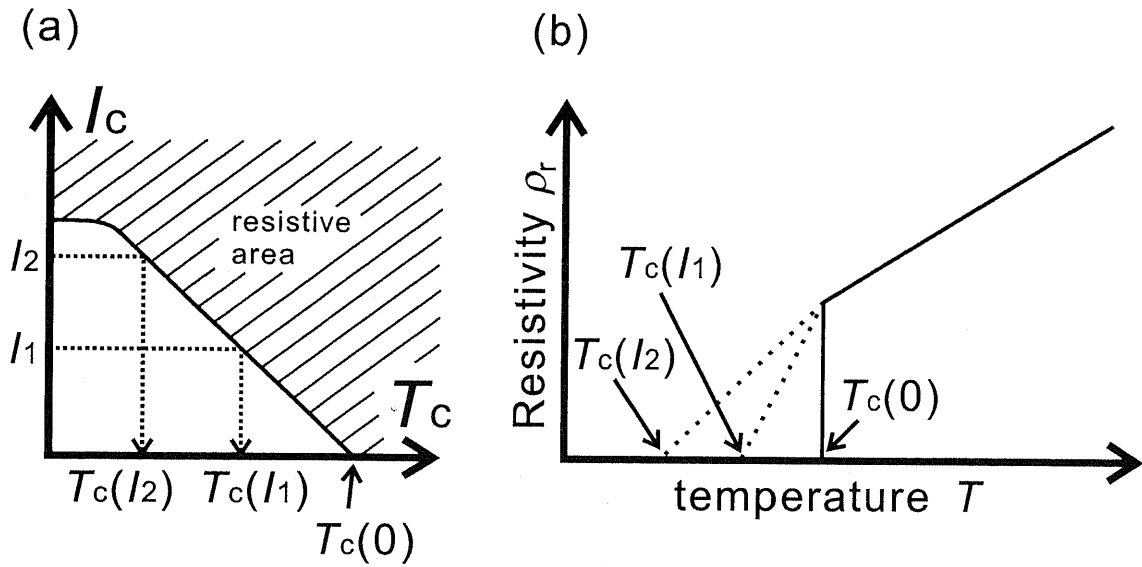
Figure 4.1: Resistance dependence on current and temperature. (a) I_c–T_c characteristics. If current I_1 flows through the bridge, the critical temperature is $T_c(I_1)$. (b) R–T characteristics. The curve becomes smoother along with the increase in I.

Using these graphs, we can calculate P. The procedure of the calculation is as follows:

1. Input the current value I into I_c–T_c graph and obtain $T_c(I)$. (Fig. 4.1-(a))

2. ρ_r–T curve is determined by $T_c(I)$. (Fig. 4.1-(b))

3. Input the bridge temperature T into ρ_r–T curve and obtain $\rho_r(I, T)$.

4. ΔR is obtained from $\rho_r(I, T)$ / (width × thickness) · Δlength.

5. ΔP is obtained from $I^2 \cdot \Delta R$.

4.3   Heat Conduction

4.3.1   Theory

The heat conduction model used for the thermal analysis is shown in Fig. 4.2-(a). For ease of calculation, we adopted cylindrical coordinate system.

The bridge and the heat conduction layers can be cut into mesh blocks like Fig. 4.2-(b). By applying heat balance equation

$$\text{(heat increase)} = \text{(inflow of heat flux)} \tag{4.2}$$

29

to the mesh blocks, we can calculate the heat conduction and understand the thermal behavior of this device.

In a small time fraction Δt,

(heat increase)

$$= \rho C_\mathrm{p} \cdot \frac{dT}{dt} \Delta t \cdot (\pi r \cdot \Delta r \cdot \Delta x)$$
$$= \rho C_\mathrm{p} \cdot \frac{dT}{dt} \cdot \pi r \cdot \Delta r \cdot \Delta x \cdot \Delta t, \tag{4.3}$$

where ρ is the density, C_p is the specific heat, T is the temperature of the mesh, and t is time.

(inflow of heat flux)

$$= \left[\{ \pi r \Delta x \cdot q_r - \pi (r + \Delta r) \Delta x \cdot q_{r+\Delta r} \} + \{ \pi r \Delta r \cdot q_x - \pi r \Delta r \cdot q_{x+\Delta x} \} \right] \Delta t$$
$$= \left\{ \pi r \Delta x \left(q_r - q_{r+\Delta r} \right) - \pi \Delta r \Delta x \cdot q_{r+\Delta r} + \pi r \Delta r \left(q_x - q_{x+\Delta x} \right) \right\} \Delta t$$
$$= \left\{ \pi r \Delta x \left(-\frac{dq_r}{dr} \Delta r \right) - \pi \Delta r \Delta x \cdot q_{r+\Delta r} + \pi r \Delta r \left(-\frac{dq_x}{dx} \Delta x \right) \right\} \Delta t$$
$$= \left\{ \left(-\frac{dq_r}{dr} - \frac{dq_x}{dx} \right) - \frac{q_r}{r} \right\} \pi r \cdot \Delta r \cdot \Delta x \cdot \Delta t \qquad (\because q_{r+\Delta r} \fallingdotseq q_r)$$
$$= \kappa \left\{ \left(\frac{d^2T}{dr^2} + \frac{d^2T}{dx^2} \right) + \frac{1}{r}\frac{dT}{dr} \right\} \pi r \cdot \Delta r \cdot \Delta x \cdot \Delta t, \tag{4.4}$$

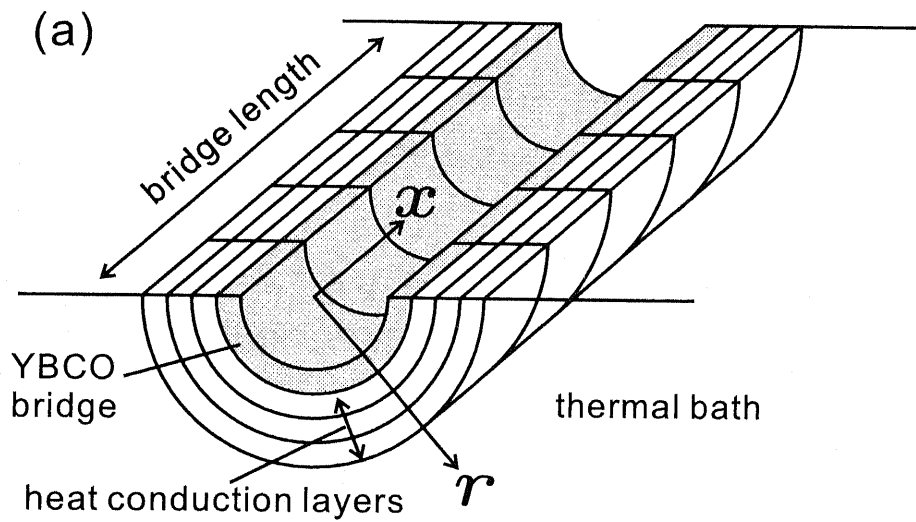where q is heat flux. In the equation modification, Fourier's law shown below was used:

$$q_x = -\kappa \frac{dT}{dx}, \tag{4.5}$$

where κ is the thermal conductivity.

From Eq. (4.3) and (4.4), we obtain

$$\rho C_\mathrm{p} \cdot \frac{dT}{dt} = \kappa \left\{ \left(\frac{d^2T}{dr^2} + \frac{d^2T}{dx^2} \right) + \frac{1}{r}\frac{dT}{dr} \right\}$$
$$\therefore \frac{dT}{dt} = k \left(\frac{d^2T}{dr^2} + \frac{d^2T}{dx^2} + \frac{1}{r}\frac{dT}{dr} \right), \tag{4.6}$$

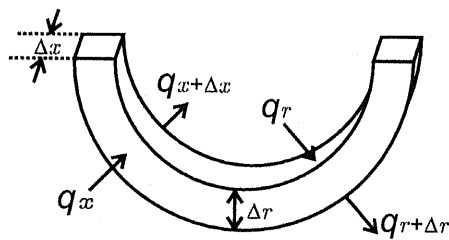where $k = \kappa/\rho C_\mathrm{p}$, called 'thermal diffusivity'.

Figure 4.2: Heat conduction model used for the thermal analysis of the device. (a) Schematic picture. (b) A mesh block.
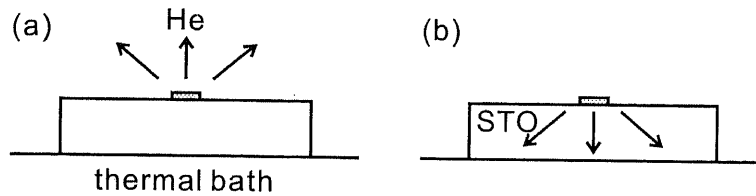
Figure 4.3: Path of heat conduction. (a) He gas. (b) STO substrate.

4.3.2 Substance of Heat Conduction

The candidates of the substance that conducts heat are these two:

- Helium (atmosphere)

- STO substrate

First, we assumed that the heat conduction is performed only by He (Fig. 4.3-(a)), but the simulation results showed that the time required to cool down the bridge is too long; the heat capacity of gas is too small compared with solid.

Another evidence that the heat conduction through He is not dominant is that the characteristics measured in vacuum were identical to that measured in He atmosphere.

Therefore, we concluded that it is STO substrate that conducts heat (Fig. 4.3-(b)).

4.4 Heat Radiation

Heat radiation is another way of device cooling. The amount of heat radiation is given by Stephan-Boltzmann's law

$$P = \sigma \cdot S \cdot T^4, \tag{4.7}$$

where P is radiated power, σ is a constant, S is the area, and T is the temperature. In the case of black body radiation, $\sigma = 5.67 \times 10^{-8}$ Wm^{-2}K^{-4}.

We tried to apply this effect to the device, but it turned out that heat radiation is not dominant as a cooling process of this device. Radiated power is much smaller than generated power (Tab. 4.1).

4.5 Physical Constants

4.5.1 Thermal Conductivity

Thermal conductivity of YBCO has dependence on temperature [9,10]. Roughly, the behavior is like Fig. 4.4-(a).

32

Table 4.1: Example of generated power and radiated power.
(current: 10 mA, bridge width: 5 μm, bridge thickness: 100 nm)

bridge temperature	generated power	radiated power
10 K	0 W/μm^2	$\sim$6$\times$10^{-16} W/μm^2
100 K	$\sim$4$\times$10^{-5} W/μm^2	$\sim$6$\times$10^{-12} W/μm^2
1000 K	$\sim$4$\times$10^{-4} W/μm^2	$\sim$6$\times$10^{-8} W/μm^2

As for STO, detailed data of thermal conductivity are not reported so far. Generally speaking, thermal conductivity of insulators behaves like Fig. 4.4-(b). $\kappa \propto T^3$ at very low temperatures, and $\kappa \propto T^{-1}$ at higher temperatures.

4.5.2 Specific Heat

There are some reports about the specific heat of YBCO [11,12]. We trusted and used these data for simulation.

As for STO, detailed data of specific heat are not reported so far. Therefore we estimated it using Debye's model. According to Debye's model, specific heat C_{p} of insulator is given by

$$C_{\mathrm{p}} = \frac{dE}{dT}, \tag{4.8}$$

where

$$E = 3Nk_{\mathrm{B}}T \left(\frac{T}{\Theta_{\mathrm{D}}}\right)^3 \int_0^{\Theta_{\mathrm{D}}/T} \frac{3x^3}{e^x - 1} dx, \tag{4.9}$$

N is the number of atoms, k_{B}=1.38$\times$10^{-23} J/K is the Boltzmann constant, Θ_{D} is Debye temperature. C_{p}–T/Θ_{D} graph is shown in Fig. 4.5.

When $T \gg \Theta_{\mathrm{D}}$, C_{p} is given by $3Nk_{\mathrm{B}}$. An STO crystal unit cell consists of 5 atoms (Sr$\times$1, Ti$\times$1, O$\times$3) and the molecular weight of STO is 87.6+47.9+16.0$\times$3=183.5. From these data, we obtain the specific heat of STO at $T \gg \Theta_{\mathrm{D}}$:

$$3 \times (5 \times N_{\mathrm{A}}) \times k_{\mathrm{B}} \div 183.5 \text{ g/mol} = 6.8 \times 10^2 \text{ J/kg} \cdot \text{K}, \tag{4.10}$$

where N_{A}=6.02$\times$10^{23} mol^{-1} is the Avogadro constant.

However, Θ_{D} of STO is not sure; we chose the value so that the simulation fits the measurement results.
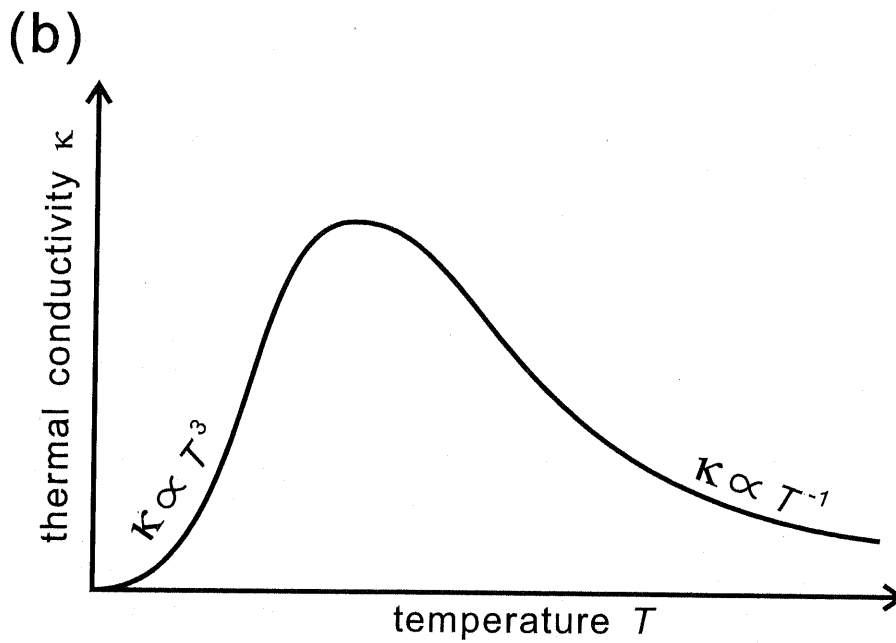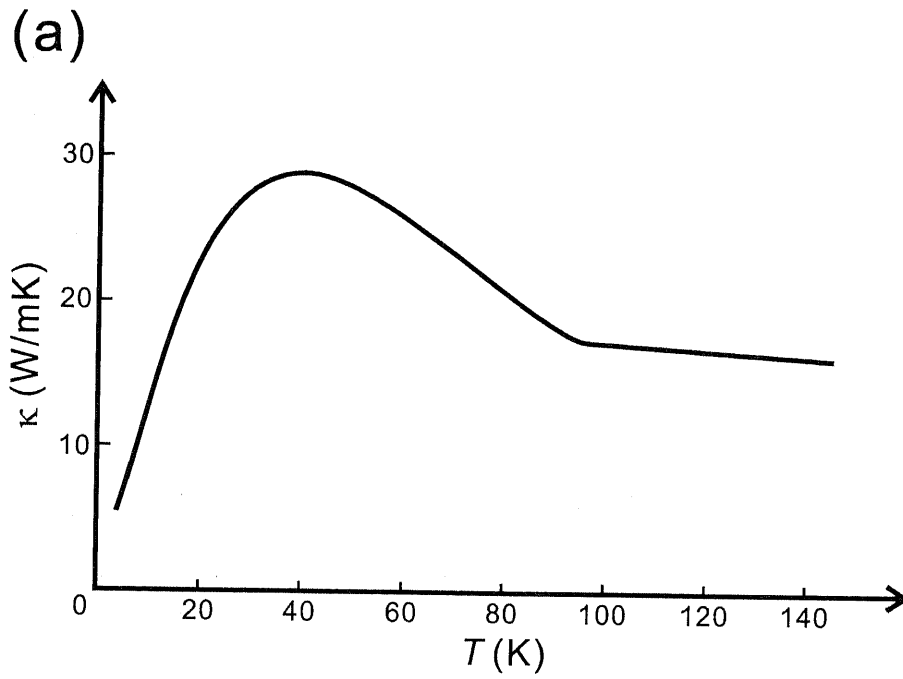
(a)

(b)

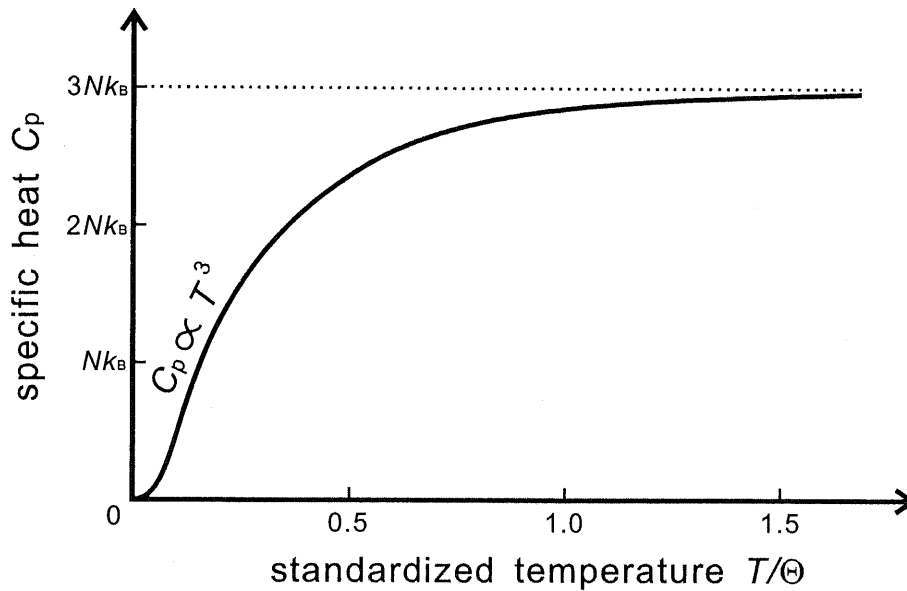Figure 4.4: Temperature dependence of the thermal conductivity. (a) YBCO [10]. (b) Insulators.

Figure 4.5: Specific heat of N atoms.

Table 4.2: Other physical constants needed for the simulation.

density of YBCO	6.4×10^3 kg/m^3
density of STO	5.120×10^3 kg/m^3
critical current density of YBCO @10 K	$10^{10} \sim 10^{11}$ A/m^2
resistivity/T of YBCO in resistive state	$\sim 10^{-8}$ Ωm/K

4.5.3 Other Physical Constants

Other physical constants necessary for the simulation of the thermal activity are shown in Table 4.2. The density of YBCO and STO are necessary to calculate the thermal diffusivity. The critical current density J_c is needed to calculate the critical current I_c; multiplying J_c by the cross sectional area of the bridge, we can get I_c. We also need the resistivity of YBCO to calculate the heat generation, but here in this table we listed 'resistivity/T', not resistivity, because the resistivity of YBCO above $T_c(0)$ is proportional to temperature, as can be understood from Fig. 4.1-(b). Multiplying 'resistivity/T' by temperature, we can get the resistivity at that temperature.
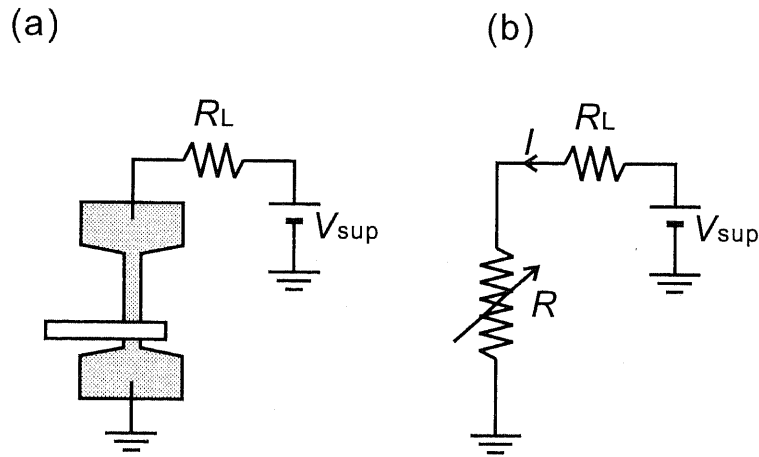
(a)   (b)

Figure 4.6: (a) Schematic picture of the device and its peripheral circuits. (b) Equivalent circuits of the device (no current injection).

4.6   Simulation Procedure

First, we simulate the device characteristics without the quasi-particle injection. The schematic picture of the device is shown in Fig. 4.6-(a) and its equivalent circuits are shown in Fig. 4.6-(b).

The procedure of the simulation is as follows. A flow chart of this procedure is shown in Fig. 4.7.

1. Reset the time counter; $t=0$.

2. Assume that $I=0$.

3. Calculate T_c and then R, according to the procedure written in section 4.2.

4. Compare $V_{sup}/(R_L+R)$ with I; if I is larger, go to the next step; else add ΔI to I and go back to step 3, because it means that 'R is too small' = 'T_c is too high' = 'I is to small'.

5. Calculate heat generation at the bridge.

6. Calculate heat conduction for all the meshes and determine the temperature.

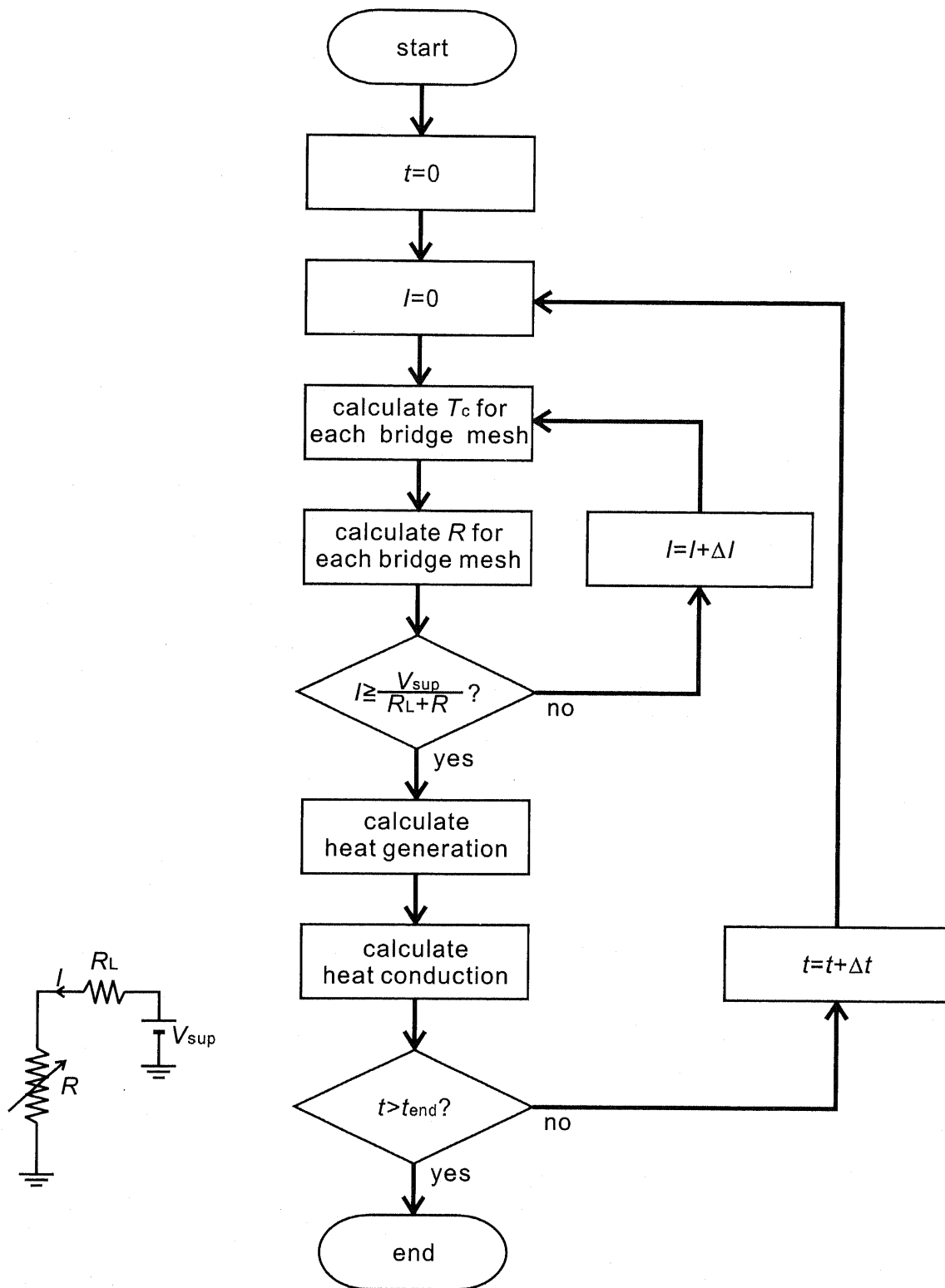7. Increase the time counter and go back to step 2.

Figure 4.7: Flow chart of the simulation.

4.7 Simulation Results: I_d–V_{ds} Characteristics and the Bridge Temperature

The simulation results of the I_d–V_{ds} characteristics without injection (Fig. 4.6-(b)) are shown in Fig. 4.8-(a) and 4.9-(a). The thermal bath temperature of Fig. 4.8-(a) is 20 K and that of Fig. 4.9-(a) is 60 K. The width and the length of the bridge are 4 μm and 60 μm, respectively. These graphs agree to the measurement results shown in Fig. 3.4-(a) to some extent. The graphs of the temperature distribution shown in Fig. 4.8-(b) and 4.9-(b) are very interesting. These graphs mean that the resistive area and the superconductive area exist together stably at the same time. Along with the increase in V_{ds}, the resistive area expands, so that the resistance R is proportional to V_{ds}. This is why I_d is fixed to I_n.

Accurately speaking, however, the width of the bridge is not uniform; there are fluctuations in width due to fabrication process such as lithography and ion milling. Taking this fact into consideration, we simulated the characteristics of a device whose bridge has some narrow points. The results are shown in Fig. 4.10. The temperature around the narrow points rises first, and then gradually the heated area expands. This behavior perfectly corresponds to the measurement results in section 3.7.
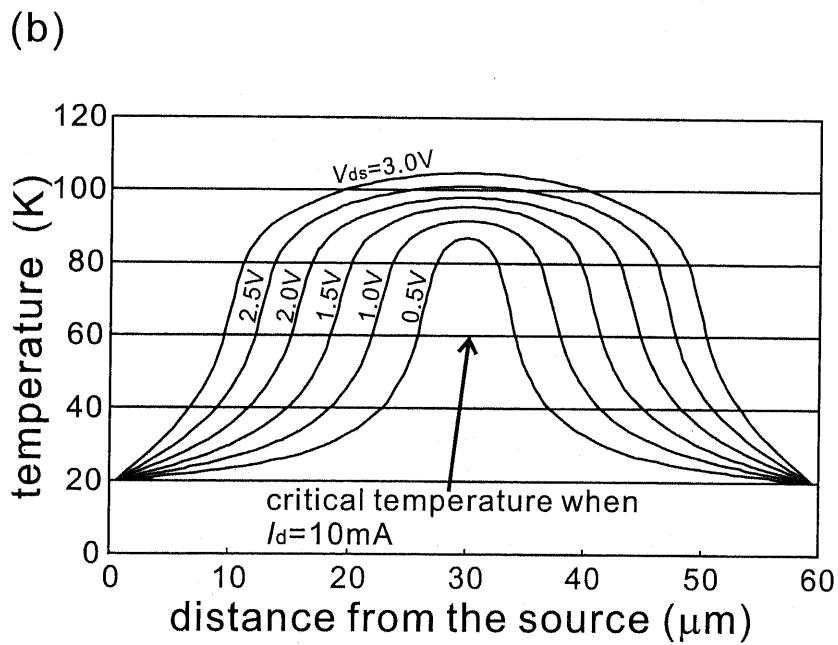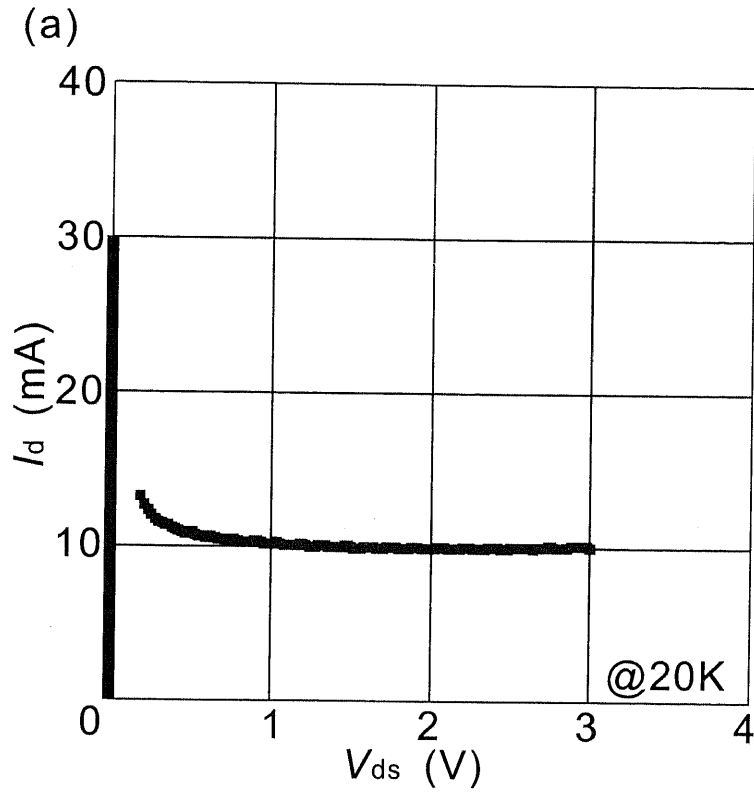
Figure 4.8: Simulation results. (a) I_d–V_ds characteristics at 20 K. (b) Temperature distribution.
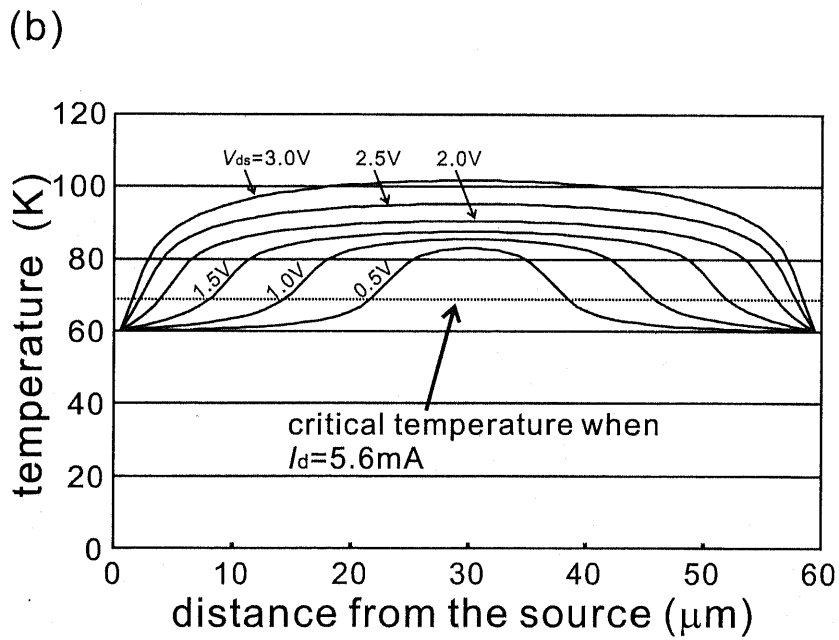
(a)

(b)
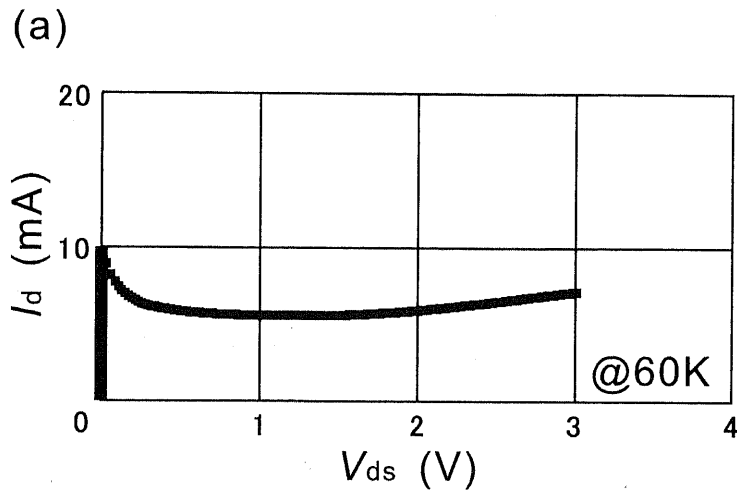
Figure 4.9: Simulation results. (a) I_d–V_{ds} characteristics at 60 K. (b) Temperature distribution.

(a)

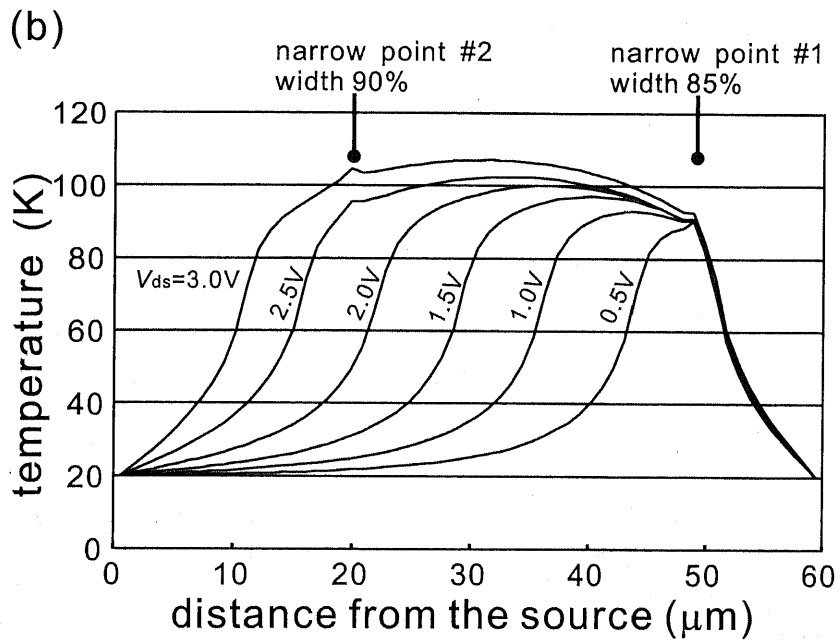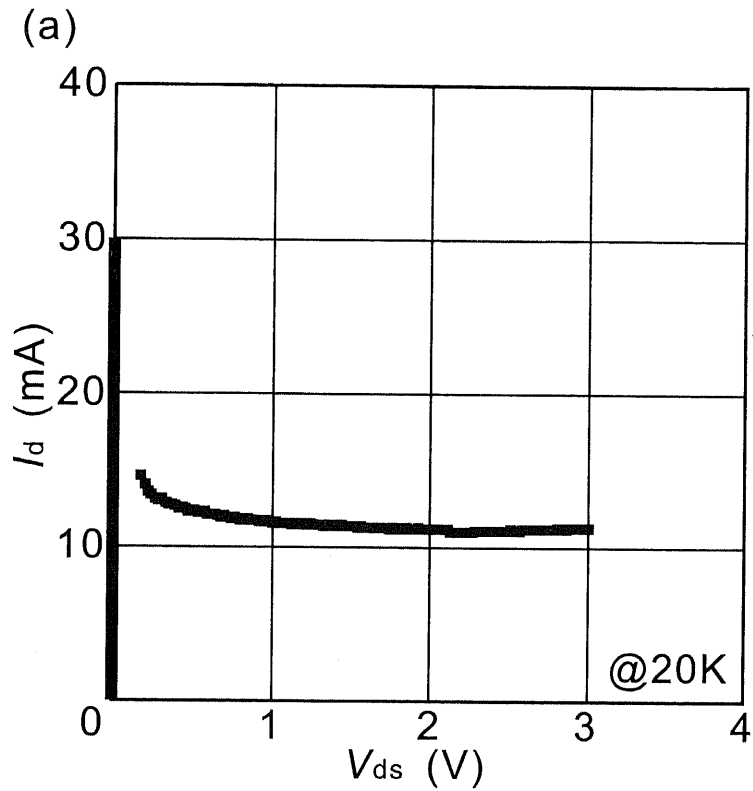**(b)**

narrow point #2
width 90%

narrow point #1
width 85%

Figure 4.10: Simulation results in the case the bridge width is not uniform. (a) I_d–V_{ds} characteristics at 20 K. (b) Temperature distribution. The temperature around the narrow point rises first.

Chapter 5

Switching Characteristics

5.1 Introduction

In this chapter, the switching characteristics are discussed from various points of view. First, the measurement results and the simulation results of the switching characteristics are compared and the reliability of the simulator is ensured. Then, the characteristics dependence on the device size is calculated by simulation and the scaling effects are evaluated.

There are two kinds of operation modes for this switching device: non-latching mode and latching mode. "Non-latching" means that I_d is fixed and the state of the device can be switched only by V_{inj} (Fig. 5.1-(a)). On the contrary, "latching" means that not only V_{inj} but also I_d must be reset to 0 after the device has become ON because once V_{inj} becomes high and the device is turned ON, it will not be reset even if V_{inj} becomes 0 (Fig. 5.1-(b)).

Whether the operation mode is non-latching or latching depends on the value of I_d. If I_d is settled to a value lower than I_n, the device is operated in non-latching mode, and if I_d is higher than I_n, it is operated in latching mode.

5.2 Non-Latching Mode Operation

5.2.1 Measurement Results

We have tested if non-latching operation is possible, because non-latching operation has an advantage from the viewpoint of making the peripheral circuits as simple as possible.

We measured the switching speed of this device. For the measurement, we used the circuits shown in Fig. 5.2. The results are shown in Fig. 5.3 and 5.4. Fig. 5.3 was measured at 20 K and Fig. 5.4 at 60 K. The bridge dimensions were 20 μm in length, 4 μm in width, and 100 nm in thickness. The rise time and the fall time can be read from these graphs; they are listed in Table 5.1.
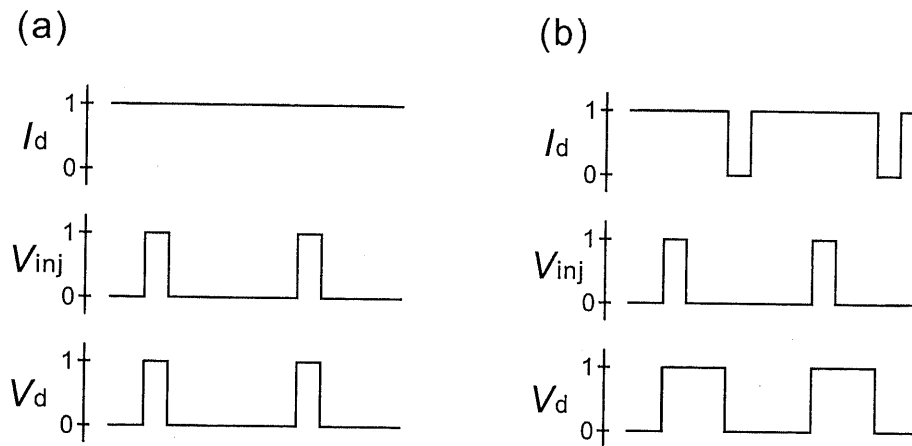
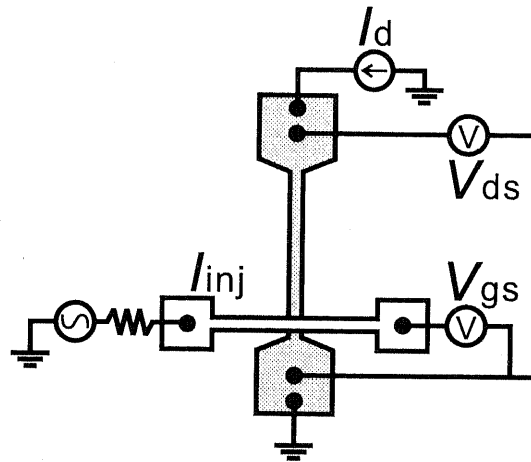Figure 5.1: Timing chart. (a) Non-latching mode. (b) Latching mode.

Figure 5.2: Circuit for response time measurement.

Qualitatively, the rise time is shorter at higher temperature and the fall time is shorter at lower temperature. This can be explained by the fact that the state of this device is determined by the temperature of the bridge; when the bridge is at a high temperature, it becomes resistive and V_{ds} appears, and when at low temperature, it becomes superconductive and V_{ds} disappears. Therefore, the rise time is short and the fall time is long when the thermal bath temperature is high because the bridge is easily heated but it is difficult to cool it down. Vice versa in the case of low thermal bath temperature.

The circuit for ON/OFF operation is the same one as that shown in Fig. 5.2 and the results are shown in Fig. 5.5 and 5.6. Fig. 5.5 is the results of the device with the bridge length of 20 μm and Fig. 5.6 is that of 60 μm bridge. When V_{inj} was applied to the gate electrode, V_{ds} appeared. However, V_{gs} also rose to as

(a)
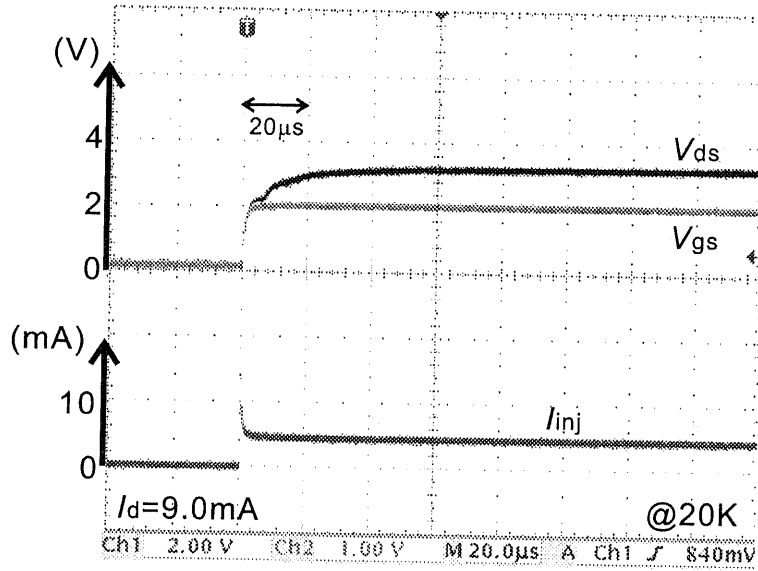
(b)
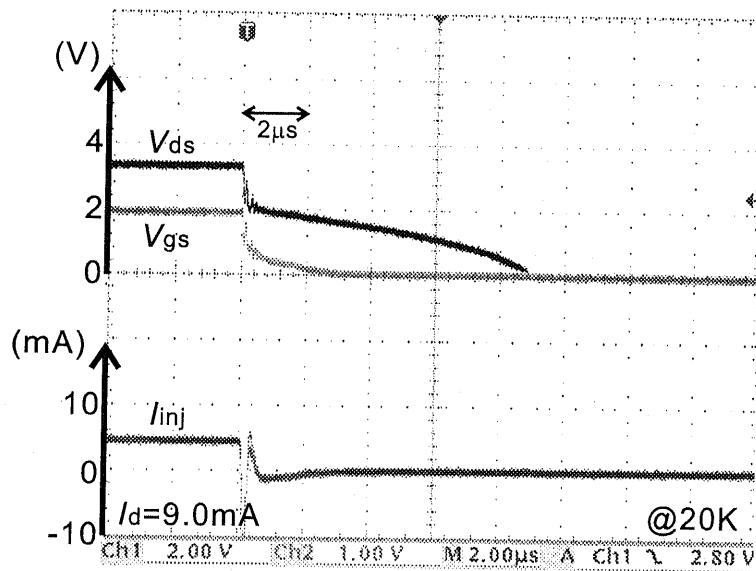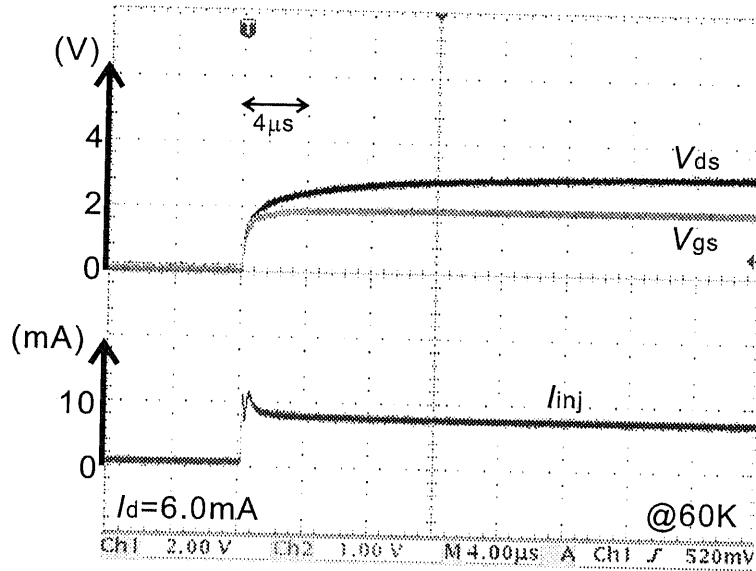

Figure 5.3: I_{inj}, V_{ds}, V_{gs}–t characteristics @20 K. I_d was fixed to 9.0 mA. (a) Up edge. (b) Down edge.
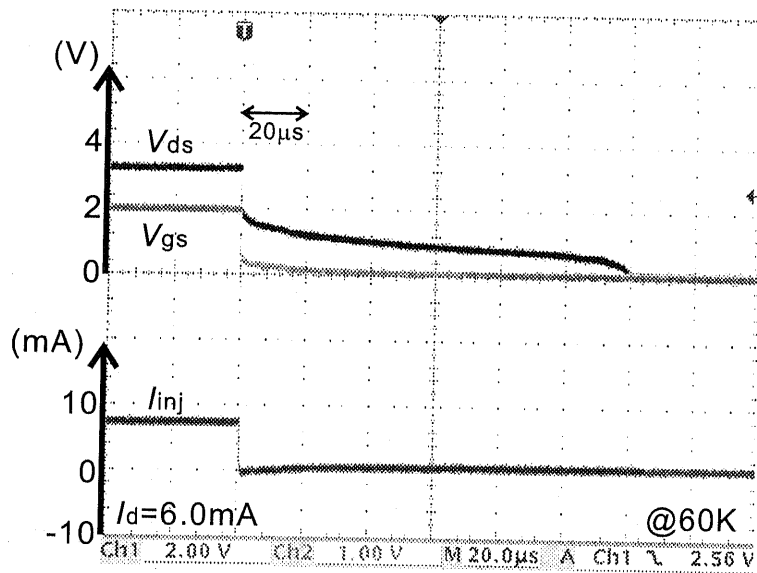
44

Figure 5.4: V_{ds}, V_{gs}, I_{inj}–t characteristics @60 K. I_d was fixed to 6.0 mA. (a) Up edge. (b) Down edge.

Table 5.1: Rise time and fall time.

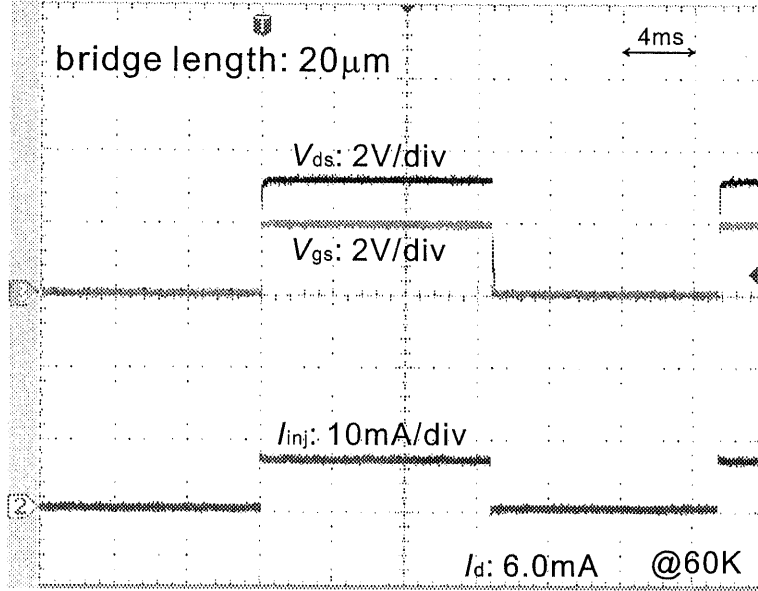|	rise time	fall time
20 K	~50 μs	~10 μs
60 K	~20 μs	~120 μs

Figure 5.5: Non-latching operation of the device with the bridge length of 20 μm. I_{d} was fixed to 6.0 mA. The amplification factor is 3.2/2.0=1.6.

high as 2 V. In order to operate this device with the voltage generated by SFQ circuits, V_{gs} must be kept much lower.

The relation between the voltage gain $V_{\mathrm{ds}}/V_{\mathrm{gs}}$ and the position of the injector x is described by an equation

$$\frac{V_{\mathrm{ds}}}{V_{\mathrm{gs}}} = \frac{I_{\mathrm{d}} \times (l - x) + (I_{\mathrm{d}} + I_{\mathrm{inj}}) \times x}{(I_{\mathrm{d}} + I_{\mathrm{inj}}) \times x}, \tag{5.1}$$

where l is the length of the bridge and x is the distance from the source to the injection area (Fig. 5.7).

Now let us apply this equation to the measurement results in Fig. 5.5. Substitute V_{ds}=3.2 V, V_{gs}=2.0 V, I_{d}=6.0 mA, I_{inj}=7.0 mA, l=20 μm and we obtain x=8.7 μm.

Then, using this value, we can estimate the voltage gain of 60 μm-bridge device. Substitute I_{d}=5.0 mA, I_{inj}=7.5 mA, l=60 μm, which are the values of Fig. 5.6, and we obtain $V_{\mathrm{ds}}/V_{\mathrm{gs}} = 3.4$. However, the measurement result was only
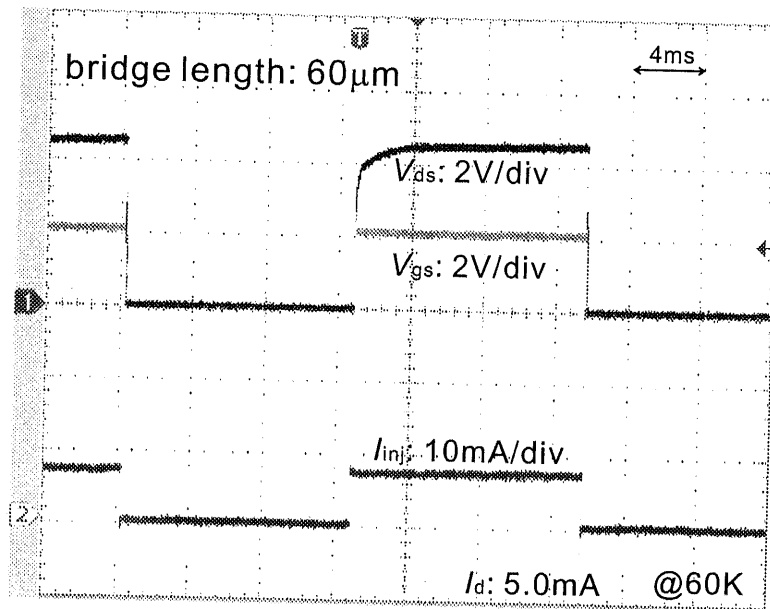
Figure 5.6: Non-latching operation of the device with the bridge length of 60 μm. I_d was fixed to 5.0 mA. The amplification factor is 4.4/2.0=2.2.

2.2. This fact infers that the whole bridge did not change to resistive state when I_{inj} was injected; the area near the drain may have remained superconductive. In order to investigate this phenomenon, we simulated the thermal behavior of this device.

5.2.2 Simulation Results

The schematic picture of the device and its equivalent circuits are shown in Fig. 5.8. The simulation was done based on the circuits in Fig. 5.8-(b). The difference from Fig. 4.6 is the existence of the gate electrode. Because of this change, a few new parameters were introduced: V_{inj}, R_{inj}, and $I_2(=I_{inj})$. R was divided into R_1 and R_2.

As for the current gain, we considered it to be unity, because there was almost no current gain when I_{inj} is small, as shown in Fig. 3.9.

Examples of the simulation results of non-latching mode operation are shown in Fig. 5.9 and 5.10. The former is V_{ds}, V_{gs}, $I_{inj}-t$ characteristics and the latter is the temperature distribution of the bridge. The length, width, and thickness of the bridge are 60 μm, 4 μm, and 100 nm, respectively. The characteristics shown in Fig. 5.9 agrees with Fig. 5.3 very well, which proves that the simulation method is reliable.

The temperature distribution shown in Fig. 5.10 brings us important information. When the device is operated in non-latching mode, whole bridge does not
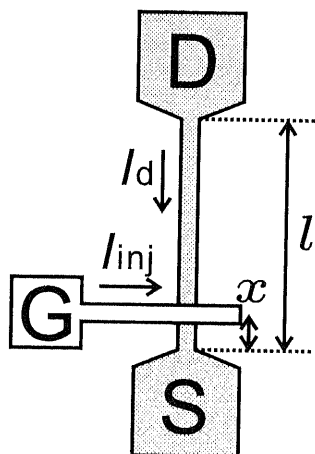
47

Figure 5.7: Parameters for the calculation of voltage gain.

(a)   (b)
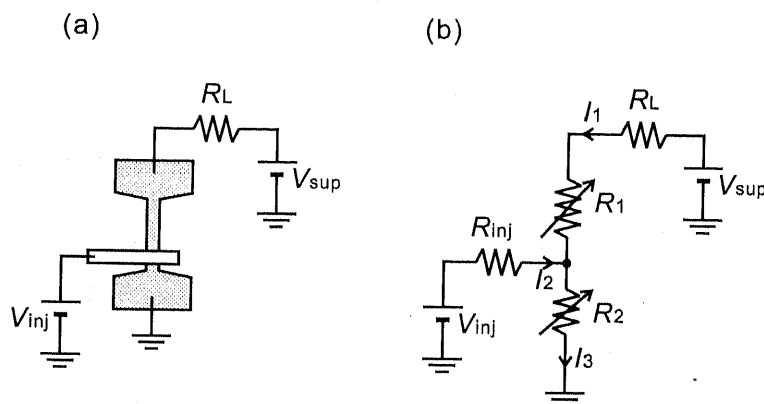
Figure 5.8: (a) Schematic picture of the device and its peripheral circuits. (b) Equivalent circuits of the device.

become resistive. The temperature rises only at the area near the gate electrode and the rest of the bridge remains superconductive; high temperature area hardly spreads towards the drain. The hypothesis described in section 5.2.1 was correct.

Anyway, the response time was too long and the voltage gain was too low for practical use when the device was operated in non-latching mode, and the reason of this drawback is that I_d is too small to produce enough heat. In order to make whole bridge resistive and obtain high voltage gain, I_d must be larger than I_n, the device being operated in latching mode.

48

(a)

(V)
4
2
0

20µs

V_{ds}

V_{gs}

(mA)
10
0

I_{inj}

I_{d}=7.5mA (0.25I_{c}) @20K

V_{inj}=2V, injection point: 3µm

(b)

(V)
4
2
0

2µs

V_{ds}

V_{gs}

(mA)
10
0

I_{inj}

I_{d}=7.5mA (0.25I_{c}) @20K

V_{inj}=2V, injection point: 3µm
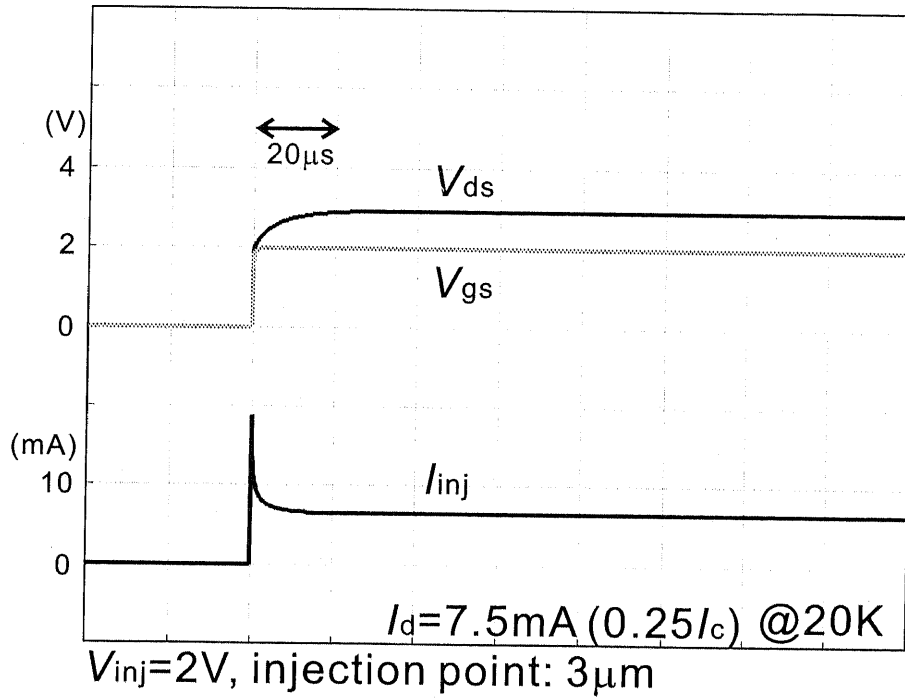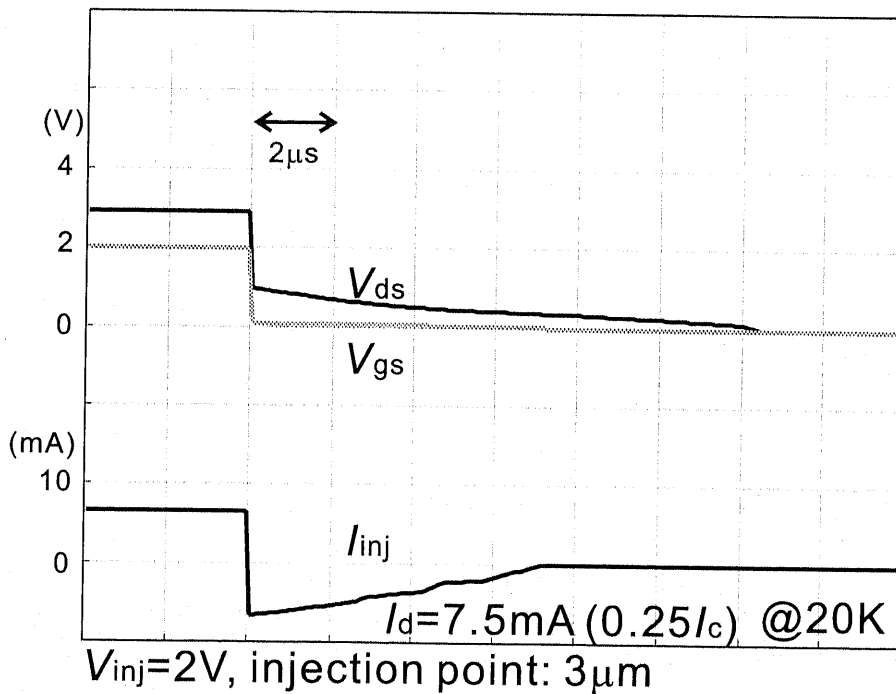
Figure 5.9: V_{ds}, V_{gs}, I_{inj}–t characteristics in non-latching operation.
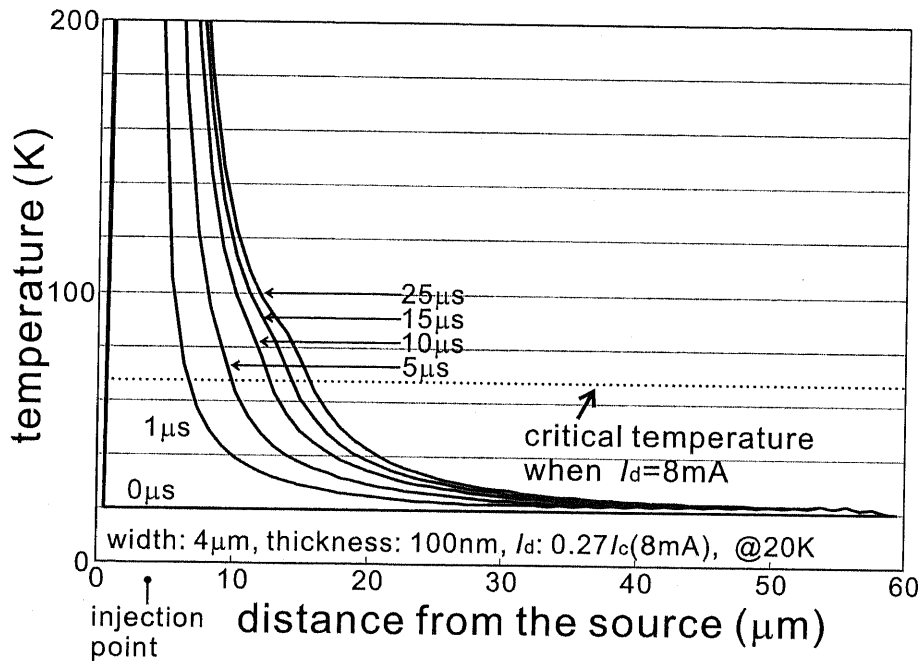
Figure 5.10: Device temperature in non-latching operation. More than half of the bridge remains superconductive.

5.3 Latching Mode Operation

5.3.1 Measurement Results

Such being the case, we operated the device with latching mode. The measurement circuit is shown in Fig. 5.11. Different from the circuit in Fig. 5.2, I_d was provided by V_{sup} and R_L, not by a current source, to prevent the device from being overheated. If a current source was used, once the device was turned on, the device temperature would rise higher and higher, and finally the device may break down. If a voltage source was used, I_d decreases as the device temperature rises and the resistance increases; the voltage applied between the drain and the source never exceeds V_{sup}.

The results are shown in Fig. 5.12. The bridge dimensions were 60 μm in length, 6 μm in width, and 100 nm in thickness. V_{sup}=6.0 V in (a) and V_{sup} =5.0 V in (b), and R_L was 100 Ω. Therefore the initial value of I_d is 60 mA in (a) and 50 mA in (b). At the up edge, vibrations were observed. They are probably caused by the parasitic capacitance and inductance. The real waveform of I_{inj} is steeper than that shown in Fig. 5.12 because the high frequency characteristics of the differential amplifier is not so good, as written in section 3.3.

The up edge of V_{ds} showed saturation because I_d decreased with the increase in V_{ds}, but the response time was about 1/100~1/1000 of that of non-latching
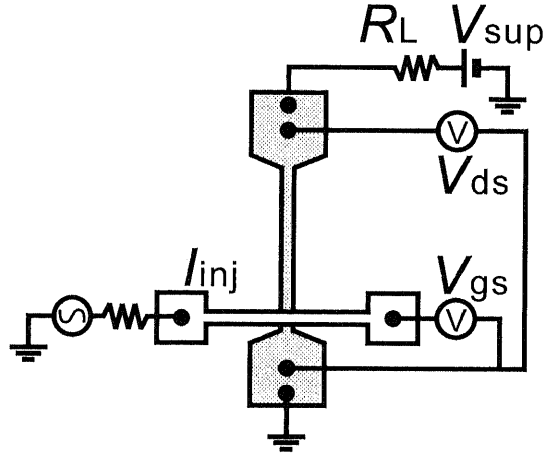
50

Figure 5.11: Measurement circuit for latching mode operation. I_d was provided by voltage source, not by current source, lest the device should be overheated.

operation.

5.3.2 Simulation Results

The simulation results of the circuits in Fig. 5.11 are shown in Fig. 5.13. The values of the parameters were determined so that the results would fit with the measurement results in Fig. 5.12-(a). From the results, it can be said that the features such as the saturation in V_{ds}, the gradual decrease in V_{gs} after a peak, and the gradual increase in I_{inj} after the decrease to under zero, are in good agreement with the measurement results, though the vibrations do not appear in the simulation because the parasitic effects are not considered.

We concluded from the results above that the simulation is quite reliable. Based on this, we decided to simulate latching mode operation of the circuits shown in Fig. 5.2 and discuss the switching characteristics.

Fig. 5.14-(a) is the V_{ds}, V_{gs}, I_{inj}–t characteristics and Fig. 5.14-(b) is the temperature distribution. The bridge dimensions are 4 μm in width and 100 nm in thickness; the same as the fabricated devices. The bias current I_d was set to $0.98I_c$. From Fig. 5.14-(a), turn on slew rate is estimated to be about 0.6 V/ns. It turned out that the slew rate increases exponentially against I_d. The detailed results are shown later. From Fig. 5.14-(b), it is obvious that whole bridge changed to resistive state, different from the case in non-latching mode operation.

The results of a small-sized device are shown in Fig. 5.15. The bridge dimensions are 1 μm in width and 10 nm in thickness. I_d was set to $0.97I_c$. The values of V_{gs}, I_{inj}, and the bridge temperature were drastically reduced by the scaling. They are by far lower than those in Fig. 5.14.

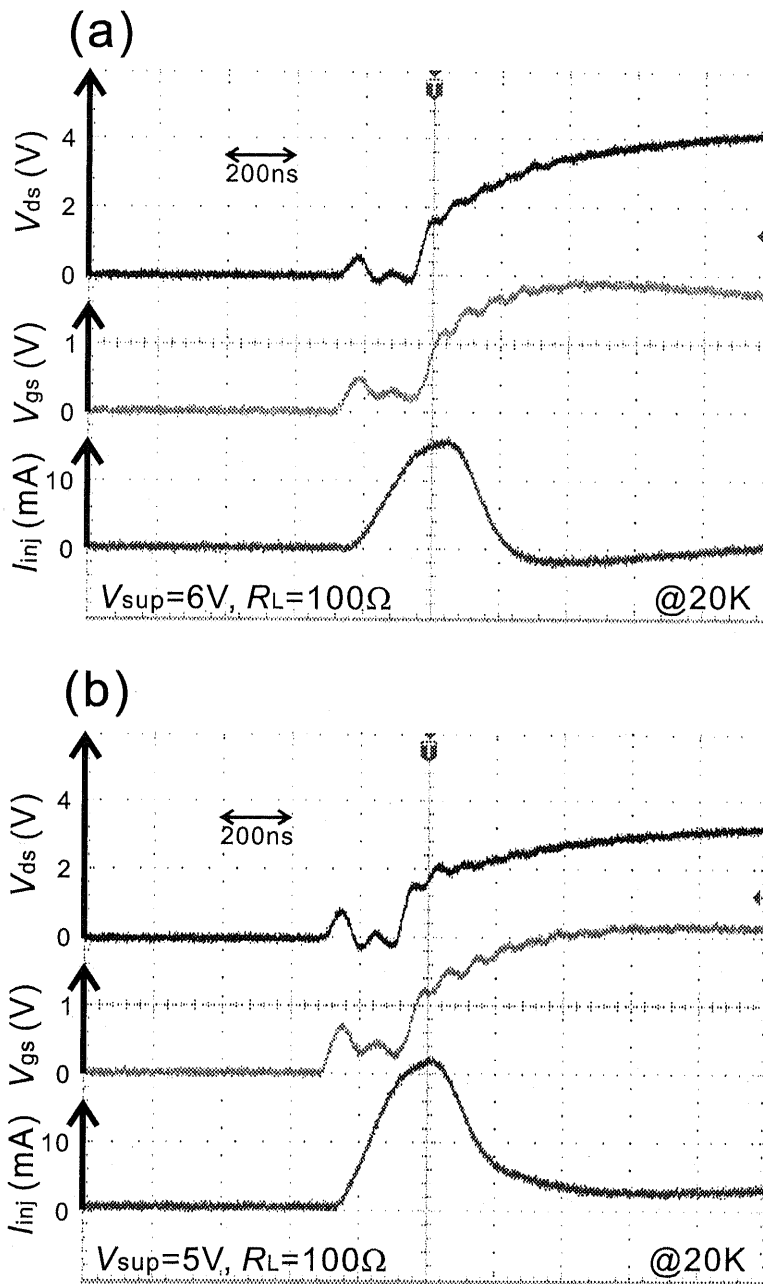51

Figure 5.12: Latching mode turn on characteristics @20 K. (a) Initial bias current = 60 mA = $0.91I_c$ (V_{sup} =6 V, R_L = 100 Ω). (b) Initial bias current = 50 mA = $0.76I_c$ (V_{sup} =5 V, R_L = 100 Ω).
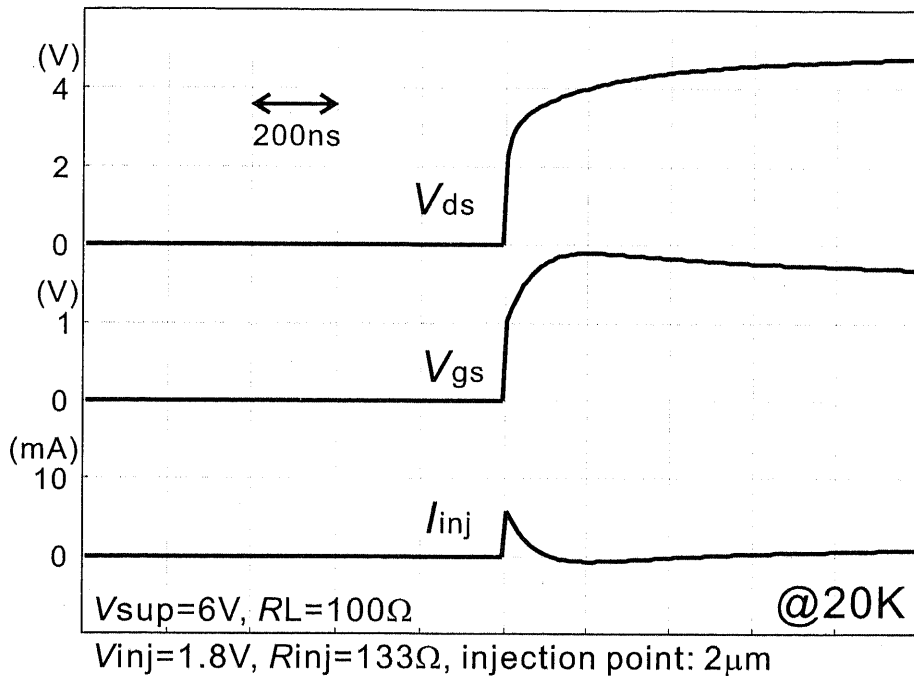
Figure 5.13: Simulation results of latching mode turn on characteristics @20 K.

Slew Rate

We investigated the turn on slew rate dependence on the thermal bath temperature and the bridge dimensions. The dependence on the thermal bath temperature is shown in Fig. 5.16. Over 20 K, the slew rate decreases as the temperature increases. At a high temperature, I_c is small and thus I_d must be also small. The amount of heat generation is determined by $I_d{}^2 R$ and this value is related to the heat conduction speed. Therefore, the slew rate is large at low temperatures. Below 20 K, however, the slew rate is almost the same. Actually, the slew rate at 5 K is even smaller than that at 20 K. This fact seems to conflict with the explanation above, but it is easily understood by the I_c–T characteristics in Fig. 3.7; I_c is roughly the same below 20 K. Under such a condition, the slew rate is large at higher temperature because the heat required to change the state to resistive is small; at 5 K, the temperature must rise by $(T_c(I_d)$-5) K to become resistive, but at 20 K, only $(T_c(I_d)$-20) K is required.

The dependence on the bridge width is shown in Fig. 5.17. The top speeds are almost the same regardless of the bridge width, but the speed when I_d is smaller varies widely: in the case of 4 μm width bridge, slew rate falls slowly with the decrease in I_d, but in the case of 0.1 μm width bridge, it falls very steeply.

The same inclination was observed for the dependence on the bridge thickness, which is shown in Fig. 5.18. Therefore, in order to obtain the top speed, the bias current I_d must be set to just under the critical current I_c, especially when the

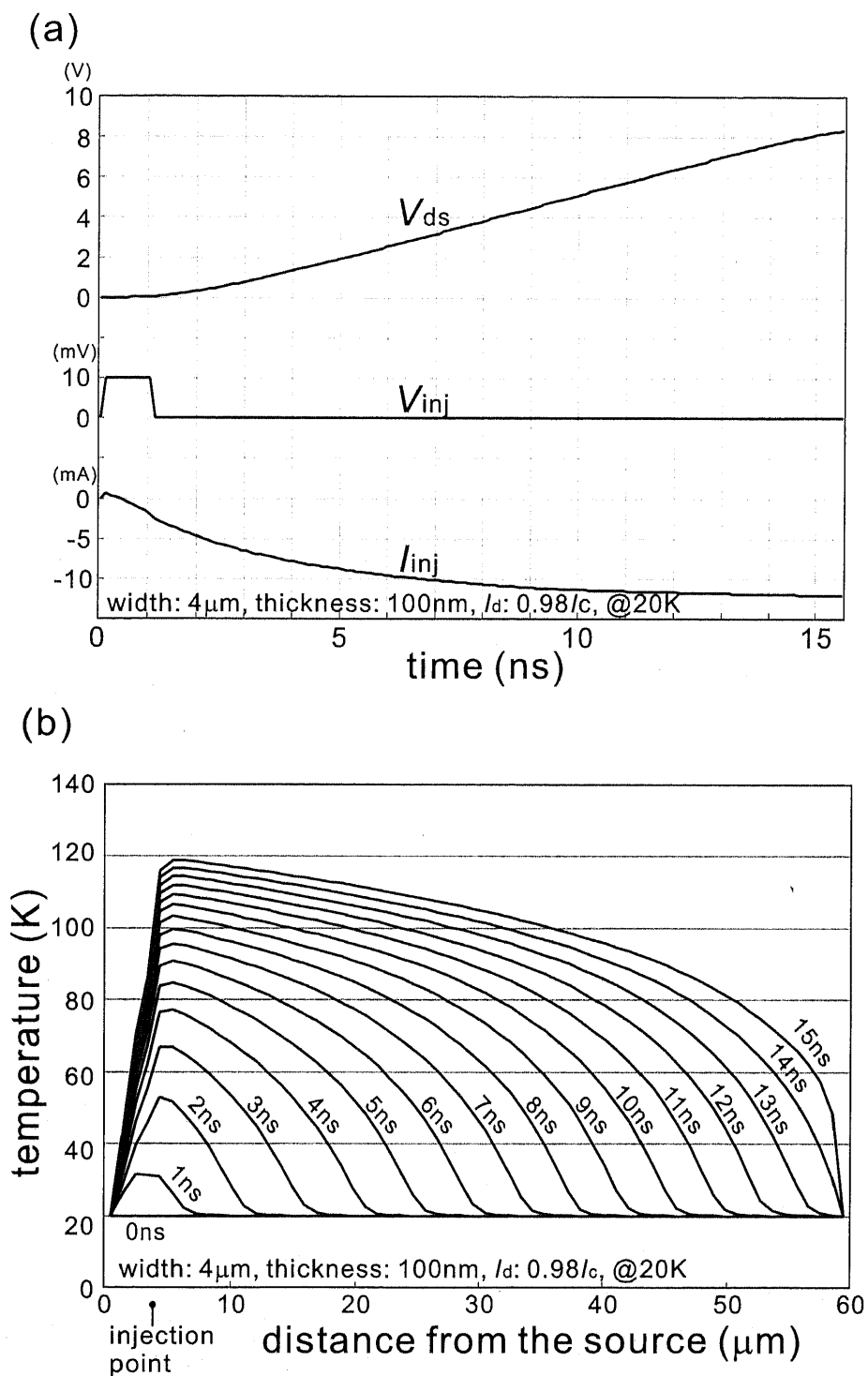Figure 5.14: Characteristics of the device with the bridge dimensions of 4 μm in width and 100 nm in thickness. (a) V_{ds}, V_{gs}, I_{inj}–t characteristics. (b) Bridge temperature distribution.
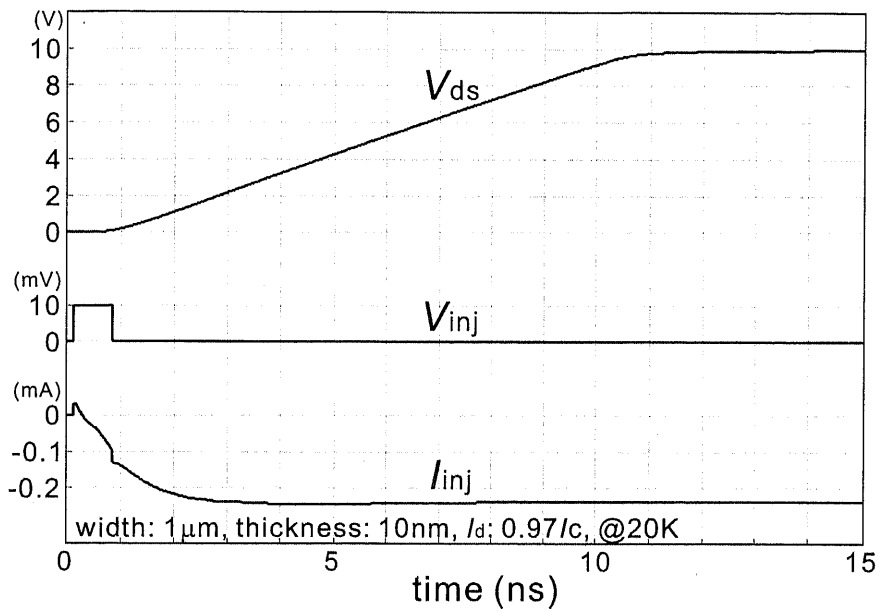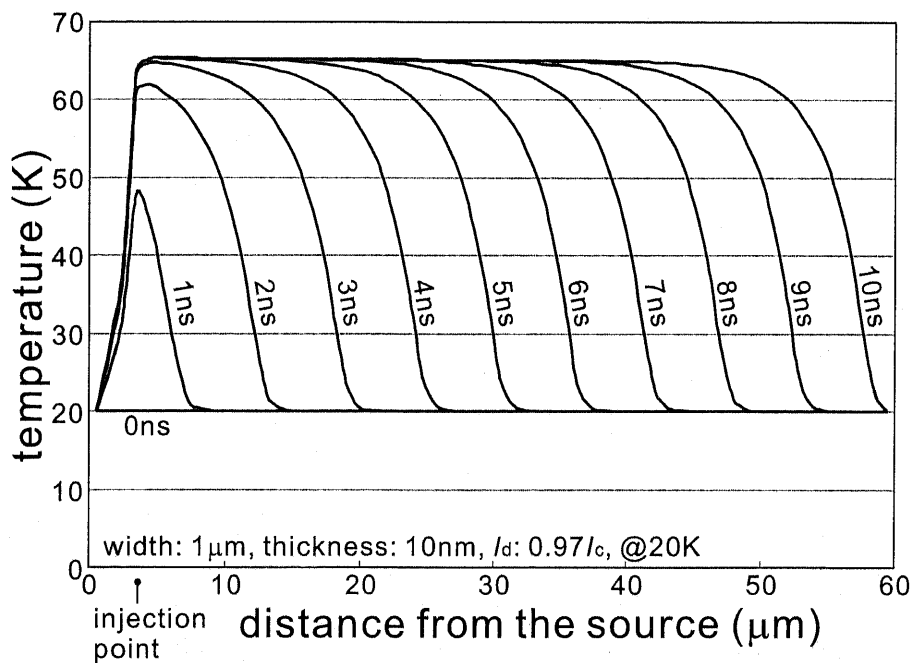
(a)

(b)

Figure 5.15: Characteristics of the device with the bridge dimensions of 1 μm in width and 10 nm in thickness. (a) V_{ds}, V_{gs}, I_{inj}–t characteristics. (b) Bridge temperature distribution.
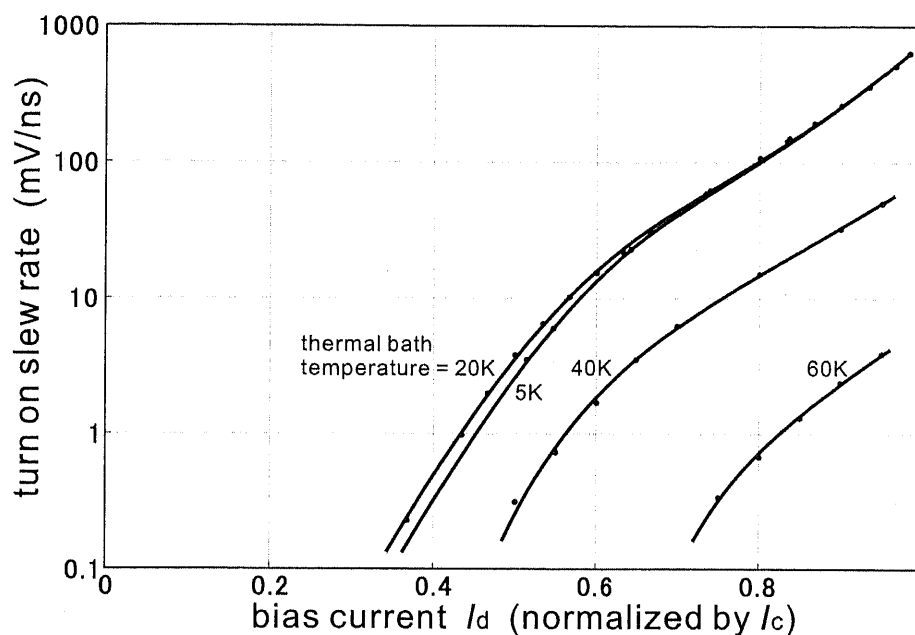
Figure 5.16: Slew rate dependence on the thermal bath temperature.

device size is small.

ON/OFF Operation

As described above, the turn on slew rate becomes large along with the increase in I_d. However, as for the reset time, it becomes longer if I_d is large; the reset time is determined by the time required to cool the device down to below $T_c(I_d)$.

Simulation results of device cooling time is shown in Fig. 5.19. (a) is the results of the device with the bridge dimensions of 4 μm in width and 100 nm in thickness. The thermal bath temperature is 20 K. Here we show some numerical examples. If I_d is set to $0.7I_c$, $T_c(I_d)$ is about 40 K and the reset time is about 100 ns. If I_d is set to $0.9I_c$, $T_c(I_d)$ is about 25 K and the reset time is 1~2 μs. These results are discouraging; the operation frequency would be limited by this reset time.

One of the solutions for this problem is scaling of the device. The temperature of small-sized device is much lower, which is clear from the comparison between Fig. 5.14-(b) and Fig. 5.15-(b), and moreover the cooling process itself is also fast because the heat capacity is proportional to the device volume. Fig. 5.19-(b) is the results of a small device. The bridge dimensions are 1 μm in width and 10 nm in thickness. The cooling time is drastically shortened compared with (a).

The simulation results of ON/OFF operation are shown in Fig. 5.20. (a) is the results of a device with the dimensions of 4 μm in width and 100 nm in thickness. the operation frequency is 5 MHz. (b) is the results of a smaller device. The
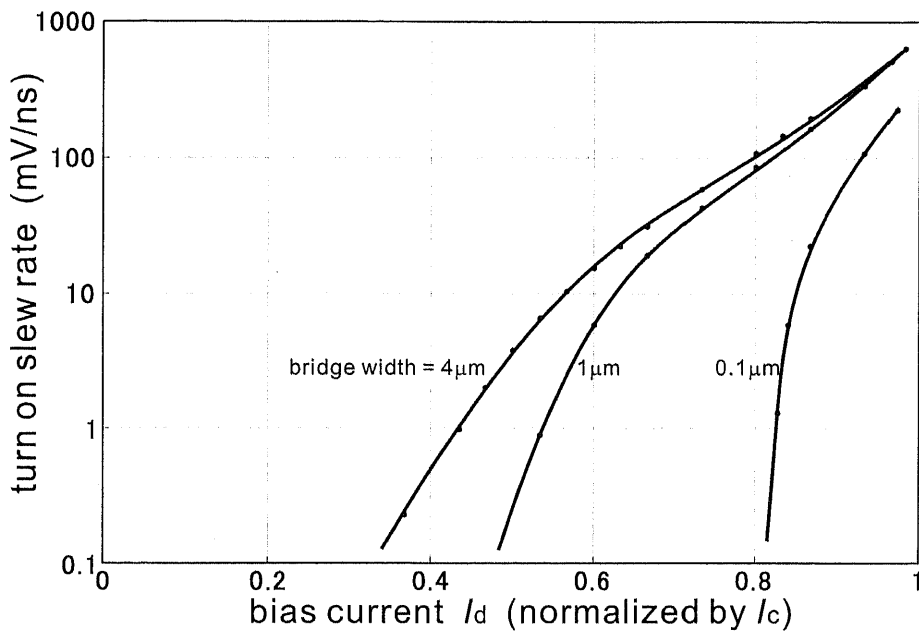
Figure 5.17: Slew rate dependence on the bridge width.
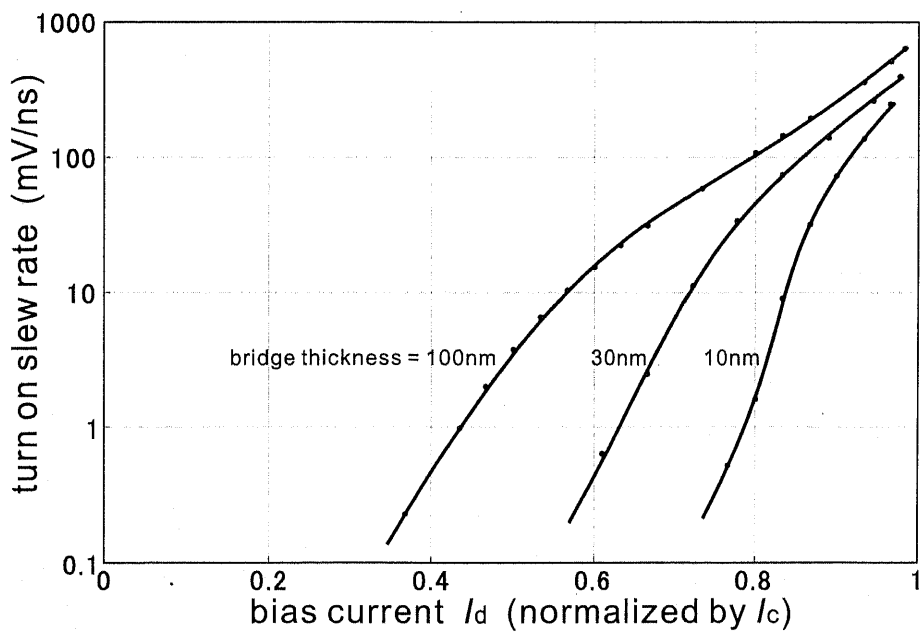
Figure 5.18: Slew rate dependence on the bridge thickness.

dimensions are 1 μm in width and 10 nm in thickness. The operation frequency is 55 MHz; about 10 times as fast as the results in (a).

We can expect further improvement by scaling down the device more and more. Another way to make faster switching device is to increase J_c, that is, to improve the crystallinity of YBCO, because the larger I_d is, the higher the slew rate becomes, as is understood from Fig. 5.16–5.18.
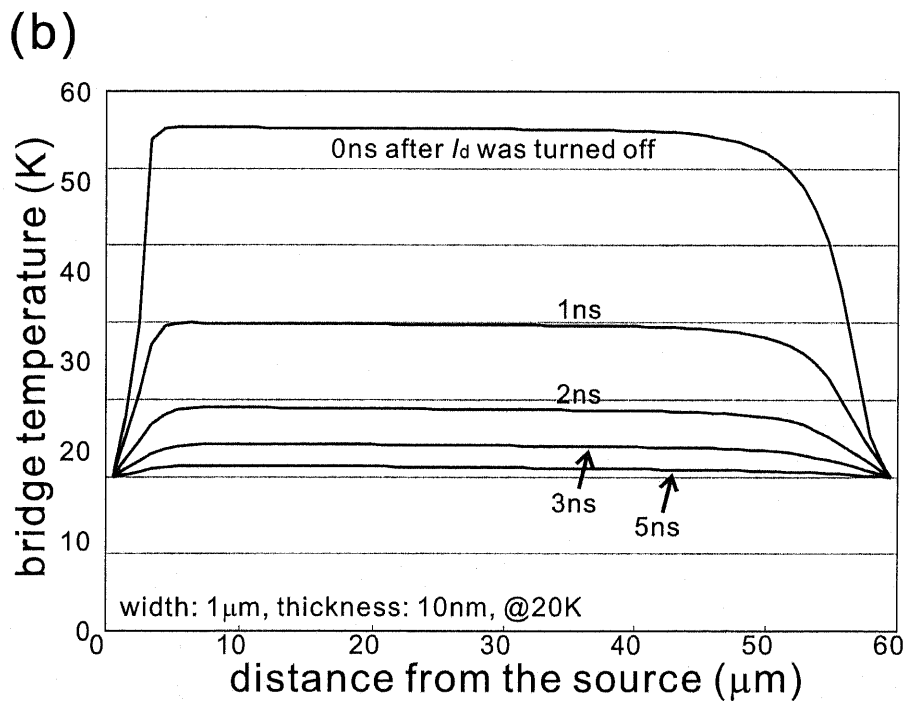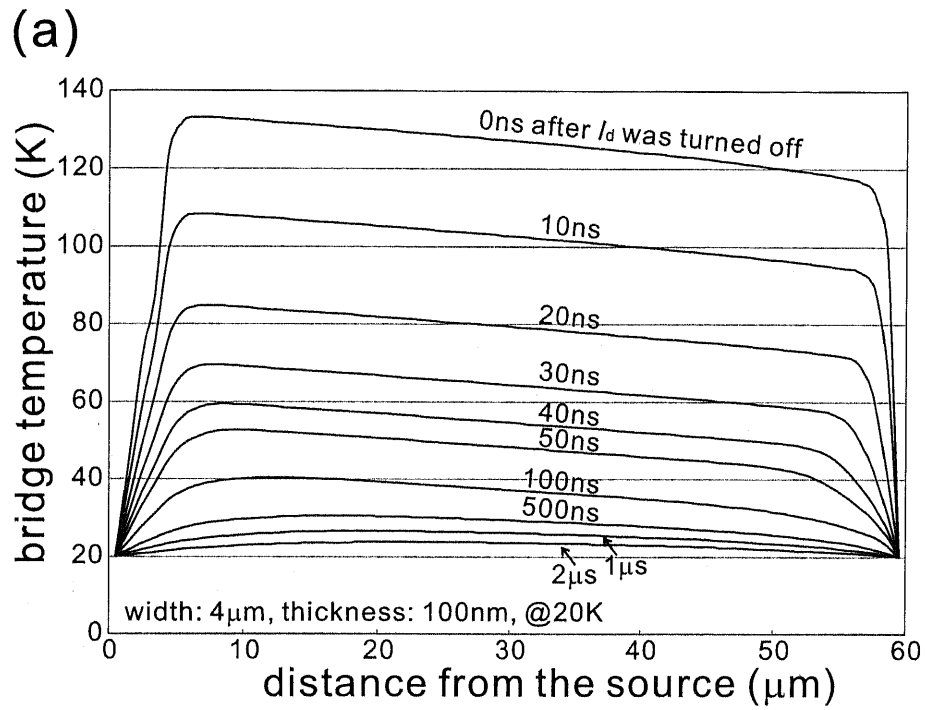
Figure 5.19: Temperature distribution of the bridge after I_d is set to 0. (a) bridge width = 4 μm, bridge thickness = 100 nm. (b) bridge width = 1 μm, bridge thickness = 10 nm.
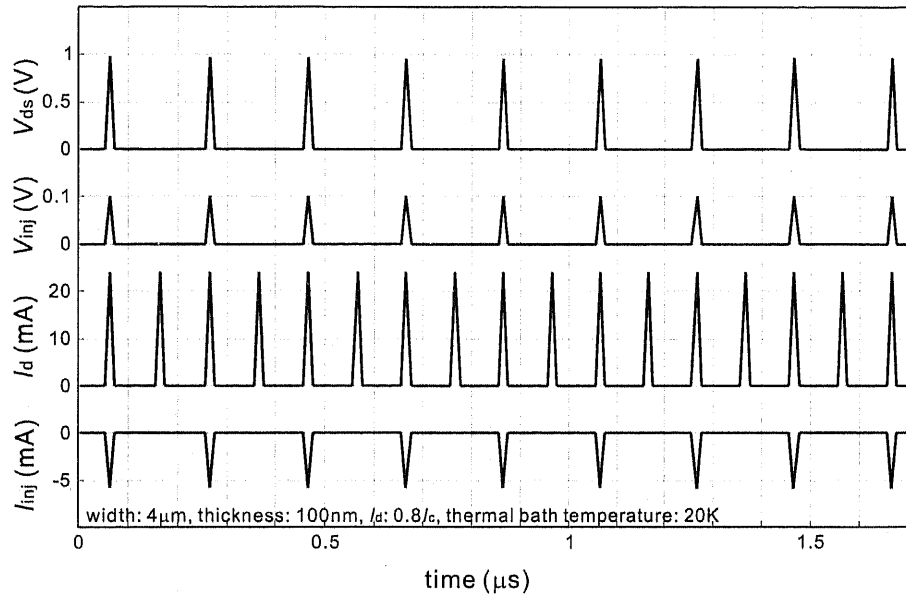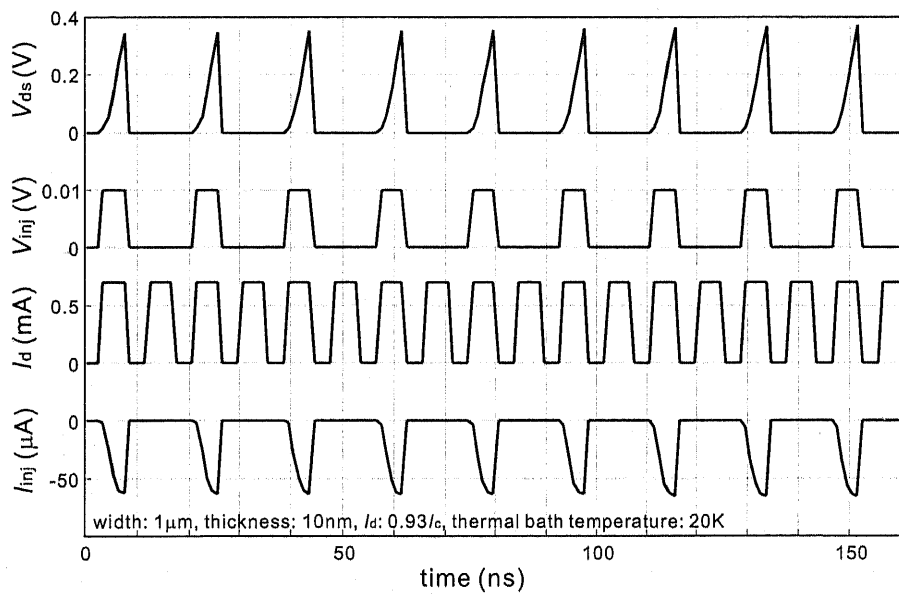
Figure 5.20: ON/OFF operation. (a) The bridge dimensions are 4 μm in width and 100 nm in thickness. V_{ds} repeats turn-on and off at the frequency of 5 MHz. (b) The bridge dimensions are 1 μm in width and 10 nm in thickness. The frequency is 55 MHz.

Chapter 6

Conclusion

We have fabricated high T_c superconductive quasi-particle injection devices aiming at the use for the interface between SFQ and CMOS circuits.

We used YBCO as the material for the superconductive bridge and Au as the injector. The critical temperature T_c of the YBCO film was over 80 K. In order to inject large current into the bridge with very low voltage, we tried to make the contact resistance between Au and YBCO as low as possible. For this purpose, we did not deposit any insulator layer between the bridge and the injector; Au was deposited directly on the YBCO film in-situ with PLD method. And then annealing in 1 atm O_2 atmosphere at 500 °C was performed. Consequently, the contact resistivity of 10^{-7} Ωcm^2 was achieved.

The length, width, and thickness of the YBCO bridge were 20~100 μm, 4~6 μm, and 100 nm, respectively. The width of the Au gate electrode was 5~10 μm and thus the contact area was 20~60 μm^2, the contact resistance being about 1 Ω.

We measured the fundamental characteristics of this switching device: R–T characteristics, I_d–V_{ds} characteristics, etc. I_d–V_{ds} characteristics of the bridge were quite peculiar. I_d is almost fixed to a constant value I_n regardless of V_{ds} when the bridge is in resistive state.

We tried to explain this behavior by thermal analysis based on the heat generation and the heat conduction. By this simulation, the temperature distribution within the bridge was acquired and the characteristics of the device were successfully explained. It turned out that the whole bridge does not turn to resistive state at once. The superconductive area and the resistive area can exist together within the bridge and the length of the resistive area depends on V_{ds}, so that the resistance R is proportional to V_{ds}. This is why I_d is fixed to I_n.

Next, the switching characteristics of this device were investigated. There are two kinds of operation modes: non-latching mode and latching mode. If the bias current I_d is smaller than I_n, the device is operated in non-latching mode and if I_d is larger than I_n, it is operated in latching mode. If you want to operate the device in latching mode, not only V_{inj} but also I_d must be reset to 0 after the

device has become resistive. Therefore, in order to make the peripheral circuits as simple as possible, non-latching operation is recommended.

However, when the device was operated with non-latching mode, the voltage amplification factor defined as V_{ds}/V_{gs} was only 2∼3 and the turn on voltage V_{gs} was 1∼2 V, which is too high for actual use. The time required for switching was 10∼100 μs; the operation at a few kHz is the limit. The reason of this poor performance was clarified by simulation. According to the simulation results, when the device is operated in non-latching mode, whole bridge is not in resistive state even if V_{inj} is applied; the area near the drain remains superconductive.

Therefore we tried latching mode operation. In order to prevent the device from being overheated, we used a voltage source as a power supply instead of a current source. Because of this, the up edge of V_{ds} showed saturation, but the response time was about 1/100∼1/1000 of that of non-latching operation. The simulation results showed that when the device is operated in latching mode, the turn-on slew rate increases exponentially against I_d and it almost reaches 1 V/ns at 20 K. However, the time required to cool down the bridge to a temperature such that $I_c(T) > I_d$ becomes longer along with the increase in I_d. An effective way to shorten the cooling time is to downsize the device. If the bridge width and thickness are reduced to 1 μm and 10 nm respectively, operation at more than 50 MHz is possible.

The results obtained from the measurements were not sufficient for the practical use as the interface devices, but the simulation results showed that a device with high performance can be fabricated by scaling down the device dimensions.

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Bibliography

[1] U. Ghoshal, S. V. Kishore, A. R. Feldman, L. Huynh, and T.Van Duzer: "CMOS amplifier designs for Josephson-CMOS interface circuits", *IEEE Trans. Appl. Supercond.* **5**, No.2, pp.2640-2643, Jun. 1995.

[2] O. A. Mukhanov, S. V. Rylov, D. V. Gaidarenko, N. B. Dubash, and V. V. Borzenets: "Josephson output interface for RSFQ circuits", *IEEE Trans. Appl. Supercond.* **7**, No.2, pp.2826-2831, Jun. 1997.

[3] N. Yoshikawa, T. Abe, Y. Kato, and H. Hoshina: "Component development for a 16Gb/s RSFQ–CMOS interface system", *IEEE Trans. Appl. Supercond.* **11**, No.1, pp.735-738, Mar. 2001.

[4] T. Kobayashi, K. Hashimoto, U. Kabasawa, and M. Tonouchi: "Three terminal YBaCuO Josephson device with quasi-particle injection gate", *IEEE Trans. Magn.* **25**, No.2, pp.927-930, Mar. 1989.

[5] C. W. Schneider, R. Moerman, D. Fuchs, R. Schneider, G. J. Gerritsma, and H. Rogalla: "HTS quasiparticle injection devices with large current gain at 77K", *IEEE Trans. Appl. Supercond.* **9**, No.2, pp.3648-3651, Jun. 1999.

[6] Yu. M. Boguslavskij, K. Joosse, A. G. Sivakov, F. J. G. Roesthuis, G. J. Gerritsma, and H. Rogalla: "Quasiparticle injection effects in $YBa_2Cu_3O_x$-based planar structures at high operating temperatures", *Physica C* **220**, pp.195-202, 1994.

[7] K. Takeuchi and Y. Okabe: "Injection controlled superconducting links", *Jpn. J. Appl. Phys.* **28**, No.10, pp.1810-1815, Oct. 1989.

[8] J. W. Ekin, T. M. Larson, N. R. Bergren, A. J. Nelson, A. B. Swartzlander, L. L. Kazmerski, A. J. Panson, and B. A. Blankenship: "High-T_c superconductor/noble-metal contacts with surface resistivities in the 10^{-10} Ωcm^2 range", *Appl. Phys. Lett.* **52**, No.21, pp.1819-1821, May 1988.

[9] S. D. Peacor, R. A. Richardson, F. Nori, and C. Uher: "Theoretical analysis of the thermal conductivity of $YBa_2Cu_3O_{7-\delta}$ single crystals", *Physical Review B*, **44**, No. 17, pp.9508-9513, 1991.

[10] V. W. Wittorff, N. E. Hussey, J. R. Cooper, Chen Changkang, and J. W. Hodby: "Thermal conductivity of single crystals of $YBa_2(Cu_{1-x}Zn_x)_3O_7$", *Physica C*, **282-287**, pp.1287-1288, 1997.

[11] Y. Wang, B. Revaz, A. Erb, and A. Junod: "Direct observation and anisotropy of the contribution of gap nodes in the low-temperature specific heat of $YBa_2Cu_3O_7$", *Physical Review B*, **63**, 094508, 2001.

[12] T. Atake et al.: "Heat capacity of the high temperature superconductor $Ba_2DyCu_3O_7$", *Physical Review B*, **37**, No.1, pp.552-, 1988.

Papers and Presentations

[1] 滋賀秀裕, 岡部洋一: "準粒子注入を用いた超伝導体–半導体インターフェイ
ス素子の試作", 2000 年春季第 47 回応用物理学関係連合講演会講演予稿集,
No.1, 28a-G-23, pp.269, Mar.2000.
(H. Shiga and Y. Okabe: "Fabrication of a quasiparticle injection device for
superconductor-semiconductor interface", Extended Abstracts (The 47th
Spring Meeting, 2000); The Japan Society of Applied Physics and Related
Societies, No.1, 28a-G-23, pp.269, Mar.2000.)

[2] H. Shiga and Y. Okabe: "Quasi-particle injection device for the interface
between superconductor and semiconductor", Abstracts of 2000 Applied
Superconductivity Conference (ASC2000), 4EG03, pp.99, Sep.2000.

[3] H. Shiga and Y. Okabe: "Quasi-particle injection devices for interfaces
between superconductors and semiconductors", *IEEE. Trans. Appl. Su-
percond.* **11**, No.1, pp.940-943, Mar.2001.

[4] 滋賀秀裕, 岡部洋一: "準粒子注入を用いた超伝導体・半導体間インターフェ
イス素子の試作", 2001 年春季第 48 回応用物理学関係連合講演会講演予稿
集, No.1, 29a-ZC-1, pp.292, Mar.2001.
(H. Shiga and Y. Okabe: "Fabrication of a quasiparticle injection device for
superconductor-semiconductor interface", Extended Abstracts (The 48th
Spring Meeting, 2001); The Japan Society of Applied Physics and Related
Societies, No.1, 29a-ZC-1, pp.292, Mar.2001.)

[5] H. Shiga and Y. Okabe: "High-Tc quasi-particle injection devices for the
interfaces between SFQ and CMOS circuits", Extended Abstracts of 8th
International Superconductive Electronics Conference (ISEC'01) P3-A7,
pp.461-462, Jun.2001.

[6] 滋賀秀裕, 岡部洋一: "準粒子注入を用いた超伝導体・半導体回路間インター
フェイス素子の試作", 2001 年秋季第 62 回応用物理学会学術講演会講演予
稿集, No.1, 14a-G-1, pp.193, Sep.2001.
(H. Shiga and Y. Okabe: "Quasiparticle-injection type interface devices
between superconductor and semiconductor circuits", Extended Abstracts

(The 62nd Autumn Meeting, 2001); The Japan Society of Applied Physics, No.1, 14a-G-1, pp.193, Sep.2001.)

[7] H. Shiga and Y. Okabe: "HTS quasi-particle injection devices for interfaces between SFQ and CMOS circuits", *IEICE Trans. Electron.*, accepted.

[8] 滋賀秀裕, 岡部洋一: "準粒子注入を用いた超伝導体・半導体回路間インターフェイス素子の試作", 2002 年春季第 49 回応用物理学関係連合講演会講演, accepted.
(H. Shiga and Y. Okabe: "Quasiparticle-injection type interface devices between superconductor and semiconductor circuits", The Japan Society of Applied Physics and Related Societies (The 49th Spring Meeting, 2002), accepted.)